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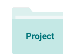

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PS-2-06

Facile approach of enhanced heat mitigation between 3D stacked layers by Introducing a sub-micron thick heat spreading materials

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Abstract:

Polder and Van Hove in 1971 forecasted, it is possible to transfer heat between the planer surface by phonon tunneling mechanism, having interlayer separation that is comparable to the phonon wavelength. Towards that, in this work we examined the heat mitigation issues widely prevalent in 3D stacked ICs using finite element analysis. We observed batter heat mitigation by using optimized thickness of heat spreader sandwiched between ICs, containing TTSVs. FEM result shows nearly 15 °C reduction in temperature from 313°C to 298 °C of the top most IC in a 3D stack compared with the case without TTSV and heat spreader in the ILD plane.

Key words:
ILD (Inter layer dielectric), heat spreaders, TTSV (Thermal through silicon via).

1. Introduction:

The ongoing demand towards electronics, for consumers to get satisfaction with low price and high performance and reliable devices are motiving towards 3D IC. Because of stacking of multiple layers on a single chip area with each IC's of interconnections spread in ILD's are biggest huddle for heat trapping in those layers as heat zones we call hot spots in IC's. this is in an ongoing research, people have done introducing TTSV's (i.e. Thermal Through Silicon Vias) is an effective heat conductor from top IC to bottom sink [2], heat spreaders of high thermal conductivity [3], and also followed by TTSV's with heat spreaders, introducing peltier element for active cooling, and also using pyroelectric effect [4]. But all these from the fabrication point of view is very difficult to introduce other elements in such a finite area. We need to conduct heat from hot spots to heat sink, if we will introduce the lower thick ~nm's [1] that leads to high thermal conductivity by phonon tunneling if the width of layer is less than the thermal wavelength of phonons that are transferring to the stacked layers.

2. Modelling Structure:

In order to examine the thermal mitigation, the stacked 3D structure (Fig.1) was simulated using COMSOL Multiphysics and physics used for FEM simulation as heat conduction in solids with stationary study. The heat sink of 120 µm containing IC-1 followed by 8 µm of ILD-1. Then IC layers of 20 µm each followed by 8 µm ILD layers. In between the device layers and ILD's we have inserted heat spreader with varying thickness from 2 µm to 100 nm. The dimensions of each layer we have taken for FEM simulation as 50 µm×50 µm along with TTSV diameter of 4.85 µm followed with liner of 0.15 µm as per ITRS roadmap standards. We took the boundary heat source of 1.0W/mm^2 and observed heat mitigation in stacked layers as discussed in section below.

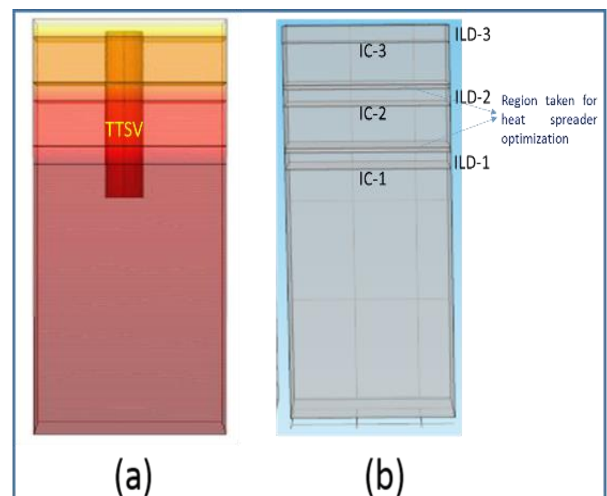

Fig.1 Simulated schematic of heat removal model using with (a) only heat spreaders and (b) with TTSV and heat spreaders.

3. Results and Discursion:

In order to cool down IC layers we need to mitigate it otherwise heat may accumulate and crate hotspot. It can be observed from Fig.2 that at top IC layers heat is very prominent without any TTSV and heat spreaders. After insertion of heat spreader as CVD diamond having heat conductivity of 2000 W/mK with varying thickness of 2 µm, 200 nm, 100 nm and 150nm. From Fig. 2 one can easily realize that 150 nm thick CVD diamond heat spreader is efficiently mitigating the heat of proposed stacked layers of 3D IC. This might be because of submicron separation between IC layer and ILD which makes this less than the thermal wavelength of phonon transmission [5].

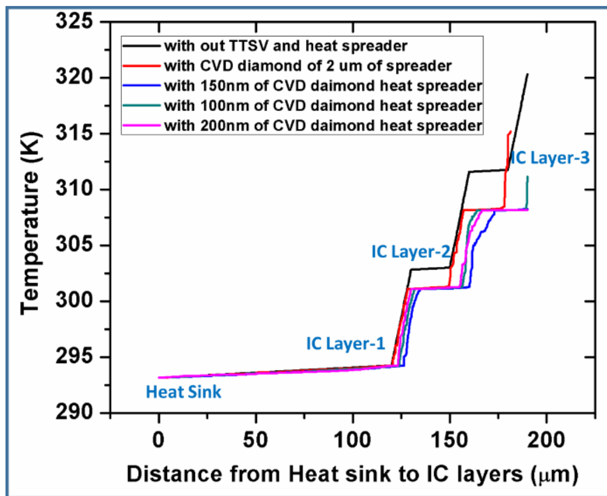

Fig. 2 Heat cooling improvement can be achieved with the insertion of 150nm heat spreader, it particularly will be more with selection of higher thermal conductivity heat spreader material.

Furthermore, in order to confirm the heat mitigation in presence of TTSV. The comparative graph is plotted as shown in below Fig 3.

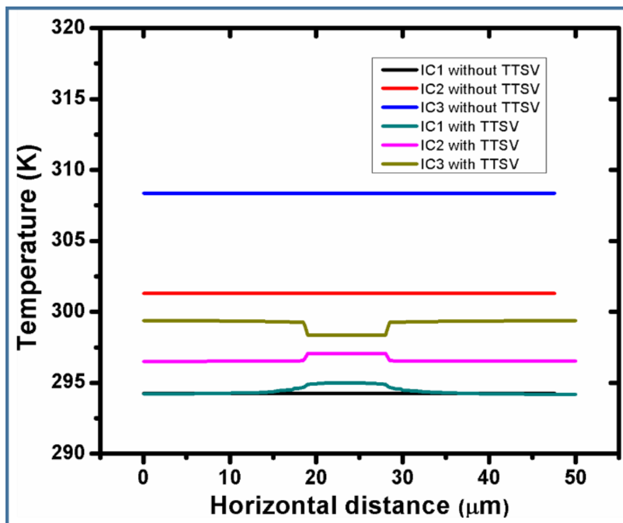

Fig. 3: comparison of temperature in stacked layers with TTSV and Without TTSV

From Fig.3 we infer that, in presence of TTSV heat mitigation is more prominent and clear. In order to compare the impact of heat spreader of thickness 150 nm, towards heat mitigation; we sandwiched heat spreader between IC layer having TTSV and the simulation result as shown in Fig. 4, clearly shows improved heat mitigation with heat spreader compared with the scenario without it.

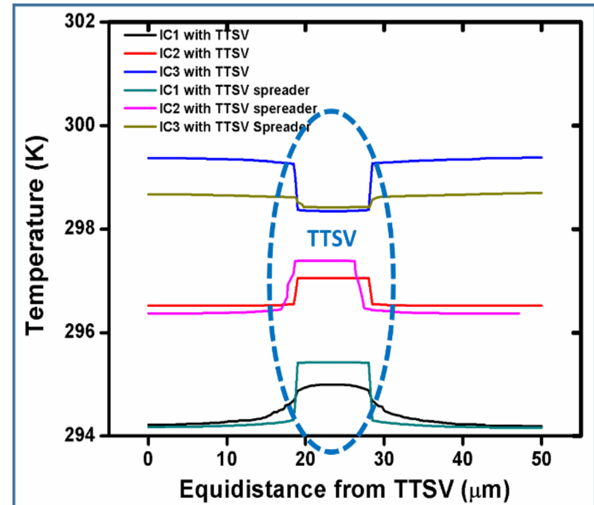

Fig 4. Comparison TTSV without any heat spreader and with heat spreader.

3. Conclusions

From this work, it is one with facile technique for enhanced heat mitigation in stacked layer of 3D IC, because of submicron layer thickness i.e. 150nm is easy to fabricate and occupancy of minimal volume, here we demonstrated that heat spreader is sandwiched in between both TTSV's and IC and ILD layers, so it is suggestable at the fabrication point of view we need to bond either homogeneous bonding of spreader layers by depositing on each substrates or heterogeneous bonding of substrate with heat spreader. For the both fabrication we need TTSV to be fabricated initially before bonding of layers i.e via middle approach is preferable and then bonded is suggestable.

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