Power Combining Amplifiers for Mobile Millimetre Wave Block Up Converters

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Abstract

The use of power combining techniques allows the realization of millimetre wave solid state amplifiers with output power levels that are not achievable from a single solid state source. The need for efficient and low cost amplifiers for mm-wave systems has propitiated an intense area of research during the last years in power combining techniques.

This thesis presents the development of compact and efficient power amplifiers based on new power combining structures using solid state devices. In addition, the implementation of a mm-wave block up-converter (BUC) is included, with the aim to evaluate the performance of the amplifier in a real system. The developed power combiner is based on a travelling wave architecture, which is demonstrated to be a very convenient solution at mm-wave frequencies because of its high efficiency and compactness. The new structure proposed, consists of a double side waveguide geometry which provides a 50% size reduction compared to existing solutions. This structure is validated by manufacturing a 12-way power combiner and amplifier prototype. In order to achieve the goal of testing the amplifier in a real system, an L-to-Ka band block up-converter is then designed and implemented. The performance of the block up-converter is demonstrated for a single and a double conversion architectures. Finally, the performance of the BUC is demonstrated under digital modulated signals.

Dedication

To my family, specially to my parents and my brother, for always being there encouraging and trusting me. Thank you for all the unconditional support and for listening patiently to all my incomprehensible microwaves stuff.

Also to Belén, my soulmate and best friend, for your incredible love and constant willingness to cheer me up all the time.

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Journal papers

[J1] J. A. Garcia-Perez, G. Goussetis and S. Kosmopoulos, "A Compact 12-Way Slotted Waveguide Power Combiner for Ka-band Applications", *IEEE Microwave and Wireless Components Letters* (2016).

Conferences

[C1] J. A. Garcia-Perez, G. Goussetis and S. Kosmopoulos, "1-to-4 Double-Side slotted waveguide power Divider/Combiner for Ka-band power amplifiers", *SBMO/IEEE MTT-S IMOC* 2015.

[C2] Garcia-Perez, J.A.; Kosmopoulos, S.; Goussetis, G., "A Custom L-to-Ka Band Block Up-converter (BUC) for Millimetre Wave Testbeds", *IET Active and Passive RF Devices Conference Proceedings* 2017.

Chapter 1

Introduction

The rapid development of wireless technologies in the recent years has resulted in changes in our society never before seen. Since the early days of the Internet and its recent implementation in mobile devices, the need for media contents and broadband speed is growing at an exponential rate. Nowadays, being connected at every moment is taken as a base service in our daily lives. Related to this, a wide range of new applications and services such as music and video streaming, HD and 4K television, Internet of Things (IoT) and many others are getting more attention. This new huge demand for data and its expected trend to keep growing in the next years, is creating a whole new set of problems related to how to cope with such amount of traffic with an already crowed radio frequency spectrum. In order to serve all these new technologies, the frequency bands allocation is being moved to mm-wave bands. At these bands, the radio frequency spectrum is not crowded and the higher bandwidths available can provide gigabit speeds in wireless technologies or serve a huge amount of users.

As an example, in satellite communications, recent advances have produced the first Ka-band satellite system able to provide up to 90 Gbit/s [1] and there is an interest in moving to higher bands such as Q-band and V-band [2] to implement internet satellite access at these bands. In addition, the classical digital broadcast system (DVB) protocols are being improved (DVB-S2X) [3] to include higher modulation schemes in order to increase data rate, and smaller roll-off factors and improved filtering to reduce carrier spacing. Furthermore, in mobile communications, the new generation also named 5G is expecting to allocate frequency bands at mm-wave

frequencies and to use advanced techniques such as massive MIMO to increase the system capacity [4].

All these new applications (and many more expected to appear from the development of these technologies) need of new hardware components capable to provide functionalities at these frequency bands. A key component in any radio frequency system is the block up-converter (BUC). This part is used to translate a lower frequency signal to a high frequency and amplify the signal to have enough power level to be radiated and reach the receiver. The main drawback of BUC at mm-wave bands is to include power amplifiers that achieve high power levels in a compact, low-cost and efficient way. Traditionally, power amplifiers were created using vacuum tube technology which are bulky and expensive. However, in the forthcoming scenarios, where thousands of systems are likely to be needed, the associated costs to this type of amplifiers would end up in impracticable budgets.

As an alternative, the development in solid state technology has led to a new strategy to create power amplifiers using low cost and reliable transistors. However, the power output of amplifiers using this technology is very low compared to that of travelling wave tubes. Thus, this has propitiated an intense research to develop new power amplifiers based on the efficient and compact combination of several solid state amplifiers so that the output power is enough to reach the required levels of the new emerging applications [5].

1.1 Objectives and thesis outline

The objective of this thesis is to research on compact and efficient power combining amplifiers using solid state technology and new power combining structures. In addition, the design and development of a low cost focused L-to-Ka band block up-converter has been carried out with the objective of comparing the performance of a commercial power amplifier with a custom power combining amplifier design.

In order to complete the objectives, the thesis is structured in 6 chapters, including this introductory chapter.

Chapter 2 contains a review of the existing solutions and trends in power combining techniques. This chapter is organised following a subdivision of power combining

techniques and their working principle. For each technique, a literature review of previous research is presented. Also, for each technique, its advantages and disadvantages are discussed.

In Chapter 3, the design and manufacturing of a passive 12-way power combiner prototype is presented. This prototype is based on a travelling wave approach and consists in a double side slotted waveguide structure. First of all, general design guidelines for this type of combiners are presented. Secondly, the detailed design process for the proposed prototype is described, including simulated results. Finally, the manufacturing process of the prototype is discussed and the measured results are presented.

In Chapter 4, the passive prototype designed and manufactured in Chapter 3 is used to manufacture a power combining amplifier by including amplifier chips in the design. Firstly, the design of the printed circuit board for the chips is presented and the manufacturing of a test board for a single chip described. Then, the design and manufacturing of the complete boards for a 12-way power combining amplifier is presented.

In Chapter 5, a block up-converter from L-band to Ka-band is designed and implemented. Design guidelines and a performance evaluation between two different architectures are discussed. Finally, the implementation and measurement of a prototype is presented.

Chapter 6 presents a summary of the work carried out in the thesis, conclusions and future work.

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Chapter 2

Literature review

2.1 Introduction

The need for high power in microwave and radio frequency applications have been present since the early days. The generation and amplification of RF signals is needed in almost every system in order to have power levels adequate to reach long distances or to drive the input of a device with enough power. Classical power amplifiers were built using travelling wave tube amplifiers. However, since the development of solid state electronics, there have been an increasing interest in developing power amplifiers based on this technology. In this chapter, a literature review of different power amplifier technologies is presented. Two main technologies are discussed, namely travelling wave tube amplifiers (TWTA) and solid stage power amplifiers (SSPA).

2.2 Travelling wave tube amplifiers (TWTA)

Since their invention in the mid 1940s to early 1950s the TWTA is the most used vacuum electronic amplifier in communication systems for high power and wide bandwidth applications (both military and commercial applications). Very high powers (10W-10kW) can be achieved and the frequency of operation can go up to 1000 GHz [1]. Among typical designs are the helix and coupled cavity TWT, magnetron, klystron and crossed field amplifier. Their efficiency is about 70% for

narrowband applications and 50% for broadband applications and they are still the best solution for space applications due to their high isolation provided by the vacuum device. Advances in research have improved the performance of the original devices. However, their still considerable weight, size and cost as well as their really high voltage requirement make them not such a good solution for other applications. Additionally, TWTA have bad linearity because of their saturated operation, which involves more extra costs in expensive and complex linearisation techniques. Therefore they are not appropriate for modern complex modulations used in new communication standards in which high linearity is crucial. One alternative is to operate the amplifier in back off at the expense of efficiency, which would imply big costs in efficiency improvement techniques. In Fig. 2.1 a schematic of a TWTA based on helix architecture is shown.

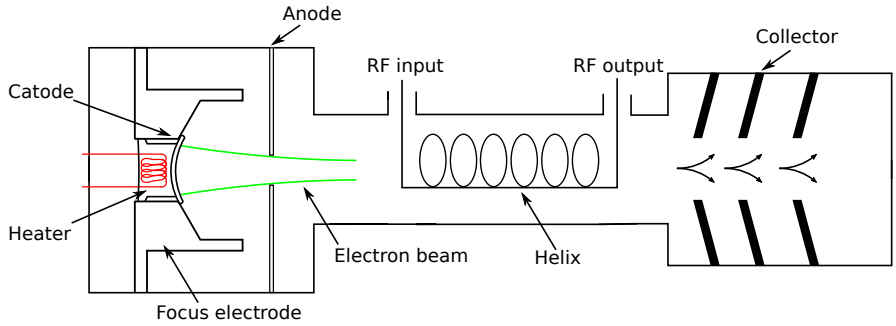

Figure 2.1: Helix TWTA schematic.

2.3 Solid state power amplifiers (SSPA)

Due to the development of solid state circuit technology, power amplifiers realized using Microwave Monolithic Integrated Circuit (MMIC) chips are becoming more popular in recent years. Due to their reduced size, weight, cost and the possibility of mass production, they are becoming the main technology that will replace the actual TWT amplifiers in many applications, including RADAR, airborne communications and terrestrial applications. Also, they can be easily mass produced using modern IC manufacturing techniques. Power amplifiers need to provide high output powers, broad bandwidth, high linearity and low noise among other characteristics. At single device level at high frequencies, MMICs are not able to provide high amount of output powers. Even with wide band-gap high power devices such as Galilum Nitride

GaN, output powers above 10 W are difficult above 30 GHz [2]. Therefore, in order to achieve output powers comparable to the high levels of TWTA in some applications, it is necessary to combine several of these MMICs amplifiers [3]. Consequently, an extensive research have been carried out facing the new challenge of creating power dividers/combiners at high frequencies. Hence, different combining techniques have been develop to achieve efficient SSPA amplification with higher output powers.

2.4 Power combining concepts

Power amplifiers based on power combining techniques are widely used to achieve higher output powers from several MMIC chips. The general architecture consists of a power divider that distributes the input power between the MMIC chips and then a power combiner that collects all the output powers into a single output. Benefits of power combining amplifiers are graceful degradation, lower cost, better thermal management and smaller size. Among desirable characteristics for a good power combiner include [4]:

- Low loss matching elements.
- Minimum loss in the combining (high combining efficiency).
- Minimum phase and amplitude imbalance.
- Good input and output matching (VSWR).
- Efficient thermal dissipation.

In general, power combining techniques can be grouped into four main categories [5], shown in Fig. 2.2: chip-level, circuit-level, spatial and a multi-level combination of the previous.

In [6] a comparison between chip-level and circuit-level efficiency is presented. In general, for a MMIC chip-level combiner, it is better to have large gate periphery which produces higher output power but lower gain and efficiency. On the other hand, smaller gate amplifiers with higher efficiency can be combined externally. Therefore, it is very common to have both techniques in a power combiner amplifier. In general, the power divider and combiner are identical due to the reciprocity theory, and can be connected inversely to form a dividing/combining network.

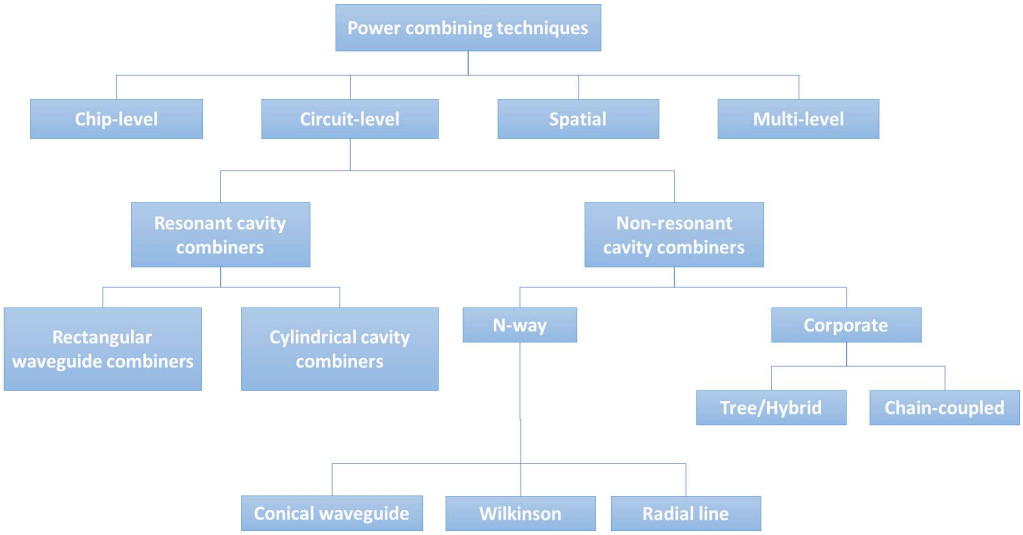

Figure 2.2: Different power combining techniques.

2.4.1 Chip-level power combiners

This power combining technique consists of including several transistors in a single chip combined in one or several stages in order to achieve higher output power. Hence the power combining is done internally in the chip as shown in Fig. 2.3. It has the advantage of small size and easy manufacturing using IC mass production technology. Therefore, the associated cost is very low compared to external circuit-level combiners.

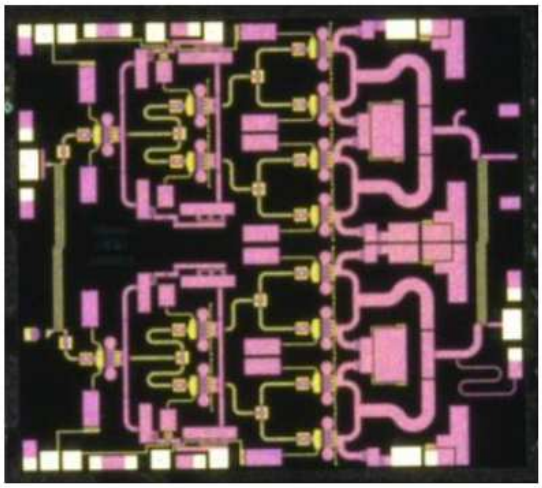

Figure 2.3: MMIC with chip-level power combiner (TGA2595) [2].

The main limitation of this technique is the difficulty to produce electrically small lines at high frequencies in a chip which is much smaller than a wavelength, thus incurring in a higher price since the die size mainly determines the manufacturing

costs. Moreover, the design of matching networks and phase/amplitude balance between stages become more difficult with the number of devices. In addition, the thermal management becomes an important drawback when many devices are combined on chip.

2.4.2 Circuit-level power combiners

At circuit level the power combiners can be divided into resonant or non-resonant cavity combiners. Resonant combiners can be further divided into rectangular or cylindrical cavity combiners. Similarly, non-resonant combiners can be divided into N-way and corporate combiners.

2.4.2.1 Resonant cavity combiners

This type of combiners provide very high combining efficiencies, in the order of 85-90%. However, because of the resonant nature, they have narrowband operation bandwidth. The basic operation principle is the insertion of coupling elements in the points of maximum field of a resonant cavity so that the power is extracted uniformly between the elements. The first resonant cavity combiner was proposed by Kurokawa and Magalhaes in 1971 [7] to build a power combiner for an oscillator at X-band. This design is shown in Fig. 2.4, where IMPATT diodes are inserted in the magnetic field maximum position in the resonant waveguide. A modification of this circuit was done by Harp and Stover to use a cylindrical cavity [8]. By introducing the IMPATT diodes in the periphery of the cavity a higher density was obtained. A more recent design using resonant waveguide cavity at Ka-band using coupling slots was presented by Xin Jiang [9].

The problem of narrow bandwidth and the high order modes generated as the number of diodes is increased, led to a further research in non resonant power combiners. In addition, the tuning of resonant combiners is more difficult than non resonant designs.

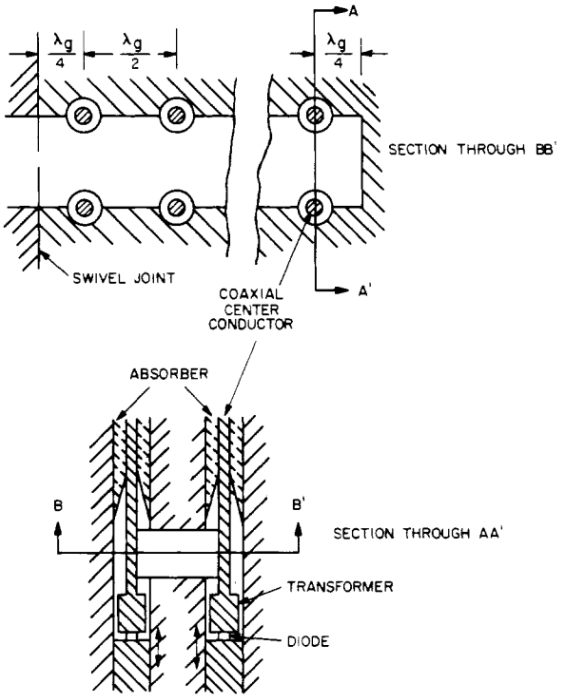

Figure 2.4: Kurokawa's waveguide resonant combiner from [7].

2.4.2.2 Non resonant combiners

The non resonant nature of these power combiners increase the bandwidth capabilities. They may be subdivided into N-way power combiners and corporate power combiners. The first non resonant power combiner was presented by Russell and Harp [10] using conical waveguides and improving the bandwidth to 15% [11](Fig. 2.5).

N-way combiners perform the division/combination of the power in a single-step. As a result these combiners have higher efficiencies because there is no necessity of several combining stages. Another advantage of these combiners is the increased bandwidth. However, they have isolation problems which are normally reduced by introducing isolation resistors. A classical power combiner of this type is the Wilkinson power divider/combiner [12]. In this design, the output line of impedance $\sqrt{(}N)Z_0$ is fed by an input power of impedance Z_0. The isolation between ports is achieved by means of resistors connected between the output ports as seen in Fig. 2.6.

The main problem of the N-way Wilkinson combiner is the difficult design of the isolation resistor connections when the order is bigger than 2. In addition, the resistors can not be connected in a planar design and need of a 3D structure.

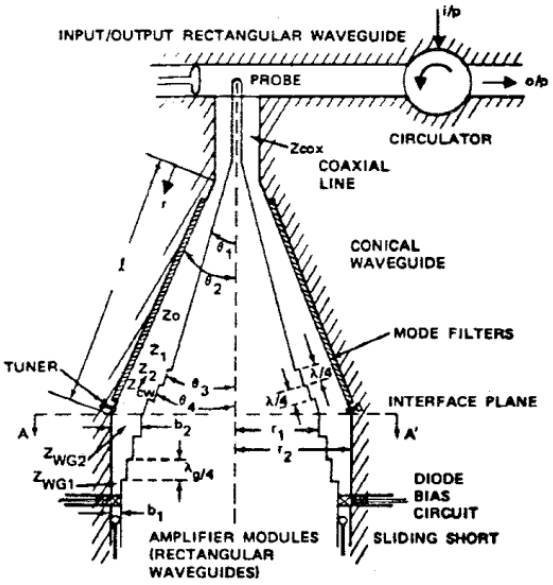

Figure 2.5: Russell's non resonant conical waveguide combiner [10].

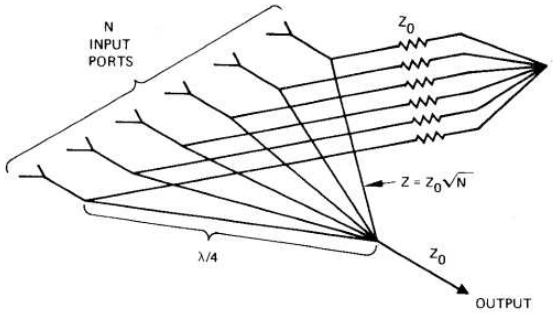

Figure 2.6: N-way Wilkinson combiner schematic from [12].

Radial combiners solve this problem by connecting the isolation resistors between adjacent division lines. The first radial combiner was introduced by Schellenberg in 1978 [13]. The 12-way design demonstrated a combining efficiency of 87.4% with an output power of 4.4 W at 8.5 GHz.

Lastly, corporate power combiners use several stages to divide/combine the power. They can be subdivided into tree/hybrid combiners and chain-coupled combiners. The three/hybrid combiner is composed of 2 way power dividers/combiners arranged in several stages which provides binary division/combination of the power such that $N = 2^k$, where k is the number of stages. An example block diagram of a 3 stages corporate power combining amplifier is shown in Fig. 2.7.

In this architecture a very good isolation between ports can be achieved. Normally, in these architecture, hybrid splitters such as branch-line/rat-race (for planar designs) or magic-tee (for waveguide designs) are used to achieve a better isolation

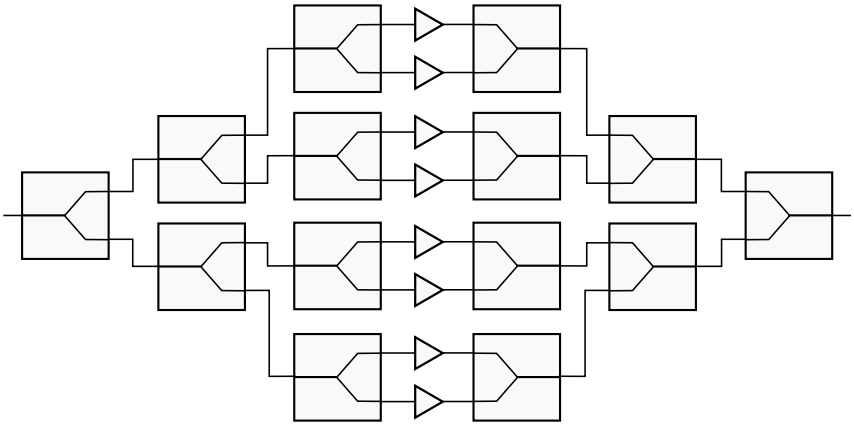

Figure 2.7: 3 stages corporate power combining amplifier block diagram.

between ports. The main drawback of this architecture is that for higher orders, the transmission lines become very long and the losses associated are very high. Therefore if the number of chips is large the combining efficiency will drop and the power output will be significantly decreased. This efficiency can be calculated as $\eta = 10^{kL}$ where L is the loss per divider and k is the number of stages [14] (Fig. 2.8). Also, the number of chips combined can only by a power of 2 which reduces the versatility of the designs.

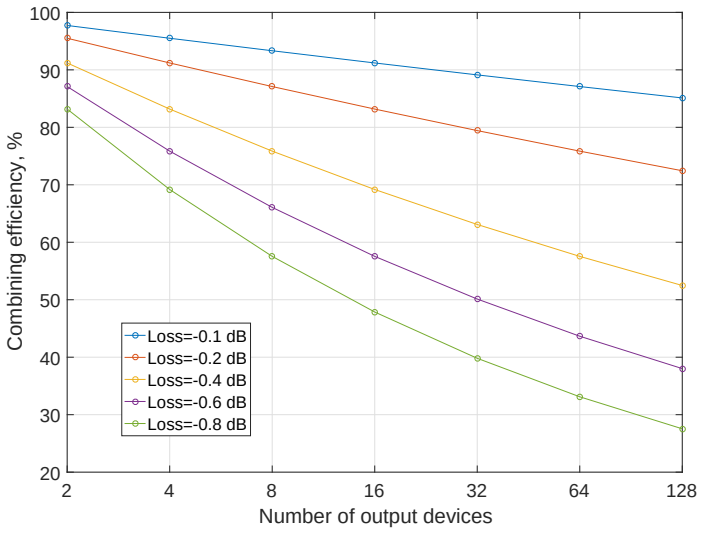

Figure 2.8: Power combining efficiency for corporate power combiners.

In [15] a corporate combiner with efficiency better than 80% and power of 50W was demonstrated at Ka-band, from 31 GHz to 36 GHz. This design had outstanding results using dielectric loaded waveguides combiners. However, the resulting amplifier is very bulky. At V-band, a 12.8 W from 59 to 63 GHz was demonstrated in [16]. This design used hybrid ring rat-race combiners.

Another type of corporate structure is the chain-coupled or also called travelling wave power combiner. It was first proposed by Mohr in 1961 [17] and used by Knox in 1995 [18] to combine 47 elements to get 400 W at X-band. In this approach, each stage of an N-way combiner couples a fraction of 1/N of the total power output. Thus, the transmission lines lenght problem associated with the tree corporate combiner is eliminated and the size reduced. A big advantage of this approach is that it can be extended by just adding additional couplers with $-10log(N)$ coupling coefficient. Therefore this combiner has the highest adaptability and versatility. Also, this approach can achieve wider bandwidth compared to resonant structures and the efficiency can go up to 90%. Additionally, if the divider and combiner are connected in reverse order, the phases at the output ports are compensated. As a result, the design is simplified [19]. On the other hand, the coupling coefficient needed can be difficult to obtain for some coupler architectures. A schematic of this structure is shown in Fig. 2.9.

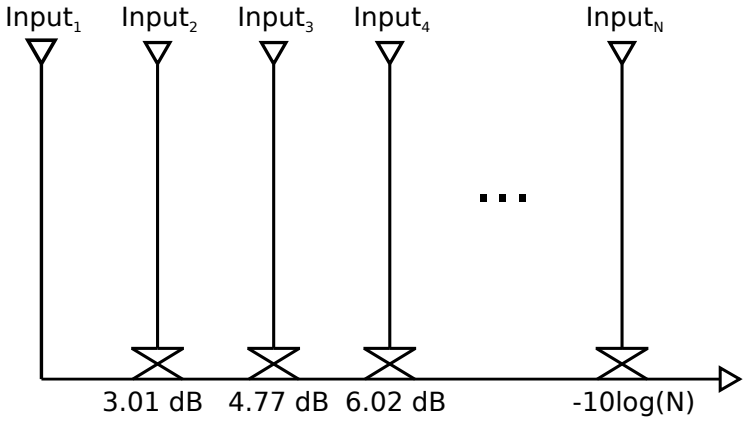

Figure 2.9: Chain-coupled power combiner schematic.

If each coupler is designed to be reflectionless, the design can be simplified to the separate design of the stages with the required coupling ratio. This idea was first introduced by Sanada in 1995 [20]. This technique has been an active research topic in recent years. In [21], a 25 way divider at W-band was designed using the method of moments achieving a 86% efficiency. Ridge waveguide couplers were used in [22] at Ka-band with in-phase outputs and efficiency better than 84%. In [23] a 4 way power divider/combiner based on microstrip probes inserted in a waveguide demonstrated a bandwidth of 15% and power combining efficiency of 80%.

2.4.3 Spatial power combiners

High losses of circuit level combining techniques using a large number of devices are combined can be significantly reduced by using spatial or quasi-optical power combining techniques [24]. Spatial power combining is sometimes called quasi-optical combining since it uses lenses and other elements typically used in optical devices to guide and distribute/collect electromagnetic power. In general, spatial power combining has the best performance when the number of devices to be combined is bigger than 32 (5 stages for a corporate tree combiner) [25]. This technique results in the highest combining efficiency since the elements are combined in free space by coupling beams of electromagnetic energy radiated from an antenna or by directly coupling the elements to waveguide modes. Consequently, since all the devices are combined in parallel, the losses are independent of the number of devices combined. Therefore, the efficiency will depend on the careful design of the feed and collection networks to reduce power losses. Fig. 2.10 shows the concept of power combining in free space.

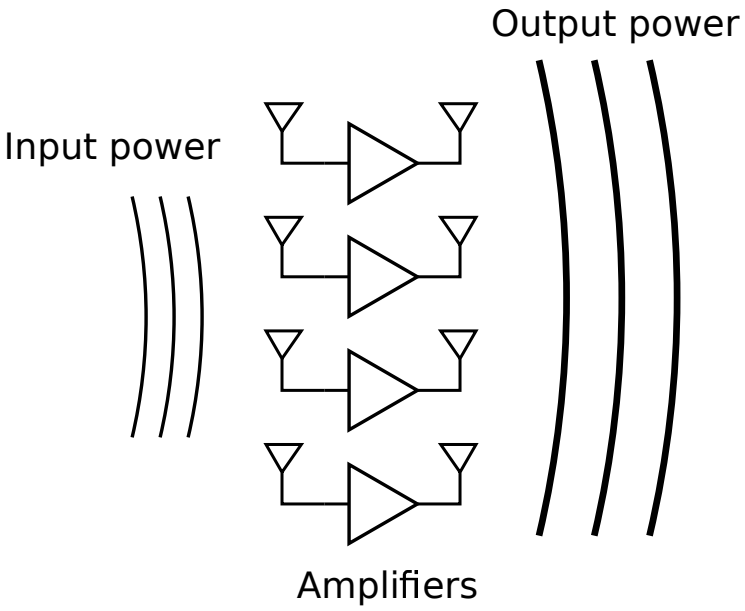

Figure 2.10: Spatial power combining concept.

The spatial power combiner types can be divided into two main categories: "tile" and "tray". The main difference between them is the distribution of the elements respect to the direction of propagation of the incident electromagnetic wave. Hence, in a tile architecture, the devices are placed in arrays normal to the direction of propagation and in the tray architecture the devices are placed in trays in a longitudinal direction.

2.4.3.1 Tile architecture

In the tile approach (Fig. 2.11), there are two main configurations that have been developed: grid and active array.

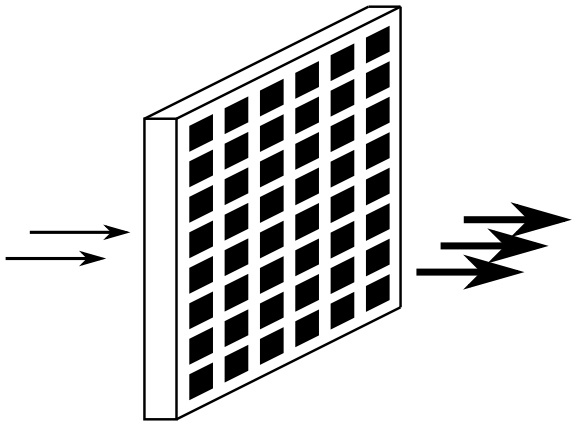

Figure 2.11: Tile architecture approach.

The first introduced was the grid amplifier in 1991 by Kim [26]. This design consist of a grid of devices connected in the intersections of a metallic mesh. Each device is a differential transistor that has its input connected to the horizontal or vertical wires and the output to the perpendicular wires. Thus, the input and output waves are in orthogonal polarization and they are isolated one from the other. A detail of the unit cell is shown in Fig. 2.12. The advantage of this design is that it can be monolithically fabricated. However, due to the small size of the cells (much lower than a wavelength), the grid wires act as a single antenna elements [27] and as a result the device size is very small limiting the gain and power.

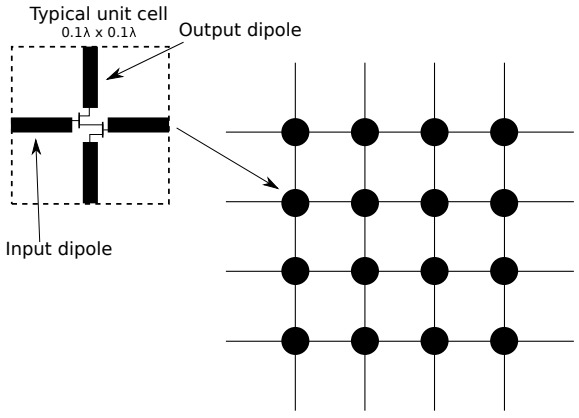

Figure 2.12: Grid amplifier cell detail.

The active antenna array is the other common tile architecture. In this design, any possibility of antenna elements (slots, patches, etc) are spaced at about half wave-

length as in a typical array. The amplifiers are connected between the input and output arrays in a similar way to the grid approach and they are also orthogonally polarized (Fig. 2.13). The bigger distance between cells allows the use of bigger devices with higher gain an power. The first design using folded slots was demonstrated by Tsai in 1994 [28]. In this work a 4x4 array is designed and it obtained a gain of 32 dB at 4.24 GHz with 8% bandwidth.

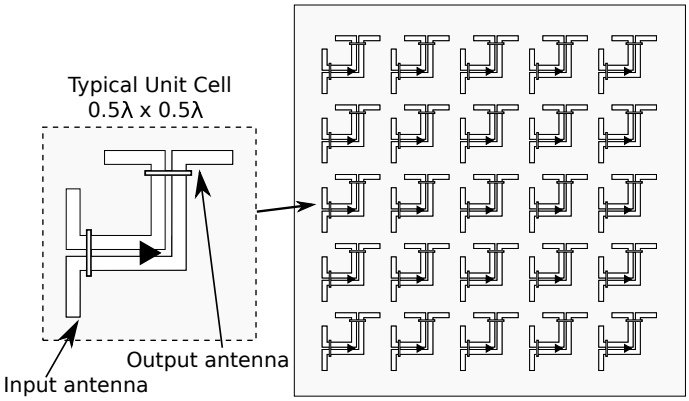

Figure 2.13: Active array amplifier cell detail.

The tile approach has the main problem of difficult heat dissipation. Since the chips are all placed in the same tile, the heat generated in the most internal devices is difficult to be removed. In addition, this design has a narrow bandwidth because the antennas used are normally resonant.

2.4.3.2 Tray architecture

This approach accommodates the active devices in trays longitudinal to the direction of propagation of the electromagnetic wave (Fig. 2.14). By using end-fire antennas the energy is coupled to the circuit placed on the trays. As a consequence of using these antennas this technique has a wider bandwidth and the heat removal is much more easier since each tray can dissipate a fraction of the total heat. The main problem of this technique is the complex assembly and bigger size compared to tile architectures. In addition, the trays are normally placed inside waveguides which does not have an uniform electric field. Therefore, the trays in the middle will saturate before the ones in the sides. Moreover, at millimetre wave frequencies, the size of the waveguides is comparable to the size of the chips and this approach is no longer a good solution as number of chips that can be combined is drastically reduced.

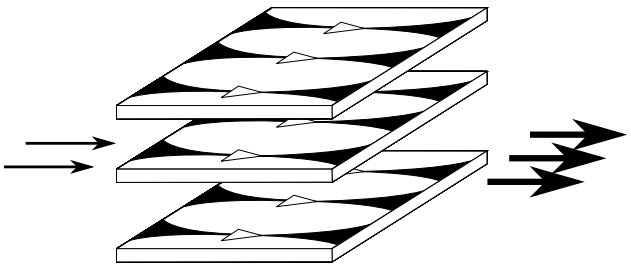

Figure 2.14: Tray architecture approach.

The idea was first proposed by Cheng in 1998 [29] and was further improved to reach 120W at X-band [30]. There has been some research to solve the illumination problem by using dielectric loaded waveguides by Belaid in 2003 [31]. At Ka-band, there are some work to use this approach but the size limitations results in low power and low device density [32] [33].

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Chapter 3

Travelling wave power combiner

3.1 Introduction

Many power combining techniques have been widely used in many different applications over the years [1, 2]. Controlling power and phase can be advantageous for phased array systems while coherent phase and equal power division are key parameters for power amplifiers in which power output depends on efficient combination of power. The most valuable application for power combiners in recent years is using this technology for building power amplifiers from solid stage devices. These amplifiers consist of many solid state chip amplifiers (usually in MMIC die form) so that its output power is comparable to that of traditional travelling-wave tube amplifiers (TWTA) [3]. For this purpose different techniques such as corporate [4], tile [5], tray [6], radial [7], travelling-wave [8] and spatial power combining [9, 10] are used. Power combining can be exploited to address limited availability and increased costs of higher power output MMICs, associated thermal management as well as to enhance graceful degradation [11, 12]. Recently, Ka-band and higher mm-wave bands are attracting interest for 5G as well as for satellite broadband applications [13], [14]. In this chapter the design and manufacturing of a 12-way travelling wave power combiner/divider consisting of a double slotted waveguide to microtrip coupling structure is described.

The main characteristics of the combiner are

- Operation at Ka-band. Center operation frequency at 30 GHz.
- Low insertion loss (IL). Efficiency higher than 80%.
- Good input matching, better than 20 dB return loss (RL).
- Equal power division at output ports.
- High order. 12 way division objective.
- Easy design and scalability.

3.2 Travelling-wave technique

Among the different possible techniques, the travelling wave power combining solution addresses the aforementioned problems by cascading a series of reflectionless unit cells accommodating the chips [15]. The possibility of easy integrating a bulk metal base in direct contact with the chips, increases the thermal management capabilities. Moreover, phase imbalance of the total back-to-back structure can be simply mitigated by connecting the divider and combiner in reverse order. This technique also benefit of simple design and scalability.

3.2.1 General Theory

This technique has been widely studied in recent years. It is mainly based in the original work by Sanada [16, 17], where coaxial probes are inserted in a waveguide to create a power divider. The design of this approach consists of N dividing cells which extract $P_{out_i} = P_{in_{Total}} \frac{1}{N}$ of the total input power (Fig. 3.1). Each one of these cells is normally designed to be reflectionless so that the interaction between adjacent cells is reduced.

The related coupling coefficients for each cell can be calculated in terms of its S-parameters. Therefore, each cell is considered as a 3-port network where port 1 is the input port, port 2 is the output port to next cells and port 3 is the coupled port which extracts the required amount of power at that stage (Fig. 3.2). Then, for an N stages power divider, the design process can be separated in the simpler design

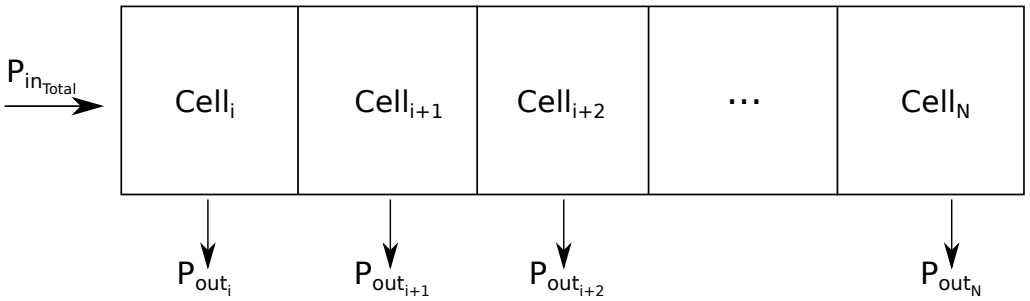


Figure 3.1: Schematic of a travelling wave power divider.

of each cell independently of the others, as long as the required S-parameters for all the cells are met. This has also an advantage which is the validity of this process regardless of the coupling structure used.

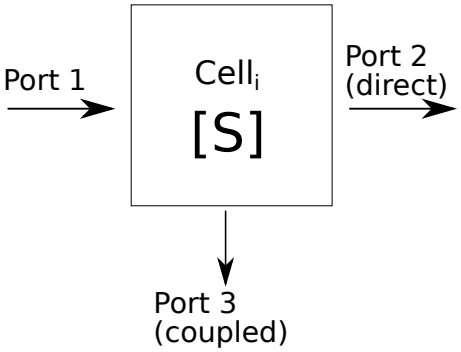


Figure 3.2: Representation of the S-parameters port network for a single cell.

The S-parameters required for an equal power division and zero reflected power at the input of each cell are [18]:

$$|S_{11}^i|^2 = 0 \tag{3.1a}$$

$$|S_{21}^i|^2 = \frac{N-1}{N+1-i} \tag{3.1b}$$

$$|S_{31}^i|^2 = \frac{1}{N+1-i} \tag{3.1c}$$

Once the coupling structure geometry has been selected, this S-parameters are calculated for each of the N cells of the design. After having all the cells designed, they are connected together to form the complete power combiner. This technique has a drawback which is the difficult control of an equal phase at the output of all the ports. This can be compensated for a single combiner/divider by adding transmission line lengths at the output ports. In the case of a power amplifier where the

dividing and combining networks must provide a perfect phase balance [19, 20], this technique provides great benefits easily compensating the phase imbalances at the output ports. By connecting the divider and combiner in a reverse order, the paths followed by the input signal throughout all the ports is the same. Therefore, the final phase at the output port of a back-to-back travelling wave power combiner is completely compensated so that:

$$\phi_{div_{itoN-i+1}} + \phi_{comb_{N-i+1toi}} = \phi_{Total} \tag{3.2}$$

Where $\phi_{div_{itoN-i+1}}$ and $\phi_{comb_{N-i+1toi}}$ are the phase delay from cell i to cell N-i+1 in the divider and from N-i+1 to i in the combiner. ϕ_{Total} is the phase delay experienced by a signal from the input port to the output port through any of the dividing/combining ports. This reverse order connection and phase compensation is shown in Fig. 3.3.

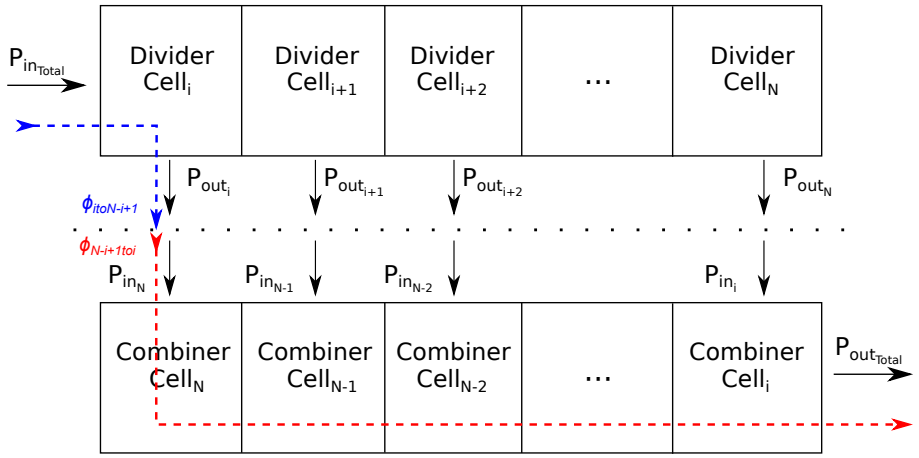


Figure 3.3: Back-to-back power divider and combiner structure. Phase path through one cell depicted.

3.2.2 Double side slotted waveguide unit cell

In many mm-wave applications mass and cost are a priority. System weight and performance can imply an important cost variation. As the final power amplification stage of a transmitter system is the main responsible for cost, compact and efficient power combiners are needed to reduce associated budget.

The following design is a new and compact travelling wave power combiner. This design is based on a waveguide structure which couples the energy to two output

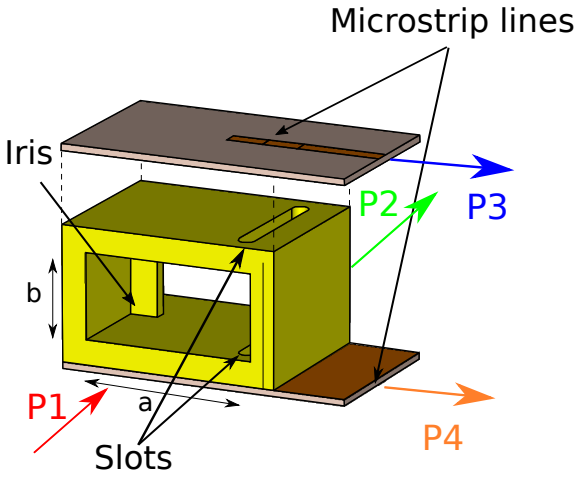


Figure 3.4: 3D model for a single cell.

microstrip ports through slots placed in the top and bottom walls of the waveguide (Fig. 3.4). Using slots to couple the required power has been previously studied by Mortazawi [21,22]. The novelty of this design compared to that one is the inclusion of a two side coupling device which doubles the number of output ports per cell [23]. Therefore, the inclusion of slots on both the top and the bottom waveguide walls provides a total length reduction of up to 50% compared to previous designs.

In each cell, a reactive element is used for controlling the power coupled to the microstrip ports as well as to improve the input matching. In this design the reactive element is an inductive iris but it is noted that any other element can be used (capacitive iris, double irises, posts, among others).

3.2.3 Cell design

This cell structure consists of a 4 port network where the coupled ports share half of the power split compared to the standard 3 ports network coupled ports described in previous sections. Therefore, in order to design this power combiner, the equations in (3.1) need to be modified to account for the extra output coupled port:

$$|S_{11}^i|^2 = 0 \tag{3.3a}$$

$$|S_{21}^i|^2 = \frac{N-i}{N+1-i} \tag{3.3b}$$

$$|S_{31}^i|^2 = |S_{41}^i|^2 = \frac{1}{2(N+1-i)} \tag{3.3c}$$

As can be seen, as the cell stage increases, the power continuing to next cells (S_{21}) decreases and the power coupled to the microstrip output ports (S_{31} and S_{41}) increases. It is noted that for the last cell all the power needs to go to the coupled ports and in cell $N-1$ half of the power needs to go to the last cell and half to the coupled ports (a quarter for each microstrip port in this design).

There are different ways of achieving the required S-parameters for the power combiner. The easiest but most time consuming strategy is brute optimisation of the geometric parameters of the coupling structure. This is very inefficient when resonant coupling structures (as in this design) are used due to the large simulation times required. A more efficient strategy is the one proposed by [16, 17]. Here the cell is represented in terms of an equivalent circuit so that the unit cell design can be divided in the separate design of its circuit elements to achieve the required coupling and matching.

The top view and equivalent circuit for a single cell is shown in Fig. 3.5. This equivalent circuit is represented in terms of admittances. When working with equivalent admittances it is convenient to normalise respect to the characteristic admittance of the line. In this case, the waveguide has an equivalent admittance that can be calculated as the inverse of the equivalent impedance [24], given by:

$$Y_0 = \frac{\sqrt{1-(\frac{f_c}{f})^2}}{\eta} \tag{3.4}$$

Where f_c is the cut-off frequency which depends on the waveguide dimensions (a and b) and the propagating mode TE_{mn} in this case) and is given by:

$$f_c = \frac{1}{2\sqrt{\epsilon\mu}}\sqrt{(\frac{m}{a})^2+(\frac{n}{b})^2} \tag{3.5}$$

In the following, all the admittances values (in lowercase) given are normalized to the characteristic admittance of the waveguide.

The slot and microstrip coupling structure are represented by an admittance which has a conductance g^i_{slot} and a susceptance b^i_{slot}. The iris admittance is represented by y^i_{iris} and it is added to the matched waveguide at port 2 to form y^i_L. Also, y^i_k is the load admittance y^i_L translated over the distance between the iris and the slot centre plane defined by a transmission line of length l^i_k. As previously said, the cells

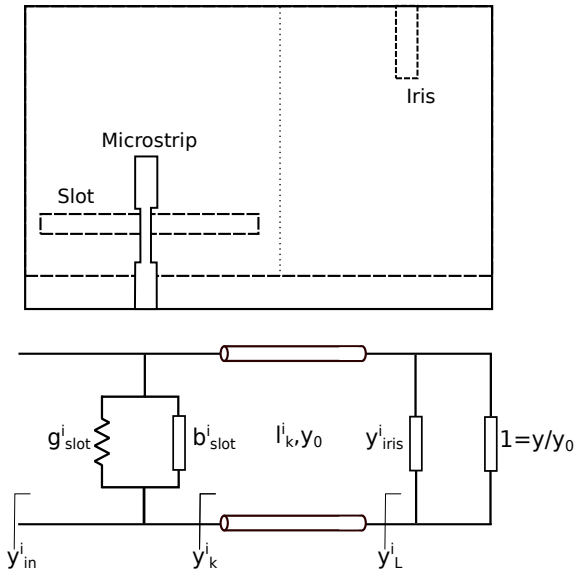


Figure 3.5: Single cell top view and equivalent circuit representation.

are designed to be reflectionless. Therefore, in terms of equivalent admittances, the the input admittance at port 1 needs to be equal to the characteristic admittance of the waveguide. This means that it is perfectly matched so:

$$y_{in}^{i} = 1 \tag{3.6}$$

The other condition required is that the power coupled to the microstrip ports and to the following stages meet the ratio defined by (3.3). This relationship is directly linked to the conductance seen at the slot plane. Therefore, the conductance needed for each cell is given by:

$$g_{slot}^{i} = \frac{1}{N - i + 1} \tag{3.7}$$

It is noted that this conductance is accounting for both slots. Since the top and bottom coupled ports are symmetric, the conductance for each of them is half of the conductance at the slot plane defined in (3.7). By controlling this conductance the power ratio extracted by the microstrip ports can be easily controlled. In order to have also a matched cell at the input, equation (3.6) needs to be met. Looking at the equivalent circuit in Fig. 3.5 it can be seen than for a perfectly matched cell the following conditions need to be achieved [15]:

$$g^i_{slot} + g^i_k = 1 \tag{3.8a}$$

$$b^i_{slot} = -b^i_k \tag{3.8b}$$

This means that the iris translated admittance over l^i_k will compensate the susceptance at the slot plane so that it becomes zero looking from the input port and also it will add the remaining conductance up to 1 which means zero reflection:

$$y^i_{in} = g^i_{slot} + g^i_k + jb^i_{slot} + jb^i_k = 1 \tag{3.9}$$

Since the admittance y^i_k does not affect the conductance of the slot g^i_{slot} as it only adds an additional conductance g^i_k, the design of the slots and microstrip lines can be independent of the iris design.

3.2.3.1 Slots and microstrip design

The design of the slots and microstrip is performed by setting the unit cell geometry in a commercially available electromagnetic simulator (CST in this case). The power coupling to the output ports is achieved by designing the slot and microstrip lines. The slot lengths can be set to half of the free space wavelength $\lambda_{free}/2$. This provides a good coupling due to the resonant operation. However, in practice this length is affected by the dielectric constant of the substrate on top of the slots which makes its length to increase. A good starting value for the slot lengths is between half wavelength in free space and half of the guided wavelength.

The microstrip line on top of the slots consist of 3 well differentiated parts (Fig. 3.6). Looking from the output port, the first line is a 50Ω microstrip line at the operation frequency. The next line is a quarter-wavelength impedance transformer to translate the impedance at the input of the third microstrip line to the matched 50Ω line. The third and last microstrip line is a another quarter-wavelength transformer ended in an open circuit. This line transforms the open circuit at the end of the line into a short-circuit at the edge of the slot so that a virtual connection between the slots and the microstrip line is created. Consequently, this short-circuit improves the power coupling between the slot and the microstrip and accordingly between

the waveguide and the microstrip line. The initial dimensions for these lines are a quarter-wavelength for both transformers and an arbitrary length for the output line since this one is matched and can be extended without affecting the results (if no losses are considered). The initial width for the three lines is set to the width of a 50Ω line at the operation frequency.

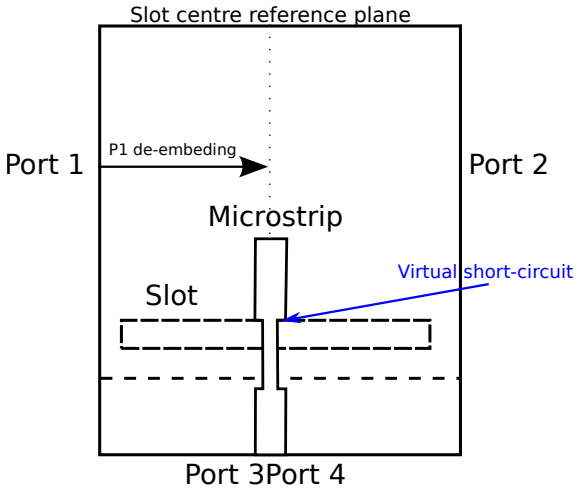


Figure 3.6: Slots and microstrip model with port 1 de-embedding plane.

Taking into account the premises above, the structure of an unit cell without the iris is simulated in a full wave electromagnetic simulator (CST in this thesis). In order to measure the conductance of the slots and microstrip lines, the input port (Port 1) is de-embedded to the slot centre plane. Therefore, the S-parameters and admittance resulting from the simulations will take into account the distance from the input to the slot centre and thus they will directly reflect the conductance at this plane. The relationship between input admittance and S_{11} for normalized admittances is given by:

$$S_{11}^{i} = \frac{1 - y_{in}^{i}}{1 + y_{in}^{i}} \tag{3.10}$$

Consequently, the input admittance that will be calculated from simulation, which is directly the admittance at the slot centre plane, can be obtained as:

$$y_{in}^{i} = \frac{1 - S_{11}^{i}}{1 + S_{11}^{i}} \tag{3.11}$$

It is important to note that the input admittance seen in the simulations will include the matched waveguide at port 2 ($y_{port2} = 1$). Thus, in order to eliminate the effect

of port 2, it is necessary to subtract its admittance from the simulated:

$$y^i_{slot} = y^i_{simulated} - 1 \tag{3.12}$$

By simulating the structure and parametrising its dimensions it is easy to map the parameter values that give the required conductance g^i_{slot} at the frequency of operation. The resulting susceptance b^i_{slot} will be compensated using the iris at the same time that the matching at the input will be controlled. In general, sweeping the structure parameters will give quick results and a set of different conductances which can be used.

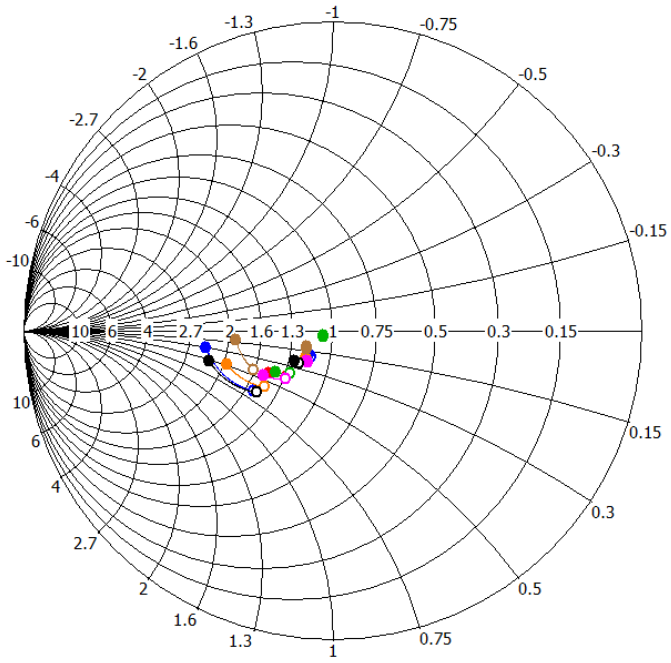


Figure 3.7: Admittances for a parameter sweep represented in a Smith chart.

Looking at the Smith chart representation of the input admittance it is very easy to see at a glance how the structure parameters affect to the resulting conductance. In Fig. 3.7 an example of the resulting admittance from a sweep plotted in a Smith chart is shown. By limiting the frequency range to the desired operation band it is easy to find the parameter set that give less variation over the required conductance at the slot plane. As discussed above, the normalized conductance in the Smith chart is greater than unity (horizontal axis) and (3.13) need to be used to calculate the slot conductance alone:

$$y^i_{slot} = y^i_{simulated} - 1 = g^i_{slot} + jb^i_{slot} - 1 \tag{3.13}$$

3.2.3.2 Iris design

Once the parameters that result in the needed conductances given by equation (3.7) have been obtained, the following step is the design of the iris and its distance to the slot plane that will meet the conditions in (3.8).

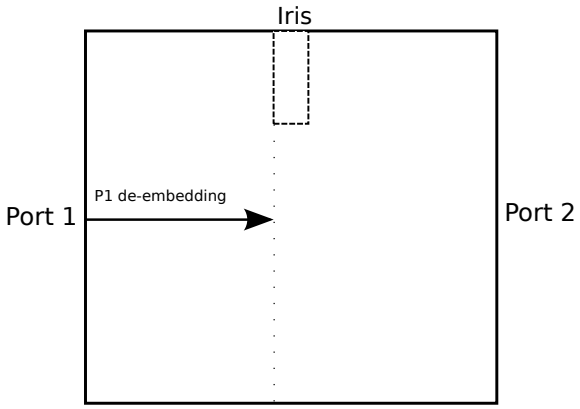


Figure 3.8: Iris model with port 1 de-embedding plane.

Following the same procedure than for the slots and microstrip structure, the iris is modelled in CST. In this case, the de-embedding of the input port is set up to the iris input plane as shown in Fig. 3.8. This will allow to calculate the admittance at this plane without the effect of the input distance to the iris.

This admittance needs to have a value such that its translation over a transmission line of length l^i_k is y^i_k, that from (3.8) is given by:

$$y^i_k = g^i_k + jb^i_k = 1 - g^i_{slot} - jb^i_{slot} \tag{3.14}$$

It is known from circuit theory that the translation of an admittance over a matched transmission line length affects only to its phase being the modulus constant [25]. This is true for a lossless scenario which is a good approximation in this case due to the short lines and the low losses for a waveguide. Therefore, knowing that y^i_k is the translated admittance, the admittance looking at the iris can be any value such that it intercepts the constant VSWR circle related to y^i_k. It is important to note here that the resulting simulated admittance at the iris includes the admittance of

the matched waveguide at port 2. Consequently, as this is going to be the real case, it is not necessary to subtract the admittance of port 2.

The VSWR circle associated to an admittance can be calculated as:

$$VSWR = \frac{1 + |S_{11}|}{1 - |S_{11}|} \tag{3.15}$$

Where S_{11} is given by (3.10). Provided that the input de-embedded admittance intersects this circle at the design frequency, its translated version will pass over the required admittance y_k^i. Thus, the iris design consists of calculating its dimensions so that its input admittance has the same VSWR than y_k^i. For an arbitrary transmission line, its input admittance depends on the load admittance and the line length and is obtained as:

$$y_{in} = \frac{y_L - jtan\theta}{1 + jy_L tan\theta} \tag{3.16}$$

Where θ is the transmission line electrical length given by:

$$\theta = \beta l = \frac{2}{\lambda} l \tag{3.17}$$

In (3.17), β is the propagation constant of the line and l is the physical length of the line. Using the above equations it is easy to see that the physical length required from the iris to the slot centre plane is given by:

$$l_k^i = \frac{\lambda_g}{2\pi} \arctan\left(j \frac{y_L^i - y_k^i}{y_L^i y_k^i - 1}\right) \tag{3.18}$$

The above procedure can be easily seen graphically using the Smith chart. In Fig. 3.9, an example of how the translation of the load admittance (including the iris and port 2 admittances) results in the required admittance y_k^i.

When designing the last cell, there are some considerations that need to be taken into account. As there are no more cells after the last one, the output port 2 will not be included. Therefore the last cell need to couple all the energy to the microstrip ports. This is seen in (3.7) where a conductance of 1 is required in the last cell. Accordingly, the power going to next stages must be 0. This is not an easy task just

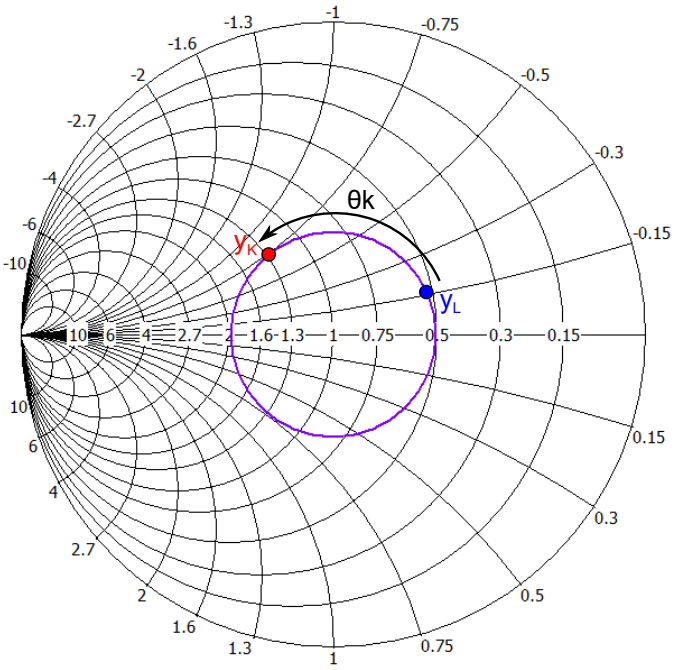


Figure 3.9: Admittance translation over a electrical length θ_k in Smith chart.

by using the standard cell geometry as the coupling needed is very high. In order to achieve these 2 conditions, a short-circuit after the last cell is used. Normally, the distance is set at a guided quarter-wavelength from the slot centre so that the maximum electric field is located at the slot plane, thereby improving the coupling.

After obtaining the dimensions for the separate microstrip, slot and iris, they are connected to form the resulting cell. If the design process has been carried out, the resulting S-parameters will be the calculated in (3.3).

3.2.4 Complete power divider/combiner

The complete power divider is modelled by cascading all the units cells and simulating the whole structure. Since the unit cells are reflectionless, intermediate lengths can be included in between adjacent cells if needed. These lines can be of arbitrary length with no effect in the total behaviour, provided that higher order waveguide modes of the slots and the iris can not interact between cells. This can be very useful if more separation between the output microstrip port is needed to accommodate possible planar circuits or biasing circuitry in case of active circuits as power amplifiers.

3.3 Design of a 12-way double slotted waveguide power combiner

Following the procedure described in previous sections, a 12-way power combiner to operate in the 29-31 GHz band have been designed and manufactured. In the next sections the design is described and simulated results are presented. Also, the manufacturing and measuring of a first prototype is described.

3.3.1 Unit cell simulations

The number of output ports for this combiner is 12. Considering that each cell includes 2 output ports, this results in a power combiner number of cells of $N = 6$ (Fig. 3.4). Using the design equations in (3.3) to calculate the S-parameters objective for each cell, we obtain the theoretical values shown in Table 3.1.

Table 3.1: S-parameters objective for a N=6 cell design

Cell number	1	2	3	4	5	6
$\mathbf{S_{21}}$ **(dB)**	-0.7918	-0.9691	-1.2494	-1.7609	-3.01	No port
$\mathbf{S_{31} = S_{41}}$ **(dB)**	-10.7918	-10	-9.0309	-7.7815	-6.0206	-3.01

These values can are represented are Fig. 3.10, where it can be seen the evolution of the coupling coefficients respect to the cell stage. As previously discussed, the coupling to the microstrip ports increases with i and the power to the next stages decreases with i accordingly.

These are the S-parameters that will need to be achieved for each cell. The related required conductances for a 6 cell design given by (3.7) are shown in Table 3.2.

Table 3.2: Conductances required at slot plane for N=6 cell design.

Cell number	1	2	3	4	5	6
$\boldsymbol{g^i_{slot}}$	1/6	1/5	1/4	1/3	1/2	1

Once the required values of conductances and S-parameters have been calculated, the design can start. The operation frequency band for this design is Ka-band (26.5 - 40 GHz). Since this prototype main purpose is to manufacture a power combining

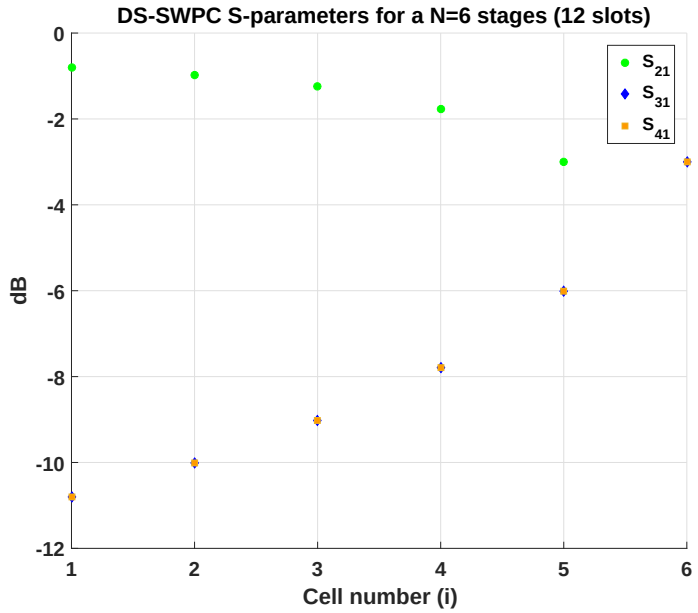


Figure 3.10: Coupling S-parameters for a double side slotted waveguide power combiner and N=6 cells.

amplifier for a block up-converter which output frequency is 30 GHz, this will be the centre frequency and a 29 to 31 GHz bandwidth considered since it is a typical Ka-band satellite band. At this frequency band the dimensions of a standard WR28 air-filled rectangular waveguide are shown in Fig. 3.11. For this waveguide and at 30 GHz, the equivalent admittance is $Y_0 = 0.001889S$ calculated from (3.4) for the propagating fundamental mode (TE_{10}). The guided wavelength is $\lambda_g = 14.04$ mm. The cell length is set to half of the guided wavelength $Cell_{L_i} = 7.02$ mm. The short circuit at the last cell can't be a quarter wavelength since it would be inside the cell length and will interfere with the iris. Therefore, an additional length of $\lambda_g/2$ is added resulting, after optimisation, in a 8.5 mm waveguide. In order to reduce future manufacturing complexity, the slots are all set to have the same width of 0.51 mm so that a single size cutter can be used.

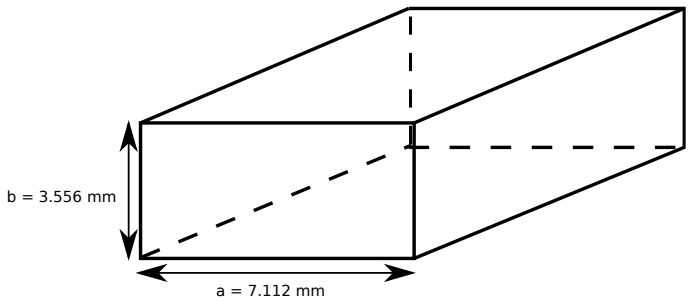


Figure 3.11: Standard WR-28 Ka-band waveguide dimensions

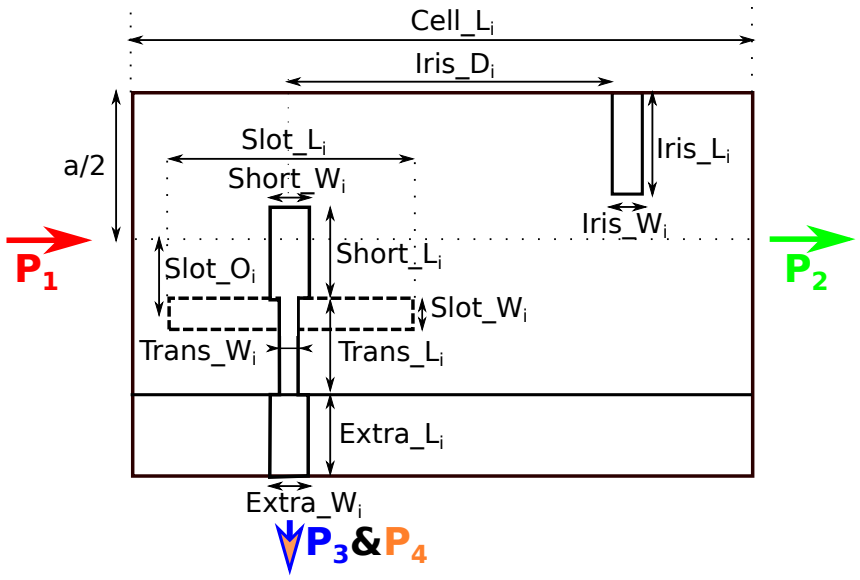


Figure 3.12: Geometric parameters used for the designed single cell.

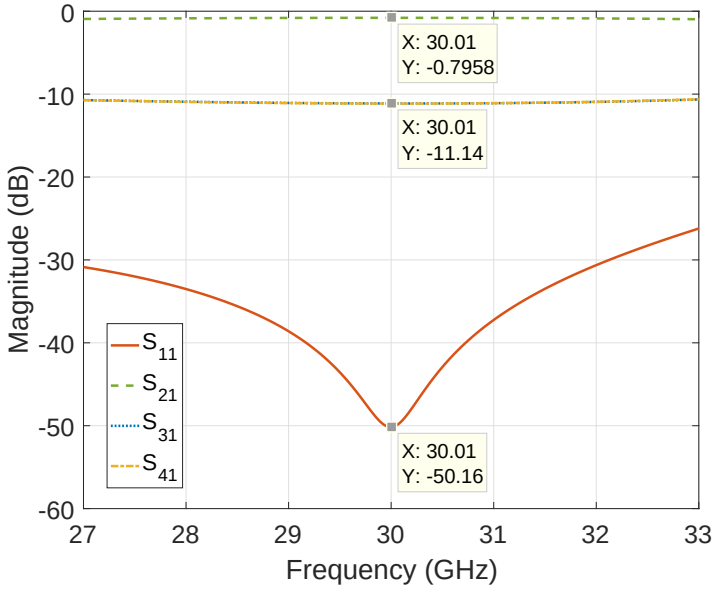
Table 3.3: Rogers RT/Duroid 6002 characteristics

ϵ_r	Thickness	Cladding	$tan\sigma$
2.94	250 um	18 um	0.0012

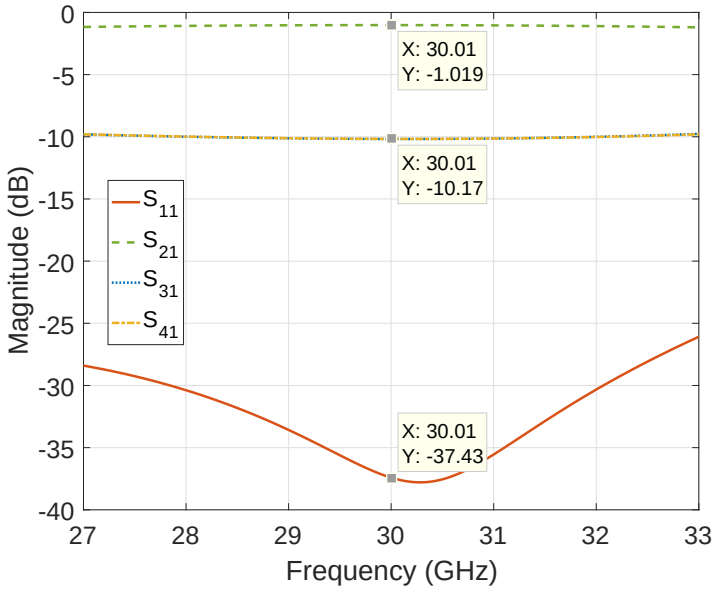
Before starting the simulations, the unit cell is constructed in CST. At this point, it is necessary to design the 3D model including parameters that can be swept in order to analyse their effect on the unit cell behaviour. In Fig. 3.12, a description of all the parameters selected for the simulation is shown. For each microstrip section the widths (W) and lengths (L) can be controlled. The input matched microstrip line name is *Extra*. The fist quarter-wavelength transformer name is *Trans* and the open circuited line is *Short*. Regarding the slot, the parameters are the offset from the waveguide centre ($Slot\_O_i$) and its width ($Slot\_W_i$) and length ($Slot\_L_i$). Additionally, the length of the cells is represented by ($Cell\_L_i$), the distance between the iris and the slot centre is ($Iris\_D_i$) and finally the iris dimensions are its width ($Iris\_W_i$) and length ($Iris\_L_i$). In order to account for the future manufacturing, the inner corners of the irises are rounded to 1 mm diameter that will be used as cutter in the milling process. In this design, the microstrip lines are designed using a Rogers RT/Duroid 6002 substrate (Table 3.3). This substrate has a high thermal conductivity which will allow the heat of the amplifiers to dissipate more easily.

By separating the slots and microstrip lines from the iris and doing sweeps of these geometric parameters, a set of dimensions that map to the required slot conductances

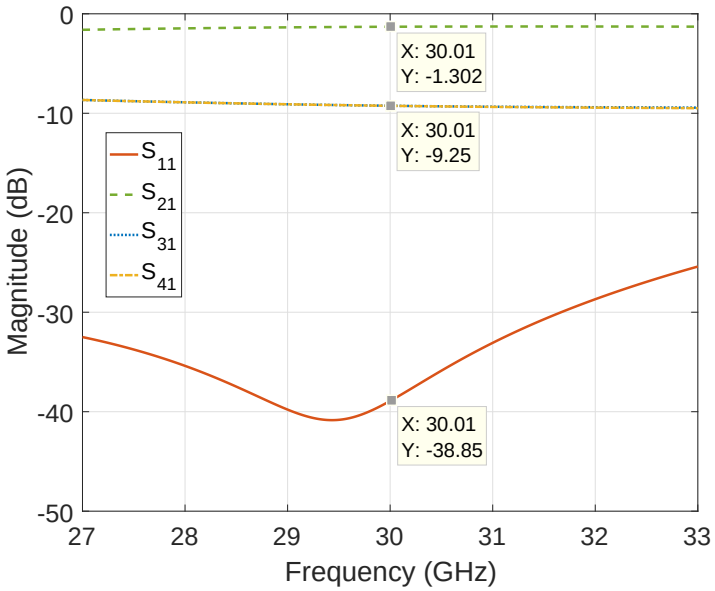
can be easily achieved. After having the dimensions that give the slot conductances required for each cell, the irises are included and each cell is made reflectionless following the design process described above. Ultimately the initial values obtained by this process yield good response and some limited optimization of the entire combiner may be required. The final S-parameters for each cell after optimisation are shown in Fig. 3.13. The results are very close to the theoretical desired values. The bigger difference appears at the last cell. This is because of its resonant nature due to the short circuit and the standing wave generated to have the maximum electric field at the slots plane.



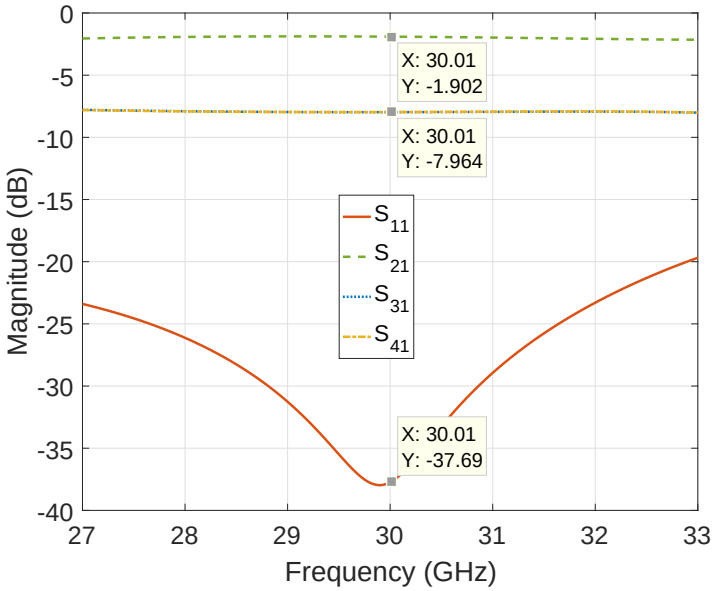
(a) Cell 1 S-parameters



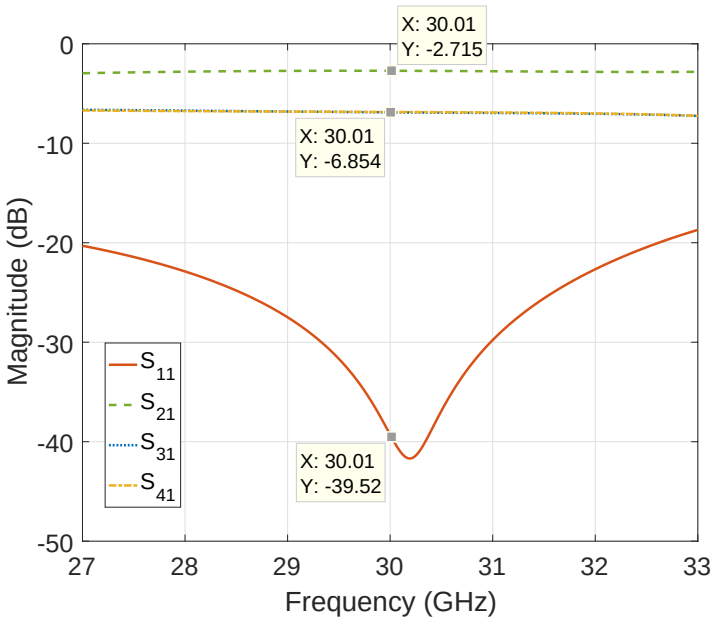
(b) Cell 2 S-parameters



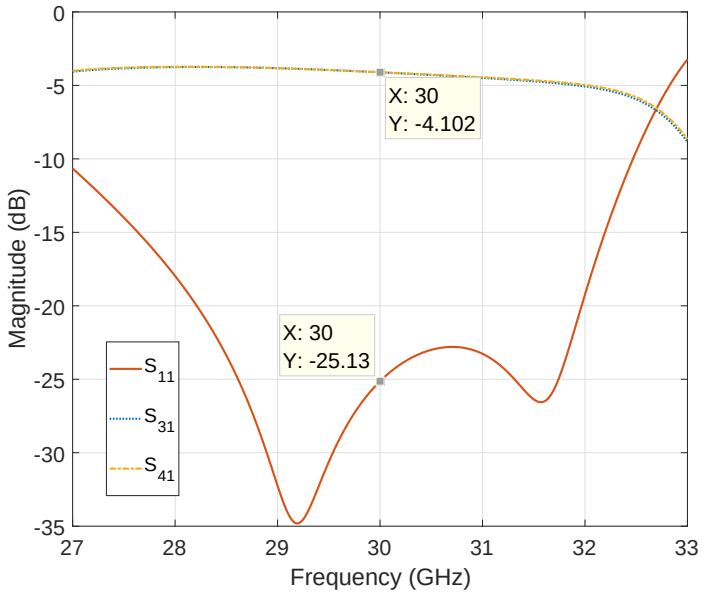
(c) Cell 3 S-parameters



(d) Cell 4 S-parameters



(e) Cell 5 S-parameters



(f) Cell 6 S-parameters

Figure 3.13: Optimised final S-parameters for the N=6 power divider/combiner.

3.3.2 Complete simulated power divider/combiner

When all the cells are optimised, the complete power combiner is simulated by putting together all the cells. Additional waveguide lengths between unit cells are included to provide space for placing the amplifier chips and biasing circuitry. The length of the lines added is 11.25 mm. The resulting 3D model of the power combiner is shown in Fig. 3.14 and the final prototype dimensions are listed in Table 3.4.

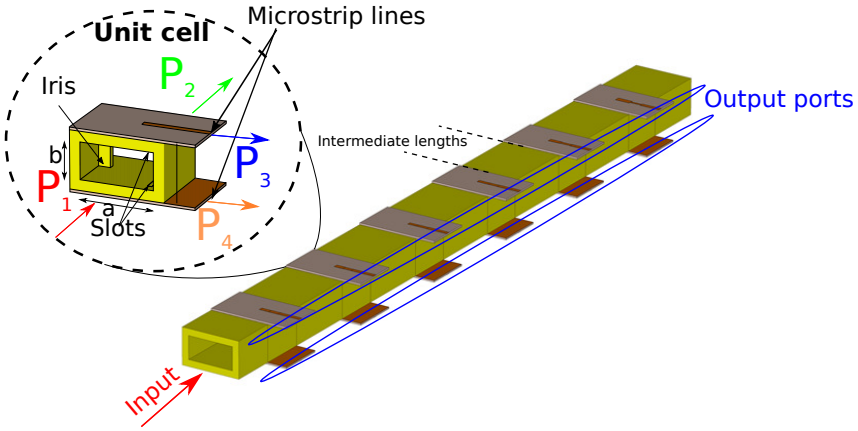


Figure 3.14: 3D view of the complete divider/combiner including intermediate lengths. Detail of a single cell depicted.

The simulated S-parameters for the complete power combiner are shown in Fig. 3.15.

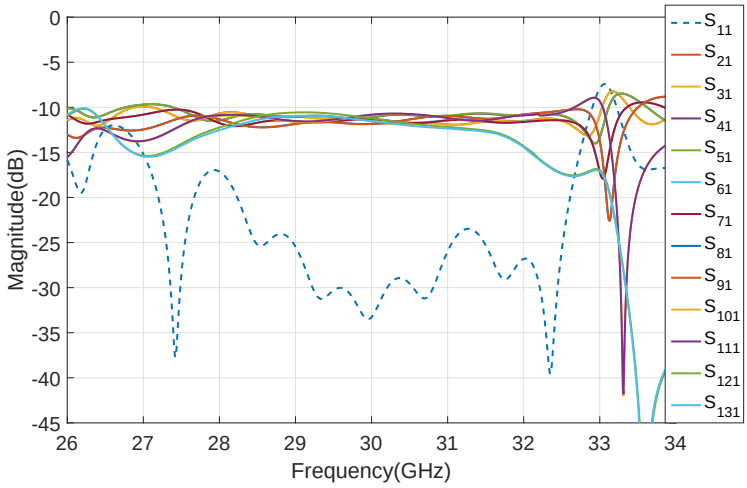


Figure 3.15: Simulated S-parameters for the final power divider/combiner.

These results show a simulated return loss below 20 dB from 28.3 GHz to 32.5 GHz, having a minimum in the operation band of -33 dB at 30 GHz. The simulated insertion loss for the output ports is related to the power division ratio. The result obtained is stable around the theoretical value given by (3.19) from 28 to 31.5 GHz.

$$S_{1k}(dB) = 10log_{10}(\frac{1}{2N}) = -10.79 \tag{3.19}$$

In terms of phase response, this designs has the disadvantage of not having a coherent phase at the output microstrip ports (Fig. 3.16). However, as discussed above, this can be easily compensated in a back-to-back structure [26].

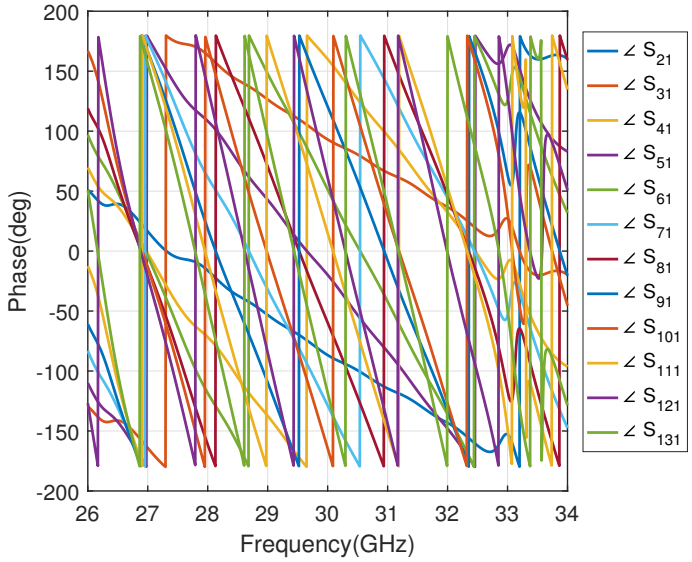


Figure 3.16: S-parameters phases. The phase at the microstrip output ports is not compensated for a single power divider/combiner.

3.3.3 Back-to-back power combiner simulations

To create a power combiner amplifier, a power divider and a power combiner need to be connected in a back-to-back structure where the amplifier chips (usually in MMIC dies for high frequency applications) are accommodated. In this design, the chips will be directly connected at the output microstrip ports. This connexion can be done in different ways depending on the type of packaging of the chip. Additionally, this lines have high losses at 30 GHz. Therefore they have a direct influence in the power efficiency of the device.

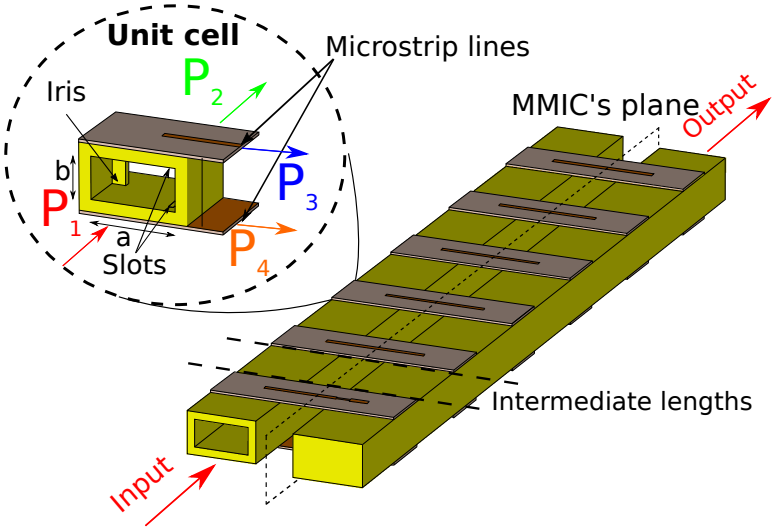


Figure 3.17: 3D simulated model of the back-to-back power divider/combiner.

Table 3.4: Final parameter dimensions for the designed power divider/combiner.

Cell number	**1**	**2**	**3**	**4**	**5**	**6**
Slot_L	5.297	5.777	5.769	5.901	6.087	6.258
Slot_W	0.51	0.51	0.51	0.51	0.51	0.51
Slot_O	2.881	2.795	2.860	2.795	2.926	2.945
Short_L	1.555	1.366	1.410	1.792	1.860	2.298
Short_W	0.618	0.701	0.554	0.585	0.679	0.810
Trans_L	1.491	1.317	1.630	1.481	1.671	1.776
Trans_W	0.648	0.595	0.567	0.569	0.501	0.351
Extra_L	3	3	3	3	3	3
Extra_W	0.63	0.63	0.63	0.63	0.63	0.63
Iris_D	0.483	0.608	0.809	1.027	1.380	0.788
Iris_L	1.148	1.134	1.009	1.361	1.7	1.5
Iris_W	0.567	0.643	1.484	1.027	1.158	1.033

Distance between divider and combiner can be extended arbitrarily since the output lines are matched to 50Ω. However, in order to keep losses as low as possible this lines will be the shortest that leave enough space for the required biasing and RF circuitry for the chips.

In order to evaluate the performance in a power combining amplifier scenario, simulations have been carried out for the passive structure. The simulated geometry consists of a back-to-back power combiner connected in a reverse order. Hence the first cell of the divider is connected to the last cell of the combiner and successively. The 3D model of the complete device is shown in Fig. 3.17.

The simulated results of the back-to-back structure are shown in Fig. 3.18. The simulated insertion loss (IL) at 30 GHz is 1.26 dB. The minimum IL in the band of interest of 29-31 GHz is at 29 GHz with a value of 1.19 dB. The maximum IL is at 31 GHz with a value of 1.39 dB. The simulated loss of the back-to-back structure is composed of the losses due to the divider and the combiner together. As a result, the insertion loss of a single combiner is half of the simulated for a back-to-back device. In this case this is 0.595 dB for the minimum IL.

One of the key performance parameters of a power combiner is its combining efficiency [27]. This is directly related to the insertion loss of the power combiner

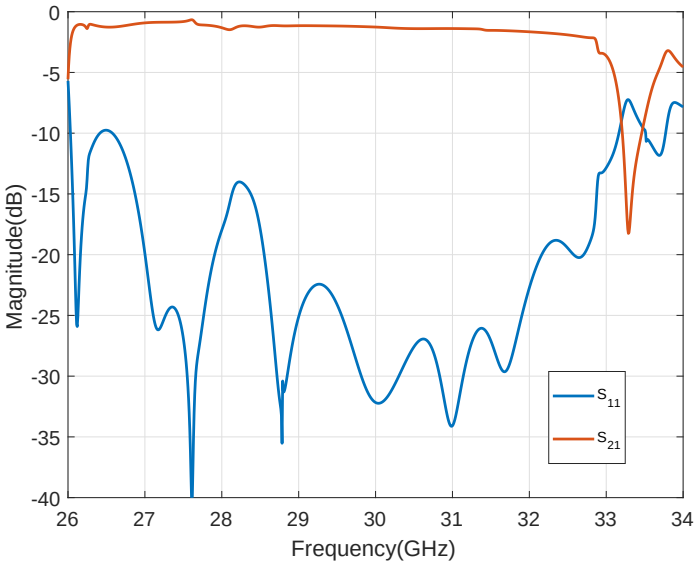


Figure 3.18: Simulated S-parameters for the back-to-back device.

(IL_{comb}), and for this design it has a minimum value given by:

$$\eta_c = 10^{\frac{-IL_{comb}}{10}} = 87.2\% \tag{3.20}$$

The simulated 3-dB IL bandwidth is 6.5 GHz, resulting in a relative 21.7% from 26.5 GHz (Ka-band cut-off frequency) up to 33 GHz. As discussed above, the unequal phase delay at the microstrip output ports can be easily compensated by connecting the divider and combiner in a reverse order. This is shown in Fig. 3.19 where the phases for the back-to-back structure through each cell are shown.

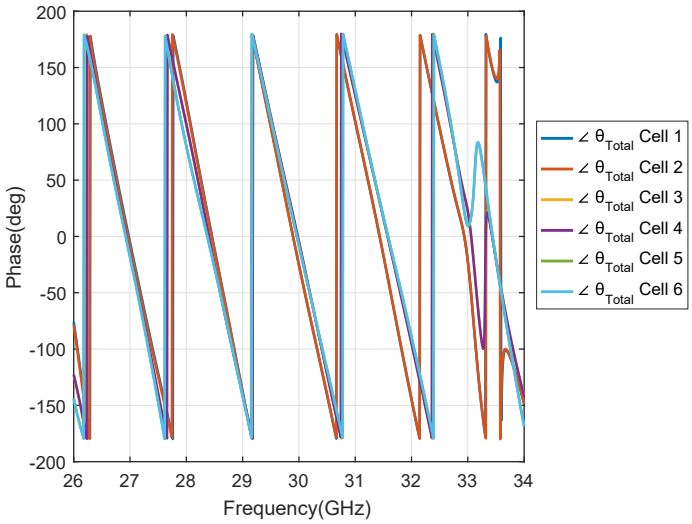


Figure 3.19: Total phase delay through each cell.

3.4 Prototype and Experimental Results

In order to validate the design simulations, a prototype of the power divider/combiner is manufactured and measured. Fabrication at high frequencies is not an easy task to accomplish. Small component sizes and tolerance issues become a big challenge to achieve accurate results. In this section, a description of the manufacturing process and considerations taken into account are shown. First, the waveguide structure is described. Secondly, the PCB manufacturing process is detailed. Finally, measured results of the prototype are discussed.

3.4.1 Metal manufacturing

As a first step, the central structure containing the waveguide sections of the power combiner needs to be manufactured in a metal block. The electrical performance, weight and robustness of the prototype will mainly depend on the type of metal used for the manufacturing. Typically, metals used for manufacturing waveguides are brass, aluminium and copper, although in general any material can be used as long as it has a good conductivity. Alternatively, it is even possible to fabricate waveguides made of plastic with internal walls plated in metal.

The most common material in commercially available waveguides is brass . However, for this prototype the material used is aluminium due to its lower weight and its softer structure, which allows easier cutting of the material in a Computer Numeric Control (CNC) machine.

3.4.1.1 3D modelling of the prototype

Considering that the microstrip lines are going to be placed on top and bottom of the waveguides, these sides of the structure need to be clear of any extra material. Therefore, reinforcement walls are added in the waveguide sides which give the structure enough robustness for the purpose and a good heat sink for thermal dissipation. Additionally, the space in between the divider and combiner waveguides is also filled with metal. The 3D modelled structure to be manufactured including the PCBs is shown in Fig. 3.20.

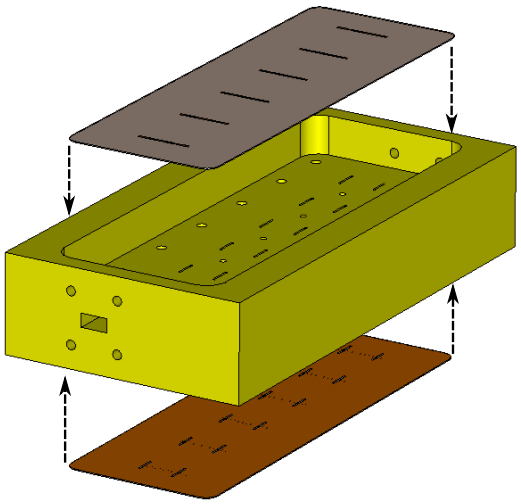


Figure 3.20: 3D model of the prototype manufactured.

In order to connect the prototype and perform measurements, the input and output port connectors are designed as WR-28 Ka-band flanges denoted by the standard UG599/U (Fig. 3.21). The dimensions for this standard flange are given in Table 3.5.

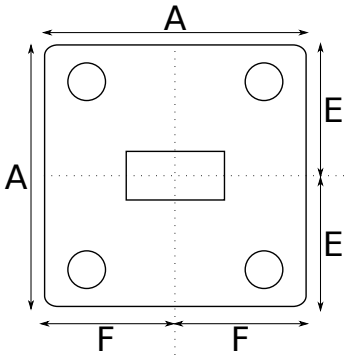


Figure 3.21: UG599/U flange standard for WR-28 waveguides.

Normally, it is necessary to manufacture a waveguide in at least 2 pieces which will be joint to close the cavity. In general, it is beneficial to cut the waveguide in the vertical propagation plane so that the current distribution in the structure is not obstructed. However, due to the geometry of this design and the necessity to attach the top and bottom PCBs, this solution is not valid. Consequently, an alternative horizontal plane cutting was used.

Since the waveguide has vertical irises inside, a cut at half the height would require a very accurate milling precision in the top and bottom metal parts and in addition a good iris an slot alignment. On the other hand, tolerances and alignment needs can

Table 3.5: UG599/U flange dimensions

Dimension	**inches**	**mm**
A	0.75	19.05
E	0.265	6.73
F	0.25	6.35
Hole Diametre	0.116	2.98

be reduced by milling the whole waveguide cavity but the top wall in a single piece of metal. As a result, the iris alignment is eliminated and the top wall containing the slots is used to close the cavity as a lid [28]. A 3D representation of the 2 pieces resulting from this cutting strategy is shown in Fig. 3.22. As can be seen, the waveguides are closed by the top lid using additional holes for screws. The diameter used was 1.6 mm (M1.6) for the centre ones (in between the slots) and 2.5 mm (M2.5) for the side ones. The size of the centre screws is the most critical since they need to leave enough space for the biasing circuitry of the amplifier chips.

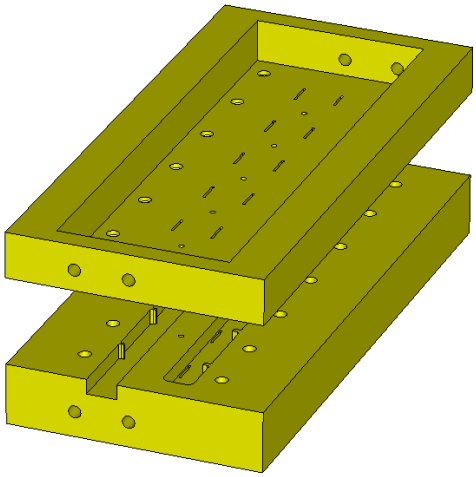


Figure 3.22: 3D model of the waveguide cutting strategy.

3.4.1.2 Aluminium prototype

Once the 3D model of the prototype is finished, it is manufactured using CNC machining. It is important to note that any inner corners produced by this manufacturing technique can not be right angles due circular shape of the cutter. Consequently, this needs to be accounted for in simulations and therefore this design considers 1 mm diameter cutters for the irises and waveguides.

For the slots, a 0.5 mm diameter was selected in the simulation to eliminate the need to change the cutter. The manufactured prototype is shown in Fig. 3.23. In order to have a better pressure and electrical contact some additional screws were added in the side walls of the structure.

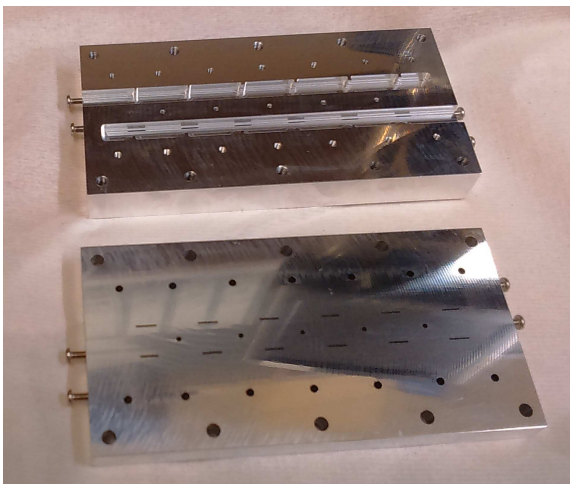


Figure 3.23: Photo of the manufactured prototype showing the 2 separated pieces.

In Fig. 3.24 a detail of the slot, iris and short circuit at the last cell are shown. As can be seen, the diameter for the short circuited waveguide inner corner is bigger as this is not so critical as the rest. This diameter was selected to be 3 mm.

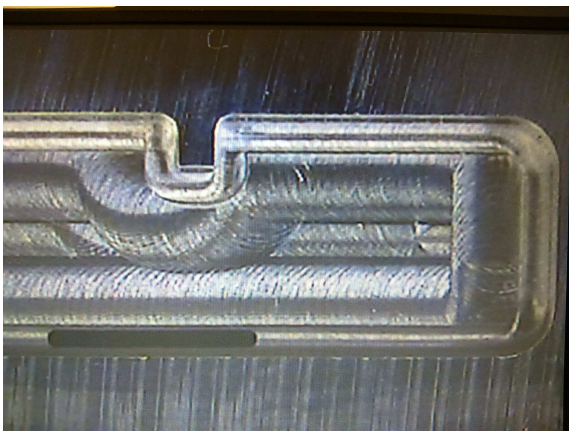


Figure 3.24: Detail photo of the slot, iris and short circuited waveguide corners rounded under the microscope.

3.4.2 PCB manufacturing

Once the aluminium waveguides are manufactured, the PCBs containing the microstrip lines are fabricated. The selection of the substrate needs to take into account the applications in which it will be used. Hence, as this is a temperature changing application, the substrate used is the Rogers RT/Duroid 6002 mentioned above in Table 3.3. This substrate is designed to have the same thermal coefficient than copper so that it is suitable for applications with changing temperature conditions. Therefore it is a good choice when working with power amplifiers, space applications or any other demanding application such as military circuits.

At high frequencies as in this case, the tolerances associated to the manufacturing process have a critical impact in the final performance of the circuit. Among different techniques available for manufacturing microstrip circuits, the photo etching can yield very good tolerances down to 25 um. On the other hand, the small substrate thickness make other techniques such as PCB milling very difficult due to the need to keep the substrate flat. Therefore, photo etching is used for this prototype.

Given the necessity of attaching the PCBs to the top and bottom of the waveguide metal structure, the same screw holes that are drilled in the waveguide are made in the PCBs. As a result, the PCBs will be kept flat on the metal structure and a good electrical contact will be achieved.

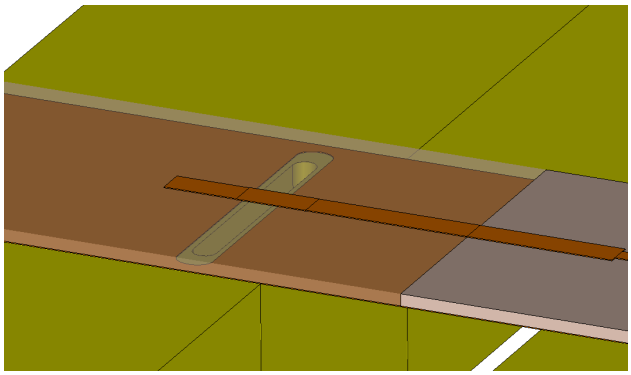


Figure 3.25: 3D model representation of the PCB ground plane slot size increment.

Since the slots of the waveguide need to couple to the microstrip lines, the same slots need to be manufactured in the ground plane of the substrate. As the alignment of the PCBs using screws could not be very accurate, some simulations increasing the slots size in the ground plane are carried out to check if some tolerance reduction

can be made with this technique (Fig. 3.25). Simulated results in Fig. 3.22 show that the difference in performance when increasing the ground plane slots size is minimum and this will be taken for the PCB manufacturing.

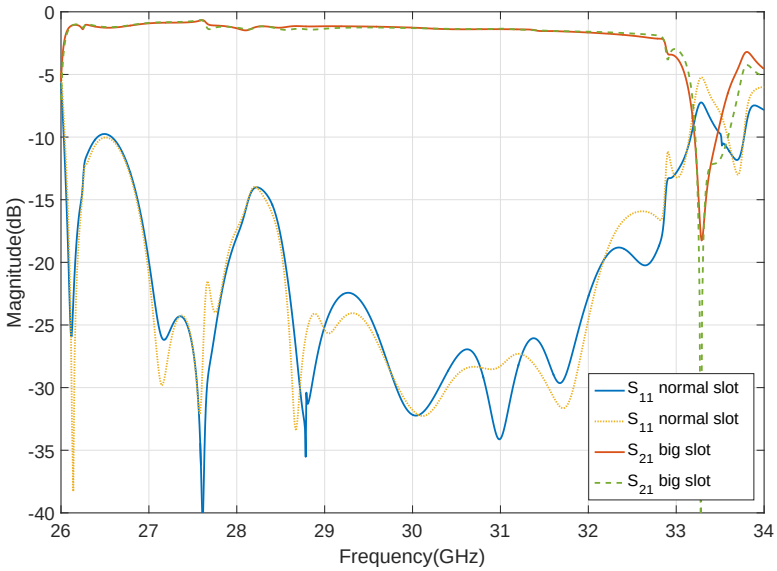


Figure 3.26: S-parameters comparison with increased slot size in the PCB ground planes.

The manufacturing steps are as follows:

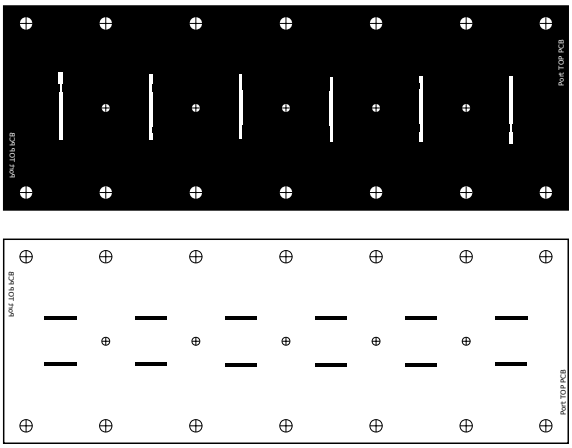
- Export .dxf files of the top and bottom PCBs.
- Create masks using a vectorial drawing tool from the .dxf file.
- Align top and bottom masks containing microstrip lines and slots respectively.
- Photo etching of the masks into the substrate.
- Hole drilling to attach the PCB on the waveguides.

3.4.2.1 Mask printing

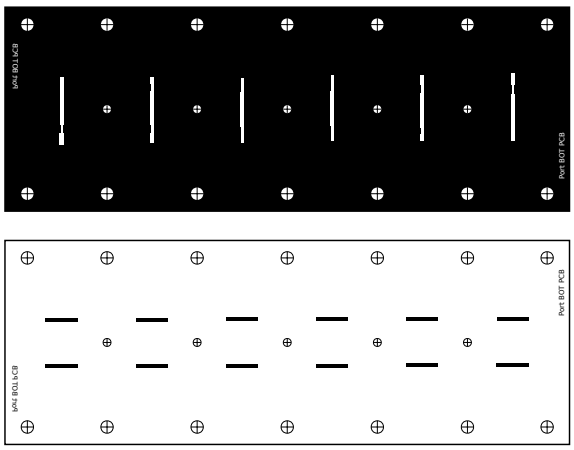
The masks for the top and bottom PCBs are imported as a .dxf file to a vector graphic editor and they are modified accordingly to be printed. In order to do this, the parts where the copper needs to be are left blank and the parts where the copper needs to be removed are filled by black. The etching applies an UV light that hardens the white parts and then some chemicals are used to remove the unexposed copper in the black parts. Each PCB has 2 masks, one for each side of the substrate.

The top mask includes the microstrip lines and the bottom mask includes the slots. Moreover, these top and bottom masks need to be well aligned so that once they are etched the slot and microstrip lines match to the waveguide slots. Therefore, additional alignment crosses inside the screw holes are drawn that help positioning the masks in the correct place.

The resulting top and bottom PCB masks are shown in Fig. 3.26. It is noted that when the mask are printed, for a better tolerance results, the ink side of the transparency is facing the substrate when the UV light is applied. In consequence, the masks need to be flipped horizontally or vertically to account for this.



(a) Top PCB masks for manufactured prototype.

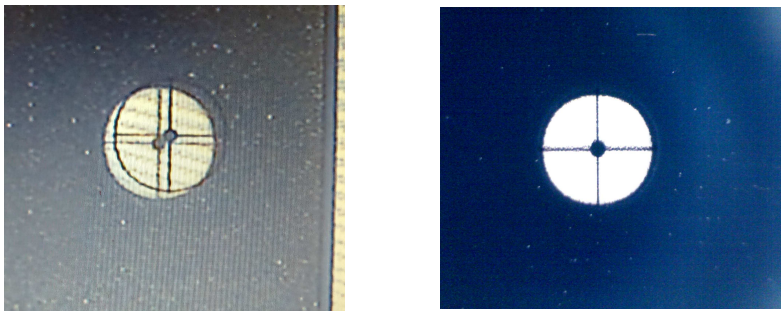


(b) Bottom PCB masks for manufactured prototype.

Figure 3.26: Masks for manufactured prototype. Each PCB has a top and bottom mask containing microstrip lines and ground plane slots respectively.

3.4.2.2 Mask alignment

As discussed above, the alignment of the top microstrip and bottom ground plane masks is very important in order to have a good PCB result. The addition of crosses in the middle of the screw hole positions has a double advantage. First, it provides a good way of aligning the masks under the microscope as can be seen in Fig. 3.26. On the other hand, they mark the centre point to drill the screw holes.



(c) Unaligned PCB. (d) Aligned PCB.

Figure 3.26: Mask alignment process under the microscope.

Once the alignment is achieved, the masks are hold in place using tape. It is important to leave enough space from the masks to the tape to avoid bending the mask when the substrate is inserted in between for etching. This can be seen in Fig. 3.27 where an example of a finished mask ready to be used is shown.

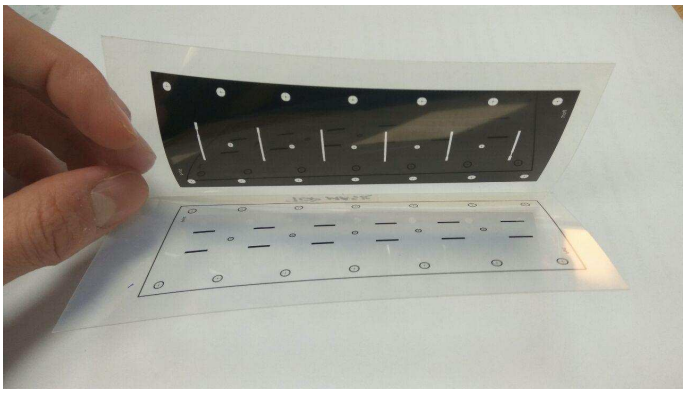


Figure 3.27: Finished mask ready to be used for etching.

3.4.2.3 PCB drilling

After the PCBs are etched, the last manufacturing step is to drill the screw holes in order to attach the PCBs on the waveguide. This is done using a drilling machine

with microscope camera, which allows a very high precision and reduced misalignments of the PCBs with the waveguide slots (Fig. 3.28).

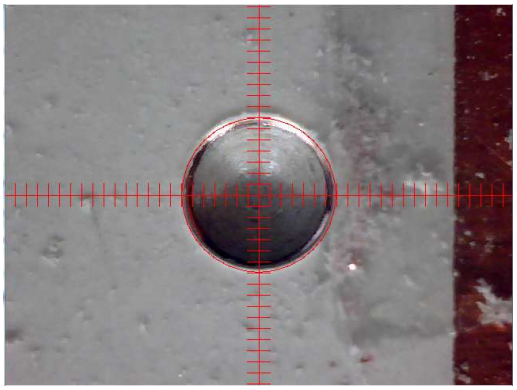


Figure 3.28: Photo after drilling a hole under the machine's microscope camera.

Once all the process is finished, the final PCBs are ready to be attached to the waveguides. Fig. 4.18 shows he aspect of a final PCB manufactured.

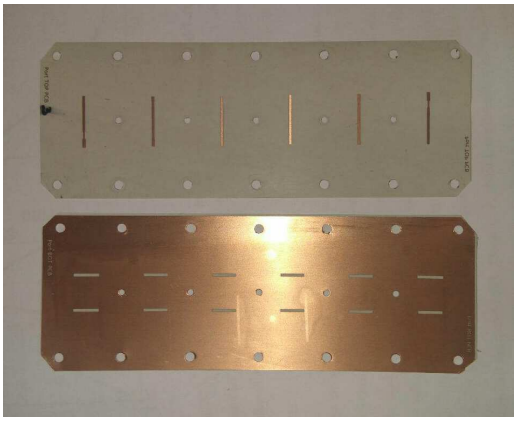


Figure 3.29: Example of a final PCB manufactured. Top side contains microsrip lines. Bottom side contain slots.

3.4.3 Measurements

With the waveguides and PCBs manufactured, the next step is to attach the PCBs and do measurements to evaluate the performance of the prototype. The correct alignment and flatness of the PCBs in their position on top of the slots is critical in order to achieve a good response. The technique chosen here is the use of the same screws that are used to close the cavity in order to keep the PCBs aligned and making a good flat contact with the aluminium. Additionally some epoxy glue could be used in between to improve electrical conductivity. However, in this prototype,

no intermediate glue was used in order to have an easier detachment of the PCBs for possible future tests. In Fig. 3.30 a photo of the assembled built prototype is shown. As can be seen, some washers were added to avoid scratches and wrinkles in the PCBs.

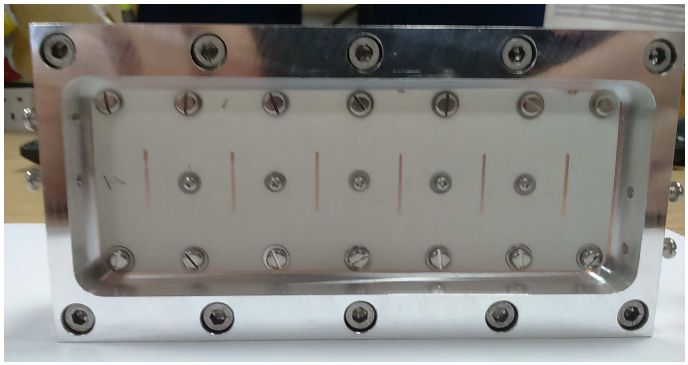


Figure 3.30: Photograph of the assembled prototype.

Measurements are carried out in the laboratory using a PNA network analyser N5225A. First the calibration is performed to have a reference plane at the output of a WR-28 waveguide flange. Before measuring the complete prototype, the S-parameters with no PCBs attached are measured. As a result, uncertainties due to bad milling manufacturing are reduced. A comparison between measured and simulated results for the waveguides only is shown in Fig. 3.31.

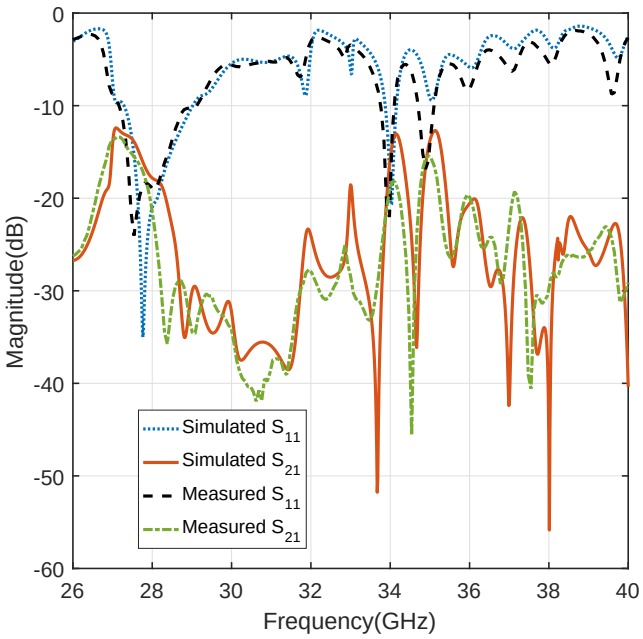


Figure 3.31: Measured and simulated S-parameter results for the waveguides without PCBs attached.

It can be seen that a good agreement between simulated and measured results are obtained. Consequently, the measurement of the prototype will be accurate regarding the waveguide structure.

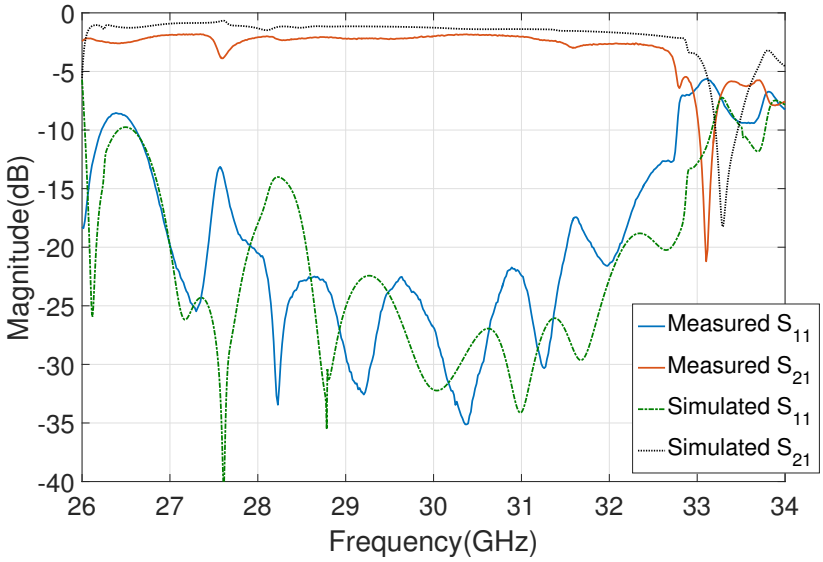


Figure 3.32: Measured and simulated S-parameter results.

A comparison between measured and previously discussed simulated results is shown in Fig. 3.32. The measured return loss (RL) is better than 21 dB within the design band and the minimum IL is 1.83 dB at 30.4 GHz. As a result, this value corresponds to a peak measured combining efficiency of $\eta_{c_{max}} = 81\%$. The measured 3-dB IL bandwidth is 6.25 GHz (from 26.5 GHz up to 32.75 GHz), corresponding to a fractional value of 20.8 %. The small differences between simulated and measured results are attributed to tolerances in fabrication. Additionally, Fig. 3.33 shows the IL in more detail.

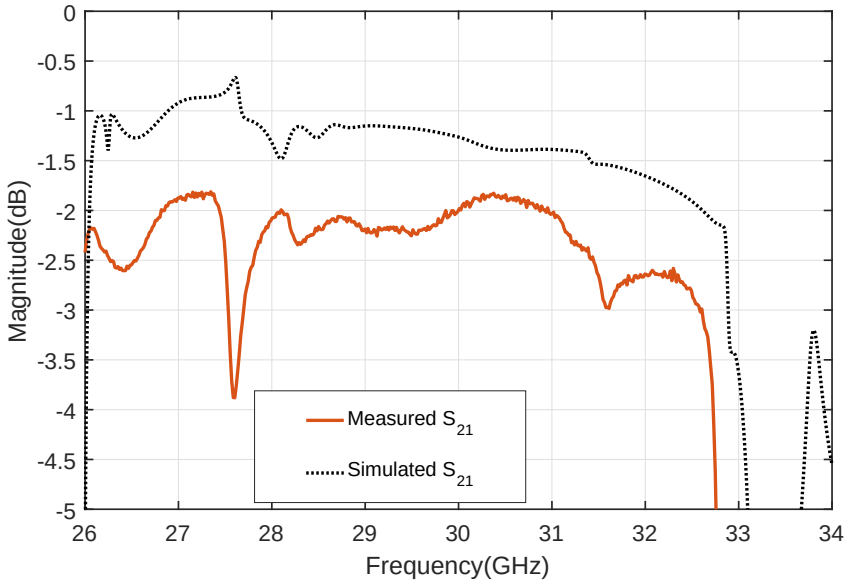


Figure 3.33: Insertion loss in more detail.

3.5 Conclusions

In this chapter, a novel compact power combiner for designing travelling wave power combining amplifiers has been presented. This design is based on a double side slotted waveguide structure. Design guidelines for a general travelling wave power combiner composed of reflectionless cells have been given. Furthermore, adapted equations and design for the proposed combiner are provided. This novel structure have a potential size reduction up to 50% compared to previous designs of this type.

The previous concept has been demonstrated by the design and manufacturing of a 12-way power combiner. Manufacturing process for the aluminium and PCBs parts are described. Results have a good agreement with simulations, showing low insertion loss and high return loss over a wide bandwidth.

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Chapter 4

Power combining amplifier

4.1 Introduction

Power amplifiers have a key role in most RF systems. Normally, at least one amplification stage is needed in all systems to boost the signal to higher power levels or compensate for transmission/component losses. Consequently, power amplifiers are the most critical part of a transmitter system as they are responsible for the highest heat dissipation, size and cost.

In satellite communications, graceful degradation is very important since replacing or repairing a system on space is very difficult or impractical. Therefore power combining amplifiers where several chips are efficiently combined to obtain higher power and graceful degradation are usually implemented.

In this chapter, a power combining amplifier design based on a 12-way double side slotted waveguide structure is presented. Design and manufacturing guidelines are provided.

4.2 Single chip test board

Power amplifiers can be found in many different forms, packaged or unpackaged [1].

Unpackaged devices are usually available as MMIC die chips. These chips are normally connected using a planar transmission line such as microstrip or coplanar by

wire bonding. Also, for MMIC placement, there are several solutions depending on the type of application (low noise, power, etc). In the case of power applications, improving thermal dissipation is the main objective. Thus, the optimal solution is to mount the MMIC on a metallic carrier [2]. Normally a copper alloy such as copper tungsten or copper molybdenum is used, which provides a good compromise between a good coefficient of thermal expansion (CTE) and high thermal conductivity. Therefore, the carrier and substrate used need to be selected accordingly to present the necessary thermal compatibility with the MMIC, otherwise the device could be damaged. This is very important especially in high power applications where the heat generated by the dissipated power modifies the mechanical structure of the chip and surrounding materials. In general, handling and mounting of bare die MMICs is difficult and costly.

Alternatively the amplifiers chips can be packaged. There are many different packaging techniques which are appropriate depending on the application and the power level of the amplifier [1]. In general, plastic packages are for low and medium power applications and ceramic packages are common in high power applications (Fig. 4.1). Therefore, materials used for the package and its geometry greatly affects to the thermal performance, size and cost of the amplifier. Moreover, handling and mounting of packaged chips is usually much easier than bare die MMICs.

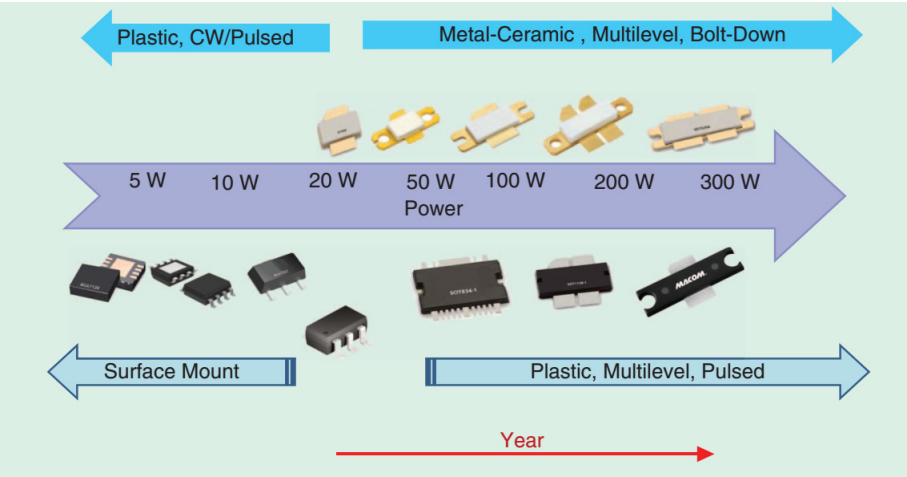

Figure 4.1: Plastic and ceramic packages with typical supported powers from [1].

Before manufacturing the complete PCBs for the prototype including each 6 chips, a single chip is mounted in a test board to assure correct operation. The selected device is the medium power amplifier model TGA4903-SM by Triquint [3]. This is a galium arsenide (GaAs) device in a QFN package that provides an output P1dB

compression point of 22 dBm (158.48 mW). As a result, the perfect combination of 12 amplifiers of this type would result in 1.9 W, which is enough power for the objective block up-converter for a laboratory environment tests. In general, this value will be reduced by the combining efficiency of the power combiner used due to losses in the device. Table 4.1 includes more detailed parameters for this amplifier model.

Table 4.1: TGA4903-SM parameters

Frequency Range:	27-32 GHz
P1dB	22 dBm
Psat	24 dBm
Gain	15 dB
Return Loss	10 dB
Bias	Vd = 5 V, Id = 170 mA, Vg = -0.6 V
Dimensions	4 x 4 x 0.85 mm

4.2.1 PCB design

In general, power amplifiers need an input and output matching networks for optimum gain, power or noise figure performance depending on the application [4]. Some commercial devices come already internally matched so that they interface directly with 50Ω lines in the input and output ports. The device for this design needs to be externally matched and its datasheet specifies the physical dimensions of the input and output matching networks that need to be implemented. In this case, the input and matching network dimensions are provided to obtain the optimum gain and power performance for the chip. However, the dimensions are given for a different substrate than the one used to design the 12-way power combiner. Therefore, to have similar performance in the new substrate, the dimensions from one to the other need to be translated.

The dimensions for a microstrip transmission line (Fig. 4.2) in a substrate are calculated from a required impedance and electrical length at a certain frequency and the substrate parameters (permittivity ϵ_r, thickness and $\tan\delta$ losses). In this way, knowing the physical dimensions in a substrate, it is easy to calculate the line

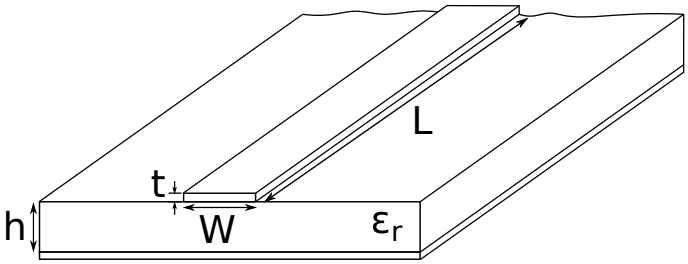

Figure 4.2: Microstrip line cross-section and physical dimensions.

impedance and electrical length and then translate these to a physical dimensions in the new substrate [5]. This process is illustrated in Fig. 4.3.

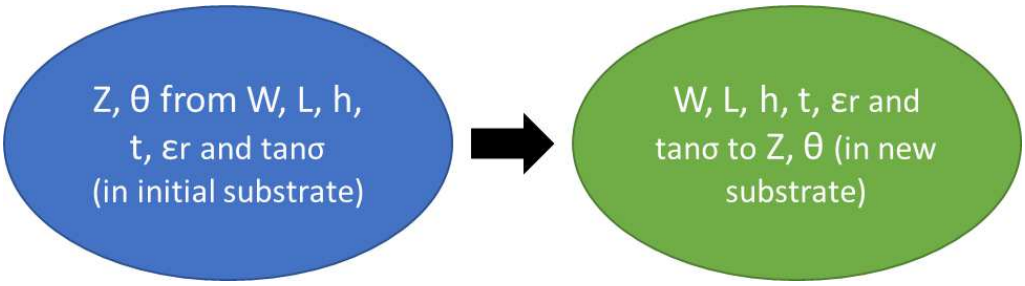

Figure 4.3: Microstrip line substrate translation process.

Following the above described steps, the substrate used in the datasheet (Rogers RO4003C 0.2 mm thick) is translated to the required Rogers RT/Duroid 6002 [6] 0.25 mm thickness (Table 3.3). The resulting layouts including the QFN package for the input (IMN) and output (OMN) matching networks are shown in Fig. 4.4.

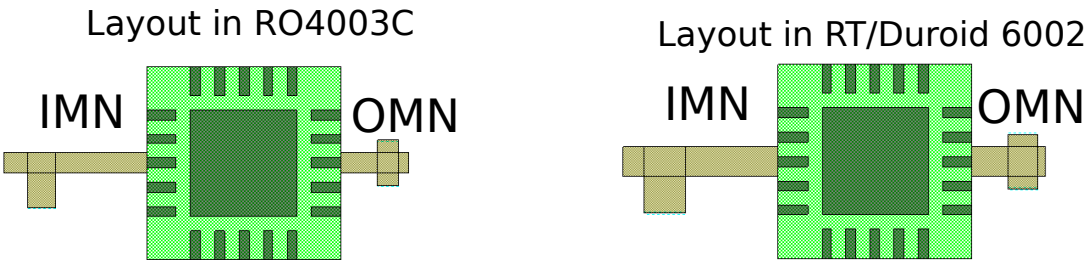

Figure 4.4: Resulting layout of the input and output matching networks in both substrates.

It can be seen that the new matching networks are bigger. This is due to the lower permittivity ($\epsilon_r = 2.94$ versus $\epsilon_r = 3.55$) and thicker substrate. To check that the response of the matching networks is maintained, the S-parameters for both are simulated. As can be seen in Fig. 4.5 the resulting S-parameters agree.

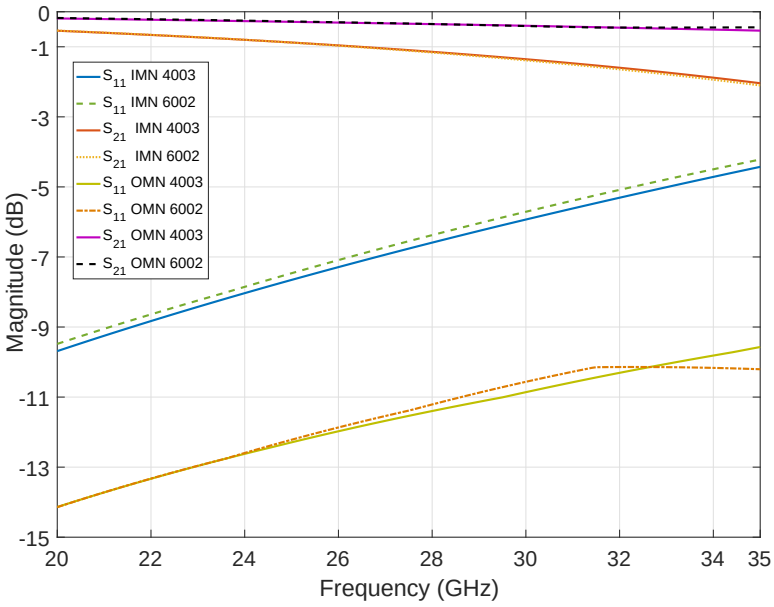

Figure 4.5: S-parameters comparison for redesigned matching networks.

Once the input and output matching networks are designed, the biasing circuitry and the pads to apply the biasing voltages are included (Fig. 4.6). These pads are designed such that they have enough area to solder a wire and they have enough space from the surrounding ground plane to avoid short-circuits. Additionally, via hole positions are selected from the recommended in the datasheet so that efficient heat sink and electrical performance can be achieved.

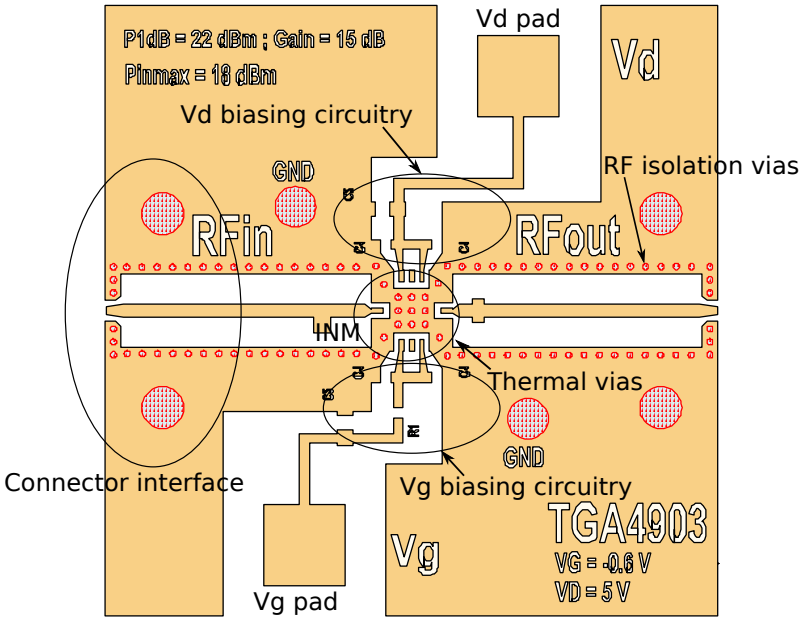

Figure 4.6: Layout of the designed test board

4.2.2 Test board manufacturing

The manufacturing process of the test PCB consists of the following steps:

- Substrate etching of the PCB layout.
- Via holes drilling and plating.
- Solder mask etching.
- Components mounting.
- Connector attachment.
- Attach the PCB on a heat sink.

First of all, the mask for the designed layout are printed and etched on the substrate. The procedure followed is the same described in Chapter 3.

The next step is drilling and plating the via holes. This process uses a drilling machine or a laser (for very small holes) that automatically drills all the required via holes with a very high precision. The correct positioning of the holes is critical for the RF performance of the chip. The most important are the ones below the chip as they act as the RF ground but also thermal sinks to remove the heat produced by the chip. Additionally, the ones below the connectors are very important to assure a good grounding to the connectors. Furthermore, a clean drilling is very important and it must be checked that any burrs produced in the drilling process are removed. If the PCB surface is not clean and flat, the components might end up not soldering properly and not working.

Once the vias are drilled, they need to be plated with conductive material to connect the top and bottom layers of the PCB. This is usually done by electroplating. In order to protect the exposed copper layers from rust and provide a surface to solder the components to the PCB later on, an immersion tin surface finish is applied.

Once the PCB metal is ready, the solder resistor mask is etched. This layer helps to solder the components by delimiting the areas of the solder pads with a solder repellent material that prevents the solder paste to spread out of the soldering area. It is important to note that for this process, the mask for the solder resistor is a negative mask. This means that similarly to the copper mask, the black parts are removed from solder resistor and white parts remain.

Once all the manufacturing process before mounting the components in the PCB is finished, the board looks as shown in Fig. 4.7. As observed, additional bigger holes were included to attach the RF connectors and also to attach the PCB to a heat sink and provide a ground connection at the screw.

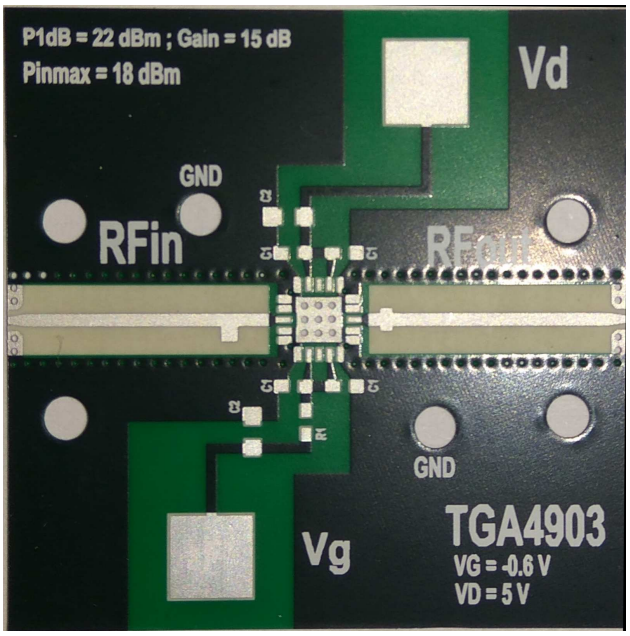

Figure 4.7: Photo of the designed test board prototype.

The next step is to mount the components on the PCB. In this process, first a stencil layout is applied to put solder paste in the pads to be soldered. Then the components are placed in their correct positions and the PCB is passed through a solder re-flow process where the heat solidifies the paste and fix the components to the PCB. The process will be described in detail for the 6 chip PCBs in the following sections.

With the components soldered on the board, the connectors are attached to the RF input and output interfaces. The connectors used are 2.4 mm coaxial End Launch connectors by Southwest Microwave for a Rogers RT/Duroid 6002. These connectors are attached to the PCB using screws so that they are easily mounted with no need to solder any component. This is very convenient at high frequencies since the precision of soldering needs to be very high to avoid spoiling the RF performance. An additional advantage of these connectors is the possibility of reusing them in many devices compared to the usual SMA soldered connectors, which are difficult to unsolder and reuse. When attaching the connectors, it is important to make sure that the pin is correctly centred in the track. Therefore a microscope view was used

to align the pin in the centre of the track as seen in Fig. 4.8. As can be seen the pin is correctly centred and touching the track. To check the connection, the continuity mode of a multimeter can be used from the input inner pin of the coaxial to the microstrip track.

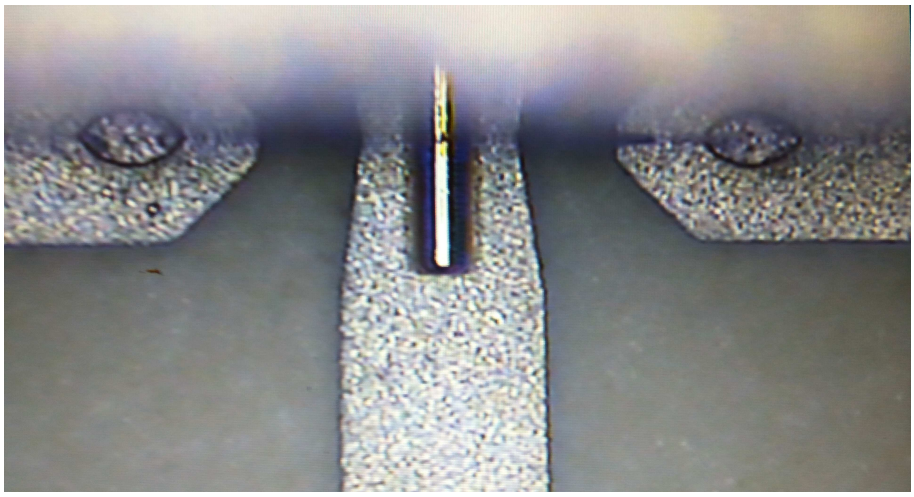

Figure 4.8: Connector pin correct alignment under the microscope.

Finally, the last step is to mount the board on a heat sink and solder the biasing cables to the drain and gate voltages pads. The ground cable is attached to one of the screws used to hold the PCB on the heat sink. The final manufactured PCB on the test bench is shown in Fig. 4.9. Since the substrate thickness is really thin (0.25 mm) and it is very flexible, in order to protect the PCB from bending, an additional aluminium sheet of 0.5 mm thickness is introduced below, in between the PCB and the heat sink. These provides an extra robustness against bending, mainly in the connectors interfaces where the PCB is more vulnerable to be bent.

4.2.3 Measurements

The measurements performed on the single chip amplifier board are carried out using a PNA network analyser model N5225. The calibration to the test ports is done using a 2.4 mm coaxial calibration kit to set the reference plane at the board connectors interface. Additionally, in order to check that the design is correct and the performance on the new substrate is maintained, an evaluation board (EVB) from Triquint is also measured. The measured S-parameters are shown in Fig. 4.10.

Analysing the figure, the input and output reflection coefficients (S_{11} and S_{22}) does

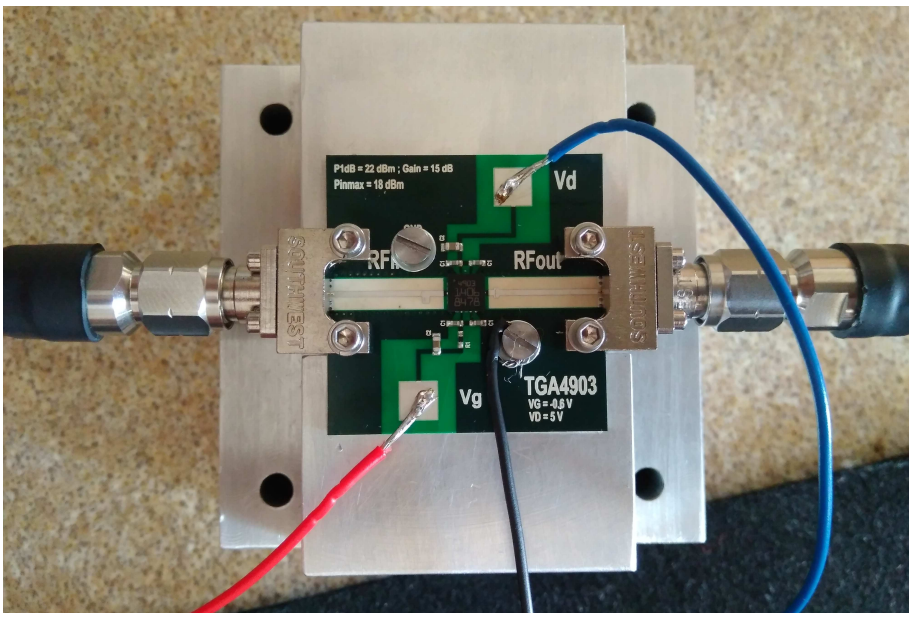

Figure 4.9: Photo of the manufactured test board under measurement.

not agree completely, but overall they have a good match and the level is approximately similar in the complete measured band. The most different parameter is the output to input isolation or S_{12}, where the manufactured prototype presents a much lower value. This may be caused by a non proper grounding of the chip caused by a bad connection of the pad below the chip with the ground. Regarding the gain, the measured S_{21} are very similar but at 23.36 GHz the prototype manufactured presents an oscillation with a peak in the gain and positive S_{22}. However, as the device is going to be operated at the 26 GHz to 34 GHz band and the gain is maintained at this range, the overall performance at these smaller range is acceptable for the performance objectives. At the centre frequency of interest of 30 GHz the measured gain of the manufactured prototype is 10.68 dB compared to 11.69 dB for the EVB. The input reflection coefficient is -12.12 dB compared to -16.78 dB for the EVB and the output reflection coefficient presents a value of -11.85 dB and -9-73 dB for the prototype and EVB respectively. Finally, the isolation is -34.5 dB for the prototype and -53.6 dB for the EVB.

Although the measured performance of the prototype in the new substrate is not as good as the one in the EVB, the performance in the operating frequency of the power combiner is good enough to meet the testing requirements. Furthermore, the better manufacturing techniques for the EVB are a factor that need to be taken into account to expect lower performance than for an in house made PCB.

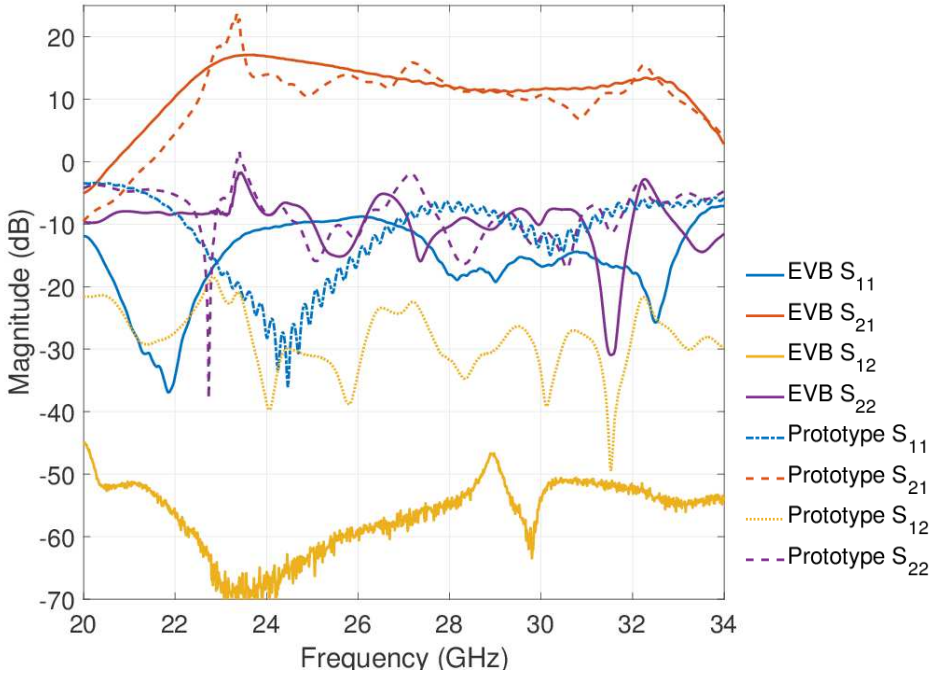

Figure 4.10: S-parameter results for the Triquint EVB and the manufactured single chip prototype.

4.3 12-way power combining amplifier

Once the performance of the chip in a single PCB for the new substrate has been tested, the complete power combining amplifier with 12 chips is manufactured. In the following sections, the procedure followed is described and the obtained results are discussed.

4.3.1 Passive structure

The first step is to manufacture a new passive combiner. In this new part an extra length in between the input and output waveguides is included to accommodate the chips. The manufacturing of this part is realized in the same way as described in Chapter 3. In addition to the process followed before, the new PCBs are designed including the circuitry needed to mount the amplifier chips, leaving space to accommodate all the biasing lines and components. Accordingly, to test the passive structure, the top and bottom PCBs are simulated and manufactured including all these extra metal areas to account for possible adverse effect in the RF performance of the device.

4.3.1.1 Thermal analysis

Before starting the design of PCBs, a thermal analysis is carried out to check the thermal performance of the device. The lifetime of the chips is directly related to the operating channel temperature [7]. It is common that the manufacturer specifies a maximum operating channel temperature for a mean expected lifetime. Therefore, a worst case scenario is simulated using CST to check that this maximum temperature is not exceeded. In this scenario, the maximum power dissipation of 2 Watts allowed for the amplifier is set for each chip and the boards are reduced to a minimum composed of the input and output microstrip lines and the via holes beneath the chips. In this scenario the metal parts touching the chips are reduced whereas in the real board the grounplane and top metal would provide additional heat sinks to remove excess heat. The maximum temperature of the baseplate is 70 °C to have a maximum channel temperature of 200 °C due to the $\theta_{jc} = 65.2\ ^{\circ}C/W$ thermal resistance of the junction to case for the chip. The power dissipated can be calculated using equation (4.1).

$$P_{dmax} = \frac{T_{channel} - T_{base}}{\theta_{jc}} \tag{4.1}$$

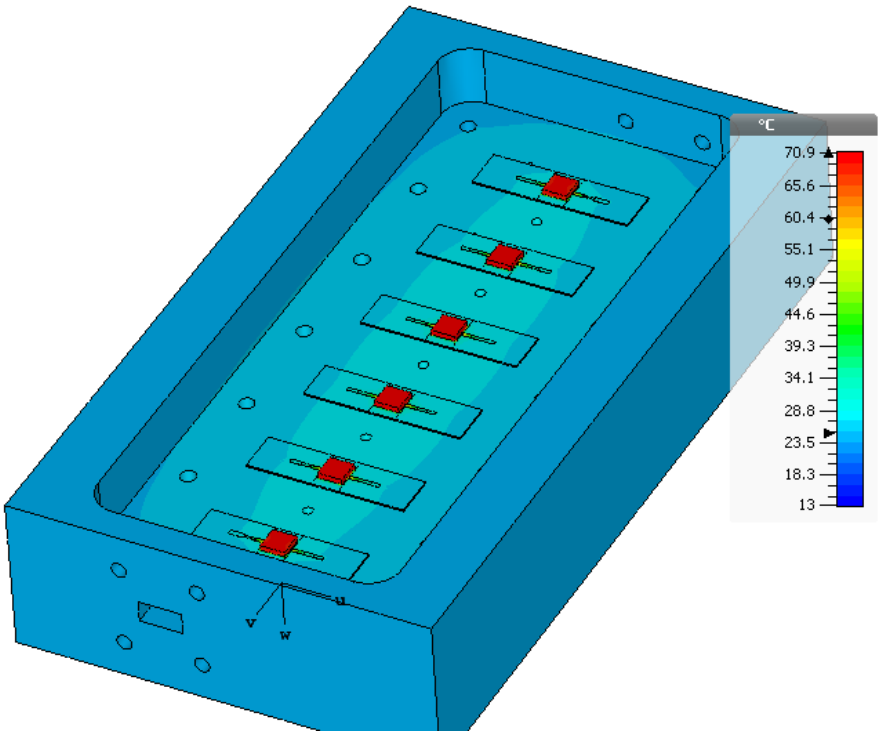

Figure 4.11: 3D model and results for thermal analysis.

The 3D model simulated and results can be seen in Fig. 4.11. As seen, the maximum temperature at the chip's packages is 70.9 °C. However, as this is the value for a chip operating at its maximum input power and the 3D model is considered as the worst case, the expected temperature will always be below the maximum simulated value. Therefore, the thermal results envisage a good thermal performance for the chips. Furthermore, additional fans can be applied to reduce the temperature and improve further the lifetime of the chips.

4.3.1.2 Phase difference tolerance analysis

One important parameter to take into account when designing power amplifiers based on power combiners is the phase coherence for a correct power summation at the output port [8]. As discussed in Chapter 3, the travelling wave combiner architecture benefits of an inherent in-phase combination when it is connected in inverse back-to-back configuration. However, this is only for the passive structure and the additional phase difference between chips due to tolerances in amplifier manufacturing might destroy the power combination at the combiner output. Consequently, before mounting the chips on the PCBs, a yield study using the phase tolerances range for the chips is carried out in order to check the performance of the power combiner within the range of possible phase values.

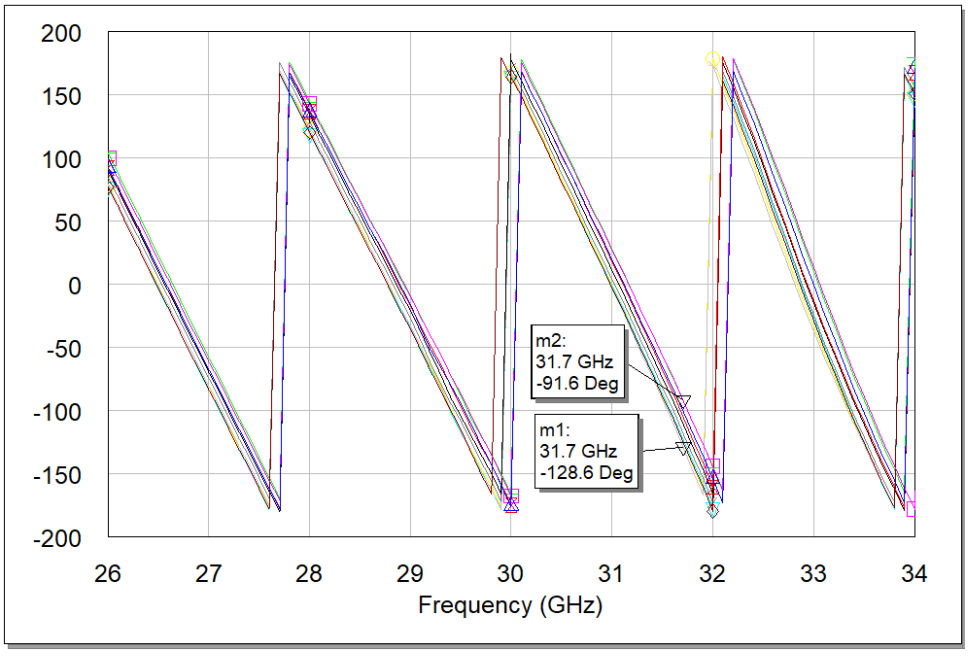

Figure 4.12: Phase response for different chip's measurements.

The range of phases within the chips tolerance is obtained by plotting the phase of the transmission coefficient S_{21} for different random chips. This data is provided by the manufacturer and in this case, 10 different S parameters files were provided to evaluate the phase performance. In Fig. 4.12 the phase response of these 10 chips is shown. As can be seen there are some differences in the phase response and the maximum phase deviation between chips is 37.1 degrees which sets the tolerance range in ± 18.55 degrees.

In order to evaluate the response of the power combining amplifier when it is exposed to this range of phase differences in the chips, a simulation is performed using the S-parameters file of the combiner and divider. Also, an amplifier model using its S parameters is introduced. Then, additional phase delays are included in the amplifiers input. These phase delays will model the phase difference between chips and their phase is set to have a deviation of ± 20 degrees from their initial value, which is set at 100 degrees for all the paths. The schematic used is shown in Fig. 4.13.

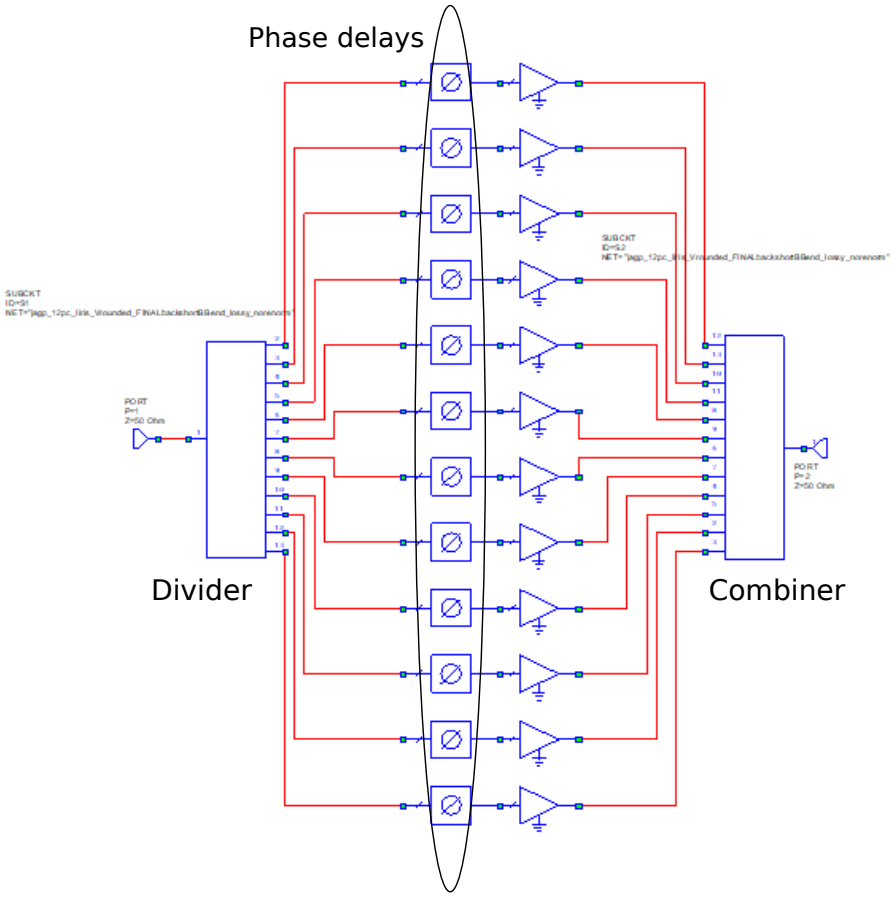

Figure 4.13: Schematic used for the phase yield analysis.

The S-parameters resulting from the yield analysis are shown in Fig. 4.14. As can be observed, the phase difference between the chips modifies the final gain of the amplifier. However, the range of variation is not really significant and the power combiner is expected to have a good performance within this phase range. The maximum value of gain variation is observed around 28.3 GHz with a deviation of 0.69 dB (or ±0.345 dB from the mean value). Finally, the input matching is not affected since regardless of the phase delay of each chip, they are all designed to be matched.

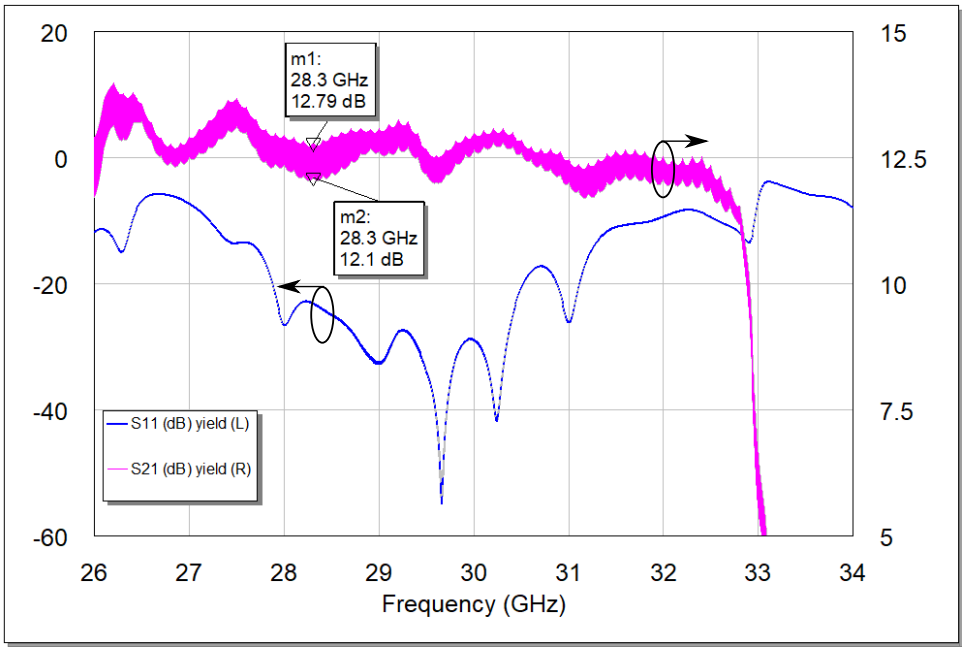

Figure 4.14: Yield analysis for phase difference between chips.

4.3.2 PCB design including chips

The new PCBs designed are in general the same boards but including the new layout for the input and output matching networks recommended by the manufacturer. Besides, the pads for the correct mounting of the amplifiers chips and components are included and also all the biasing tracks. To design the layout, the basic microstrip lines designed for the previous passive structure are used as a base drawing whereas the additional biasing newtorks, pads and matching networks are added using a CAD design tool. In Fig. 4.15 the layout for a single chip including the mentioned parts is shown. As can be seen, additional via holes are included to isolate the RF and DC parts of the circuit. The 50Ω plane is the point where the previous PCB

with no chip interfaces with the input and output matching networks of the amplifier chip.

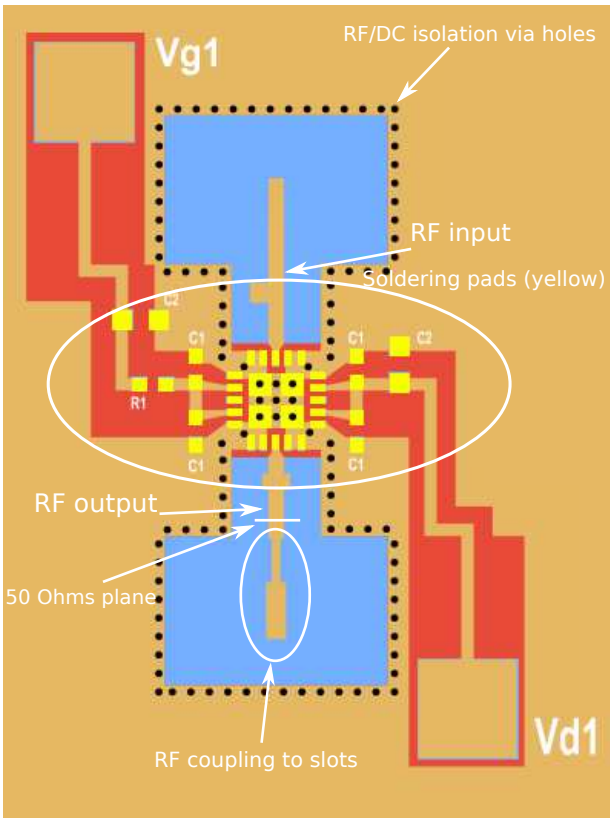

Figure 4.15: Layout for a single chip in the power combining amplifier PCBs.

The final layouts for the top and bottom PCBs are depicted in Fig. 4.16. These contain 6 chips each which are located on the slots planes of the aluminium body. As can be noticed, the top and bottom boards are flipped one with respect to the other to account for the input and output waveguide ports location. A silkscreen layer is included to easily identify ports, biasing pads and components.

Before manufacturing the boards, a top and bottom test boards are simulated and manufactured, removing the chip pad and connecting directly the input and output 50 Ω reference planes. In this way the possible adverse effects caused by all the new metal areas are checked. The simulated and measured results for these boards in the power combiner are shown in Fig. 4.17.

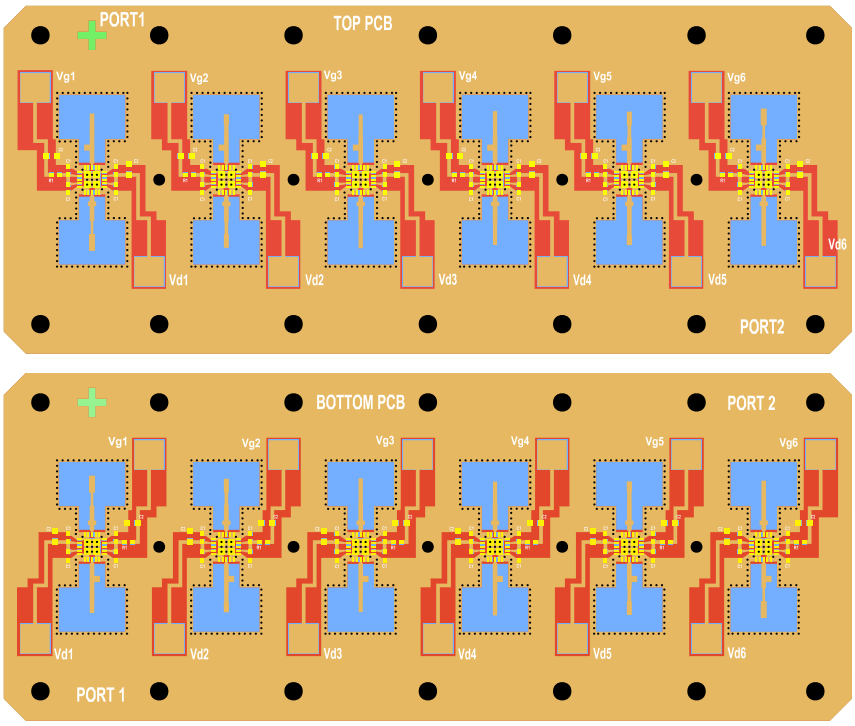

Figure 4.16: Top and bottom PCB final layout for the designed 12-way power combining amplifier.

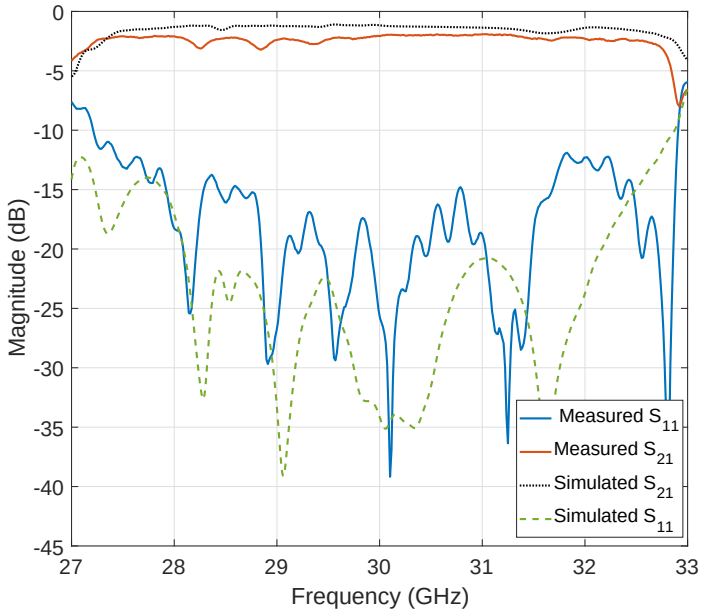

Figure 4.17: Simulated vs measured S-parameters for the test passive boards including biasing circuitry.

As observed in the figure, the behaviour of the power combiner is not affected by the extra circuitry and via holes. Some extra losses can be noticed with an approximated extra insertion loss of 0.3 dB, resulting in a total IL at 30 GHz of 2 dB. This is caused

by the extra microstrip transmission line placed instead of the chip and thus it is expected to be reduced in the final PCB with the chip mounted. After checking the correct performance of the PCBs they are manufactured. These are shown in the photo in Fig. 4.18.

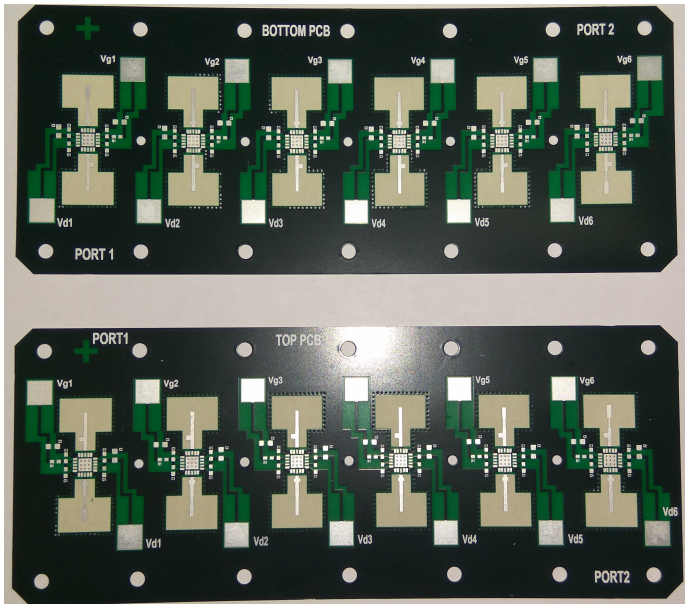

Figure 4.18: Manufactured top and bottom PCBs for the 12-way power combining amplifier.

4.3.3 Chips mounting

The next step in the manufacturing process of the PCBs is the component mounting, using a solder re-flow process. In this process, a temperature profile is applied to the boards including the components placed with solder paste on their final locations. The steps followed to solder the QFN chips and the biasing components were:

- Print solder paste using a stencil layer.
- Pick and place the components in their correct position.
- Solder re-flow process to solidify solder paste.

Before starting the mounting process, the boards and the QFN chips are put in a dryer for 24 hours at 110 °C to remove any possible excess moisture that could interfere in the correct soldering process. Since the PCBs are very thin, it is likely that if not protected, they might bend destroying the solder junctions. Therefore,

to avoid breaking the PCBs during the soldering process, they are fixed to a thicker FR4 board with high temperature tape.

The solder paste printing is a gasketing process in which the solder paste is applied using a squeegee over a stencil layout frame. The stencil frame is made of a 100 μm metal sheet that is fixed to a frame and tensed to achieve a flat and stable surface. In this frame, the pads where the solder paste needs to be applied are cut using a laser cutter (Fig. 4.19).

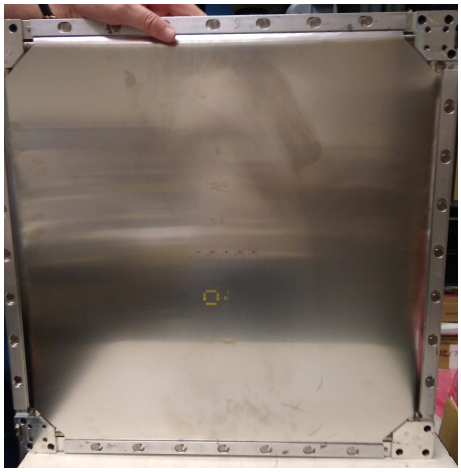

Figure 4.19: Stencil frame used for the top and bottom PCBs.

In order to achieve a good alignment between the stencil frame and the solder pads, the boards are fixed on a tray (Fig. 4.20) which is used to press the PCB against the stencil frame (Fig. 4.21). Hence, once the solder paste is pressed against the stencil layout on the other side, the solder paste will be placed correctly only in the pads and not in the rest of the PCB.

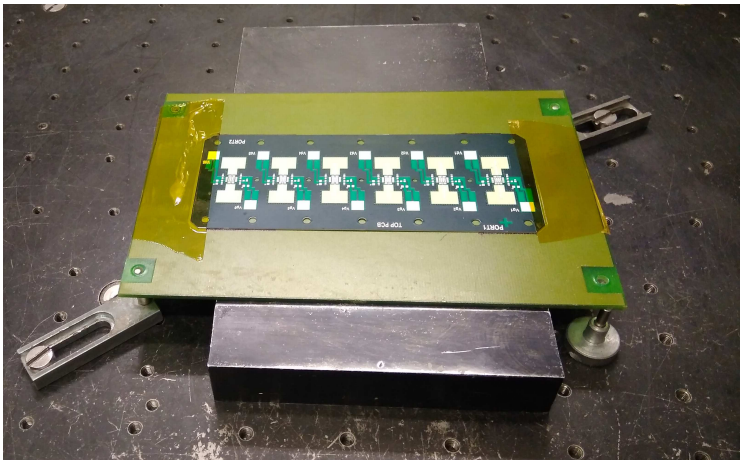

Figure 4.20: PCB on stencil application fixture tray.

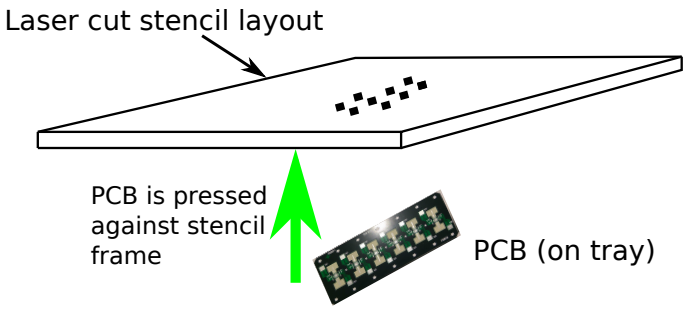

Figure 4.21: Stencil procurement process.

The PCB aligned with the stencil layout is shown in Fig. 4.22. As can be observed, all the pads of the PCB are properly centred and prepared to apply the solder paste.

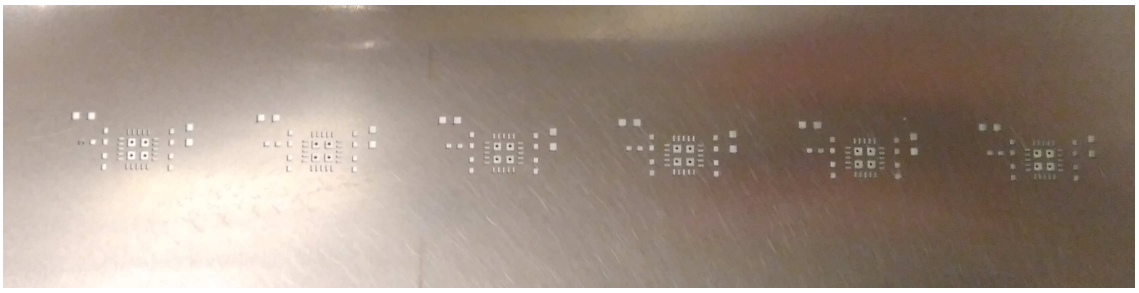

Figure 4.22: Stencil frame aligned with solder pads ready to apply the solder paste.

As mentioned above, the solder paste is pressed against the stencil layout and spread over the solder pads using a squeegee that is positioned at 60°. Once the solder paste is applied, the pads in the PCB look as shown in Fig. 4.23. As can be seen, the paste is properly applied on the pads areas and none outside them. This process assures that the components are properly soldered and any short-circuit is presented between adjacent pads.

The next step is to place the components on their positions. To do this, a pick and place process is used. For these boards, the number of components is limited to a few. Therefore, they are placed by hand. In more complex boards with hundreds or thousands of components, an automatic component pick and place machine is normally used. In Fig. 4.24 the final aspect of a chip and its biasing components is shown before solder re-flow.

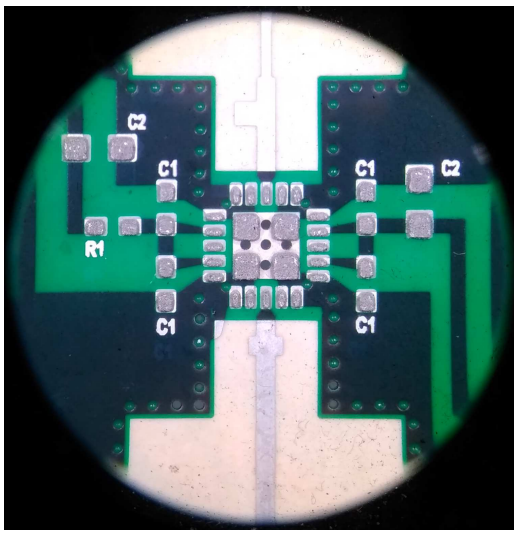

Figure 4.23: PCB pads with solder paste applied.

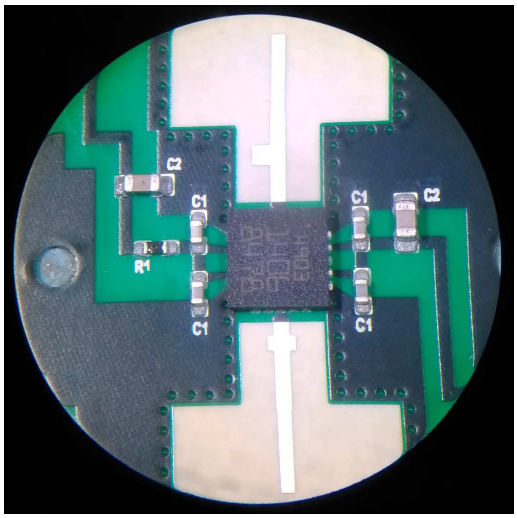

Figure 4.24: PCB pads with components placed.

The final step is to put the boards through a high temperature solder re-flow process to melt the paste and solder the components to their respective pads. The solder paste used becomes liquid at the temperature of 217 °C. However, to improve the soldering process a bit higher temperature of 230 °C is set. For these boards, a vapour phase machine is used. This machine works by heating an oil which is situated below the boards. At the exact temperature of 230 °C this oil vaporizes ascending and impregnating the air around the boards. Using this technique guarantees that all the zones in the boards see the same exact temperature and the board are not put through stress due to high temperature variations. Additionally, the vapour is inert and therefore no oxidation is created in the process. In Fig. 4.25, a photo of the boards under the oil vapour is shown.

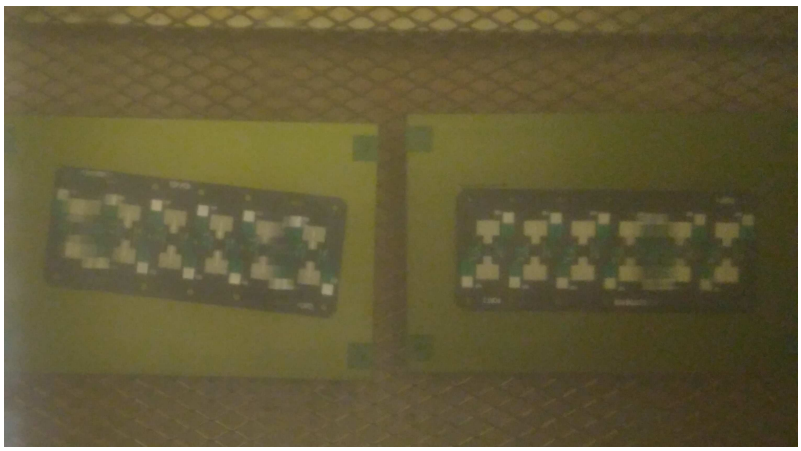

Figure 4.25: PCBs inside vapor phase machine during the soldering process.

4.3.4 Measurements

Once the top and bottom boards are finished and all the components soldered, they are attached to the passive aluminium structure. Similarly to the passive power combiner presented in Chapter 3, the attachment of the boards is done using screws. However, in this case, a very careful handling of the boards is needed due to the thin and easily bendable substrate used. In addition, the cables needed to bias the components need to be soldered. To make sure that the boards remain flat during the cable soldering, they are first attached to the aluminium block. Each chip needs a cable for the gate voltage, one for the drain voltage and a ground cable. Due to the reduced space in the boards, instead of having a single ground cable for each chip, 3 cables are attached to the centre screws to act as ground points. As a result, a total of 12 gate biasing cables, 12 drain cables and 6 ground cables are used (half for each PCB). Clearly, it can be a difficult task to easily identify which cable corresponds to each chip and an error in the biasing voltages could potentially break the chips. Consequently, each cable is labelled with the corresponding chip number and its biasing point (gate or drain). Moreover, the gate cables are blue coloured and the drain cables red coloured to further clarification. For the ground cables black colour is used. In Fig. 4.26 a photo of the final 12-way power combining amplifier prototype including all the biasing cables is shown.

To bias the device a power supply is used for each amplifier so that each chip voltage and current can be monitored independently. The gate voltages are set to -0.6 V and the drain voltages to 5 V. This gives an approximate drain current for each chip of 200 mA.

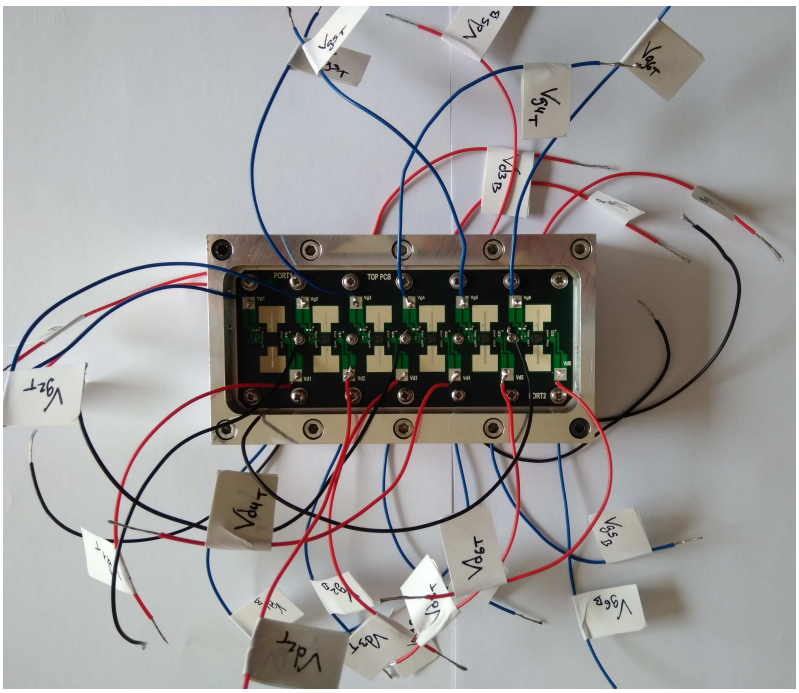

Figure 4.26: Final mounted 12-way power combining amplifier prototype.

The measurements are carried out using a PNA model N5225A from Keysight. The input and output ports are calibrated to a standard WR28 waveguide flanges. Moreover, although the thermal performance of the device is simulated and no heating risk is expected, 2 fans are situated below the prototype blowing air to improve the heat dissipation of the chips. The complete measurement set-up is shown in Fig. 4.27.

The resulting S-parameters from the measurements are shown in Fig. 4.28. As can be seen, there is a good input and output matching. In addition the reverse isolation is low with a minimum value of 17.5 dB. However, unfortunately, some problem is occurring since the S_{21} parameter of the amplifier shows a negative value over most of the frequencies.

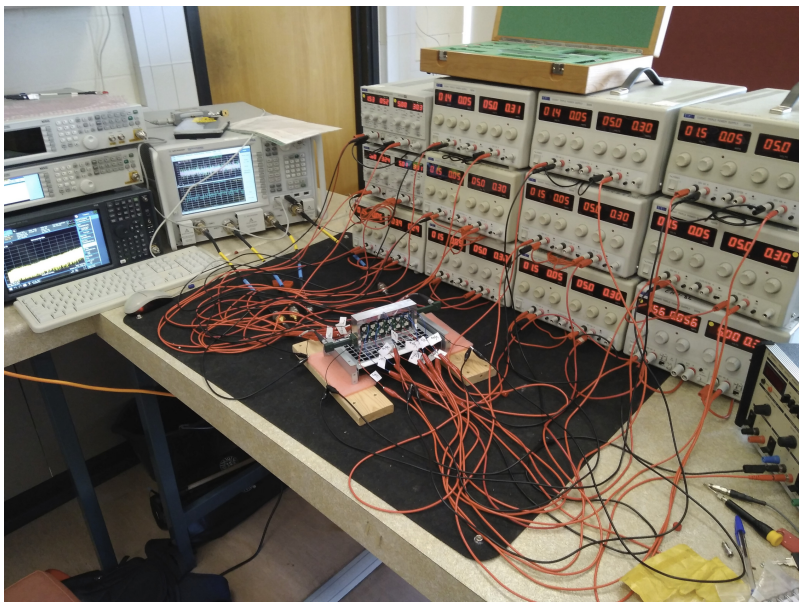

Figure 4.27: Laboratory measurement setup for the 12-way spatial power amplifier prototype.

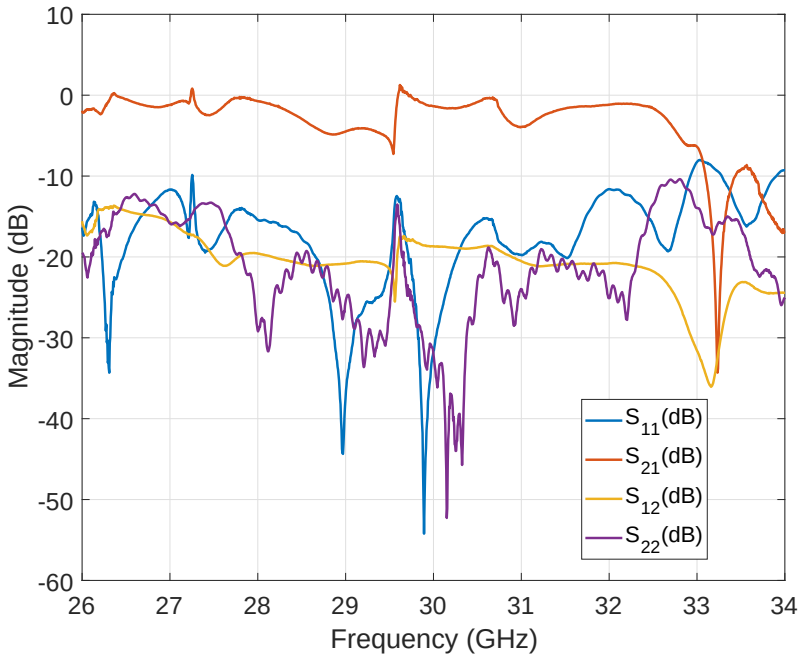

Figure 4.28: Power combining amplifier prototype measured S-parameters.

In order to know the cause of this unexpected low gain, a spectrum analyser is used to check the output spectrum of the amplifier when an input tone at 30 GHz is introduced. To identify the cause, only one amplifier is turned on at first to see the effect in the output signal. This output is shown in Fig. 4.29.

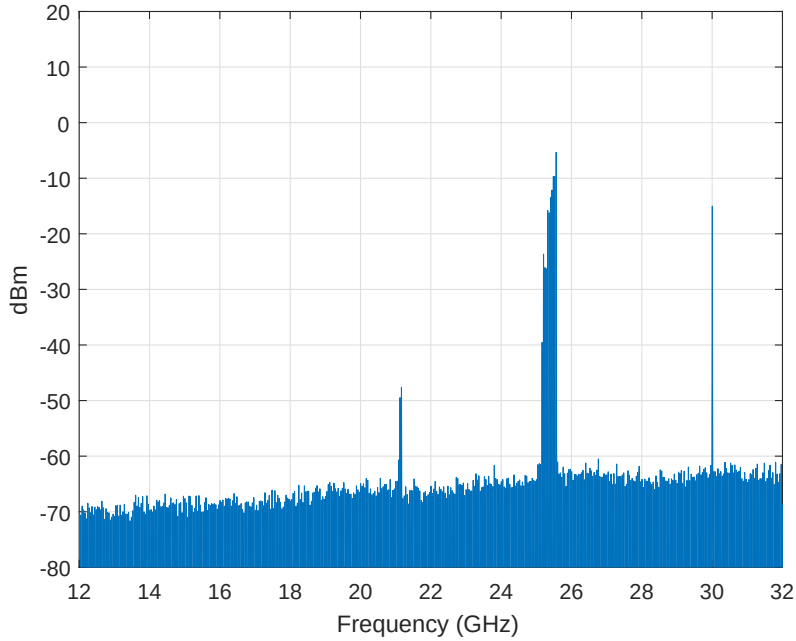

Figure 4.29: Output spectrum for a 30 GHz input tone and 1 amplifier on.

As observed, the spectrum reveals an undesired signal around 25.4 GHz and at 21.16 GHz. These are caused by oscillations and it is checked that this effect is the same activating any of the amplifiers or with a combination of them. When an oscillation is happening there are several possible solutions that can be tried to cancel the oscillation and recover the desired signal:

- Add capacitors in the biasing lines. This can be checked in the gate or drain bias and it is used to ground any undesired frequency.
- Add a bigger resistor in the gate. A drawback of this solution is a gain reduction of the amplifier.
- As a last solution, the boards need to be redesigned using the same chips or different ones.

Due to time and budget restrictions, only the first 2 solutions have been checked in this project. In order to check if a capacitor can suppress the oscillation, several ones with values range from 10 nF to 470 μF are tested in parallel with the existing capacitors in the gate and drain biasing lines. The effect of these capacitors starts to be noticeable at the output when the capacitance value is bigger than 10 μF. However, the output signal when including the capacitors results in a suppression of the 21.16 GHz oscillation but the 25.4 GHz one is still present although much

more clean than with no capacitors. This can be seen in Fig. 4.30 where the output signal when a capacitor of 50 μF is put in parallel with the capacitors in the drain lines. Similarly, including a bigger resistor in the gate has the same effect and the complete suppression of all the oscillation is not achieved.

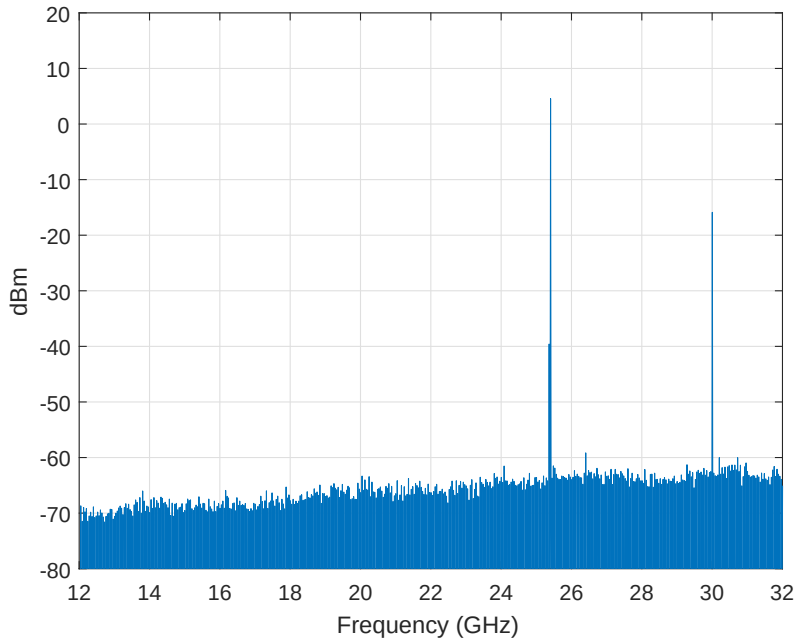

Figure 4.30: Output spectrum for a 30 GHz input tone and 1 amplifier on introducing extra capacitors.

4.4 Conclusions

In this chapter, the design and manufacturing of a 12-way power combining amplifier based on the double slotted waveguide technique described in Chapter 3 has been presented. First, the design and manufacturing of a single chip test board translated to the substrate used in the combiner is described. The performance obtained for the single chip board in the new substrate has a good agreement with the manufacturer evaluation board. Next, the manufacturing of the complete circuit boards with 6 chips each one for the final power amplifier is presented. Unfortunately, the chips in the final boards present an unwanted oscillation and the resulting gain is spoiled. Finally some techniques to help cancelling the oscillation are presented. However, in this case the total cancellation has not been possible and the redesign of the boards is set as a future work for this project to obtain the full performance of the amplifier.

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Chapter 5

L-to-Ka-band Block Up-Converter (BUC)

5.1 Introduction

In this chapter, the design and testing of an L to Ka-band block up-converter (BUC) is discussed. Design guidelines will be described and measurements for a 1.5 to 30 GHz prototype presented. This system allows the up-conversion of a modulated or unmodulated signal. In addition, it is based on a connectorized design that provides the versatility to easily change any component, to modify the output frequency or test individual components within the system to evaluate performance of different configurations (spurious response, linearity, etc). This is very convenient for a laboratory environment due to the wide range of tests and measurements that can be easily carried out with a reduced budget.

5.2 Design process

The design of a block up-converter is a complex task with many parameters and variables involved in the process. Due to the diverse architecture solution possibilities [1] and the wide range of components available in the market, several iterations are normally needed to achieve a final design. Furthermore, the difference in performance of the real components compared to the datasheet specifications could result

in additional modifications after measuring a prototype's performance.

The first step to design a block up-converter is the clear definition of the performance parameters that need to be achieved for the design. In order to check the validity of a design, the second step is to set up a general schematic of the architecture selected using existing commercial components and perform an spurious and a budget analysis to verify the feasibility of the system (frequency spectrum clean from spurious and accomplishment of the desired specifications).

During this second step, it is very important to model the components as accurate as possible in order to save further iterations. To do this, the following guidelines are considered:

- As many performance parameters as possible from datasheet are taken into account in order to have an accurate model of each part. Identifying parameter values at the operating frequency will save further design iterations.
- All the losses in the chain are modelled. This means that apart from the components parameters, the losses introduced by the cables are included by means of attenuators. This is less important at low frequencies but it is an important aspect to consider at high frequencies where short cables may introduce significant losses.
- Producing a floor plan layout to identify the final location of the components will help to estimate the losses due to cables.

The next step is to check the compliance of the simulation with the required parameters. If the objectives are met, the design can be implemented. If any of the parameters is not met, further iterations which might involve changing components or the architecture would be needed. Finally, is it a good practise to allow for some margins to account for possible performance variations from the datasheets to the real components.

5.3 L to Ka band system definition

Once all the design guidelines have been defined in the previous section, the design of a BUC from L-to-Ka band is discussed in the following. As a first step, the

desired performance parameters are defined. For this design, the parameters shown in Table 5.1 are taken as the objective performance to achieve. These are set based on a typical Ka-band satellite terminal with reduced output power as it is intended to be used in tests in a laboratory environment.

Table 5.1: Block up-converter parameters specification.

Parameter	**Value**	**Units**
Input frequency	1.5	GHz
Output frequency	30	GHz
Cascaded gain	>45	dB
Output P1dB	>30	dBm
Output IP3	>35	dB
NF	<12	dB
Power consumption	<25	W
Dimensions	<44.5x36.2x9	mm

Given the parameters above, the next step is to select the architecture to be used. Since the aim of this design is to maximize the tests and analyses that can be performed, the design of two typical architectures is considered: a single conversion and a double conversion BUC. Furthermore, the single conversion version is designed so that the same set of components from the double conversion BUC are used so that a more comprehensive comparison can be done.

5.4 Double conversion BUC design

In this double stage system, or commonly called heterodyne transmitter [2], the input L-band signal is first translated to an intermediate frequency (IF) at 8.5 GHz (X-band) and then to the final frequency at Ka-band. Although this architecture is more complex (more components are needed), it offers some advantages in terms of higher overall gain and better spurious response which results in lower complexity in filters design to remove unwanted products.

The architecture is composed of 3 differentiated parts shown in Fig. 5.1.

1. In the first one, an amplifier boost the input signal. The gain of this amplifier

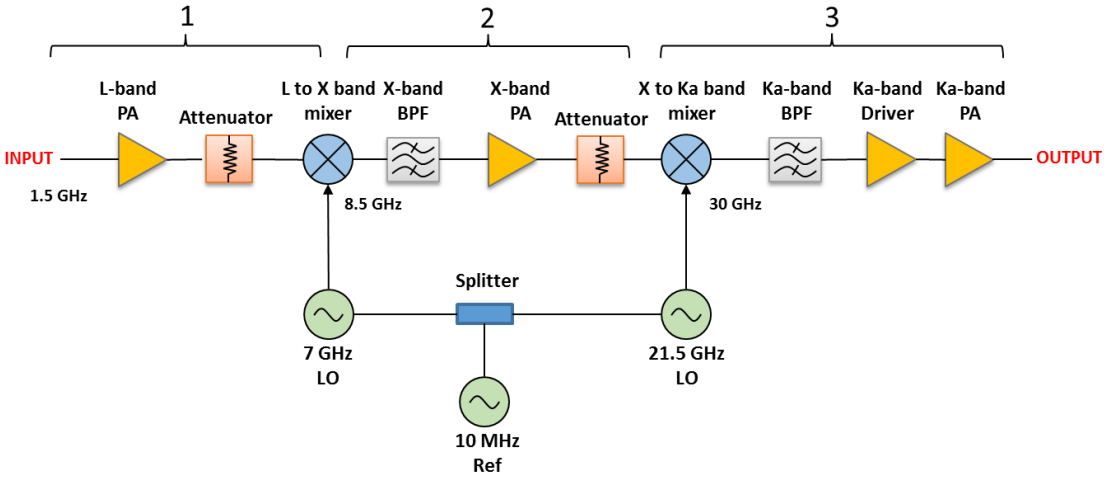

Figure 5.1: Double conversion block up-converter block diagram.

needs to be adequate to the expected input power at 1.5 GHz so that the output power does not compress the mixer resulting in non-linear behaviour.

2. In the second part, a mixer up-converts the input 1.5 GHz signal to an intermediate frequency of 8.5 GHz. Here, a filter removes the unwanted upper or lower frequency band, mixing spurious, local oscillator leakage and possible harmonics. Next, other amplifier compensates the conversion losses of the mixer (again considering not saturating its input).

3. The third and last part starts with a mixer which up-converts the intermediate signal to the final 30 GHz frequency. After another filtering to leave only the desired band, a driver and power amplification stages are included to reach the required 30 dBm power at the output. In this last stage, if a high power amplifier needs to be used, more than one drive stage might be needed in order to reach the input P1dB compression point of the last power amplifier. At the same time, the gain must be high enough to relax the input power to the mixer and avoid its compression.

The main reason to use a double conversion architecture is to reduce the local oscillator leakage to the final output [3]. If only one conversion stage was considered, the frequency of the local oscillator would be 28.5 GHz and it would fall very near to the final useful spectrum, which would reduce the bandwidth of the system or require high order and selective filters or suppression techniques, much more complex to design [4]. The local oscillator frequencies that need to be used in order to obtain

the desired frequencies for the mixing are calculated as in (5.1), where f_{LO} is the local oscillator frequency, f_{RF} the output frequency and f_{IF} the input frequency.

$$f_{LO} = f_{RF} - f_{IF} \tag{5.1}$$

Since the mixer produces both sum and difference frequency outputs, the filter after the mixer will remove the unwanted band and reduce spurious and harmonics. In this design the mixer band used is the upper band to avoid frequency inversion. Fig. 5.2 shows the frequency translated spectrum and how the filter removes the unwanted signals. The frequency inversion of the lower band can also be seen.

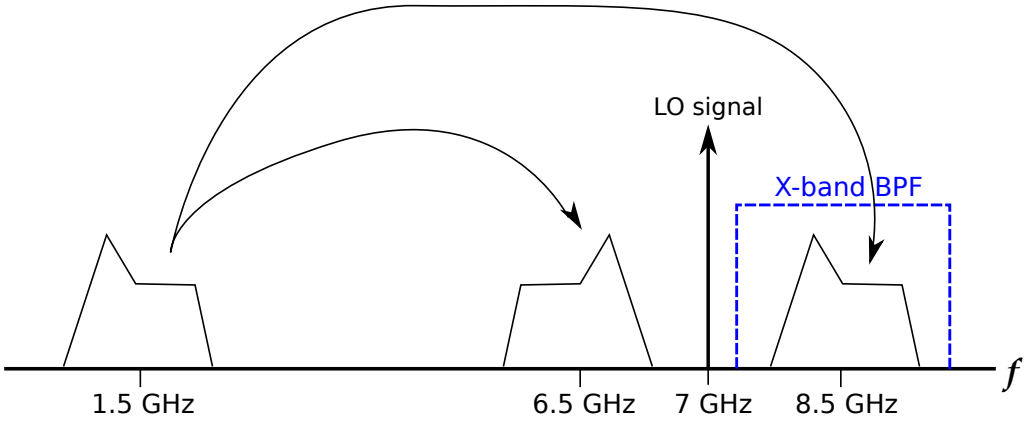

Figure 5.2: Frequency translated spectrum after the first mixer.

It is important to consider the intermediate losses between components due to cables or transmission lines. As mentioned earlier, the inclusion of these losses will increase the level of accuracy of the system simulations and reduce further iterations due to unexpected low power at any point in the chain. To model this cables in the simulations, attenuators are included in between the components. Furthermore, it is common that mixers present a high input reflection coefficient, resulting in poor matching and high reflections. Therefore, attenuators are also included in between amplifiers' outputs and mixers to protect the later from possible reflected power that could damage the devices.

5.4.1 Filters

As discussed before, filters are needed to suppress the intermodulation and harmonic products generated or leaked in the mixers. The correct filtering of the unwanted

products along the system reduces the final spurious at the output. Using the selected frequency plan where an intermediate frequency at X-band is used, two filters are manufactured at 8.5 GHz and 30 GHz.

5.4.1.1 X-band band pass filter

The X-band filter is designed in a planar microstrip technology. The geometry of the filter is a 6-th order hairpin. This filter is built by folding $\lambda/2$ resonators that are coupled between them and resemble a hair pin array giving the filter its name. Since the resonators are folded, this design approach results in compact structures and benefits from an easy fabrication since it does not need of via holes or external components. The main disadvantage is that the second passband is generated at around 2 times the first passband, in comparison to other designs as combline where the second passband can be moved further up in frequency (around $4f_o$ for a $\lambda/8$ resonators combline filter) [5]. Furthermore, if the folded resonator arms are very close, there could be coupling between them and deteriorate the response.

The main purpose of this filter is to suppress the lower mixer band (at $f_{LO} - f_{IF} = 6.5GHz$), the 7 GHz local oscillator leakage to the RF port and any spurious products. Since the most powerful signals appearing after the mixer are the first two, the filter response mask is designed to have a minimum suppression of 40 dB at 7 GHz. The maximum desired insertion loss for the design is set at 2 dB.

The filter is design in AWR Microwave Office using a Rogers RT/Duroid 5880 substrate [6] with characteristics shown in Table 5.2.

Table 5.2: Rogers RT/Duroid 5880 characteristics

ϵ_r	Thickness	Cladding	$tan\sigma$
2.2	0.51 mm	35 um	0.0009

Once the design objectives are defined, the filter is optimized and manufactured using wet etching techniques described in previous chapters. The filter simulated and measured response is shown in Fig. 5.3.

As can be observed, the agreement with the simulated results is good. However, in the centre of the band the response loose the deep peak resonances. This is due to the

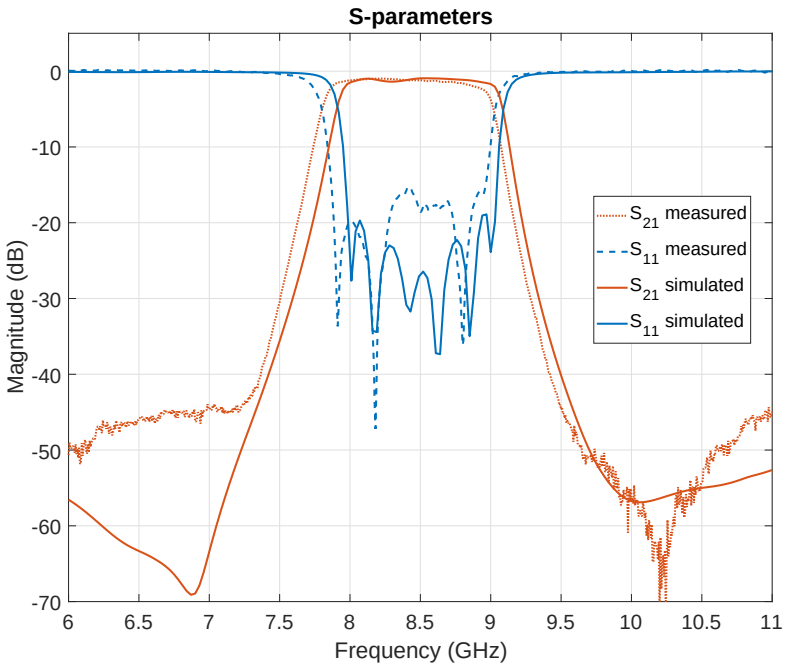

Figure 5.3: 6-th order X-band Hairpin BPF S-parameters.

in-house manufacturing process low accuracy. Nevertheless, the return loss is better than 15 dB which is enough for a general purpose filter. In addition, a frequency shift of about 100 MHz is observed to lower frequencies. This is normally caused by a deviation of the substrate permittivity value at the design frequency compared to the datasheet specification. A good solution to this is scaling the design using (5.2) considering the frequency shift to set the new centre frequency at $f_{centre_{final}}$ and then reoptimize. In this design the scaling is not performed as the frequency shift is small enough to no interfere in the frequency of interest of 8.5 GHz and still maintain the spurious rejection and insertion loss desired.

$$ScalingFactor = \frac{f_{centre_{initial}}}{f_{centre_{final}}} \tag{5.2}$$

As can be observed, the measured insertion loss is lower than 2 dB between 7.87 GHz and 8.88 GHz with a minimum value of 0.95 dB at 8.219 GHz. The 3 dB insertion loss bandwidth goes from 7.94 GHz to 8.88 GHz resulting in a 840 MHz bandwidth or 11 % relative bandwidth. The measured insertion loss at the main frequency of 8.5 GHz is 1.18 dB. Regarding the stop bands, the required value of 40 dB suppression is achieved with some margin (measured suppression is 44.59 dB), although the simulated is around 65 dB.

In order to have a robust device, the filter is mounted on a custom manufactured box with SMA connectors attached to it. The final device mounted in the box is shown in Fig. 5.4. The insertion loss at 8.5 GHz inside the box is increased to 1.7 dB which is still below the 2 dB objective.

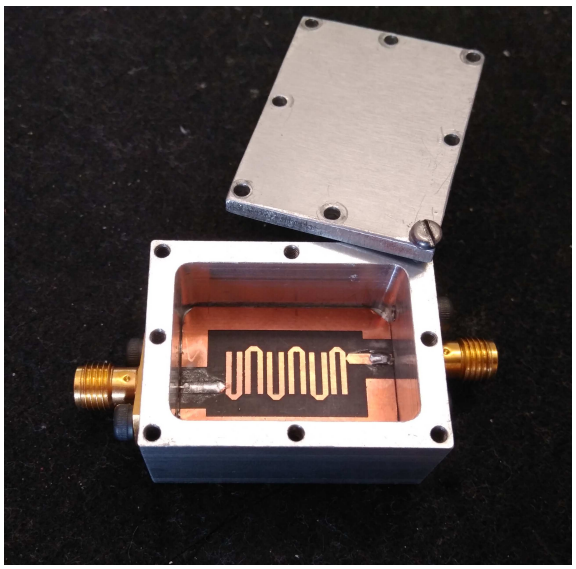

Figure 5.4: Final 6-th order X-band hairpin BPF in box.

5.4.1.2 Ka-band band pass filter

At the last stage of a BUC, reducing the losses is crucial since high frequency components are very costly and a little improvement in performance can result in a significant price increase. Since waveguide technology provides the best performance with lowest losses at higher frequencies, a 6-th order in single ridge waveguide technology is used. This filter was already been designed for a previous project and a prototype is manufactured using a technique robust to tolerances [7]. The manufacturing technique used is based on a simplified two pieces cut as described in Chapter 3 to reduce manufacturing tolerances. In this process, all the ridges and waveguides are grooved in an aluminium part and a lid is used to close the cavity. The manufactured prototype is shown in Fig. 5.5.

The simulated and measured S-parameters are shown in Fig. 5.6. As can be seen the accuracy of this manufacturing process is really high with a very good agreement between simulated and measured results. Therefore this manufacturing technique yields very good results for a really quick and simple process. The filter passband at -3 dB insertion loss is from 28.2 GHz to 32.1 GHz resulting in a 3.9 GHz 3 dB

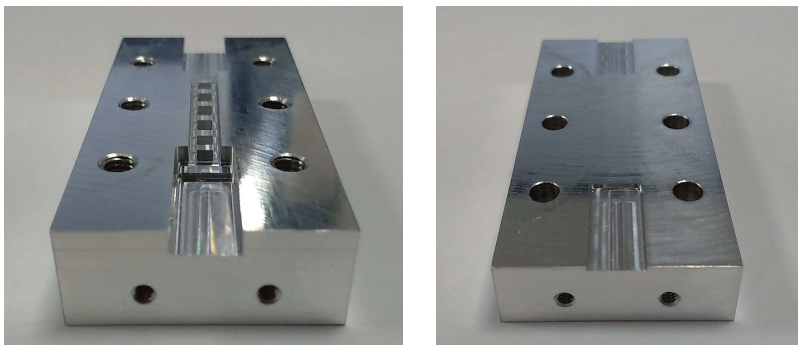

Figure 5.5: 6-th order single ridge waveguide BPF manufactured prototype.

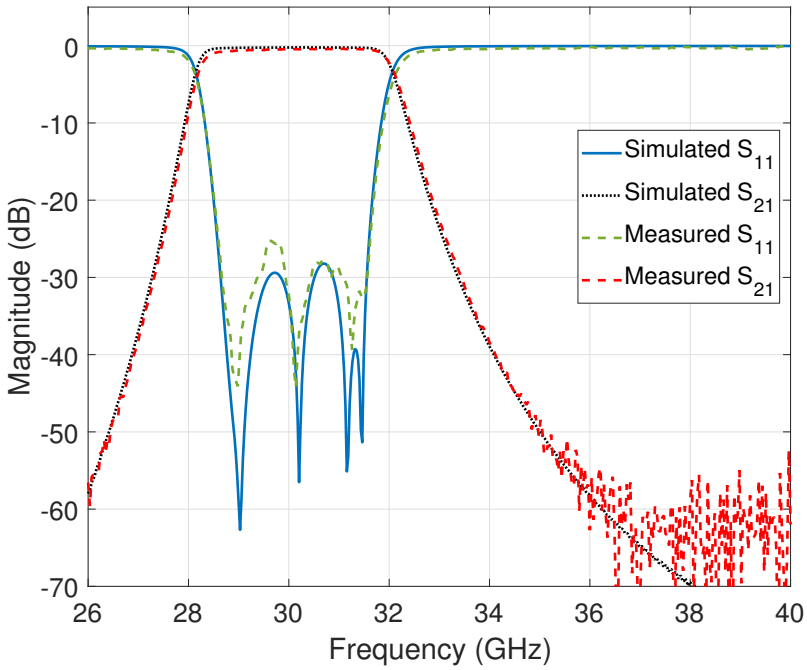

Figure 5.6: 6-th order single ridge waveguide S-parameter results.

bandwidth or 7.73% relative bandwidth. The measured insertion loss at the output frequency of 30 GHz is 0.46 dB and the measured return loss is higher than 25.3 dB in the complete passband.

5.4.2 Components selection

Once the architecture is selected, an available components search and identification is carried out. Due to the wide variety of components available in the market, this can be an arduous task. To simplify the search, the components are selected focusing on reducing as much as possible the total cost of the system. After several iterations, the selected components that match the defined performance for the

double conversion design are shown in Table 5.3.

Table 5.3: Double conversion list of components

Quatity	**Component**	**Component description**
1	ZX60-V62+	L-band amplifier
1	VAT-3+	L-band attenuator
1	ZX05-153LH+	L to X band mixer
1	X-band BPF	8.5 GHz custom filter
1	ZX60-183A+	X-band amplifier
2	FW-3+	X-band attenuator
1	MM1-1140H	X to Ka band mixer
1	Ka-band BPF	Custom filter
1	TGA4903-SM	Ka-band driver amplifier
1	CA2931-2031	Ka-band high power amplifier
1	PLO-4000	7 GHz oscillator
1	PLO-4070	21.6 GHz oscillator
1	ZX10-2-12+	Power splitter
2	141-3SM+	Cable
1	141-4SMRC+	Cable
4	141-3SMRSM+	Cable
4	2.92 mm Male to Male	Cable
4	AT40A-3637-B40-03	K-band attenuator
2	K to WR28 adaptors	Coaxial to waveguide adaptor

5.4.3 Budget and spurious analysis simulations

The performance of an RF system can be studied using RF budget and spurious analyses. A budget analysis can simulate the performance of the overall system or at specific points within it, in terms of different parameters such as gain, noise figure, and IP3 (third order intercept point) among others (power, DC consumption, etc). These measurements determine the linear and non-linear behaviour of the system. To simulate this, the system schematic is implemented in SystemVue software by Keysight including all the possible parameters for each component and considering

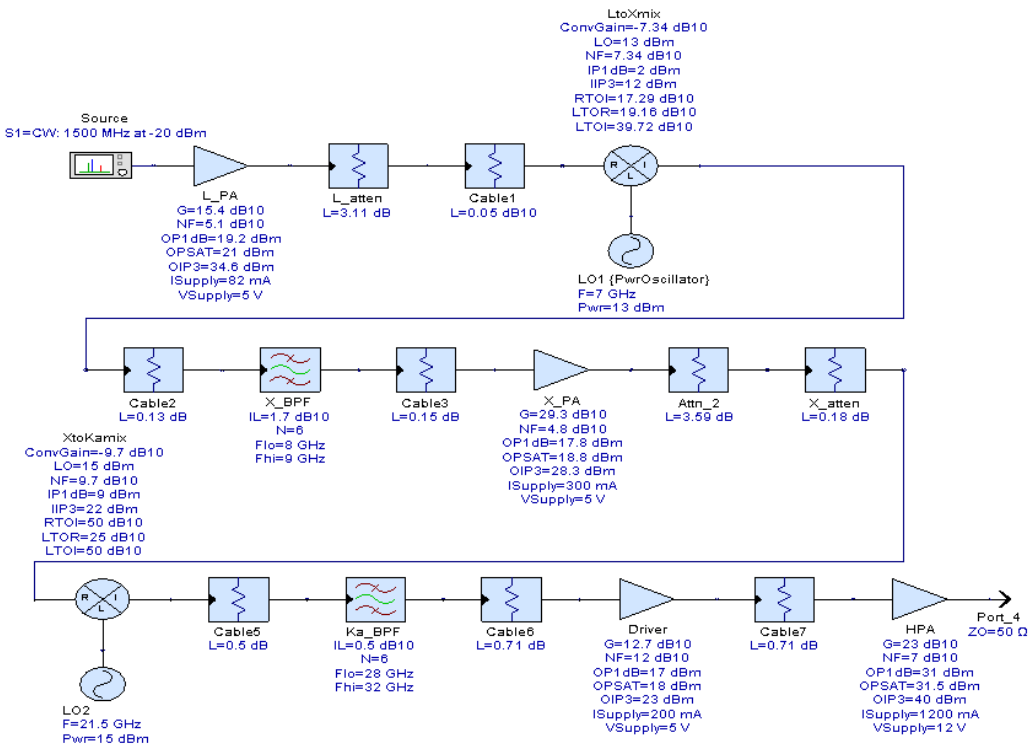

Figure 5.7: Double conversion system schematic in SystemVue.

all the intermediate losses due to cables. The simulated schematic in SystemVue with all the parameters is shown in Fig. 5.7.

5.4.3.1 Spurious analysis

In a real system, not only the desired frequencies appear at the output but also all the signals generated in the components due to mixing, harmonics or intermodulations products caused by non-linearities. Therefore, the output bandwidth of interest might end up containing undesired components that could degrade or even destroy the useful signal. To achieve a clean spectrum with no interfering high power signals, a spurious analysis is performed. The resulting output power spectrum simulated for the double conversion BUC is shown in Fig. 5.8.

As can be seen, the output spectrum is composed of the main output tone at 30 GHz and several spurious generated by the system non-linearities. These spurious simulated are below the noise floor of the system represented by the horizontal line. As a result, the expected spectrum for this system is a clean output tone at 30 GHz with no spurious signal of significant level that could affect the performance of the

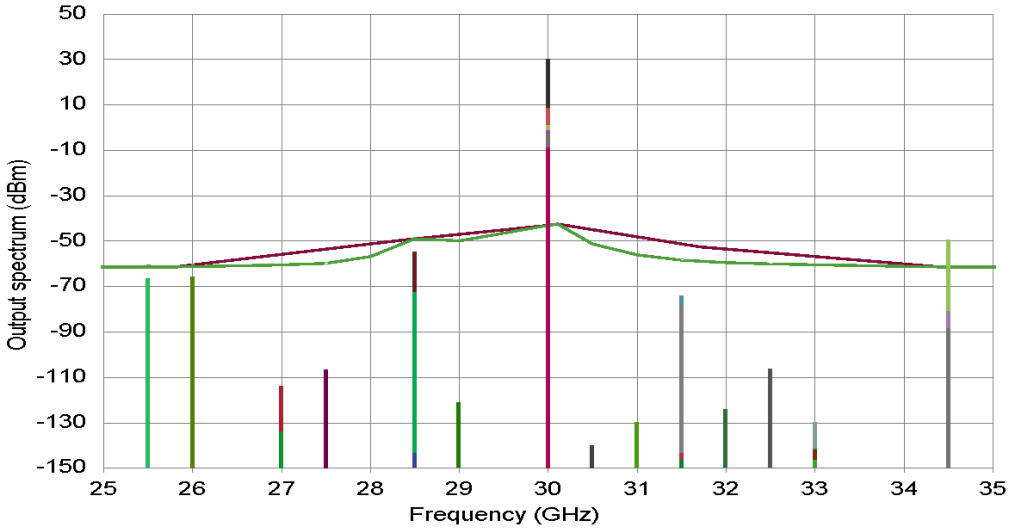

Figure 5.8: Double conversion system output spectrum for spurious analysis.

system.

5.4.3.2 Cascaded gain and P1dB compression point

The cascaded gain of the system is shown in Fig. 5.9. The cascaded gain is calculated as in (5.3).

$$G_T = G_1 = G_2 + ... + G_n \tag{5.3}$$

where n is the number of stages and G_T is the total gain of the system.

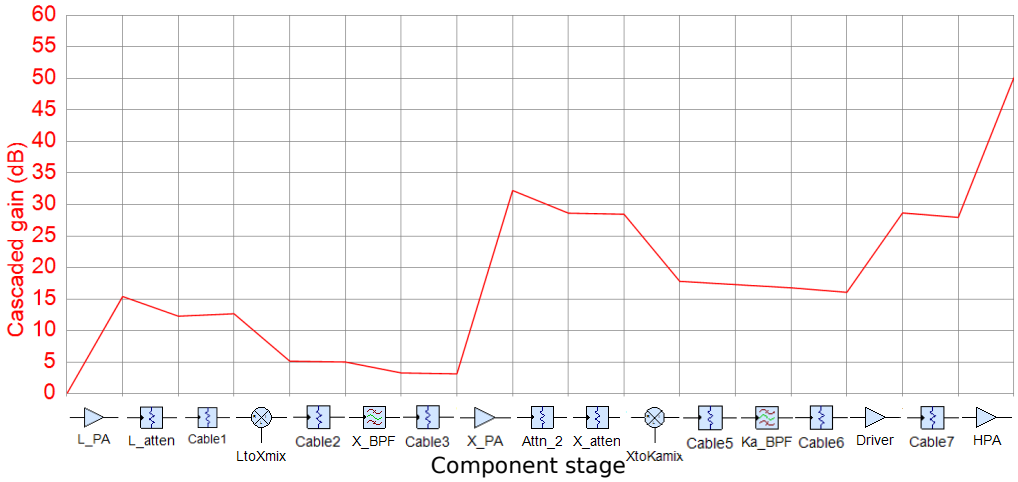

Figure 5.9: Double conversion system cascaded gain.

As can be observed, the gain reductions due to the frequency conversions and fil-

tering are compensated with the amplifiers. The last stage of driver and power amplification then boost the gain until its maximum final value of 50.33 dB. This value meet the required gain of 45 dB and set the P1dB at the input of the system at -20.7 dBm as can be seen in Fig. 5.10. This input power is consistent with the power output for a typical DVB-S2 modulator available in the market, usually in the range of -30 dBm to 0 dBm [8].

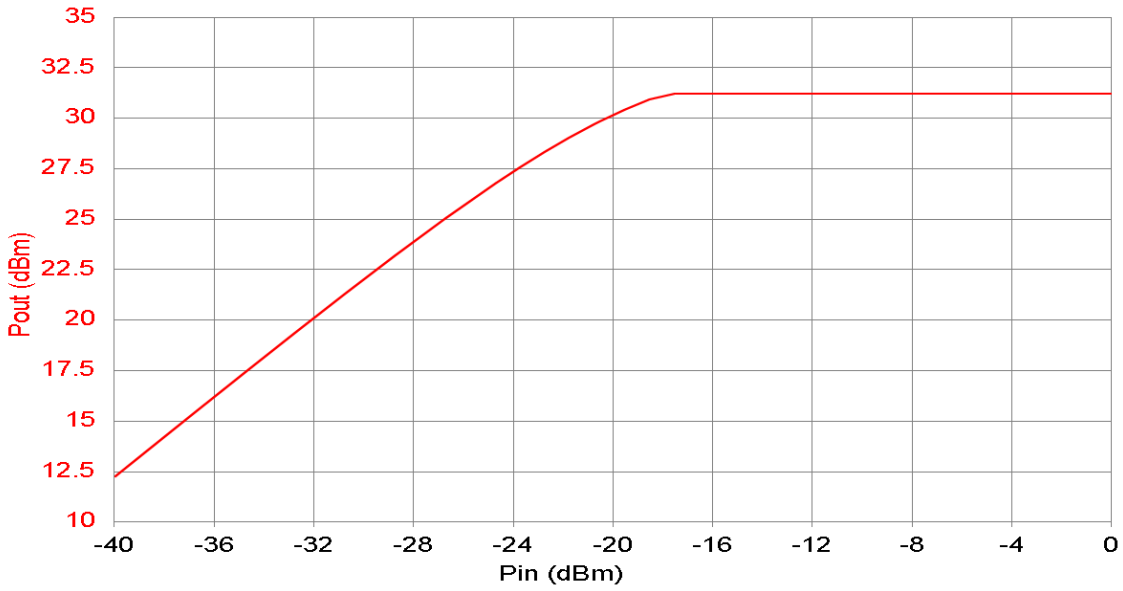

Figure 5.10: Double conversion Pin/Pout.

5.4.3.3 Third order intercept point

The simulated system cascaded output IP3 in SystemVue is shown in Fig. 5.11, with an output value of 37.46 dBm. This value represents the theoretical output power where the fundamental and third order frequency power components are equal (Fig. 5.12). In practise, the saturation of the devices makes this point impossible to reach but it is a reference value that offers an easy way to calculate how the level of the intermodulation products are in the system output and therefore the spectral regrowth produced in a modulated signal. Consequently, a high output third order intercept point will reduce adjacent channel interference in a multi-carrier system, reducing the error probability and improving the quality of the communication.

To calculate the expected third order intercept point, a two tone signal is introduced at the input of the system and the intermodulation products are analysed. All the possible variations of $mf_1 + nf_2$ appear at the output because of the non-linear

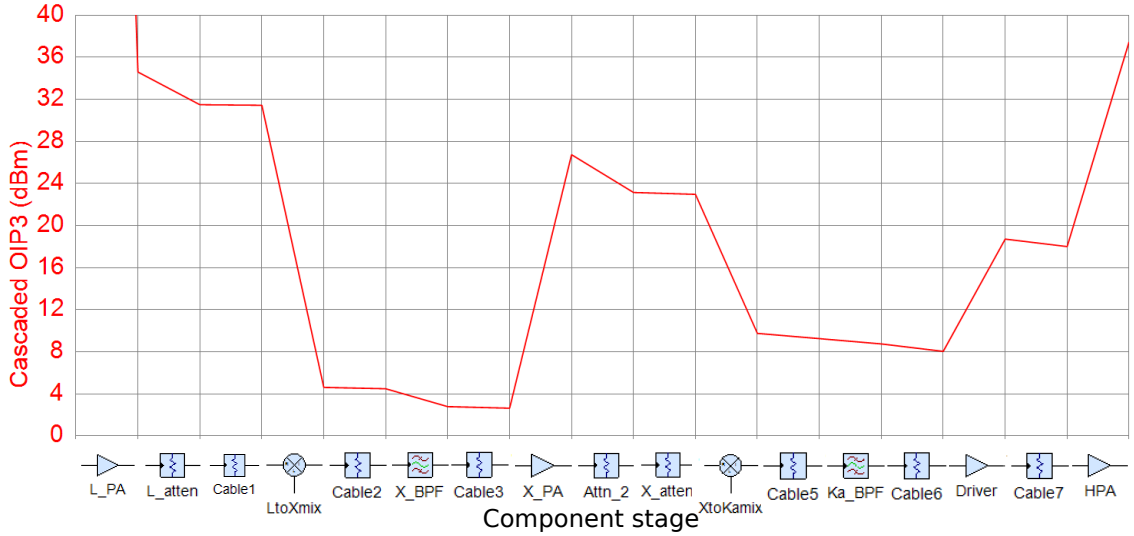

Figure 5.11: Double conversion system cascaded output IP3.

behaviour of the system. Among them, the third order ones are the most dangerous as they appear very near to the useful frequency, making impossible to filter them out (Fig. 5.13). Using the intermodulation products, the third order intercept point can be calculated as in (5.4).

$$OIP3 = \frac{IMD3}{2} + P_o \tag{5.4}$$

Where Po is the power of any of the two fundamental tones and IMD3 is the difference between one of the fundamental tones and the third order products ($IMD3 = Po - P_{3rd}$). For a cascaded system, the total OIP3 is calculated from the OIP3 of each stage using (5.5) for an N stages system.

$$\frac{1}{OIP3_T} = \frac{1}{OIP3_1(G_2G_3...G_N)} + \frac{1}{OIP3_2(G_3G_4...G_N)} + ... + \frac{1}{OIP3_N} \tag{5.5}$$

Looking at the equation, the last stage is the main responsible for the final value of the linearity of the system if the gains are high. Therefore, a last stage with a high linearity and high gain will improve the total third order intercept point and therefore the linearity of the system. A rule of thumb to know approximately the OIP3 of a device is that it is normally 10 dB higher that its output P1dB.

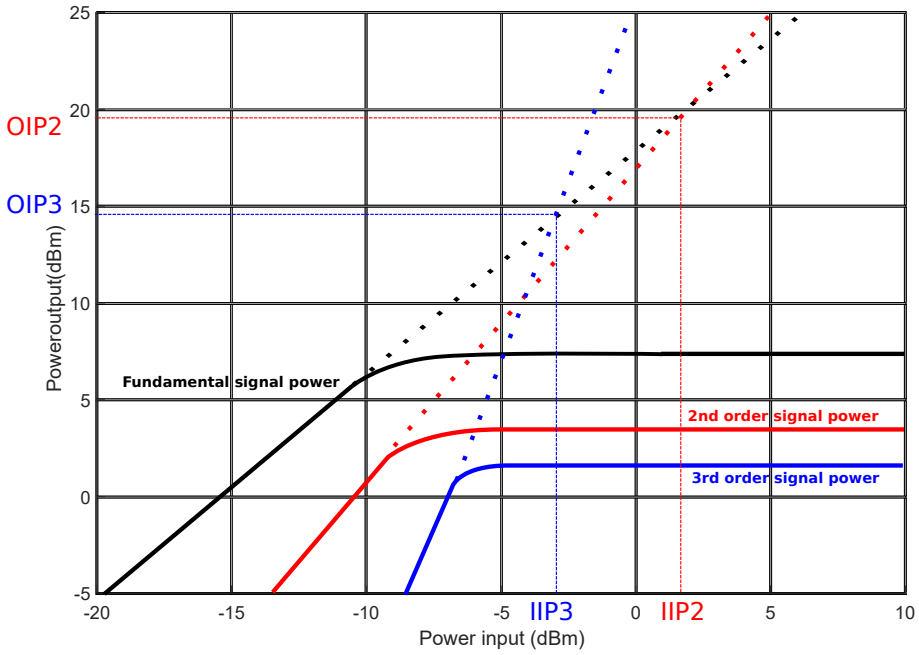

Figure 5.12: Third order intercept point interpretation from Pin-Pout curves.

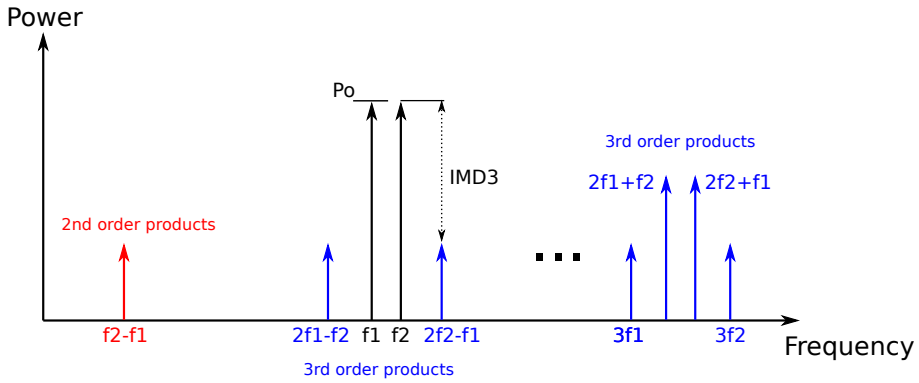

Figure 5.13: Intermodulation products spectrum.

5.4.3.4 Noise figure

The noise figure is a measure of how the signal-to-noise ratio degrades between the input and output of a system/component. Therefore the noise figure can be expressed as in (5.6). The linear form of the noise figure is normally called *noise factor* and represented by F.

$$NF = SNR_{output} - SNR_{input} > 1 \tag{5.6}$$

For a cascaded system, the total noise figure is calculated from the noise factor using (5.7).

$$NF_T = 10log_{10}(F_T) = 10log_{10}(F_1 + \frac{F_2 - 1}{G_1} + \frac{F3 - 1}{G_1 G_2} + ...) \tag{5.7}$$

This equation shows that the first stages are the main responsible for the noise characteristics of the system. Consequently, a first stage with high gain and low noise figure will provide the best overall performance. However, this measurement is more important for receivers than for transmitters due to the much lower input signals. Receiver systems usually require a minimum signal to noise ratio to be able to demodulate a signal, therefore receivers require a low noise amplification and a low total noise figure to maximize the signal to noise ratio.

Simulations of the double conversion system show a maximum noise figure of 11.10 dB. In Fig. 5.14 the predicted performance can be observed. In the first stage the noise figure takes the value of the L band amplifier noise figure and it starts growing after that in a smaller quantity that the respective component until reaching its maximum value.

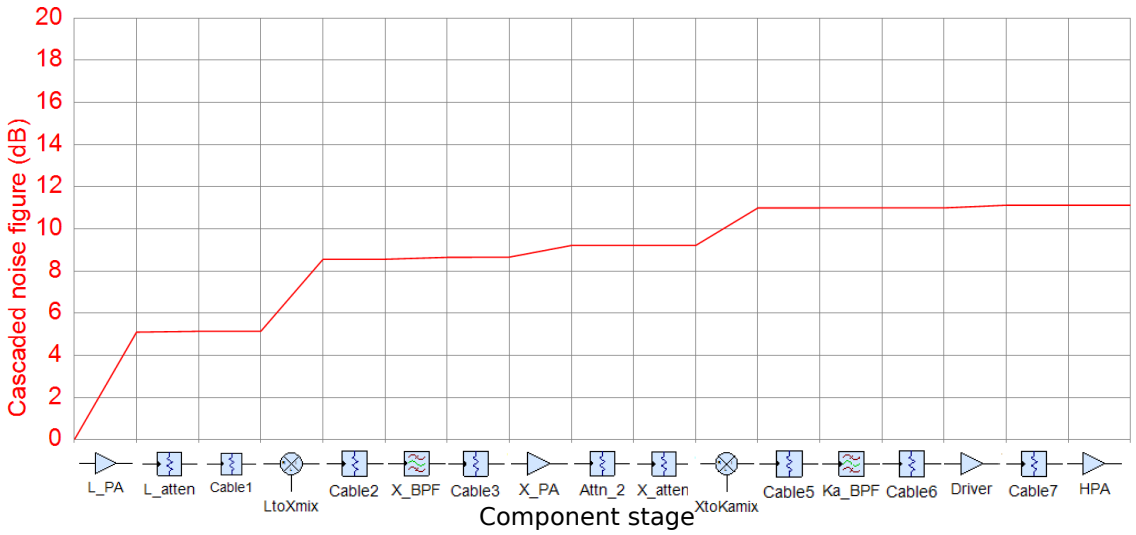

Figure 5.14: Double conversion system cascaded noise figure.

As mentioned earlier, the noise figure value for a transmitter is not very relevant as the output power levels are normally much higher than the noise floor of the system, resulting in a high signal-to-noise ratio.

5.4.3.5 Power consumption

The power consumption of the system can be computed by adding the DC power consumed by each component. For this design, the total DC power is calculated in Table 5.4.

Table 5.4: Double conversion BUC DC power consumption

Component	**Model**	**Voltage (V)**	**Current (mA)**	**Power (W)**
L-band PA	ZX60-V62+	5	82	0.41
X-band PA	ZX60-183A+	5	300	1.5
Ka-band driver PA	TGA-4903SM	5	200	1
Ka-band HPA	CA2931-2030	12	1200	14.4
7 GHz LO	PLO-4000	15	220	3.3
21.5 GHz LO	PLO-4070	15	220	3.3
			TOTAL	23.91

As can be seen, summing all the powers the resulting DC consumption for the double conversion BUC is 23.91 W which is below the maximum desired value of 25 W in Table 5.1. It is important to note that the higher power consumption comes from the last high power amplifier, therefore an efficient power amplifier can save a lot of costs in electricity in a commercial system. As mentioned in earlier chapters, this is a very active research field. For satellite systems, in the space segment, a good efficiency is mandatory in order to save scarce power in space. Also, graceful degradation is very important as it is very costly/impossible to replace components in space. Additionally, in commercial mobile operators, a lower DC consumption implies a lot of savings due to the high number of base stations.

5.4.3.6 Layout planning

Using the designed schematic and the components drawings, a layout for the distribution of the components is produced. In this way the total dimensions of the system can be estimated. These dimensions are considered to fit in a standard 2U rack box, commonly used in the market. The resulting layout is shown in Fig. 5.15, where all the components and RF connections are labelled.

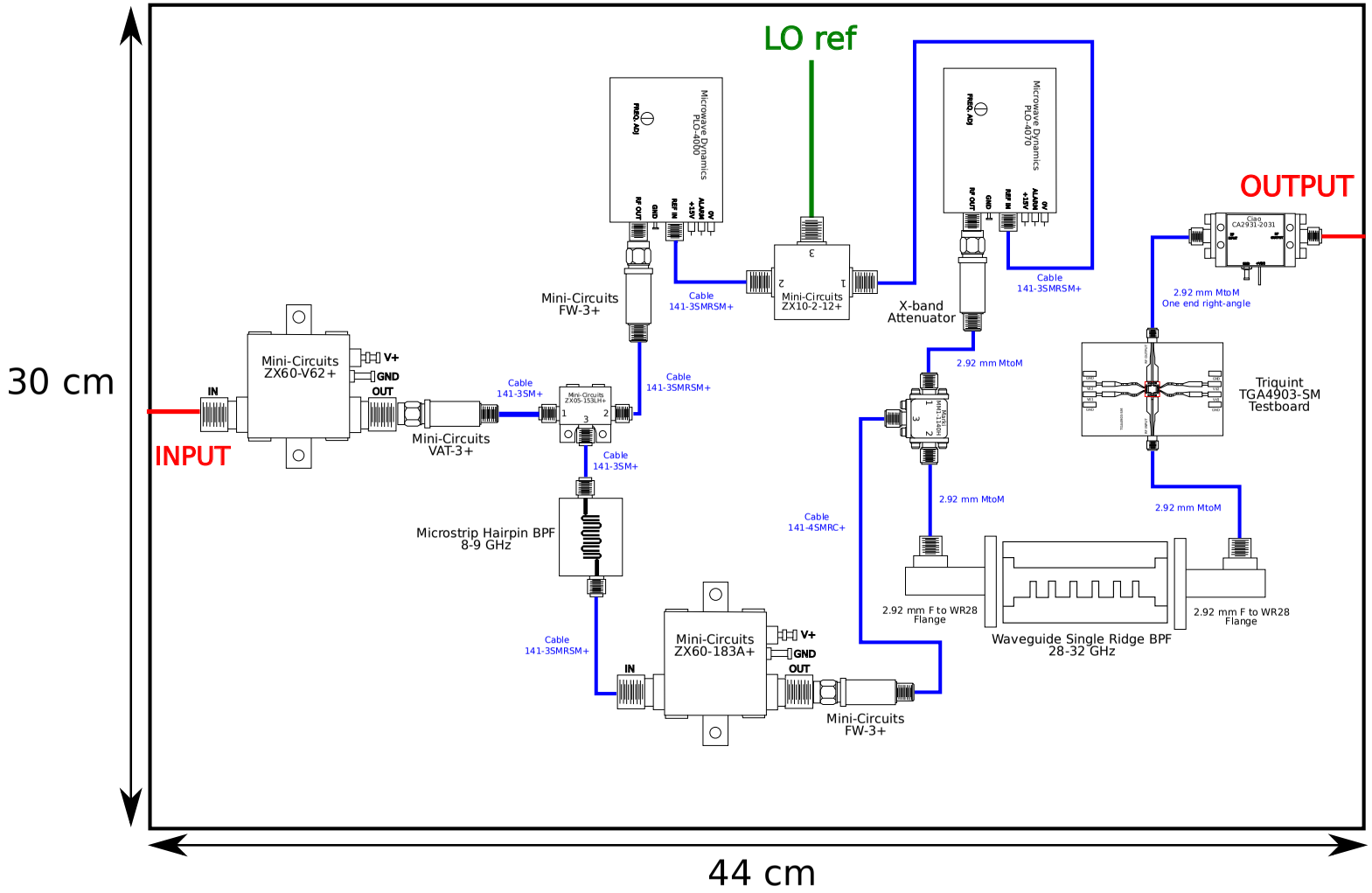

Figure 5.15: Double conversion system floor plan layout.

5.5 Single stage BUC

Once the design of the double conversion up-converter is done, an alternative approach using a single conversion stage is designed using the same available components from the previous design. In this way, a trade-off analysis between both architectures can be realised and their advantages/disadvantages identified.

Due to the decision of reusing as much components as possible, the new architecture is based on the double conversion one. However, in the new single stage architecture, the first mixer and intermediate frequency components are removed, whereas the input and output stages are kept. In consequence, one of this architecture's advantages is the size reduction as a result of the reduced number of components. In Fig. 5.16, a block diagram of the single conversion design is shown.

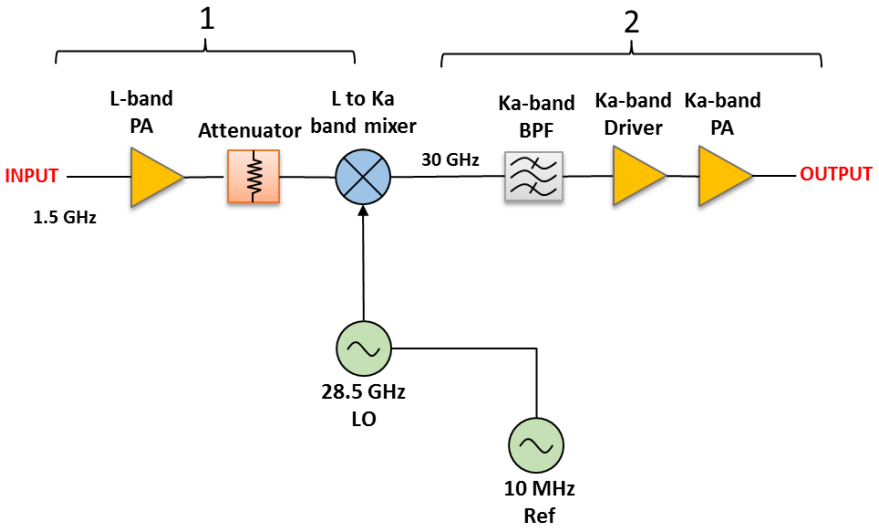

Figure 5.16: Single conversion block up-converter block diagram.

As seen in the block diagram, now the two local oscillators have been substituted by a single oscillator at 28.5 GHz. One disadvantage of the single stage architecture appears here, because of the proximity of this frequency to the final operating frequency at 30 GHz. As a result of the mixer leakage from the local oscillator port to the RF port, this frequency will appear at the output and a high rejection filter (more difficult to design) will be needed to suppress it.

5.5.1 Budget and spurious analysis

Similarly to the double conversion BUC, the single conversion design is simulated using SystemVue by Keysight. The system schematic is very similar to the double conversion one except that the intermediate stage is removed as discussed above. Fig. 5.17 shows the schematic simulated for the single conversion design. Due to this modification, the local oscillator now is 28.5 GHz to achieve the output frequency of 30 GHz resulting from summing the input 1.5 GHz and the local oscillator frequency.

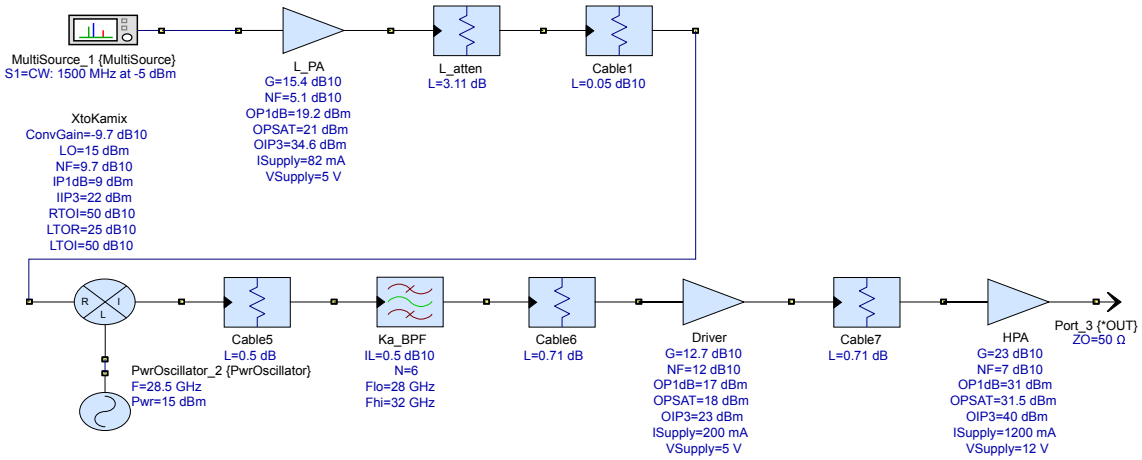

Figure 5.17: Single conversion system schematic in SystemVue.

5.5.1.1 Spurious analysis

A spur analysis for this design is depicted in Fig. 5.18. In this design, the level of the spurious around the useful frequency is much higher than for the double conversion design. As can be seen the tone at 30 GHz appears at the correct power of 30 dBm but some high power level tones at the local oscillator frequency (due to leakage), and at 1.5 GHz multiples from the input, being the higher one the resulting from the lower band generated by the mixer at $f_{LO} - f_{in} = 27$ GHz. If the output desired bandwidth is within the region free of spurious this is not a big drawback but it is desirable to have a clean spectrum and avoid out of band signals which could interfere with systems operating at these other frequencies. Additionally, the ITU organisation has a set of regulations of powers that can be emitted outside the working bands to avoid interferences.

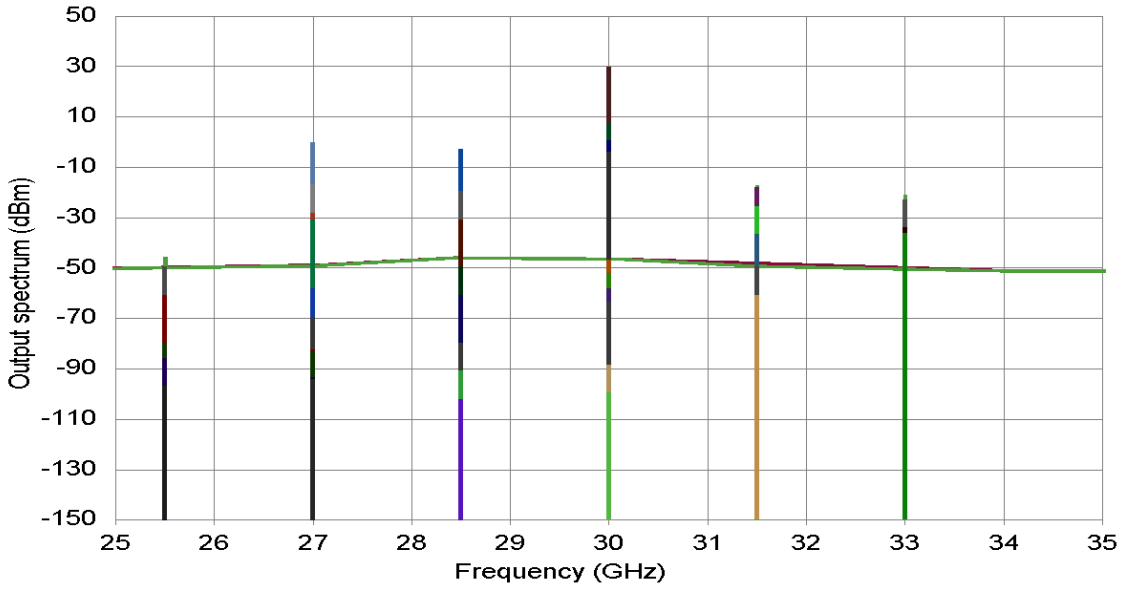

Figure 5.18: Single conversion system output spectrum for spurious analysis.

5.5.1.2 Cascaded gain and P1dB compression point

The simulated cascaded gain for this design is shown in Fig. 5.19. As can be seen, in this case the gain is reduced to about 34.3 dB thus not meeting the stated requirement of 45 dB. A low cost solution to this would be changing the input L-band amplifier with higher gain to reach the 45 dB. Nevertheless, since the purpose of this design is to use the same components, these are fixed and the gain reduction is considered another disadvantage of the single conversion architecture.

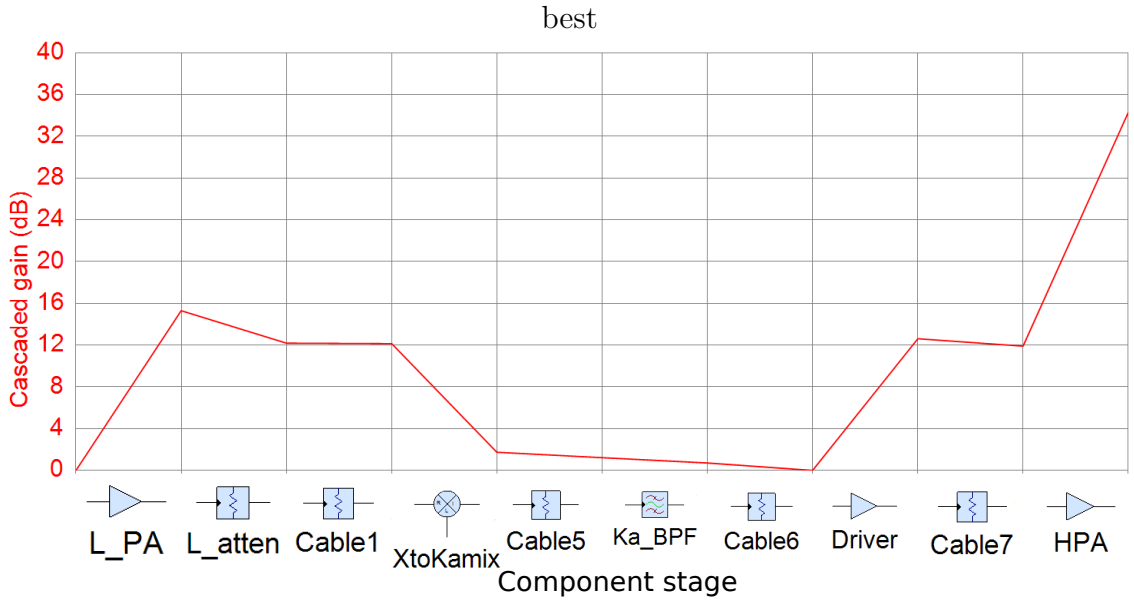

Figure 5.19: Single conversion system cascaded gain.

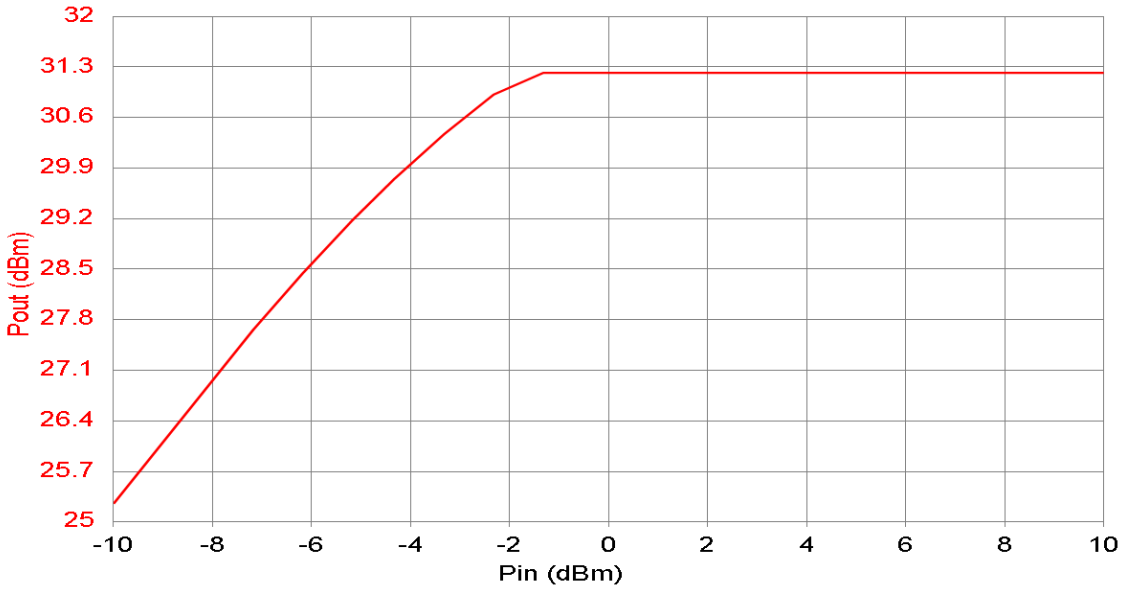

Figure 5.20: Single conversion system Pin-Pout.

The diagram for input and output power characteristic is represented in Fig. 5.20. As can be observed, in this case the input P1dB is at -3.7 dBm, which is much higher compared to the double conversion architecture. However, this level is within the typical range for satellite modulators, which is around -30 dBm to 0 dBm as discussed above.

5.5.1.3 Third order intercept point

The output third order intercept point for the single conversion design is shown in Fig. 5.21. The value for the complete system is 37.95 dBm, being this value higher than the simulated for the double conversion system. This is because, as discussed in the double conversion system, the OIP3 is primarily determined by the last stages of the system and as can be observed it is mainly reduced by the mixing stages. Therefore, as this design has only one mixer, the total OIP3 is slightly higher compared to the double conversion system. In this case, there is no notable difference between both designs and the non-linear behaviour of the two systems will be similar.

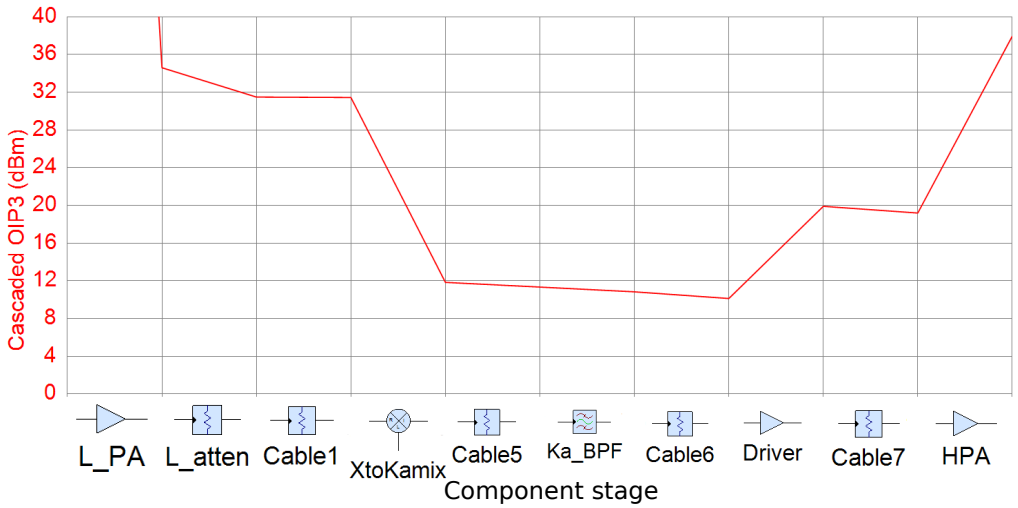

Figure 5.21: Single conversion system cascaded output IP3.

5.5.1.4 Noise Figure

Contrary to the third order intercept point, the noise figure is mainly determined by the first stages of the system. In general, the last amplification stage containing the driver and the high power amplifier, are the devices with higher noise figure. Consequently, in a single conversion system, this last stage is closer to the input and therefore the resulting noise figure will be higher than in a double conversion system, where the intermediate frequency has normally a lower noise figure. This result is shown in Fig. 5.22, where a total noise figure of 13.8 dB compared to the 11.10 dB of the double conversion system is obtained.

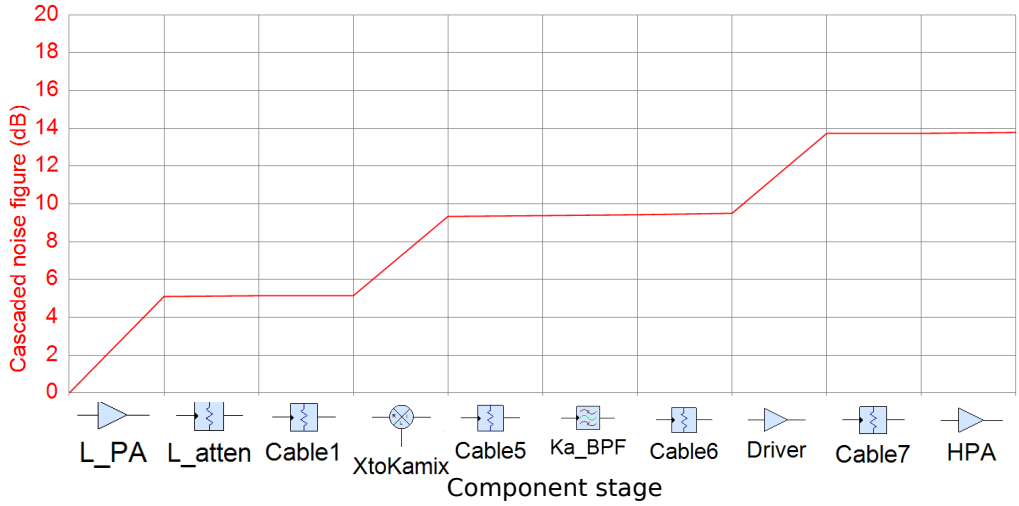

Figure 5.22: Single conversion system cascaded noise figure.

5.5.1.5 Power consumption

The power consumption for the single conversion BUC is shown in Table 5.5. As can be expected, the total DC power consumed is lower due to the reduced number of components with a value of 19.11 W. Concretely, the two components that contributed to DC consumption and now they are removed are one oscillator and the intermediate frequency amplifier. However, despite of removing them, the amount of power consumption is not greatly reduced. This is because the main consumption results from the last power amplification stage, consuming 15.4 W out of the total power.

Table 5.5: Single conversion BUC DC power consumption

Component	**Model**	**Voltage (V)**	**Current (mA)**	**Power (W)**
L-band PA	ZX60-V62+	5	82	0.41
Ka-band driver PA	TGA-4903SM	5	200	1
Ka-band HPA	CA2931-2030	12	1200	14.4
28.5 GHz	PLO-4070	15	220	3.3
			TOTAL	19.11

5.6 Measurements

Once both the double and single conversion architectures have been designed and simulated, the components are bought and the designs implemented and tested. The set up environment is set using existing laboratory equipment thus removing the need of buying the oscillators. All the simulated parameters are check but the noise figure due the measurements capabilities of the laboratory. The test set up implemented for the double conversion BUC is shown in Fig. 5.23.

As can be seen, the input signal is generated using a vector signal generator model MXG N5182B. The output signal is analysed using a spectrum analyser model PXA N9030B. As mentioned above, the local oscillator signals are created using existing laboratory equipment, concretely for the 7 GHz local oscillator a network analyser model PNA N5225A is used in CW mode and for the 21.5 GHz oscillator an analogue signal generator model MXG N51838 is used. In order to have a common

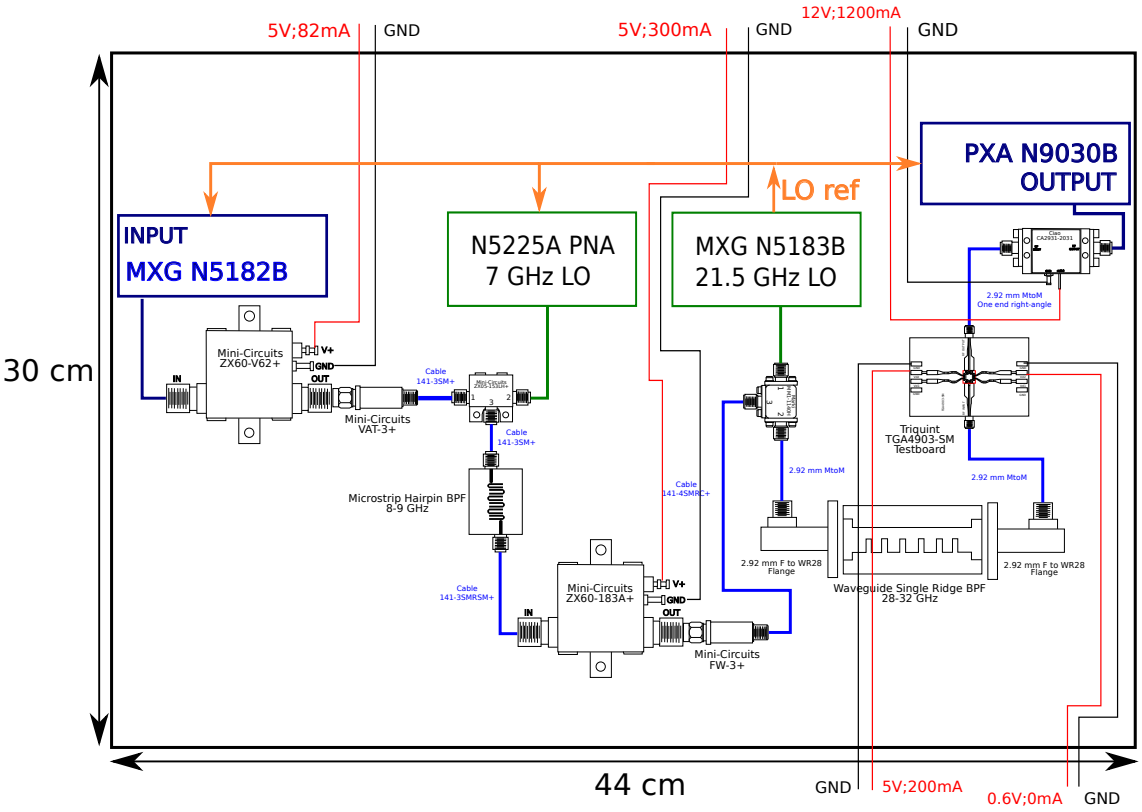

Figure 5.23: Test set up diagram.

reference for all the equipment, the 10 MHz reference output from the analogue signal generator is used because it is the more pure and with less phase noise among all the equipment. This signal is shared between the other equipment using BNC cables. Additionally, the biasing cables for the active components are supplying the necessary voltages and currents to all the devices. To do this, 3 double output power supplies are used. The final set up in the laboratory is shown in Fig. 5.24.

To build the single conversion BUC, the PNA local oscillator signal is removed and the tone at 26.5 GHz is generated by the analogue signal generator. Also, only 2 power supplies are needed for this architecture.

5.6.1 Spectrum measurements

5.6.1.1 Spurious and input 1 dB compression point

First of all, the output spectrum for both architectures is measured. The measured spectrum for the double conversion BUC is represented in Fig. 5.25. The output power for a -19.7 dBm input power is 29.8 dBm. Since the maximum input power

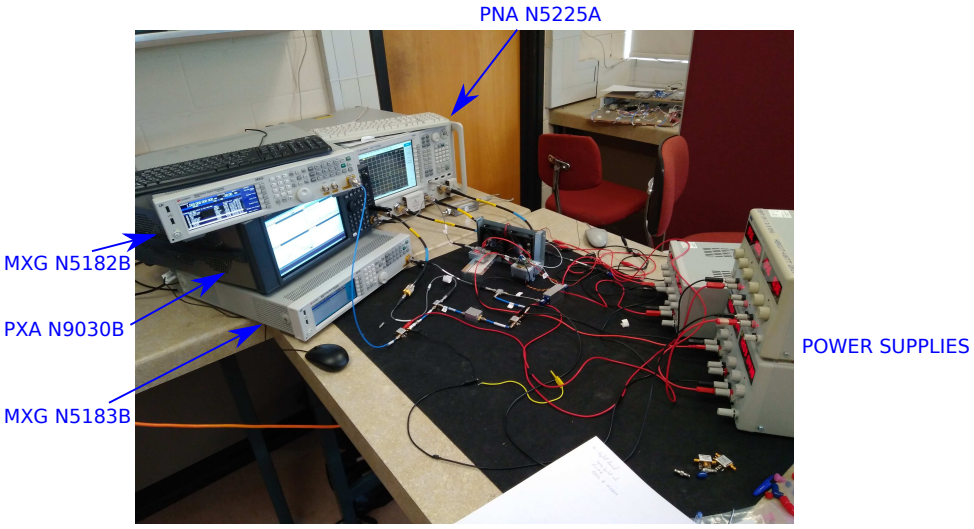

Figure 5.24: Photo of system measurement set up in laboratory.

to the spectrum analyser is 30 dBm the power is not further increased for security even considering the output cable losses. Nevertheless, it can be extrapolated that the P1dB is -19.5 dBm compared to the -20.7 dBm in simulations. This is due to the previously mentioned possible differences between real components and its specifications in the datasheet. This output power results in a total gain of 49.5 dB, meeting the requirement of 45 dB in Table 5.1.

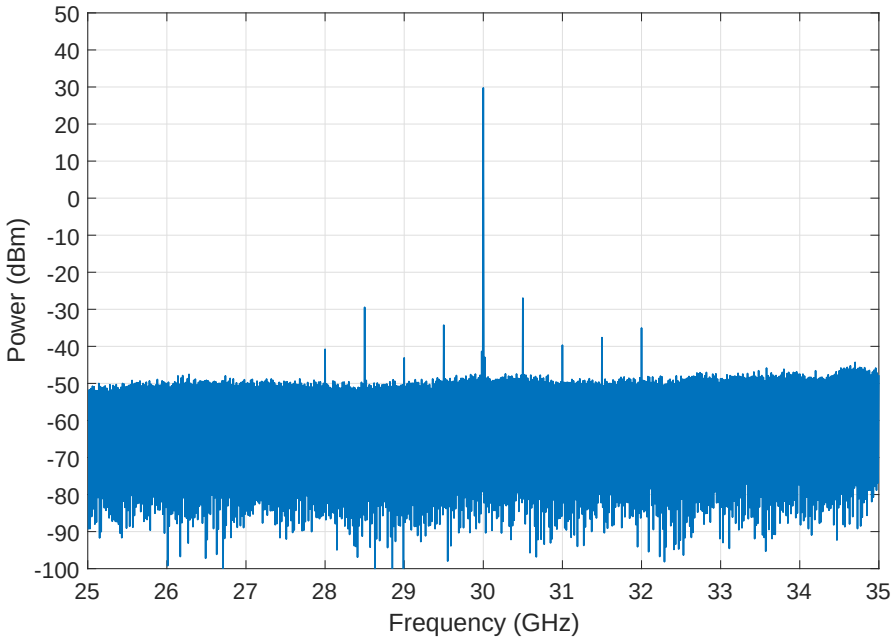

Figure 5.25: Double conversion BUC spectrum. Pin = -19.7 dBm

Regarding the spurious response, it can be seen that additional spurious have appeared compared to simulations. The inaccuracy of the simulation due to the order

of harmonics and spurious considered being very low might end up in this results. However increasing the spurious exponentially increase the simulation time. In any case, the spurious are very well below the main signal as expected, at around -60 dBc which is enough to neglect them as possible cause of interference.

In Fig. 5.26, the spectrum for the single conversion BUC is represented. Here, it can be seen that the expected spurious response is obtained. Due to the reduced number in components in simulation (and therefore the reduced spurious generated), the accuracy is better than in the more complex double conversion BUC. As can be seen, the 28.5 GHz local oscillator leakage is the higher level spurious at -7.5 dBm. This and the rest of the spurious are in general at higher power levels than in the double conversion case, being more susceptible to cause interferences in external systems.

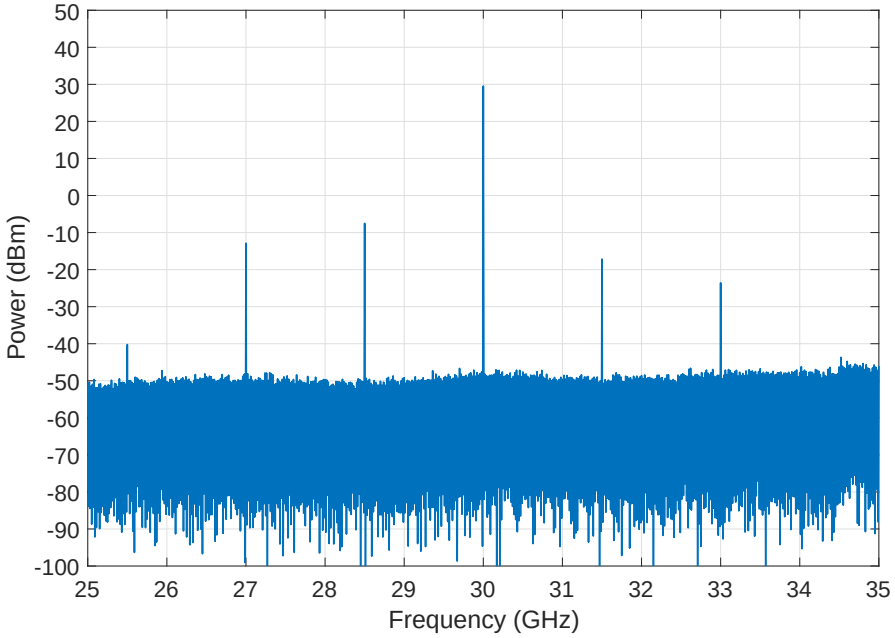

Figure 5.26: Single conversion system cascaded noise figure.

Similarly to the double conversion BUC, the calculation of the P1dB is done by reaching a near value to 30 dBm for security and then extrapolated. In this case the input power is -3.5 dBm to get a 29.5 dBm output power. Consequently, the input P1dB of the system is around -3 dBm compared to the simulated -3.7 dBm. Finally, the gain achieved for this system is 33 dB compared to the simulated 34.3 dB.

5.6.1.2 Third order intercept point

To measure the output third order intercept point, the two tone test methodology described in previous sections is used. To do this, a signal composed of two tones spaced 1 MHz is introduced at the input of the block up-converter. As a result, the output spectrum contains the two tones and the intermodulation products generated by the system non-linearities. From these power levels and using (5.4) the output third order intercept point of the complete system can be calculated.

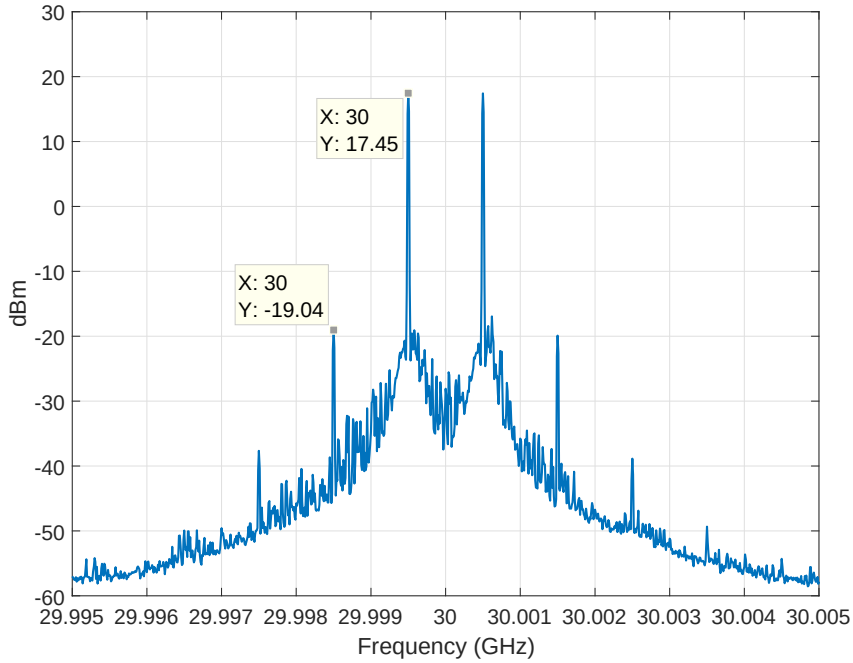

Figure 5.27: Two tone output to measure TOI for double stage BUC.

In Fig. 5.27 the output spectrum resulting from the two tone test for the double conversion BUC is shown. As can be seen, the power level of the fundamental tones is 17.45 dBm and the third order products have a -19.04 dBm level. Using (5.4) the OIP3 for the double stage system is 35.7 dBm.

On the other hand, the spectrum for the single conversion BUC two tone test is shown in Fig. 5.28. In this case, the fundamental tones are at 20.76 dBm and the third order products at -10.44 dBm. The resulting OIP3 is then 36.36 dBm.

In both systems, the measured value is lower than the simulated one. In the case of the double conversion BUC, the simulated OIP3 is 37.46 dBm versus the measured 35.7 dBm and for the single conversion BUC the simulated value is 37.95 dBm

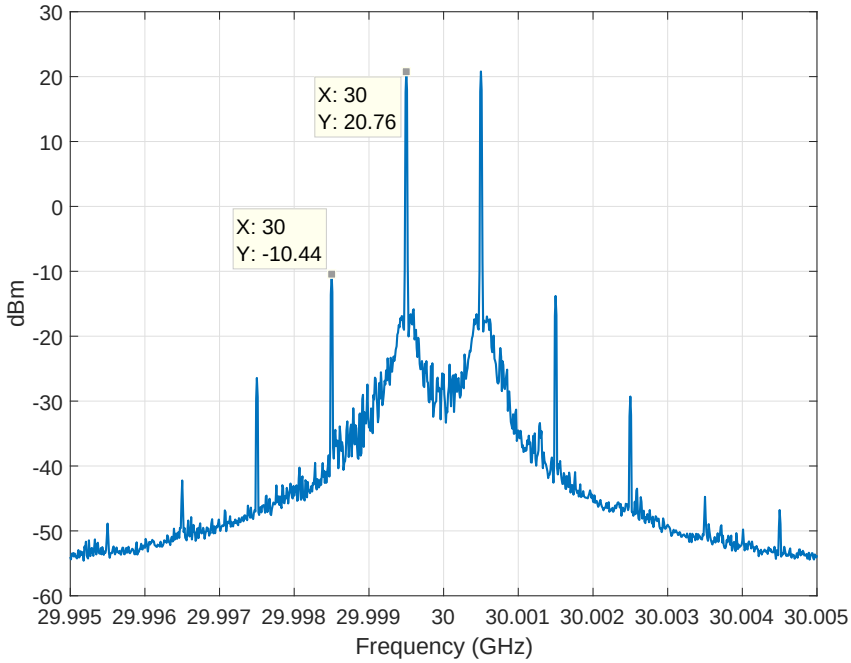

Figure 5.28: Two tone output to measure TOI for single stage BUC.

compared to the measured 36.36 dBm. This different is caused by a lower value of the OIP3 of the real components compared to the datasheet value. However, as can be seen, the expected better performance of the single conversion system compared to the double conversion one is clearly achieved.

5.6.2 Power consumption

The power consumption for the double conversion BUC is measured by adding the power consumption of all the power supplies. The calculated powers agree with Table 5.4 when the system is operating in a linear region (well below the input P1dB input power) and removing the two local oscillators. As a result, the total power consumed is 17.31 W. However, when the power is increased and the input power starts compressing the system, the current drawn by the last high power amplifier increases up to a value of about 1800 mA. Consequently, the power consumption of the system is increased to 24.51 W. As a conclusion, if the system is in saturation the power consumption will be higher than the requirement considered in Table 5.1. For the case of the single conversion BUC, the calculations are the same but removing the 1.5 W power consumed by the X-band power amplifier. This results in 15.81 W in linear region and 23.01 W in saturation.

5.6.3 Digital modulations performance

To check the performance of the systems under a modulated carrier, several tests are carried out using two types of common modulation schemes in digital communications such as a 16-QAM and a QPSK signals. Both signals have a 4 MHz symbol rate and are introduced at the input of both systems using the vector signal generator MXG N5182B used in previous sections.

5.6.3.1 OIP3 and non-linearities effect

The effect of the third order intercept point and related non-linear behaviour of the system can be evaluated in the resulting spectrum and constellation for a modulated signal. In order to verify that the higher OIP3 of the single conversion stage has an impact on the system performance the constellation and output spectrum for a QSPK is shown in Fig. 5.29 and in Fig. 5.30 for a 16-QAM signal, both at the input P1dB compression point power level.

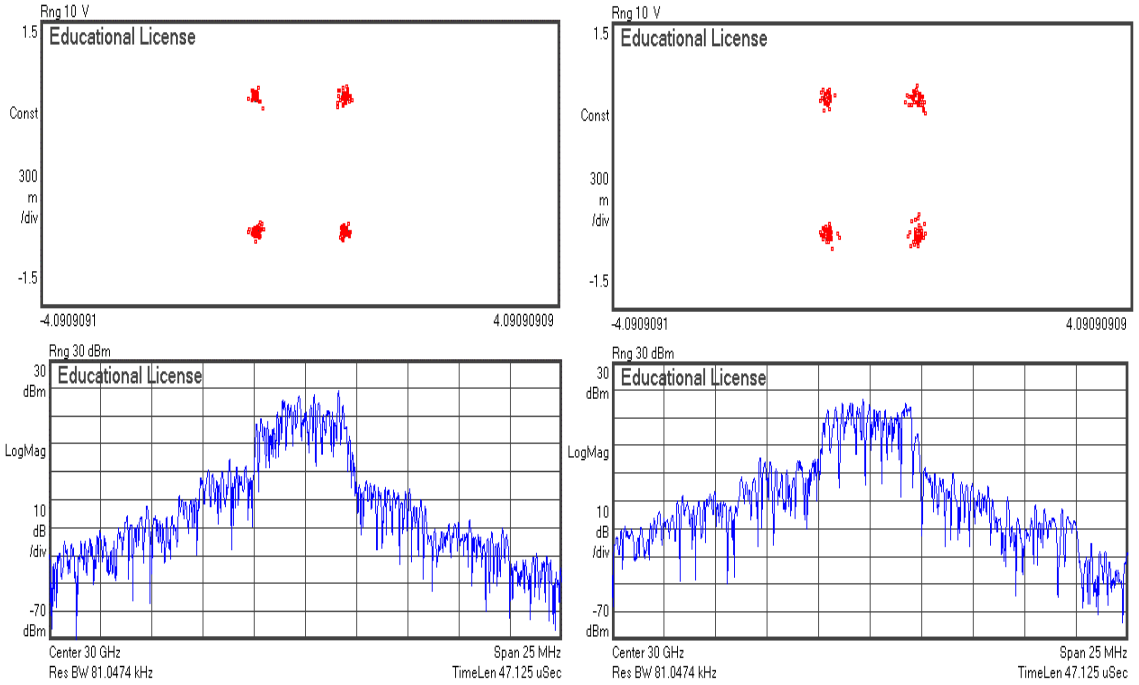

Figure 5.29: Output spectrum and constellation at P1dB for a QPSK signal. Single conversion BUC (Left) and double conversion BUC (Right).

In both figures, the subfigures in the left column are the single conversion BUC measurements and the right columns the double conversion BUC measurements. As can be noticed, the distortion of the double conversion system is higher than for the

single conversion case. Consequently, this can be directly seen in the error vector magnitude (EVM) resulting for the demodulated signal. The EVM measured value for the QPSK signal is 6.53 % and 8.55 % for the single and double conversion BUC respectively.

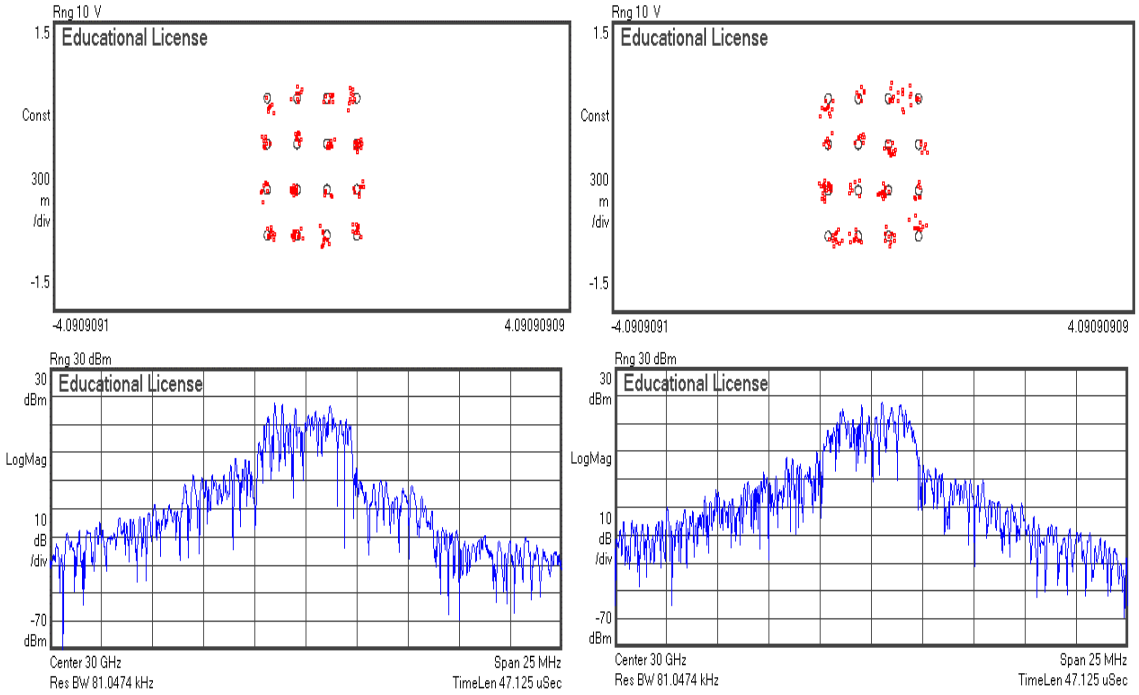

Figure 5.30: Output spectrum and constellation at P1dB for a 16-QAM signal. Single conversion BUC (Left) and double conversion BUC (Right).

On the other hand, for the 16-QAM signal, the measured EVM is 7.96 % for the single conversion system and 11.09 % for the double conversion system. The higher EVM for the double conversion system is related to the non-linear behaviour as discussed before, which results in higher third order products and therefore higher spectral regrowth. This can be noticed in the spectra, where the double conversion system plots present a higher spectral regrowth. The spectral regrowth interferes in the in band signal but also makes the system more susceptible to interchannel interference if a multi-carrier signal was used. This is because of the adjacent power level interfering with adjacent channels.

Finally, as can be also noticed, the higher order 16-QAM modulation results in a higher EVM, which is expected as the distance between symbols is shorter, thus reducing the decision area around the symbols.

5.6.3.2 Phase noise effect

The main parameter that determines an oscillator performance is its frequency stability. This parameter is normally called phase noise and it determines how it the purity of the output frequency generated [9]. If a sinusoid signal is considered and a random phase variation included, the resulting signal can be expressed as in (5.8).

$$s(t) = A\,cos(2\pi f_0 t + \phi_n(t)) \tag{5.8}$$

which can be interpreted as a phase modulated signal. Therefore, the output spectrum of the oscillator will be broadened around the centre output frequency. This is illustrated in Fig. 5.31.

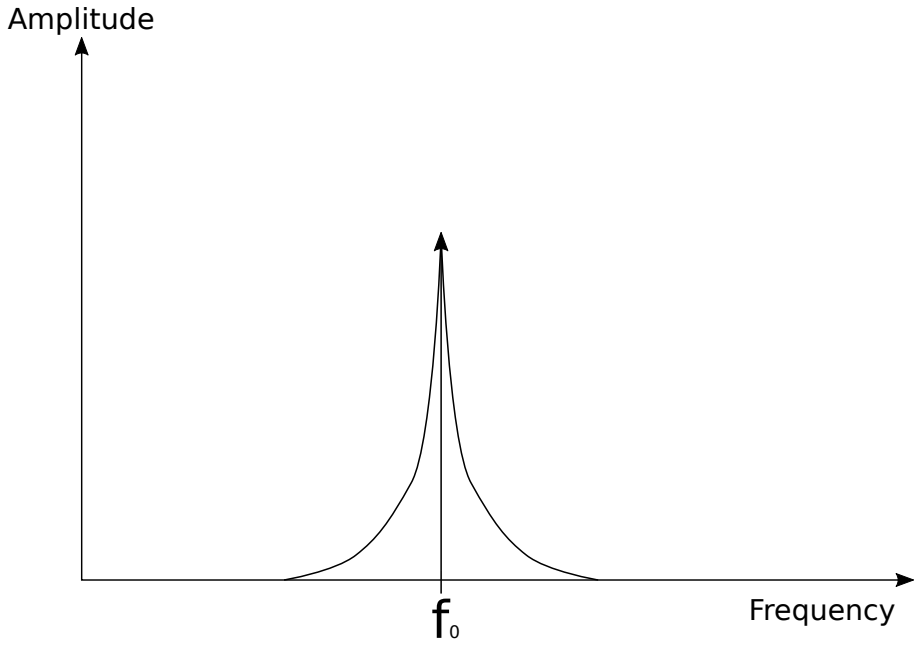

Figure 5.31: Phase noise broadening effect in oscillator output spectrum.

This effect frequency broadening results in a rotation displacement of the constellations for a modulated signal, which increased the related EVM of the system.

In order to test this effect in the BUC prototypes, the 21.5 GHz oscillator of the double conversion system and the 28.5 GHZ oscillator of the single conversion systems are now generated using the PNA N5225A instead of the signal generator MXG N51838 used previously. This is because the PNA has a worse phase noise characteristics compared to the analogue signal generator and thus the effect of the phase noise degradation can be evaluated.

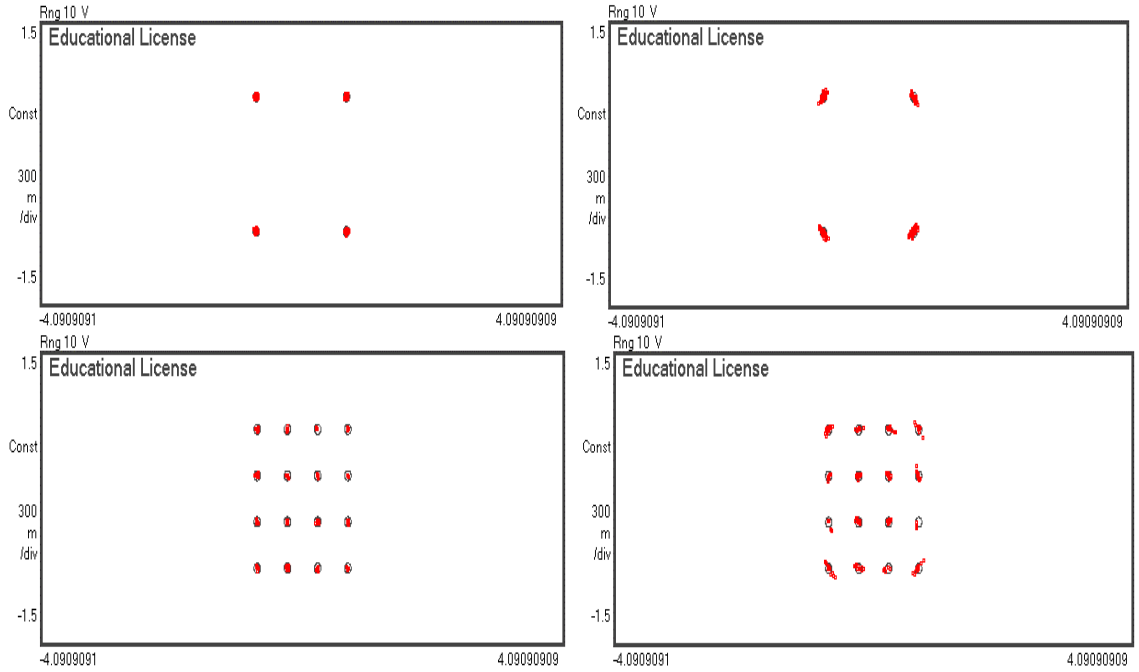

Figure 5.32: Phase noise effect in constellation for a QPSK (Top) and 16-QAM (Bottom) signals in a single conversion BUC.

The resulting measured constellations for the single conversion BUC are shown in Fig. 5.32. As can be seen the expected degradation is obtained for both QPSK and 16-QAM modulated signals. The resulting EVM for the QPSK signal is 2.32 % with good phase noise and 4.74 % for the worse phase noise case, resulting in a 2.42 % degradation. On the other hand, for a 16-QAM signal, the good phase noise EVM is 1.56 % and for the worse phase noise it is 4.63 % resulting in a degradation of 3.07 %.

In Fig. 5.33, the resulting constellations for the double conversion BUC system are shown. The measured EVM for the QPSK signal is 2.64 % for the good phase noise case and 3.72 % for the worse phase noise case, resulting in a 1.08 % degradation. On the other hand, for a 16-QAM signal, the EVM for the good phase noise case is 2.21 % and the EVM for the worse phase noise case is 3.32 %, resulting in a 1.11 % degradation. As can be noticed, in this case the degradation of the constellation is smaller than for the single conversion system. This is because the phase noise performance of the PNA depends on the frequency of operation and in this system the local oscillator has a smaller frequency at 21.5 GHz compared to the 28.5 GHz for the single conversion system. Additionally, the degradation of the 16-QAM signal is higher due to the more complex constellation and shorter symbol distance.

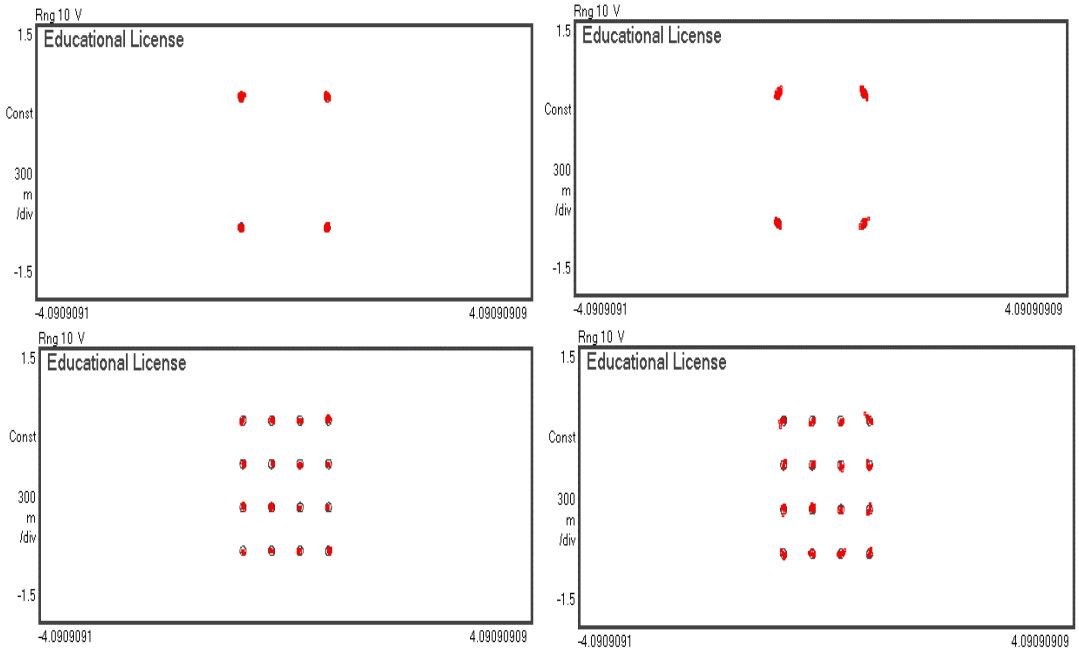

Figure 5.33: Phase noise effect in constellation for a QPSK (Top) and 16-QAM (Bottom) signals in a double conversion BUC.

5.7 Conclusions

In this chapter, the design and implementation of a L-to-Ka band block-upconverter has been presented. The design of a single conversion and double conversion architectures is described and design guidelines to reduce iterations and design time are provided. As a main objective, the cost reduction of the system is considered. To do a fair comparison, the same set of components is used for both architectures. In order to compare the performance of the two systems, the main relevant parameters such as output power and spectrum, compression, gain, third order intercept point and noise figure are evaluated. Lastly, the performance of the systems under a digital modulated signal is evaluated in terms of EVM when the input power is set at the input P1dB compression point. Also, the effect of phase noise in the constellations and the EVM is studied.

As a conclusion, the double conversion BUC system provides a better performance in terms of gain and spurious response. However, if a high spurious level is permitted or a high order and high rejection filter is used to suppress them well below the main carrier, a single conversion system provides some benefits. The main advantage is the lower cost, size and complexity compared to the double conversion system. In addition, the power consumption is lower due to the reduced number of components.

In addition, one of the objectives was to compare the performance of the commercial high power amplifier with the designed power combining amplifier in previous chapters. Due to the unsuccessful first prototype, this comparison is left as a future work for the project.

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Chapter 6

Conclusions and future work

6.1 Conclusions

This thesis has covered the development of new compact power combining amplifiers to be used in millimetre wave block up-converters. After a comprehensive analysis of the available techniques, a new design is presented focusing on compactness and graceful degradation. The design concept is then applied to a 12 chip power amplifier prototype. In addition, the design and implementation of an L to Ka band BUC is carried out in the last chapter.

In Chapter 2, an exhaustive literature review was carried out identifying the advantages and disadvantages of the existing power combining techniques for the development of power combining amplifiers. A tree diagram identifying the relationship between different techniques was presented and each technique described showing the most relevant published work related to each technique.

The objective in Chapter 3 was to develop new compact and efficient power combinig techniques. The travelling wave power combiner was identified as the most suitable power combining technique at mm-wave frequencies. This is due to the ability of accommodating a big number of chips at higher frequencies [1], where the chip sizes are comparable to the passive dividing/combining structures. Then, the design guidelines for a travelling wave power combiner are described, adding a more robust design process that uses equivalent circuit techniques to optimize design time. Using the travelling wave approach, a new design that reduces 50% the size by introducing

a double side placement of the chips is proposed. Finally, a 12-way prototype design and manufacturing is presented [2]. This prototype is manufactured using a technique based on reducing the tolerance sensitivity at high frequencies. The results presented demonstrated a low insertion loss and high efficiency, achieving similar or even better performance that existing solutions for higher number of chips and compactness.

Chapter 4 aimed to develop a power combining amplifier based on the proposed power combining technique. An existing commercial amplifier chip was used. Due to the different substrate needed for the power combiner, a substrate translation technique was demonstrated by manufacturing and testing a single chip test board. Afterwards, the design process for the final boards containing 6 chips each one was described in detail. Correct thermal performance of the prototype was analysed and demonstrated. Additionally, a phase imbalance study and a good performance over the tolerance values for the chips's phases was demonstrated. Unfortunately, the final prototype response was spoiled by an oscillation in the amplifiers response. Therefore, an attempt using different techniques by introducing capacitors and resistors in the biasing lines was done. The reduction of the oscillation and the cancellation of one of the components was demonstrated although a complete elimination could not be achieved.

In Chapter 5, the objective was to design and implement an L-to-Ka band block upconverter and evaluate the performance of the proposed power combining amplifier versus a commercially available amplifier. In this chapter, two BUC architectures are covered, namely a single conversion stage and a double conversion stage systems. The work carried out in this chapter is published in [3]. Design guidelines and tips are given to reduce design iterations and time. A discussion on advantages and disadvantages of each architecture is presented. In conclusion, a single conversion BUC benefits from lower cost and size but has lower gain, higher output spurious and worse robustness against phase noise. Unfortunately, due to the non successful power combining amplifier prototype, the last comparison using a commercial amplifier and the prototype manufactured was not possible at the time of the thesis project.

In general, the work carried out in this thesis demonstrates how new power combining techniques can be used to improve efficiency, increase compactness and robustness. These qualities are needed for a forthcoming scenario where more and

more applications at mm-wave frequencies are expected to develop. Also, the implementation of a up-conversion system to mm-wave frequencies aiming at reducing costs can provide more competitive systems due to the increasing number of systems needed to deploy mm-wave services.

6.2 Future work

The topics covered in this thesis open possible lines of future work:

- In Chapter 3, the new proposed architecture using chips in both sides of the waveguide can be further studied and investigated. The use of coupling slots to transfer the electromagnetic power to the microstrip lines requires a good contact and alignment, which results in IL in the order of 2 dB. Lowest waveguide to microstrip transition techniques can be investigated to improve the overall insertion loss of the power combining technique.
- In Chapter 4, the limited time that was available for the project did not permitted new iterations for the power combining amplifier. A natural next step for this design will be to design again the RF printed circuit board to avoid the oscillation currently present in the design. However, the availability of the chips used is very limited and the best way to proceed is redesign the circuits for a new chip model, similar or with improved performance for a future need.
- In Chapter 5, the comparison of the commercial amplifier used with the power combining prototype is open as a future work. The use of a power combining amplifier will potentially provide a better robustness against damaged amplifiers due to the graceful degradation capability. Additionally, the evaluation of the proposed BUC can be further studied under real commercial signal standards (such as DVB-S2 for satellite). Moreover, this connectorized design has the possibility of evaluating the effect of interchanging a component for another one in the performance of the complete system. This analysis could potentially bring more knowledge in system performance in digital communications and its relationship to specific RF components performance.

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