UNIVERSITAT ROVIRA I VIRGILI
COMPACT MODELING OF MULTIPLE GATE MOS DEVICES.
Hamdy Mohamed Abd El Hamid
ISBN: 978-84-690-8295-9 / D.L: T.1514-2007

COMPACT MODELING OF MULTIPLE GATE MOS DEVICES

A Thesis Presented to The University of Rovira i Virgili
Department of Electronic, Electrical and Automatic Engineering

by

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In Partial Fulfillment of the Requirements
for the Degree of Doctor of Philosophy in Electrical and Electronics Engineering

Supervised by

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Universitat Rovira i Virgili

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Departament d'Enginyeria Electrònica, Elèctrica i Automàtica

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1. Introduction
2. Short Channel Effects in undopded Multiple Gate MOS Devices
    1. SCEs in Cylindrical GAA MOS at low drain-source voltage
    2. SCEs in Cylindrical GAA MOS including DIBL Effect
    3. SCEs in DG MOSFET
    4. SCEs in FinFETs
3. Current Transport in undopded Multiple Gate MOS Devices
    1. Current Models for Long channel Devices
        1. Explicit current Model for Long channel GAA MOSFETs
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    2. Ballistic and quasi ballistic transport in multiple Gate MOS devices
4. Summary

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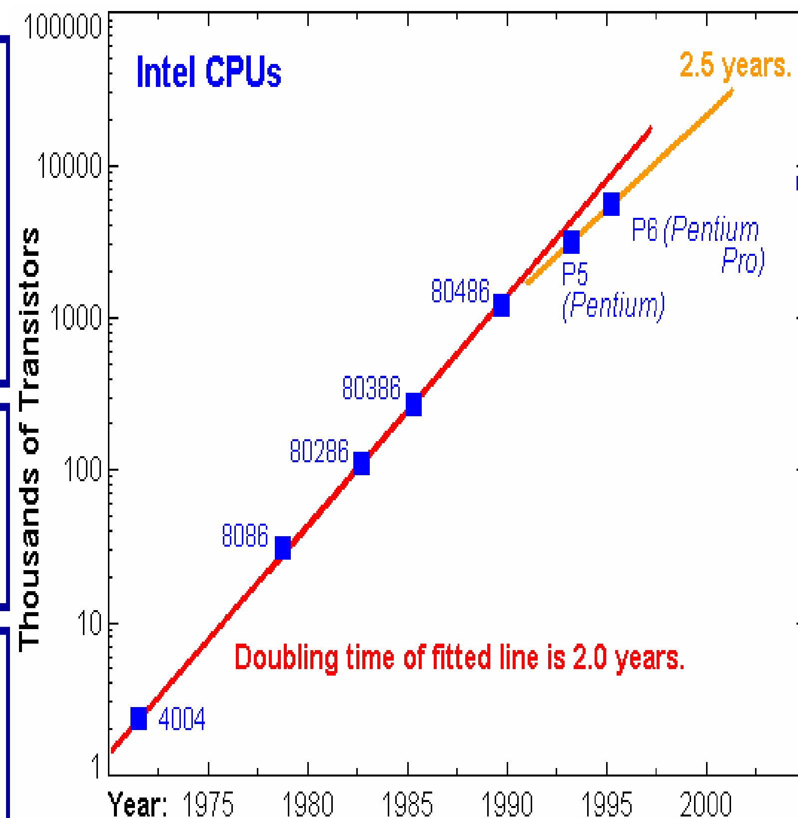
1. Introduction (Moore´s Law and ITRS)

Gordon Moore, 1965

- Moore noted that the complexity of minimum cost semiconductor components had doubled per year since the first prototype microchip was produced in 1959.

Exponential growth, however, also means that the fundamental physical limits of microelectronics are approaching rapidly.

Several observers have therefore speculated about the possibility of "the end of Moore's Law."



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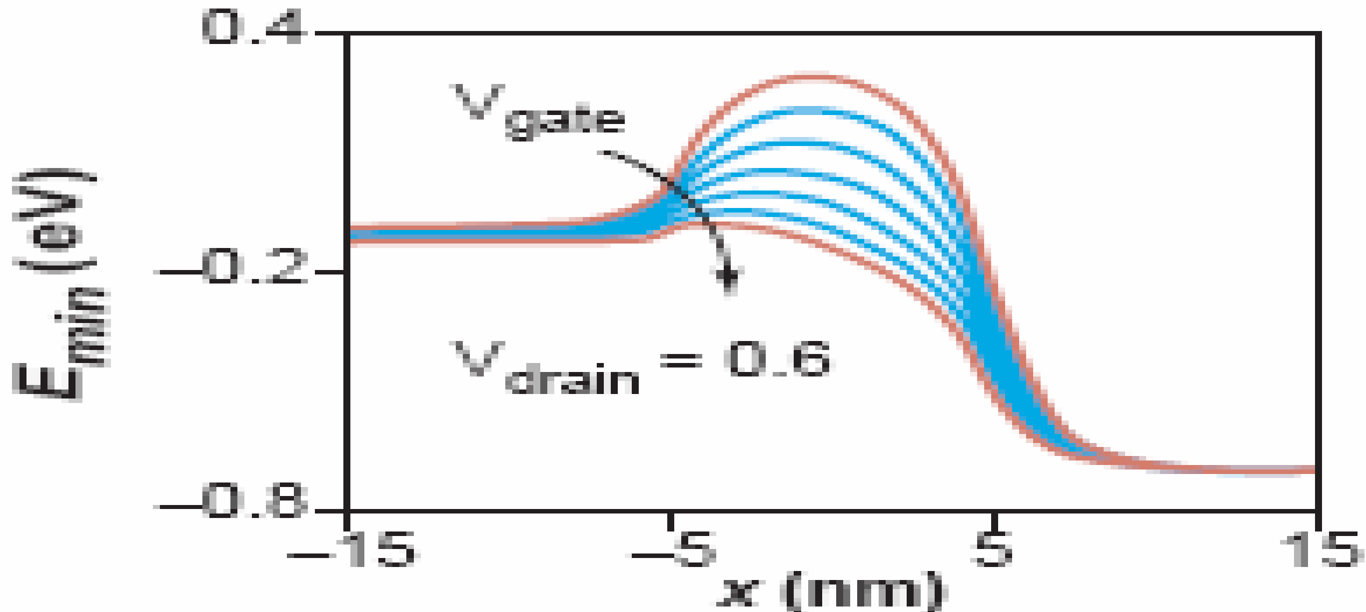
1.1 ITRS, 2001

The International Technology Roadmap for Semiconductors (ITRS)

This roadmap is generated by a global group of experts and represents their consensus. Although it notes that within the next 10 years "most of the known technological capabilities will approach or have reached their limits"



Moore´s Law Forever? M. Lundsrom, app. Phy. 2003

A few years ago, as critical dimensions approached 100 nm, a number of formidable challenges arose, ON- OFF conditions for digital applications

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Why the Devices are scaled down?

Scaling down to improve IC Performance

Scaling limits of MOSFET devices can be investigated using various criteria, including:

1- Turn-off characteristics (i.e., subthreshold swing requirements),

2- Threshold voltage roll-off requirements,

3- Process tolerance requirements,

4- Application (system-level) requirements, and

5- Source-to-drain tunneling limits.

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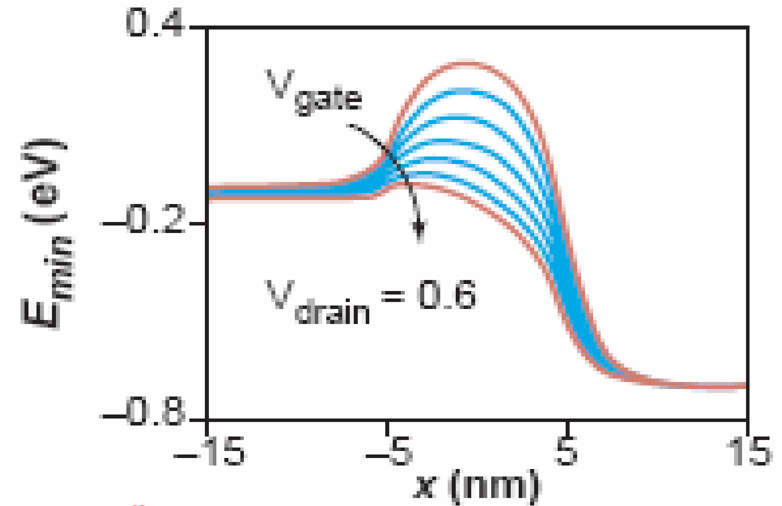
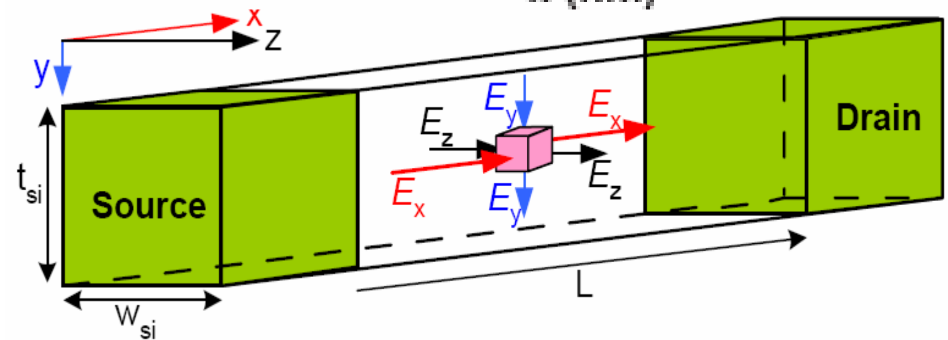
1.2 Short Channel Effects (SCEs)

- Threshold Voltage Roll-off
- Drain Induced Barrier Lowering, **DIBL**
- Subthreshold Swing, **S**



Keeping SCEs under control,
Prof. Jean-Pierre Colinge,
Tyndall National Institute, Ireland



$$Electrostatic\ Control \propto \sqrt{\frac{n\varepsilon_{ox}}{\varepsilon_{si}}\frac{1}{t_{si}t_{ox}}}$$

n=number of gates; t_{si} is assumed equal to W_{si}

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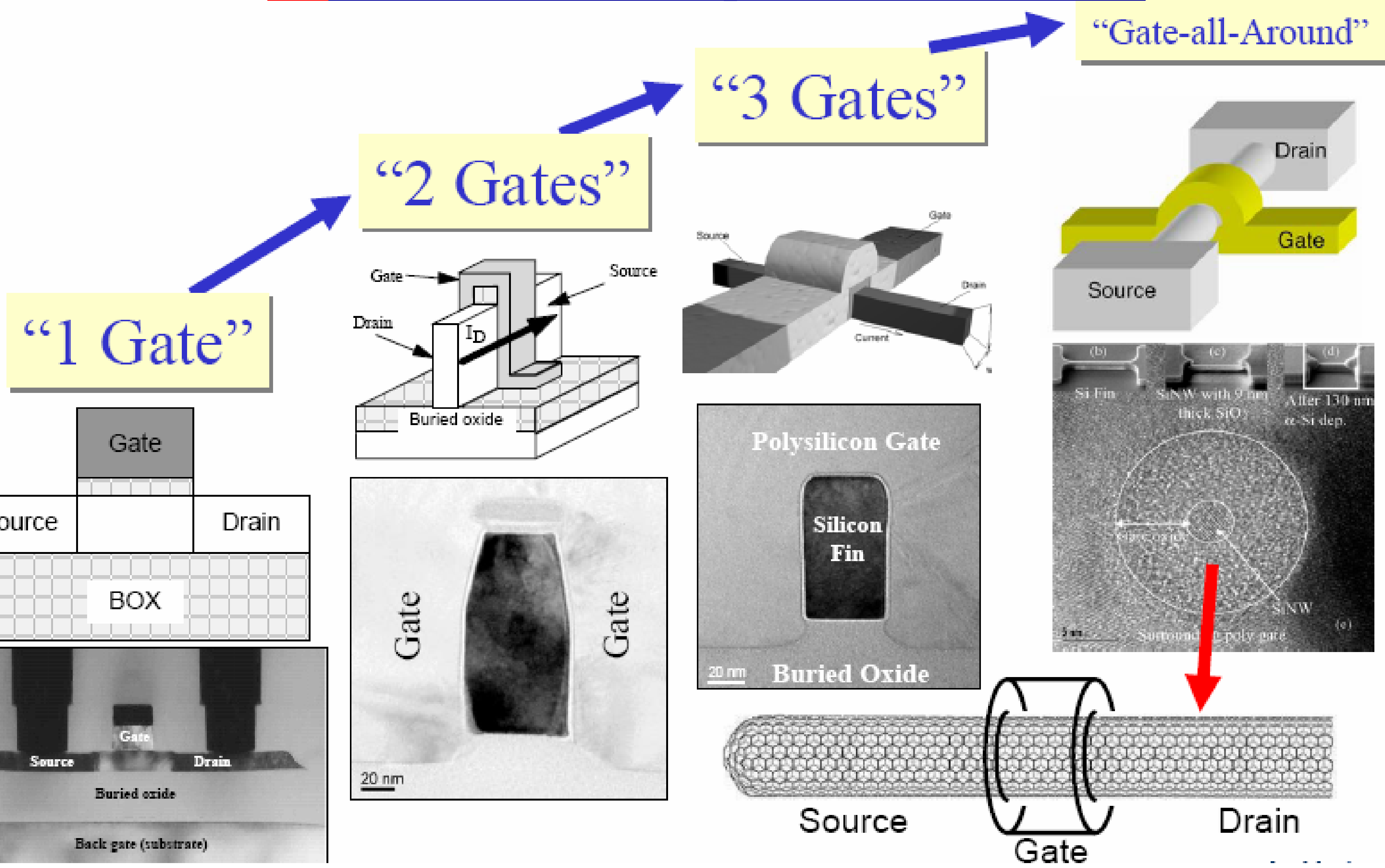
1.3 Evolution of Multiple Gate Transistors



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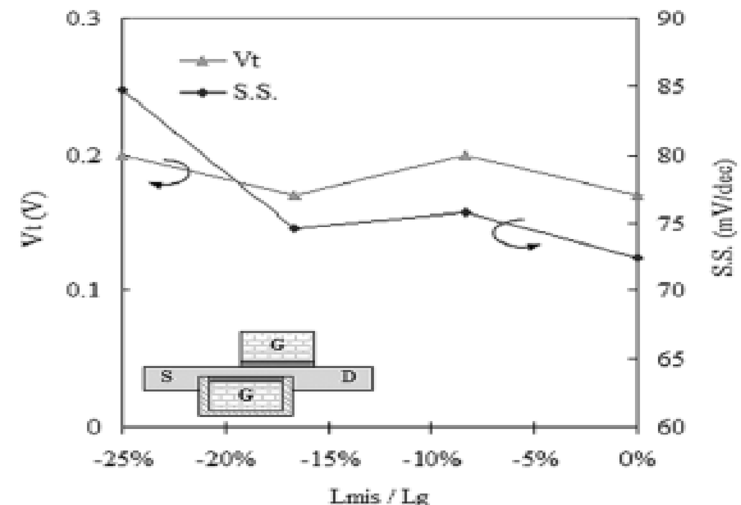
1.4 Fabricating challenges

Anyway, multiple gate structures present some difficulties in fabrication.

In double-gate MOSFETs,

The alignment of the top and the bottom gates to each other and to source/drain doping is critical for the device performance; misalignment can cause an additional overlap capacitance between gate and source or drain, as well as an additional series resistance.

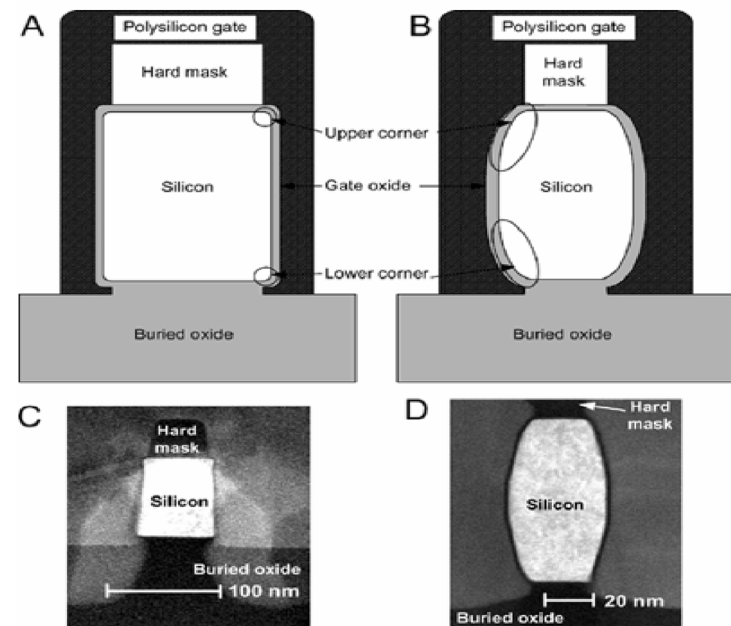
Yin, IEEE EDL, VOL. 24, NO. 10, Oct. 2003



In triple-gate structures

An inversion channel forms not only at the planar sides of the device, but also in the corners where two such sides meet. It can be avoided by reducing channel doping or by rounding the corners of the fins

Xiong et al, ¨, IEEE EDL, VOL. 25, NO. 8, Aug. 2004



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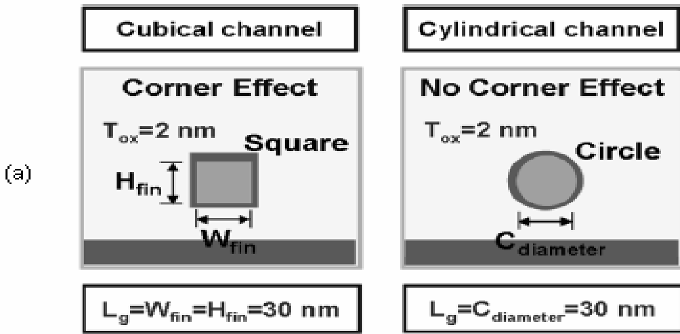
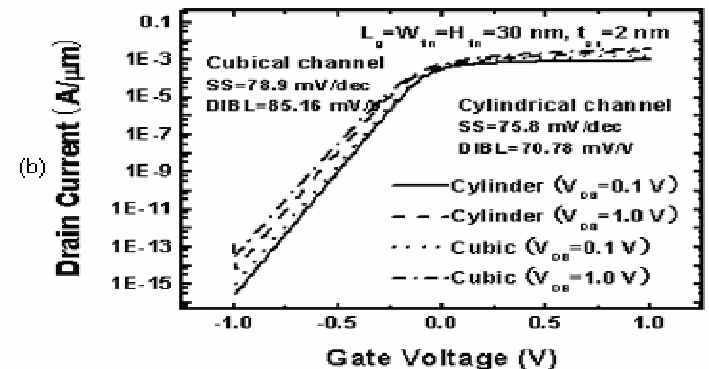
In surrounding gate MOSFETs,

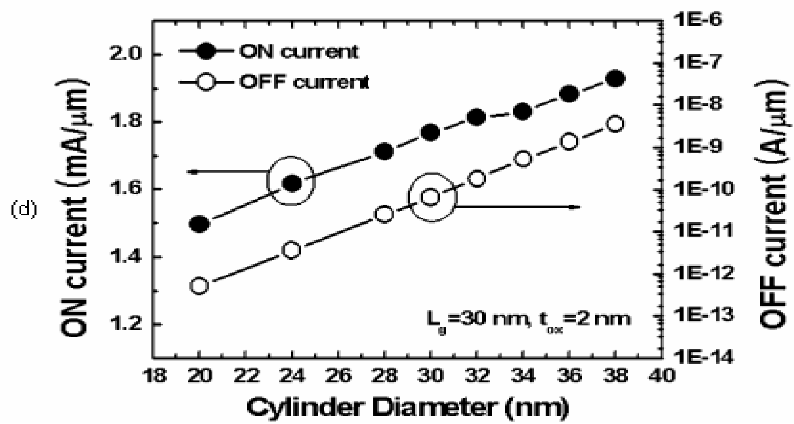
SS as well as DIBL in the ideal cylindrical-channel MOSFETs were smaller than those in cubical-channel MOSFETs with corner effects.





(c)

	Cubical Channel	Cylindrical Channel
V_{TH}	-0.1714 V	-0.1869 V
SS	78.9 mV/dec	75.8 mV/dec
DIBL	85.16 mV/V	70.78 mV/V
I_{ON}	3.56 mA/μm	2.53 mA/μm
I_{OFF}	339 pA/μm	62.1 pA/μm



Song et al, IEEE TRANSACTIONS ON NANOTECHNOLOGY, VOL. 5, NO. 3, MAY 2006

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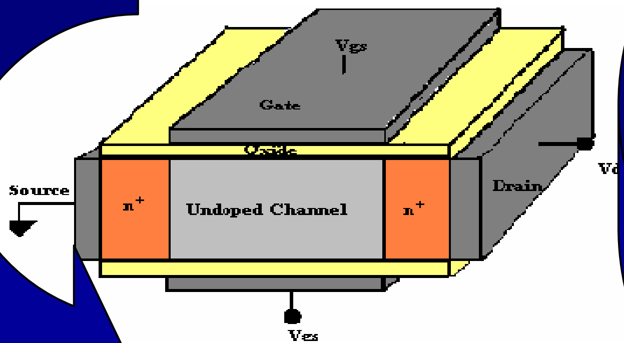
1.5 Modeling challenges

These devices need to be modeled to understand and predict the functionality of the circuits.

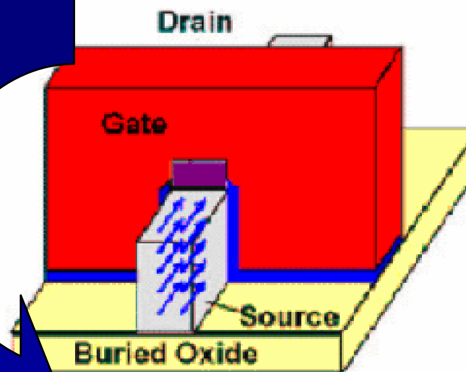
Three Multiple Gates MOS devices have been studied through this work

DG MOS



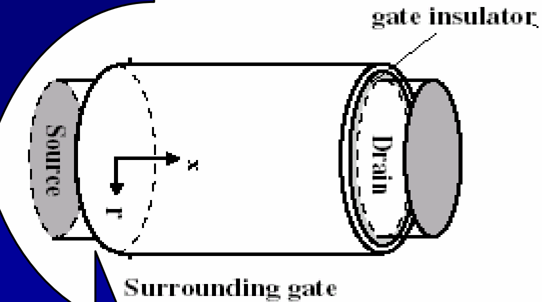
2D

FinFET



3D

GAA MOS



3D

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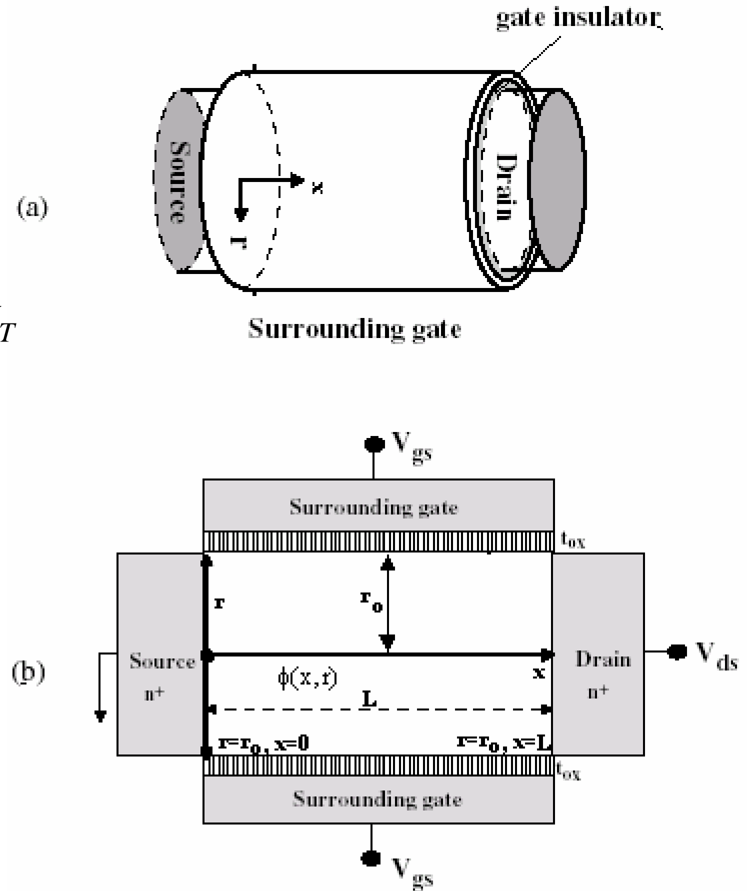
2A.1 A 2D SCEs Models for the undoped GAA MOSFET

(at low drain-source voltage)

2A.1.1 Potential Model Derivation

2-D Poisson Equation solving in cylindrical coordinates

$$\nabla^2 \phi(r,x) = \frac{q}{\varepsilon_{si}} n \quad \Rightarrow \quad n = n_i e^{(\phi-\phi_F)/V_T}$$



With the next boundary conditions

$$\phi(0,r) = V_{bi} \qquad \textbf{(at source end)}$$

$$\phi(L,r) = V_{bi} \qquad \textbf{(at drain end)}$$

and,

$$C_{ox}(V_{GS} - \phi_{MS} - \phi(x,r_0)) = \varepsilon_{Si} \left. \frac{\partial \phi(x,r)}{\partial r} \right|_{r=r_0}$$

V_{bi} is the built-in potential between source/drain end and channel

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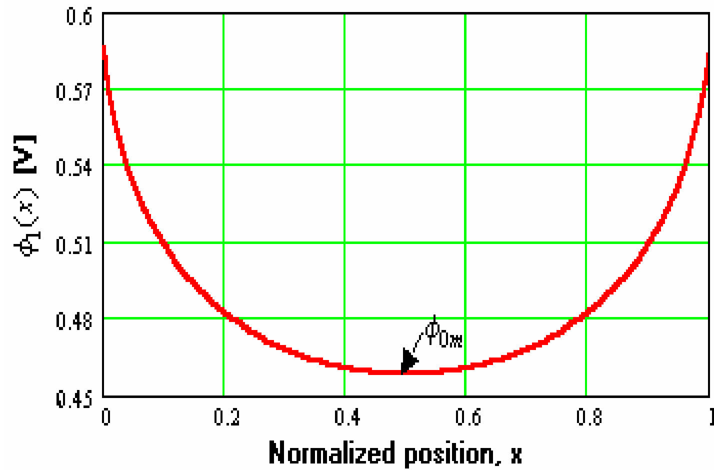
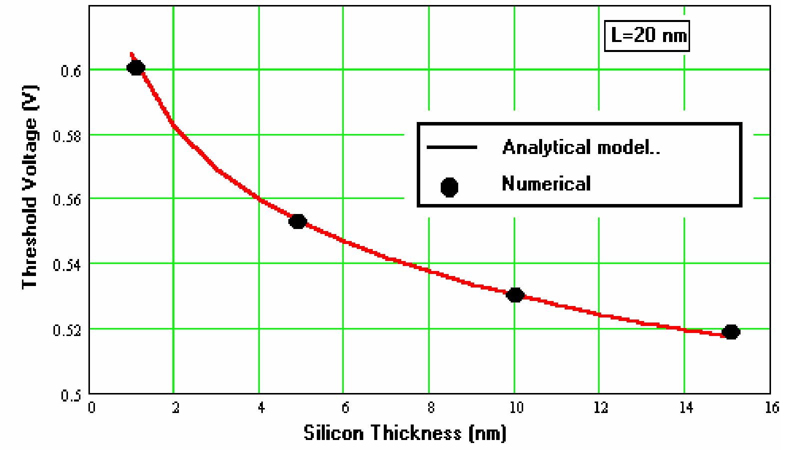
2A.1.2 Inversion charge and Threshold Volatge





(a)

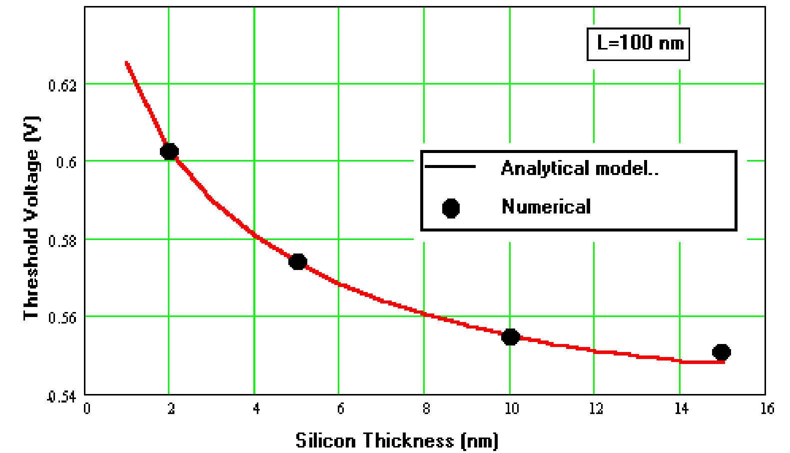
$$Q_{inv} = \int_{-t_{Si}/2}^{t_{Si}/2} n_i e^{\phi_{min}/V_T} dr = 2\int_{0}^{t_{Si}/2} n_i e^{\phi_{min}/V_T} dr$$

$$Q_{inv} \approx n_i \cdot t_{si} \cdot e^{\left[\phi_{om}+\Lambda\cdot\left(V_{GS}-\phi_{ms}-\phi_{om}\right)\cdot I_0(\eta)\right]/V_T}$$

At $Q_{inv} = Q_{TH}$

$Q_{TH} \sim 10^{12} cm^{-2}$

$$V_{TH} = \phi_{ms} + \phi_{om} + \left(V_T \ln\left(\frac{Q_{TH}}{n_i \cdot t_{si}}\right) - \phi_{om}\right) / \left[\Lambda \cdot I_0(\eta)\right]$$



(b)

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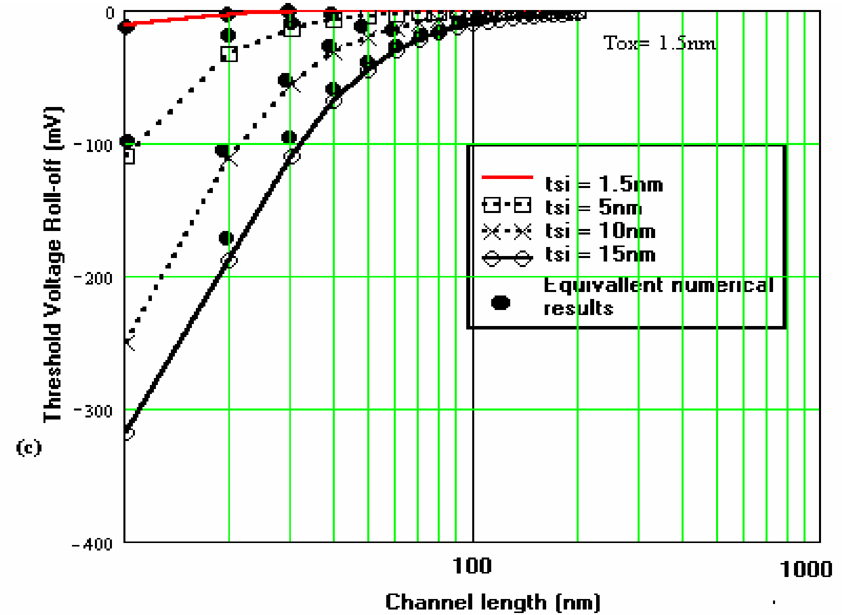
SCEs for the undoped GAA MOSFET

2A.1.3 Threshold voltage roll-off

$$\Delta V_{TH} = \left(V_T \ln\left(\frac{Q_{TH}}{n_i \cdot t_{si}}\right) - \phi_{om} \right) \cdot \frac{(1-1.25/\Lambda)}{I_0(\eta)}$$

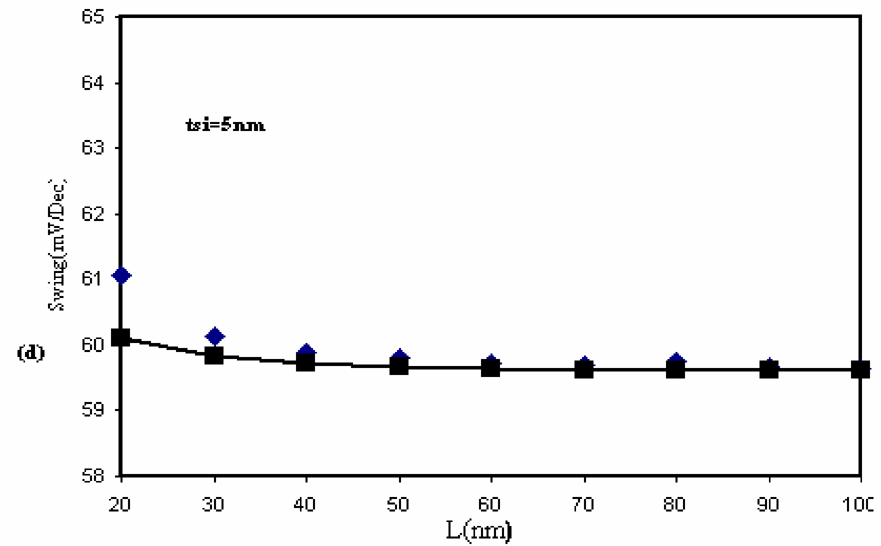


2A.1.4 Subthreshold swing

$$I_D \;\alpha \int_0^{t_{si}/2} n_i e^{(\phi_{min} - \phi_F)/V_T} dr$$

$$S = \frac{\partial V_{GS}}{\partial \log I_D} = \left[\frac{\int_{r=0}^{r_o} n_m(r) \frac{\partial \phi_{min}}{\partial V_{GS}} dr}{\int_{r=0}^{r_o} n_m(r) dr} \right]^{-1} V_T \ln(10)$$

$$S = \frac{2\frac{C_{Si}}{C_{ox}}\eta \cdot I_1(\eta) + I_0(\eta)}{I_0(\eta)\cos(\pi - 2x_m B)}$$



Hamdy et al, ,Solid-State Electronics, vol. 50, no. 5, May 2006

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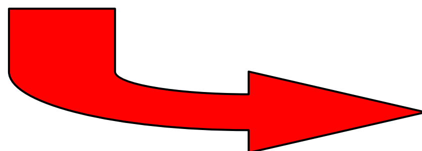
2A.2 SCEs for the undoped GAA MOSFET

[including DIBL]

2-D Poisson Equation solving in cylindrical coordinates

$$\nabla^2 \phi(r, x) = \frac{q}{\varepsilon_{si}} n$$

$$n = n_i e^{(\phi - \phi_F)/V_T}$$



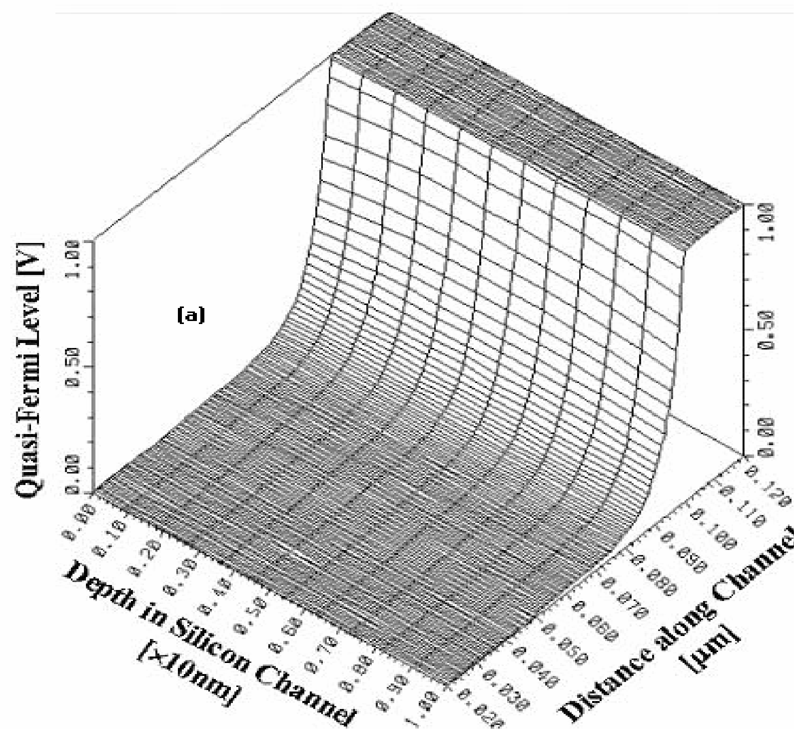
$$\phi_F(0, y) = 0$$

$$\phi_F(L, y) = V_{DS}$$

$$C_{ox}(V_{GS} - \phi_{MS} - \phi(x, r = t_0)) = \varepsilon_{Si} \left. \frac{\partial \phi(x, y)}{\partial y} \right|_{r = tsi/2}$$

$$\phi(0, y) = V_{bi}$$

$$\phi(L, y) = V_{bi} + V_{DS}$$



Vds=1V, Vgs=0.37V Undoped DG MOSFET device
Chen et., al., IEEE TED, VOL. 50, NO. 7, JULY 2003

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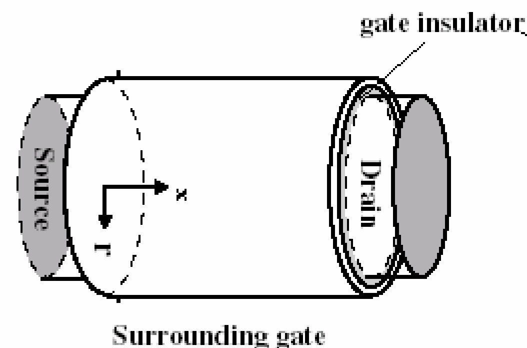
2A.2.1 Potential Model Deriviation

Divide Poisson Equation solution into two components as,

$$\phi(x,r) = \phi_0(r) + \phi_1(x,r)$$



$\phi_o(r)$, which is the solution of the 1D Poisson´s equation in the radial direction,

$\phi_1(x,r)$, which is the solution of the remnant 2D differential equation

$$\nabla^2 \phi_0(r) = \frac{q}{\varepsilon_{si}} n \qquad \text{(1-D Poisson Equation)}$$

$$\frac{1}{r}\frac{\partial}{\partial r} r \frac{\partial}{\partial r}\phi_1(x,r) + \frac{\partial^2}{\partial x^2}\phi_1(x,r) = 0 \qquad \text{(2-D Poisson Equation)}$$

Using the variable separation method to solve the 2-D part

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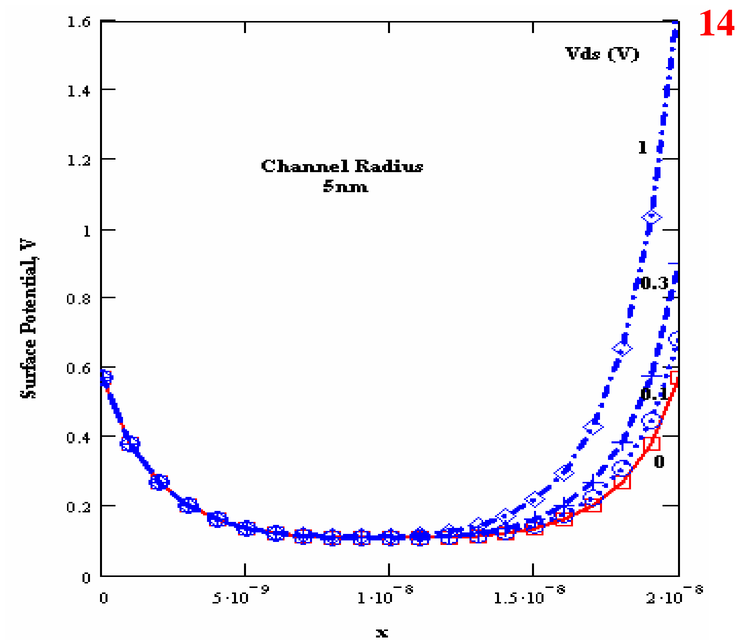
SCEs for the undoped GAA MOSFET including DIBL

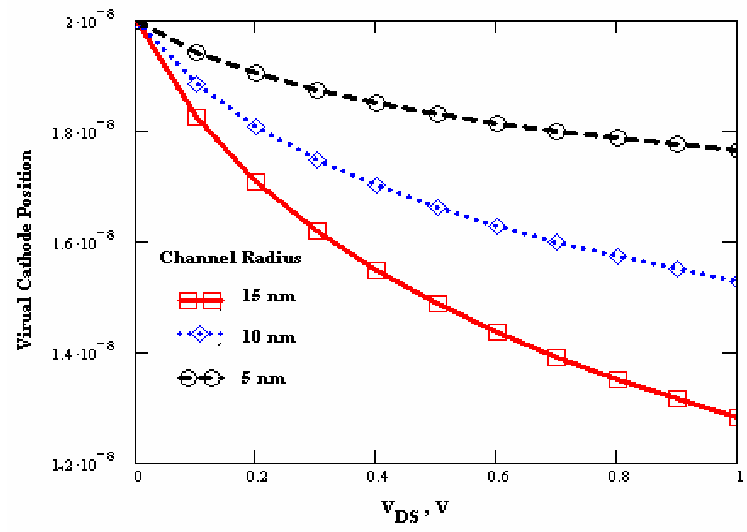
Good agreement has been obtained with 3-D numerical simulation for different V_{ds} values



Virtual Cathode (Value and position)

$$\left.\frac{\partial \phi_1(x,r)}{\partial x}\right|_{x_{min}} = 0$$

$$x_{\min} = \frac{L}{2} - \frac{r_0}{2\cdot\lambda}\cdot\ln\left[\frac{S_1\cdot\left[V_{bi}\cdot\left(1-e^{-L\frac{\lambda}{R_0}}\right)+V_{ds}\right]-\left(1-e^{-L\frac{\lambda}{R_0}}\right)\cdot V_A}{S_1\cdot\left[V_{bi}\cdot\left(1-e^{-L\frac{\lambda}{R_0}}\right)-V_{ds}\cdot e^{-L\frac{\lambda}{R_0}}\right]-\left(1-e^{-L\frac{\lambda}{R_0}}\right)\cdot V_A}\right]$$



Hamdy et al, IEEE TED,Vol. 54, No.3, March 2007

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SCEs for the undoped GAA MOSFET including DIBL

2A.2.2 Inversion charge

$$Q_{inv} = 2\int_0^{r_0} n_i e^{\phi[x_{\min},r]/V_T}\,dr$$

2A.2.3 Threshold Voltage model,

$$V_{TH} = \phi_{ms} + \frac{1}{1-S_{gs}}\cdot\left(V_T \ln\left(\frac{Q_{TH}}{2n_i\cdot r_o}\right) - S_{ds}\right)$$

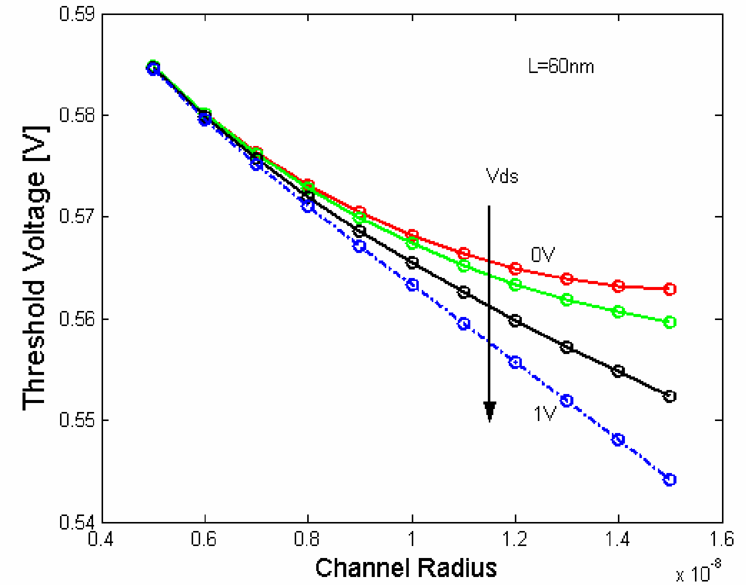
2A.2.4 For Long Channel device,

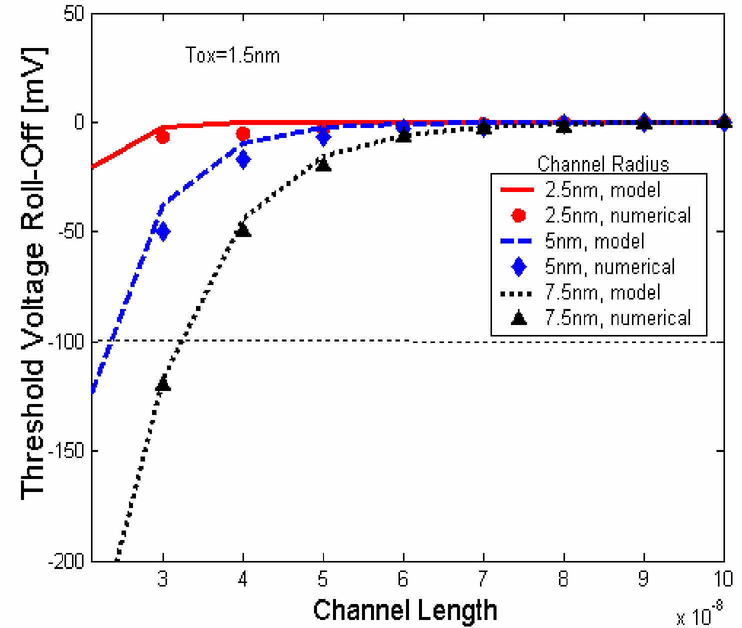
$$V_{TH} = \phi_{ms} + \left(V_T \ln\left(\frac{Q_{TH}}{2n_i\cdot r_o}\right)\right)$$

2A.2.5 Threshold Voltage Roll-off

$$\Delta V_{TH} = V_T \ln\left(\frac{Q_{TH}}{2n_i\cdot r_o}\right)\left[\frac{1}{1-S_{gs}} - 1\right] - S_{ds}$$

Hamdy et al, IEEE TED, Vol. 54, No.3, March 2007





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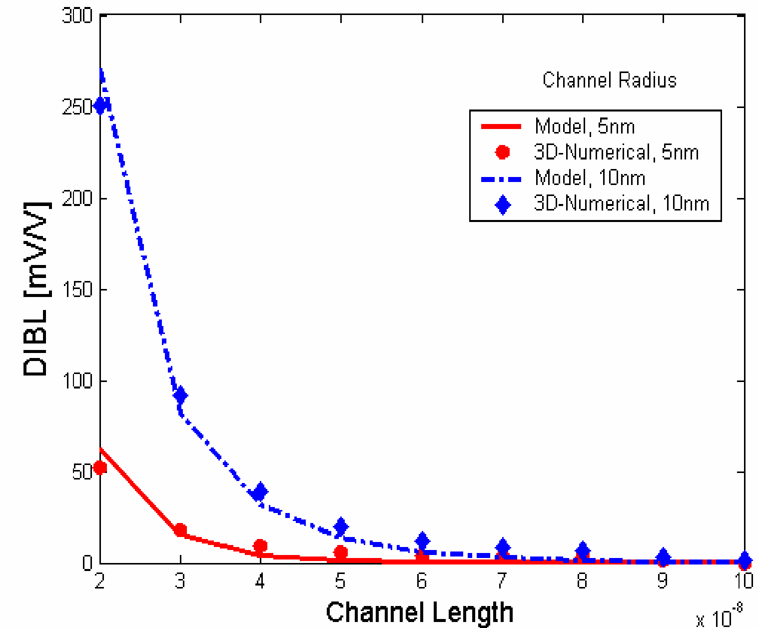
SCEs for the undoped GAA MOSFET including DIBL

2A.2.6 DIBL Calculations

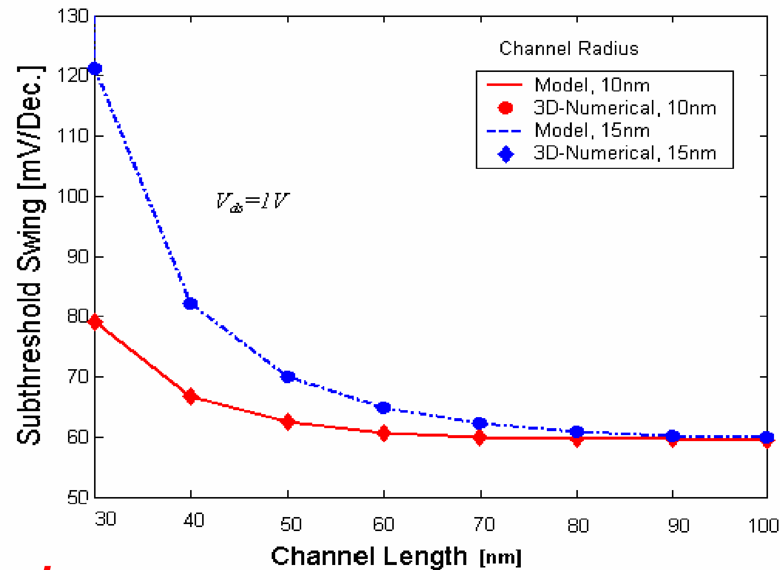
[V_{TH} (At high V_{ds})-V_{TH} (At low V_{ds})]

$$DIBL = V_T \ln\left(\frac{Q_{TH}}{2n_i \cdot r_o}\right)\left[\frac{1}{1-S_{gso}} - \frac{1}{1-S_{gs}}\right] - \left[\frac{S_{dso}}{1-S_{gso}} - \frac{S_{ds}}{1-S_{gso}}\right]$$



2A.2.7 Subthreshold Swing

$$S = \frac{\partial V_{GS}}{\partial \log I_D} = \left[\frac{\int_{r=0}^{r_o} n_m(r) \frac{\partial \phi_{min}}{\partial V_{GS}} dr}{\int_{r=0}^{r_o} n_m(r) dr}\right]^{-1} V_T \ln(10)$$



At $r = r_c = T_{si}/4$

$$Swing = \frac{V_T}{1 - S_{gs}} \cdot \ln(10)$$

Hamdy et al, IEEE TED, Vol. 54, No.3, March 2007

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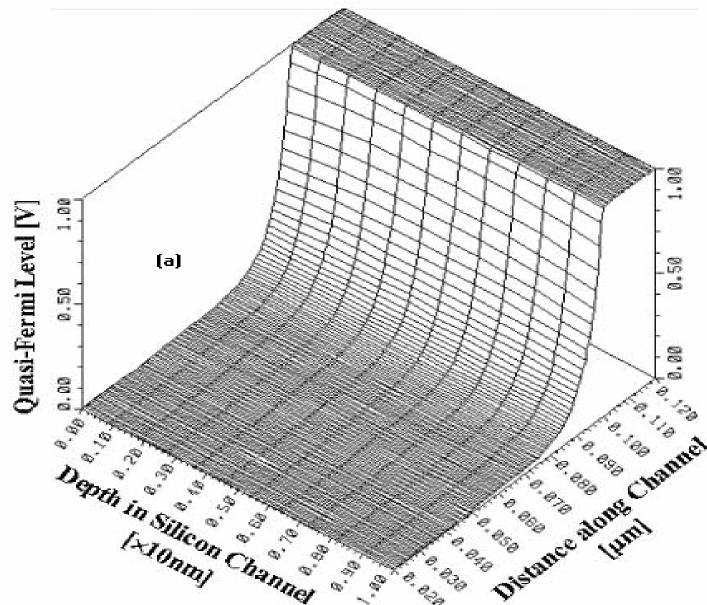
2B. SCEs for the undoped DG MOSFET

2B.1 Potential Model Derivation

$$\nabla^2 \phi(x,y) = \frac{q}{\varepsilon_{si}} n$$

$$n = n_i e^{(\phi - \phi_F)/V_T}$$



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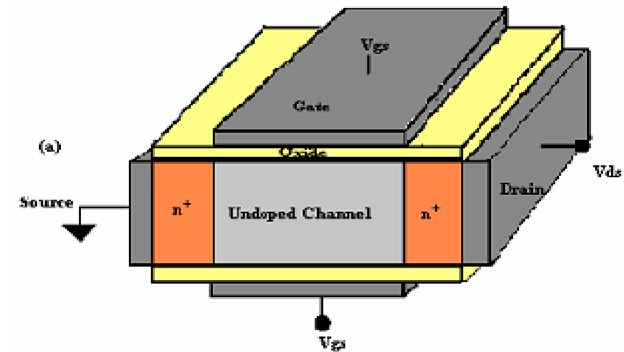

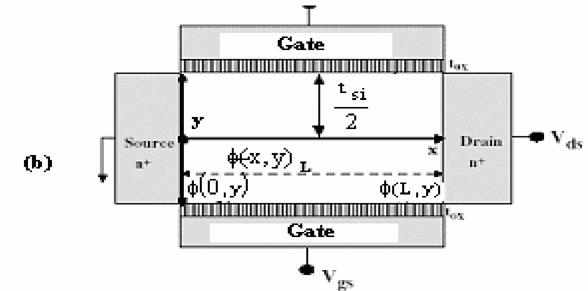

$$\phi_F(0,y) = 0$$

$$\phi_F(L,y) = V_{DS}$$

$$C_{ox}(V_{GS} - \phi_{MS} - \phi(x, y = t_0)) = \varepsilon_{Si} \left. \frac{\partial \phi(x,y)}{\partial y} \right|_{y=tsi/2}$$

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SCEs for the undoped DG MOSFET

$$\phi(x,y)=\phi_{1D}(y)+\phi_{2D}(x,y)$$

$$\phi_{1D}(y)=V_T\cdot\ln\left[\frac{B_n^{\ 2}}{2\cdot\delta}\sec^2(B_n\cdot y)\right]$$

$$\phi_{2D}(x,y)=\left[C_0\cdot e^{\lambda\frac{x-L}{t_0}}+C_1\cdot e^{-\lambda\frac{x}{t_0}}\right]\cdot\cos(\lambda\cdot y)$$

$$\delta=\frac{q}{\varepsilon_{si}\cdot V_T}n_i\cdot t_0^{\ 2}$$

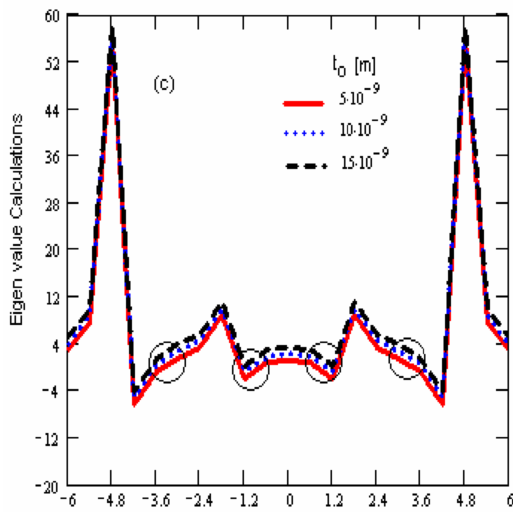
$$C_r=\frac{\varepsilon_{ox}\cdot t_o}{t_{ox}\cdot\varepsilon_{si}}$$

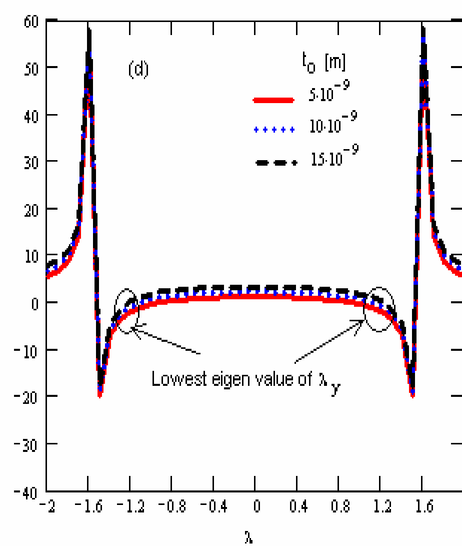
$$C_0=S_1\cdot\left[V_{DS}+V_{bi}\cdot\left(1-e^{-L\frac{\lambda}{t_o}}\right)\right]-S_2\cdot\phi_{so}$$

$$C_1=S_1\cdot\left[V_{bi}\cdot\left(1-e^{-L\frac{\lambda}{t_o}}\right)-V_{DS}\cdot e^{-L\frac{\lambda}{t_o}}\right]-S_2\cdot\phi_{so}$$

$$S_1=\frac{4\cdot\sin(\lambda)}{[2\cdot\lambda+\sin(2\cdot\lambda)]\cdot\left[1-e^{-2L\frac{\lambda}{t_o}}\right]}$$

$$S_2=\frac{4\cdot\lambda\cdot\cos\left(\frac{\lambda}{2}\right)\cdot\left[1-e^{-L\frac{\lambda}{t_o}}\right]}{[2\cdot\lambda+\sin(2\cdot\lambda)]\cdot\left[1-e^{-2L\frac{\lambda}{t_o}}\right]}$$





$$2\cdot\lambda\tan(\lambda)=C_r$$

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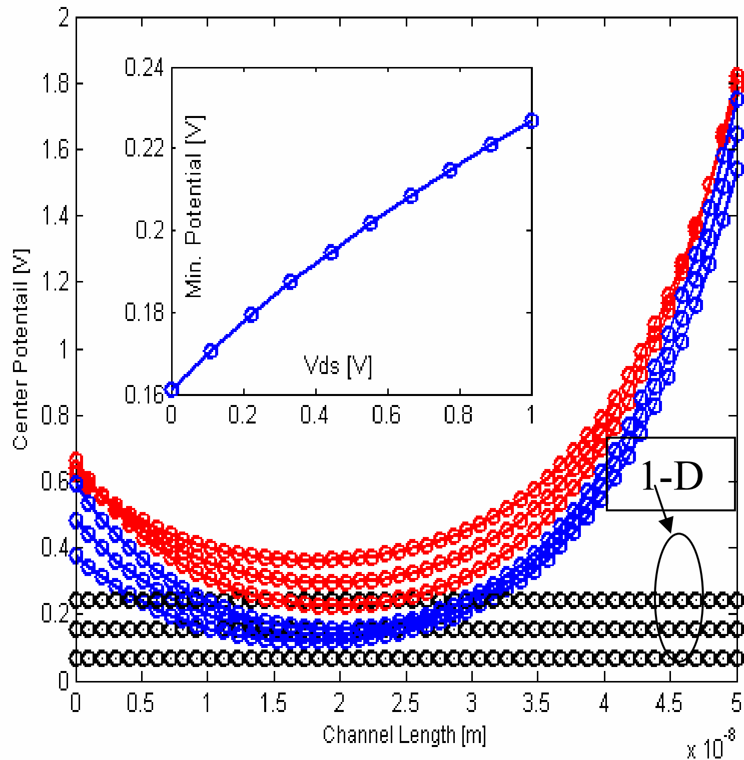
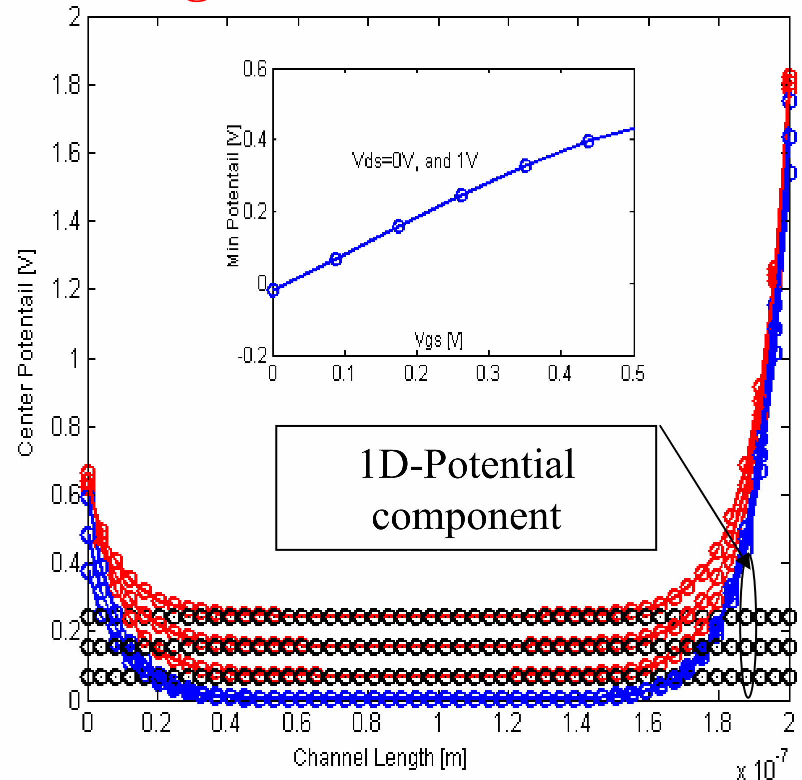
2B.2 Potential Model Testing

Short Channel DG MOSFET



Long Channel DG MOSFET



The Channel electrostatics is governed by 2D Potential

The Channel electrostatics is governed only by 1D Component

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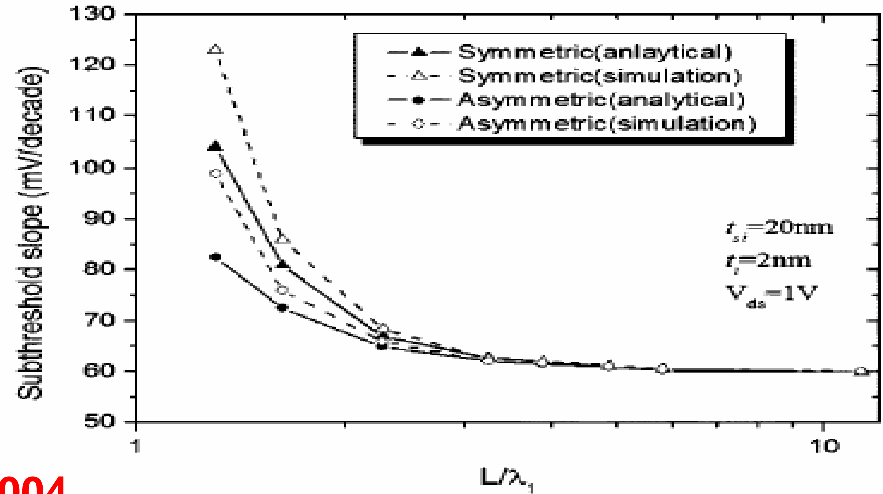
SCEs for the undoped DG MOSFET

2B.3 Subthreshold Swing

$$I_{ds} = \frac{\mu W (KT/q)\left[1-\exp\left(-qV_{ds}/KT\right)\right]}{\int_0^L \frac{dy}{\int_{-tsi/2}^{tsi/2} n_i e^{q\phi(x,y)/KT} dx}}$$

$$S \approx 2.3 V_T \left[\frac{\partial \phi_{min}}{\partial V_{gs}}\right]^{-1} \cdot \ln(10)$$

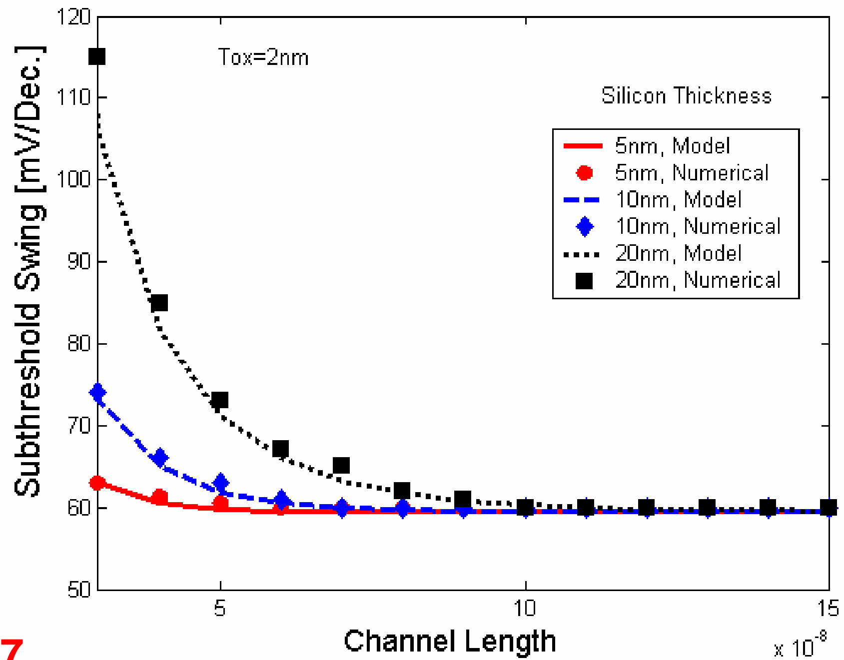


Liang and Taur, IEEE TED, vol. 51,Sep. 2004.

$$I_D \;\alpha \int_0^{t_{si}/2} n_i e^{(\phi_{min} - \phi_F)/V_T} dy$$

$$Swing = \frac{V_t}{1 - S_{gs}} \cdot \ln(10)$$

$$S_{gs} = 2 \cdot S_2 \cdot \cos\left(\frac{\lambda}{2}\right) \cdot e^{-\frac{L}{2}\frac{\lambda}{t_0}} \cdot \cosh\left[\left(x_{min} - \frac{L}{2}\right)\frac{\lambda}{t_0}\right]$$



Hamdy et al, IEEE TED, vol. 50, June 2007.

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SCEs for the undoped DG MOSFET

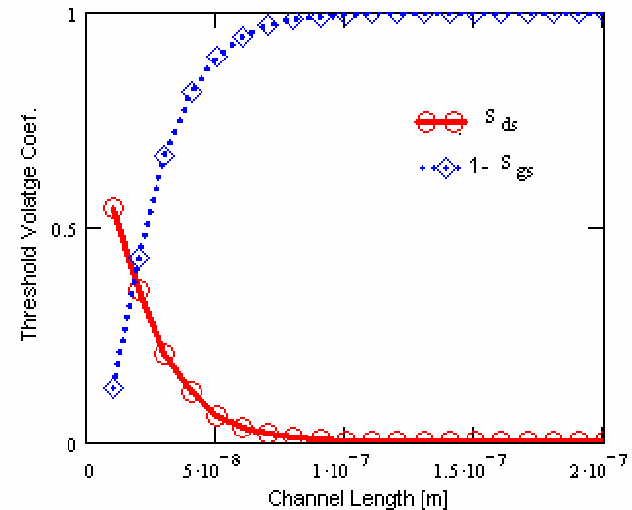
2B.4 Threshold Voltage Model

The inversion charge can found from

$$Q_{inv} = 2\int_0^{t_0} n_i e^{\phi[x_{min},y]/V_T}\,dy$$

After some mathematical manipulations

$$V_{TH} = \phi_{ms} + \frac{1}{1-S_{gs}} \cdot \left(V_T \ln\left(\frac{Q_{TH}}{2n_i \cdot t_o}\right) - S_{ds} \right)$$



S_{ds}: *is the effect of the drain-source voltage*

For Long Channel DG MOSFET

$$V_{TH} = \phi_{ms} + V_T \ln\left(\frac{Q_{TH}}{2n_i \cdot t_o}\right)$$

$Q_{TH} \sim 10^{10} cm^{-2}$

Chen Model, in IEEE TED VOL. 50, NO. 7, JULY 2003, does not include the effect of V_{ds}

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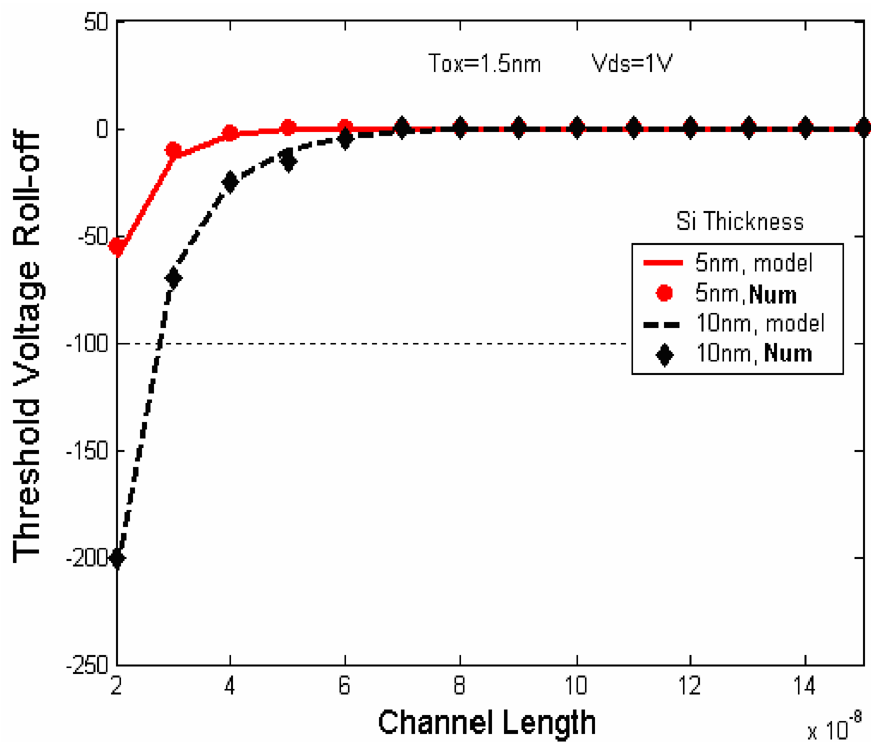
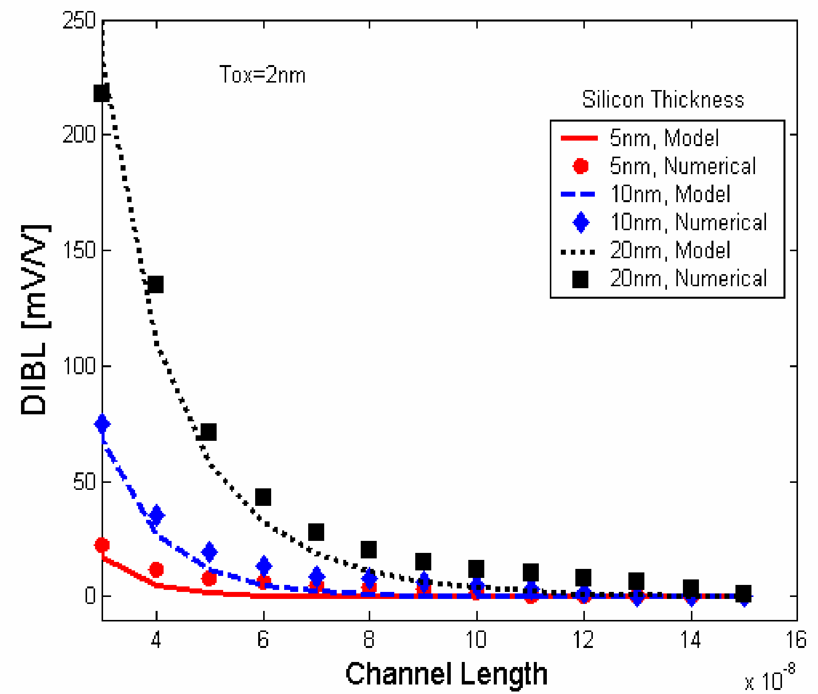
2B.5 Threshold Voltage Roll-off, and DIBL Models

$$\Delta V_{TH} = V_T \ln\left(\frac{Q_{TH}}{2n_i \cdot t_o}\right)\left[1 - \frac{1}{1 - S_{gs}}\right] - S_{ds}$$

$$DIBL = \left\{V_T \ln\left(\frac{Q_{TH}}{2n_i \cdot t_o}\right)\left[\frac{1}{1-S_{gso}} - \frac{1}{1-S_{gs}}\right] - \left[\frac{S_{dso}}{1-S_{gso}} - \frac{S_{ds}}{1-S_{gso}}\right]\right\}$$





Hamdy et al, IEEE TED VOL. 50, June 2007

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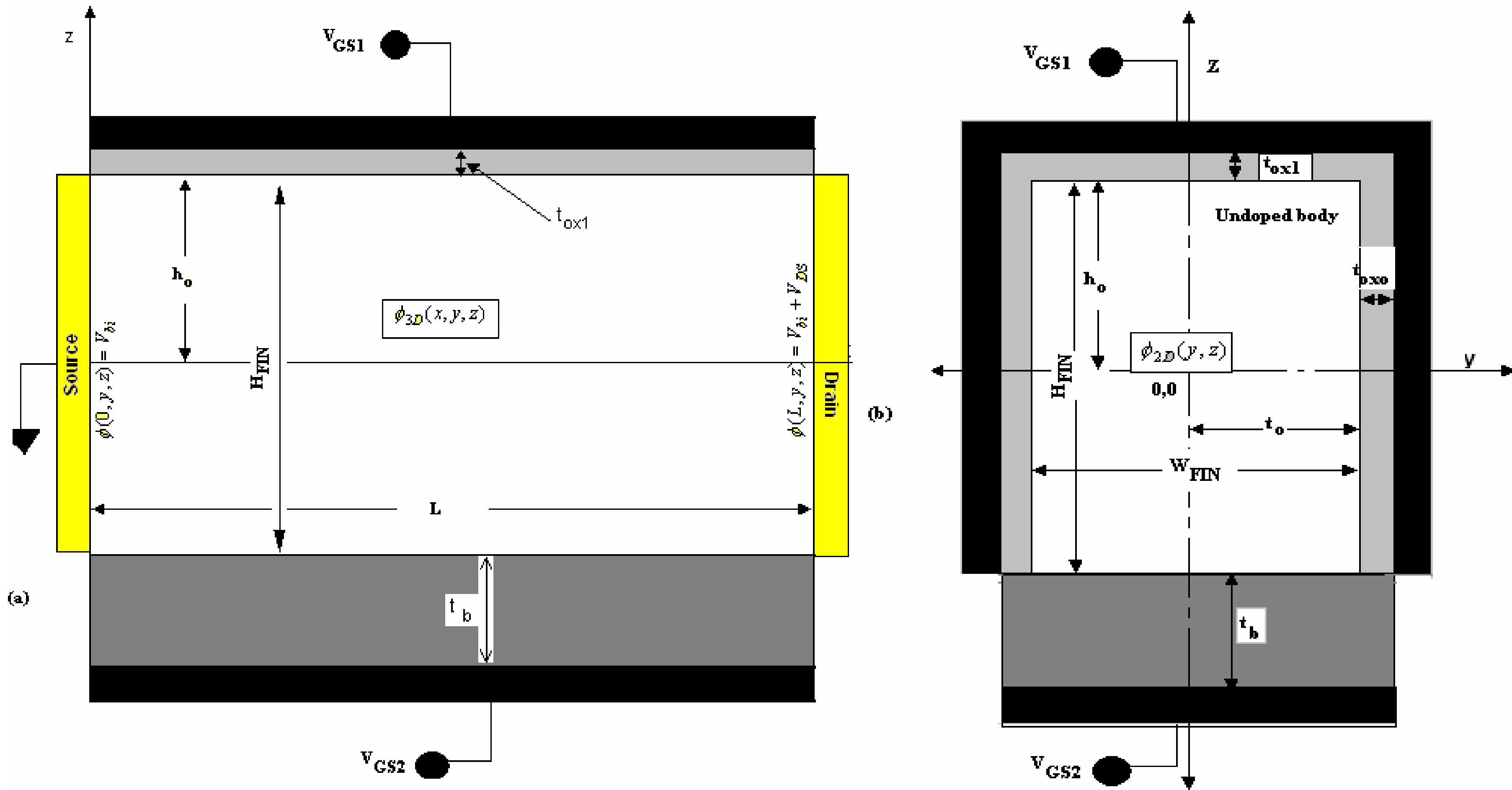
2C. SCEs for the undoped FinFET



$$\frac{\partial^2\phi(x,y,z)}{\partial x^2} + \frac{\partial^2\phi(x,y,z)}{\partial y^2} + \frac{\partial^2\phi(x,y,z)}{\partial z^2} = \frac{q}{\varepsilon_{si}} n(x,y,z)$$

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2C.1 Potential Model Derivation

Boundary condition of right gate

$$C_{oxo}\cdot\left[V_{GS1}-\phi_{ms}-\phi(x,y=t_0,z)\right]=-\varepsilon_{Si}\left.\frac{\partial\phi(x,y,z)}{\partial y}\right|_{y=t_0}$$

Boundary condition of left gate

$$C_{oxo}\cdot\left[V_{GS1}-\phi_{ms}-\phi(x,y=-t_0,z)\right]=\varepsilon_{Si}\left.\frac{\partial\phi(x,y,z)}{\partial y}\right|_{y=-t_0}$$

Boundary condition of top gate

$$C_{ox1}\cdot\left[V_{GS1}-\phi_{ms}-\phi(x,y,z=h_o)\right]=-\varepsilon_{Si}\left.\frac{\partial\phi(x,y,z)}{\partial z}\right|_{z=h_0}$$

Boundary condition of bottom gate

$$C_{ox2}\cdot\left[V_{GS2}-\phi_{ms}-\phi(x,y,z=-h_o)\right]=\varepsilon_{Si}\left.\frac{\partial\phi(x,y,z)}{\partial z}\right|_{z=-h_0}$$

Boundary condition at source end

$$\phi(0,y,z)=V_{bi}$$

Boundary condition at source end

$$\phi(L,y,z)=V_{bi}+V_{DS}$$

$$\phi(x,y,z)=\phi_{2D}(y,z)+\phi_{3D}(x,y,z)$$

$$\phi_{2D}(y,z)=\phi_{1D}(y)+\alpha_o(y)\cdot z+\alpha_1(y)\cdot z^2$$

[illegible]

$$\frac{\partial^2\phi_{3D}(x,y,z)}{\partial x^2}+\frac{\partial^2\phi_{3D}(x,y,z)}{\partial y^2}+\frac{\partial^2\phi_{3D}(x,y,z)}{\partial z^2}=0$$

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SCEs for the undoped FinFET

$$\frac{\partial^2 \phi_{3D}(x,y,z)}{\partial x^2} + \frac{\partial^2 \phi_{3D}(x,y,z)}{\partial y^2} + \frac{\partial^2 \phi_{3D}(x,y,z)}{\partial z^2} = 0$$

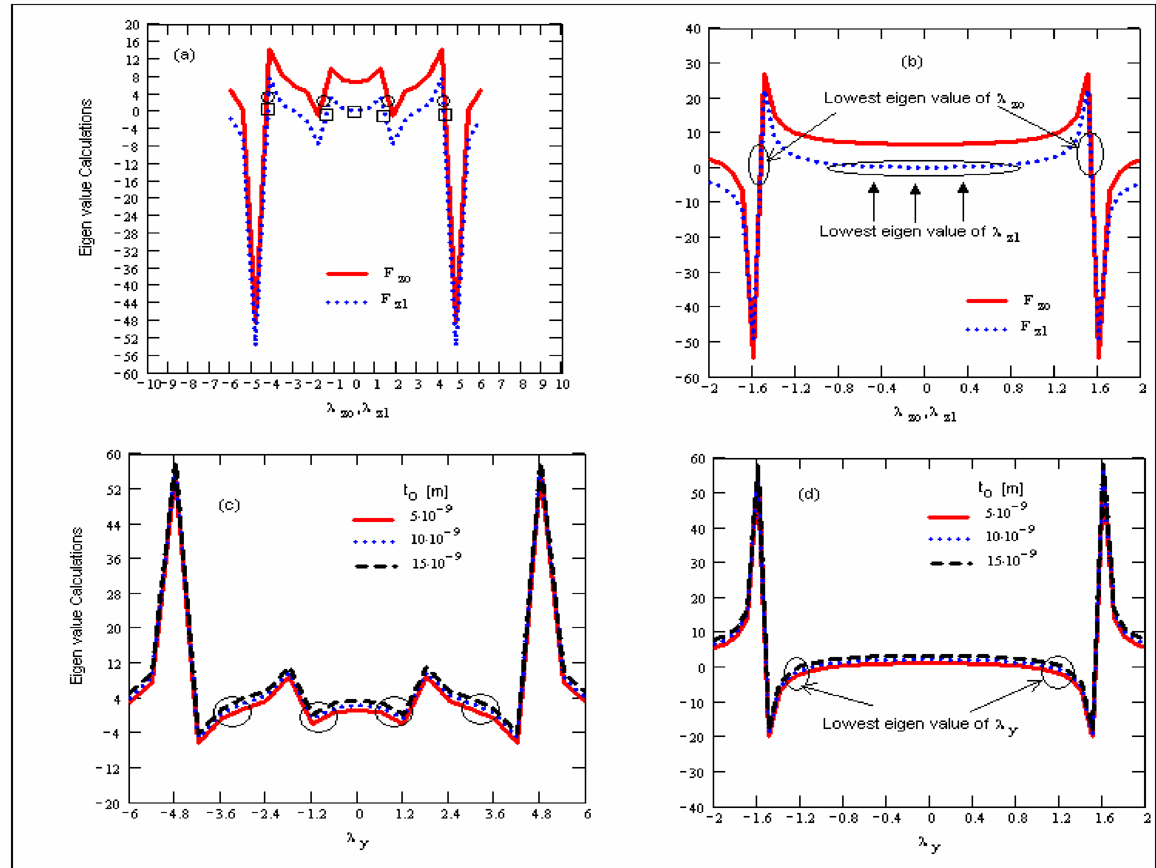
$$\phi_{3D}(x,y,z) = f(x)\cdot g(y)\cdot h(z)$$

$$\frac{f(x)''}{f(x)} + \frac{g(y)''}{g(y)} + \frac{h(z)''}{h(z)} = 0$$

$$\frac{g(y)''}{g(y)} + \gamma_y^{\ 2} = 0$$

$$\frac{h(z)''}{h(z)} + \gamma_z^{\ 2} = 0$$

$$\frac{f(x)''}{f(x)} - \lambda_x^{\ 2} = 0$$



To separate ϕ_{3D} component from the whole electrostatic potential equation we have assumed that, $\phi_{3D} < V_T$

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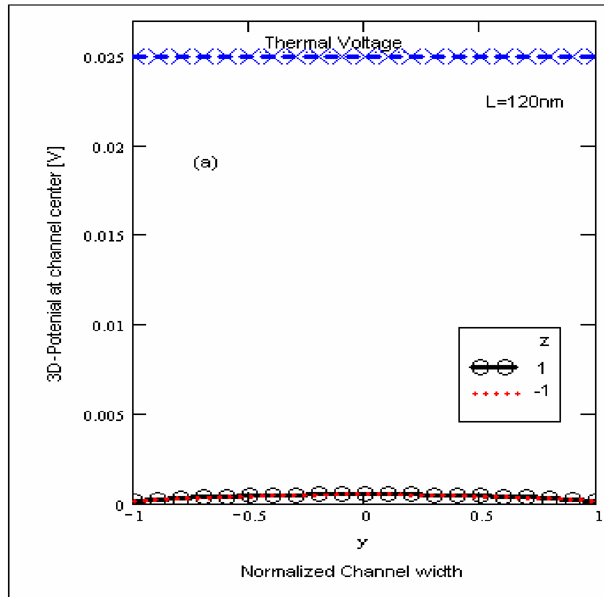
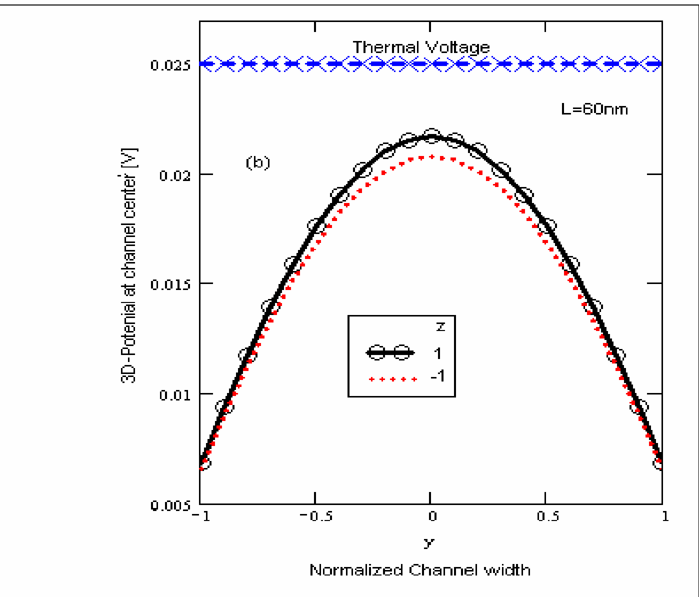
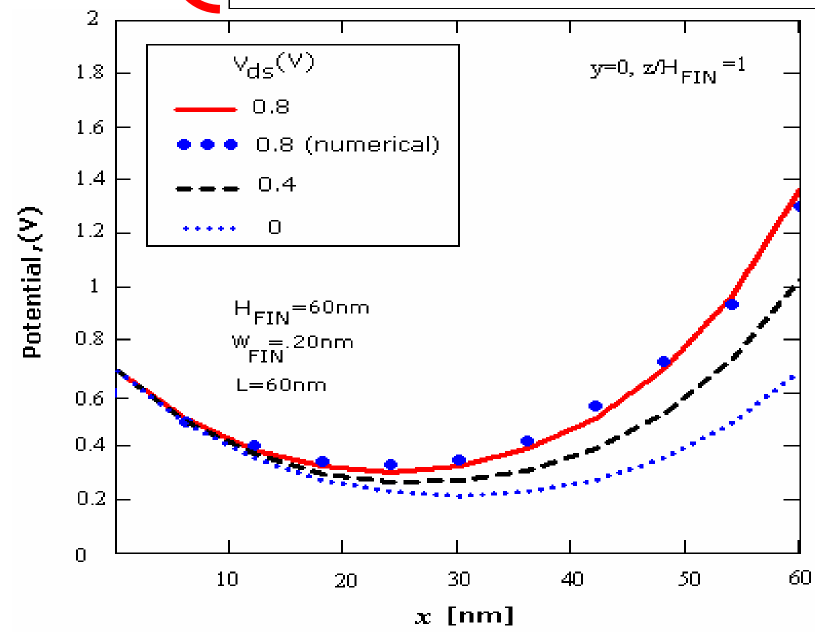
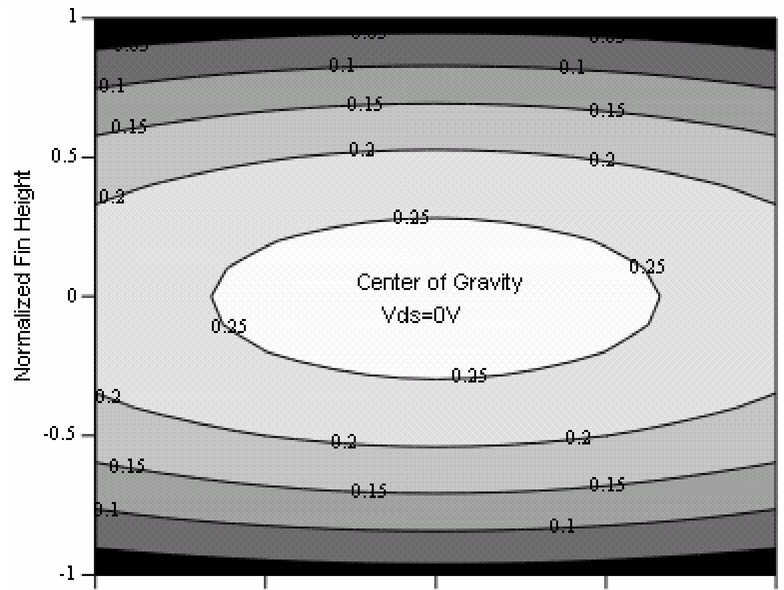
SCEs for the undoped FinFET

ϕ_{3D}<V_T validation









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2C.2 Subthreshold swing Model

$$S = \frac{\partial V_{GS}}{\partial \log I_D} = \left[\frac{2 \cdot \int_{z=-h_o}^{h_o} \int_{y=0}^{t_o} n_m(y,z) \frac{\partial \phi_{3D_min}(y,z)}{\partial V_{GS}} dydz}{2 \cdot \int_{z=-h_o}^{h_o} \int_{y=0}^{t_o} n_m(y,z) dydz} \right]^{-1} V_T \ln(10)$$

$$\Rightarrow \left. \frac{\partial \phi(x,y,z)}{\partial x} \right|_{x=x_{\min}} = 0$$

$$S = \left[1 - \sum_{\lambda_{zo,1}} K_1 \cdot \cos(\lambda_y \cdot y_c) \cdot \cos(\lambda_z \cdot z_c) + K_2 \cdot \cos(\lambda_y \cdot y_c) \cdot sin(\lambda_z \cdot z_c) \right]^{-1} \cdot V_t \cdot \ln(10)$$

Conduction paths exact Solution

$$1 - \cos(\lambda_y \cdot y_c) \cdot \cos(\lambda_z \cdot z_c) = \left[\frac{\int_{z=-h_o}^{h_o} \int_{y=0}^{t_o} n_m(y,z) \cdot \cos(\lambda_y \cdot y) \cdot \cos(\lambda_z \cdot z) dydz}{\int_{z=-h_o}^{h_o} \int_{y=0}^{t_o} n_m(y,z) dydz} \right]^{-1} V_T \ln(10)$$

$$\cos(\lambda_y \cdot y_c) \cdot sin(\lambda_z \cdot z_c) = \left[\frac{\int_{z=-h_o}^{h_o} \int_{y=0}^{t_o} n_m(y,z) \cdot \cos(\lambda_y \cdot y) \cdot sin(\lambda_z \cdot z) dydz}{\int_{z=-h_o}^{h_o} \int_{y=0}^{t_o} n_m(y,z) dydz} \right]^{-1} V_T \ln(10)$$

Hamdy et al, WCM, May 2007, USA

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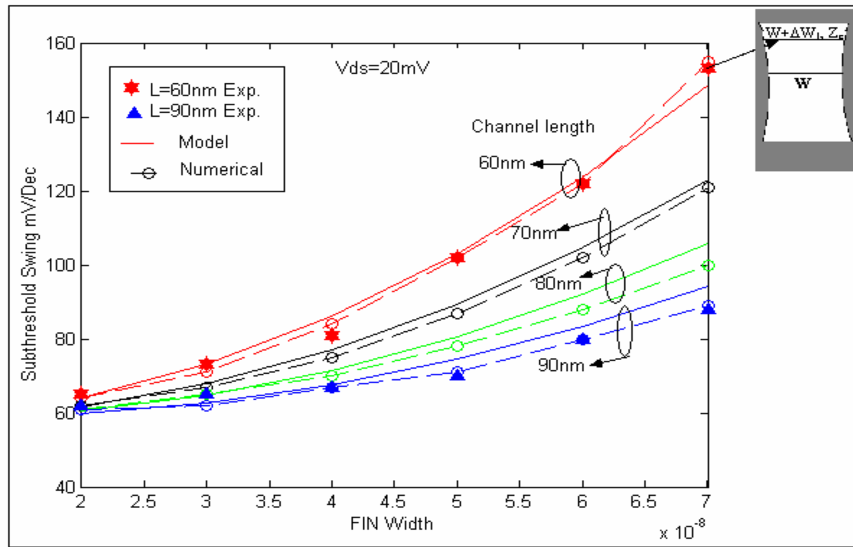
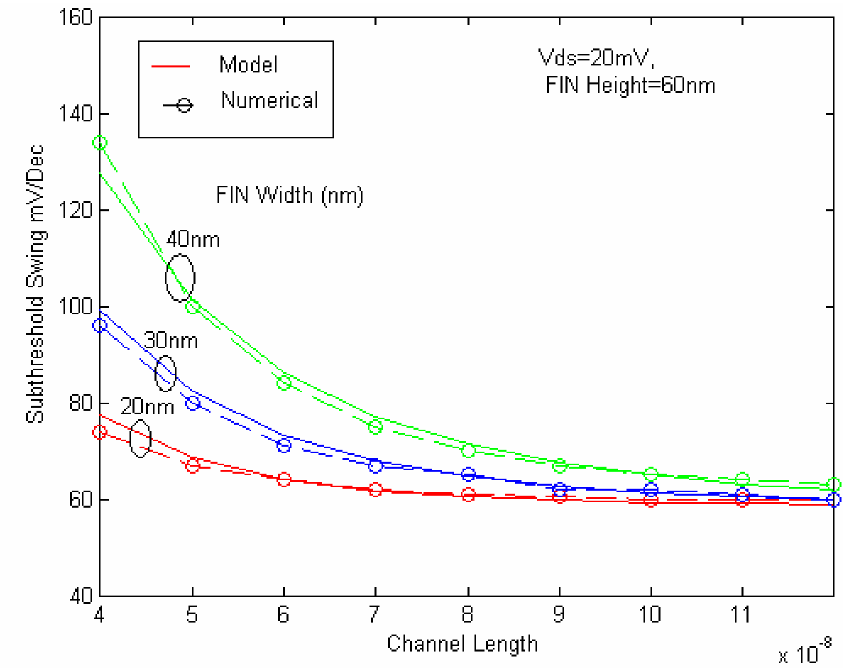
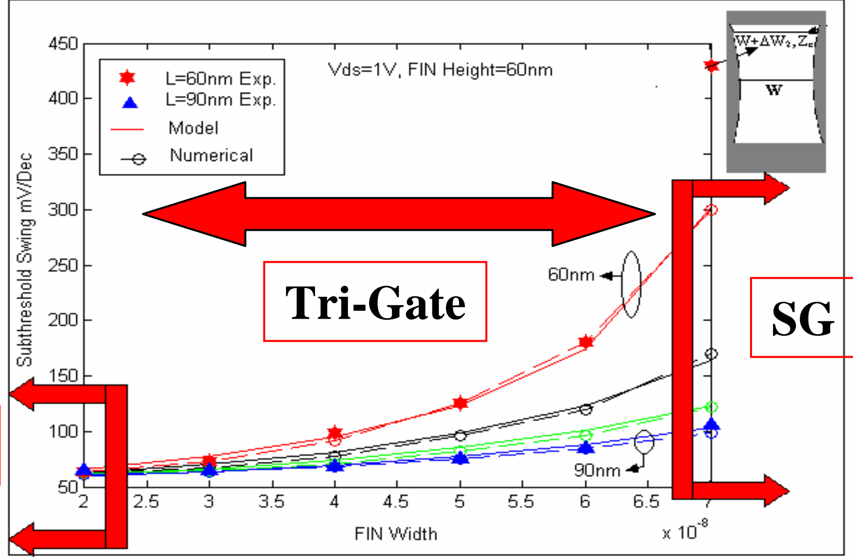
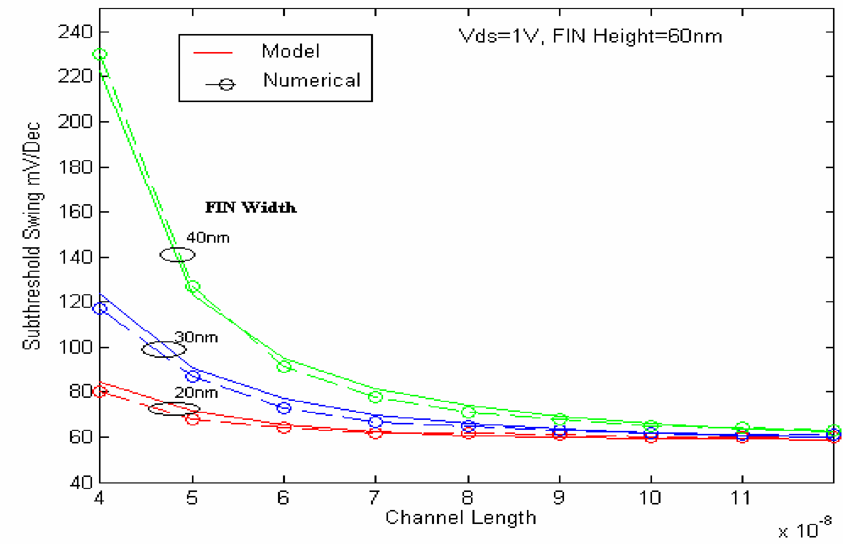
Swing Model Test







DG



Hamdy et al, WCM, May 2007, USA

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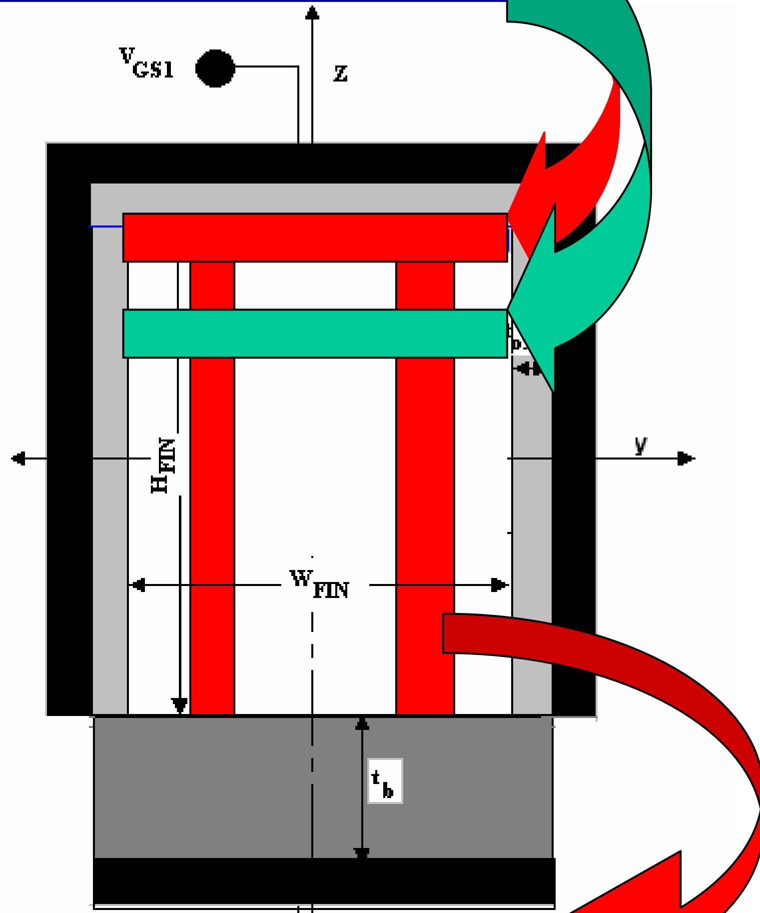
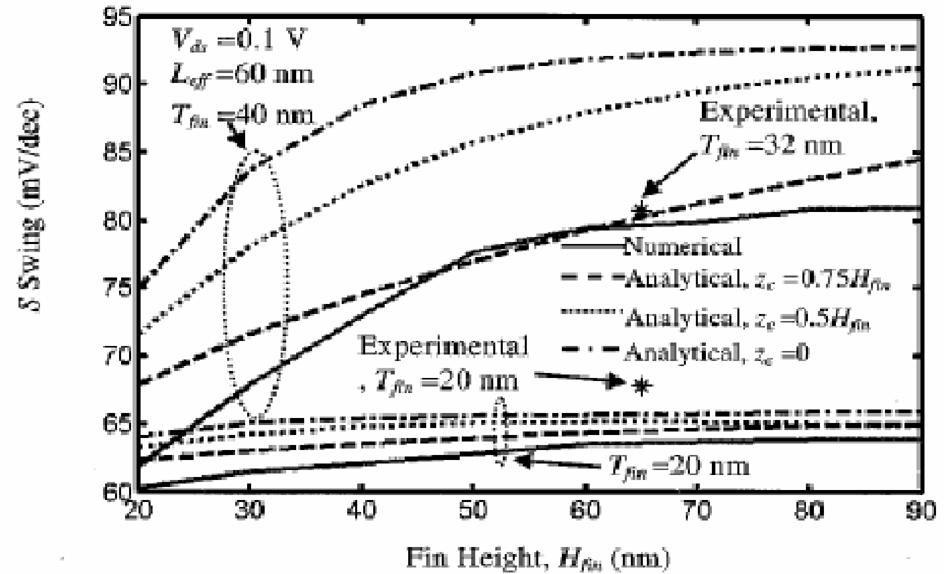
SCEs for the undoped FinFET

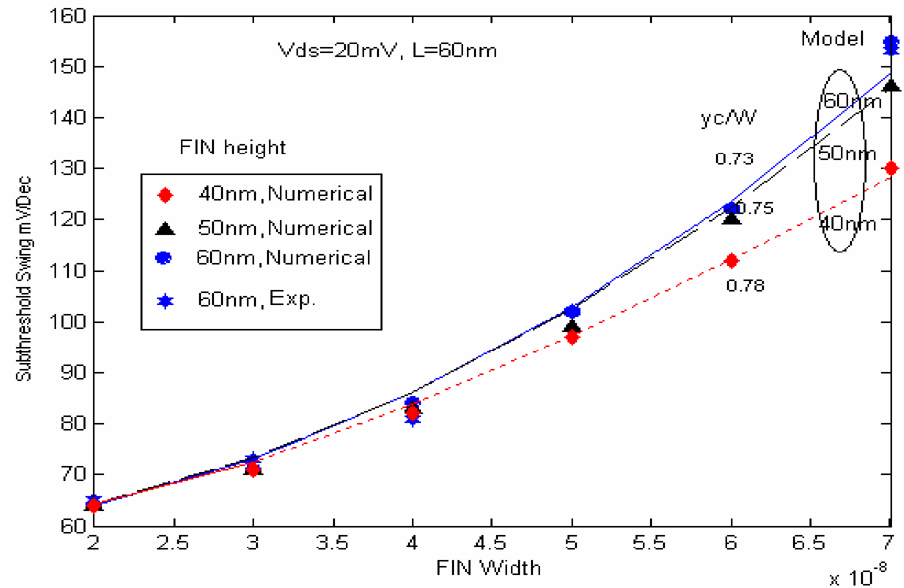
At fixed z_c =closer to Fin height



y_c closer to $W_{FIN}/2$

Pei et al, IEEE TED VOL. 49, August 2002





Hamdy et al, WCM, May 2007, USA

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2C.2 Threshold Voltage Model

$$Q_{inv} = 2\int_{y=0}^{t_o}\int_{z=-h_o}^{h_o} n_i \cdot e^{\frac{\phi_{min}(y,z)}{V_T}}\, dzdy$$

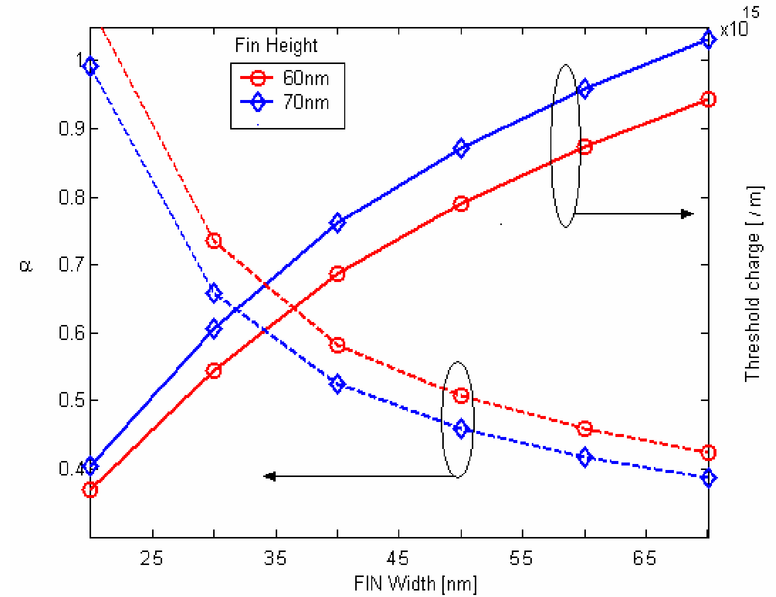
$$Q_{inv} = n_i \cdot W_{FIN} \cdot (\alpha \cdot H_{FIN}) \cdot e^{\frac{\phi_{min}(y_c,z_c)}{V_T}}$$

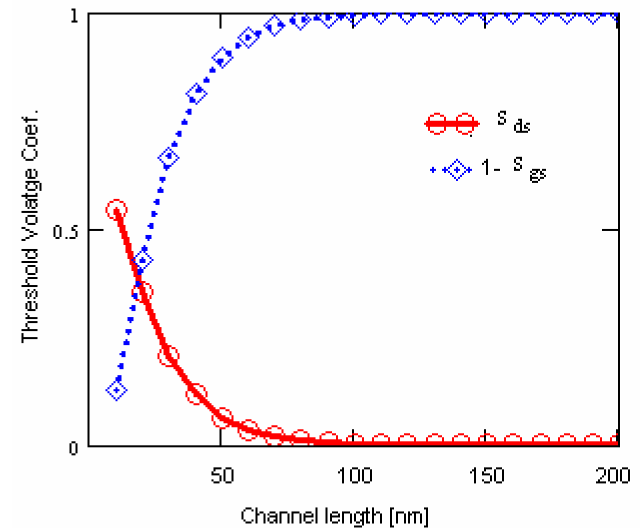
$$V_{TH} = \phi_{ms} + \frac{1}{1-S_{gs}}\left[V_T \cdot \ln\left(\frac{Q_o/\alpha}{n_i \cdot W_{FIN} \cdot H_{FIN}}\right) - S_{ds}\right]$$

$$V_{TH} = \phi_{ms} + \frac{1}{1-S_{gs}}\left[V_T \cdot \ln\left(\frac{Q_{TH}}{n_i \cdot W_{FIN} \cdot H_{FIN}}\right) - S_{ds}\right]$$

For a long channel device

$$V_{TH} = \phi_{ms} + V_T \cdot \ln\left(\frac{Q_{th}}{n_i \cdot W_{FIN} \cdot H_{FIN}}\right)$$





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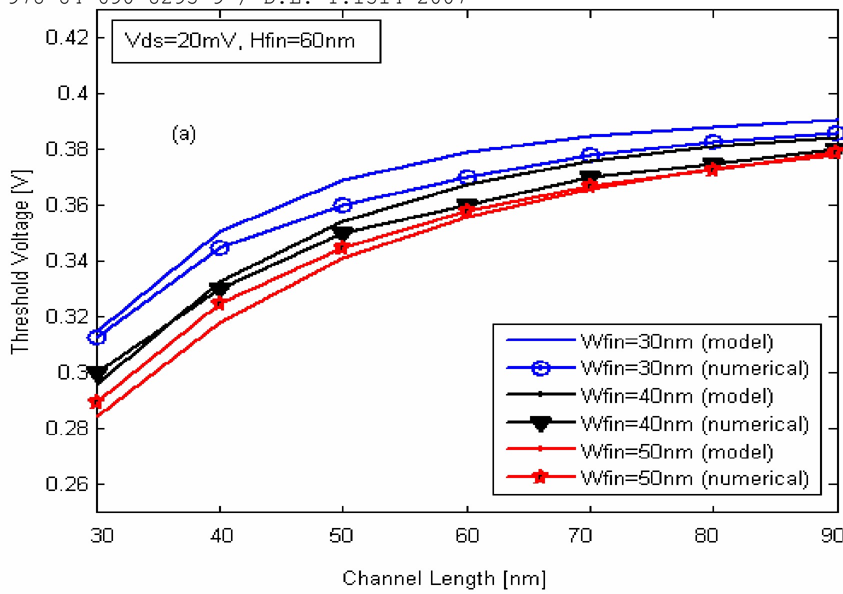
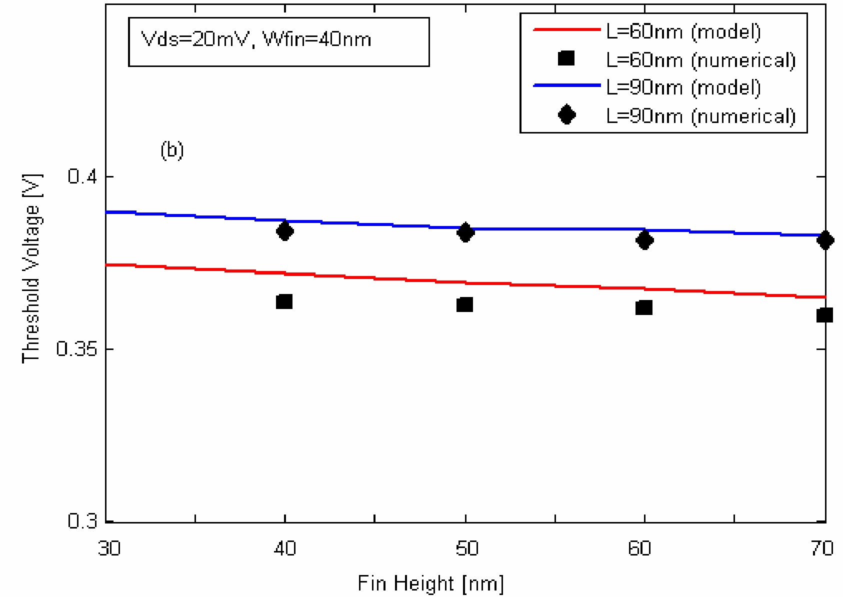
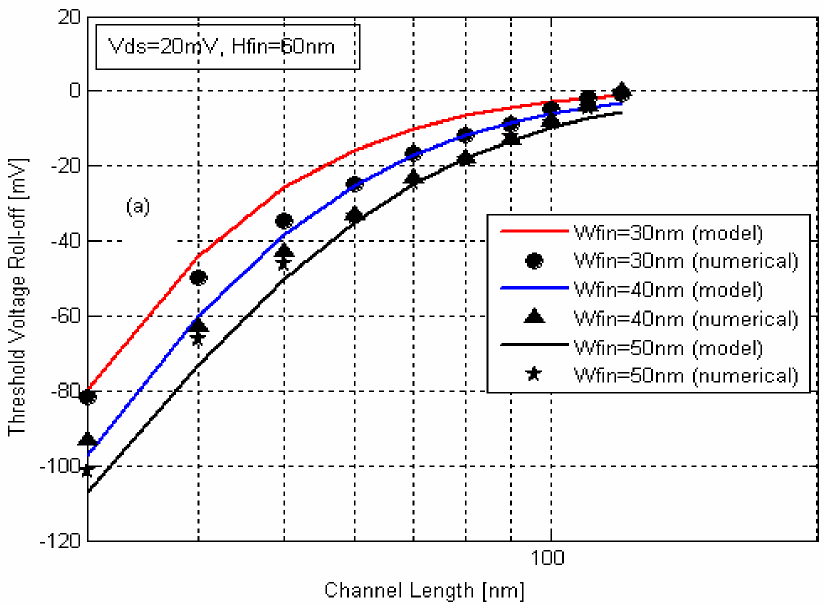
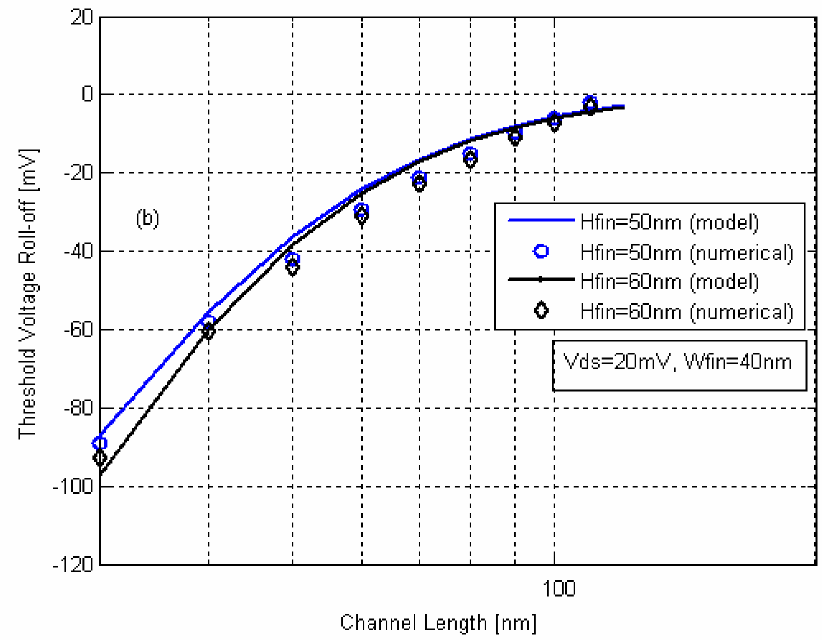
SCEs for the undoped FinFET









Hamdy et al, J. App. Phy., submitted, March 2007

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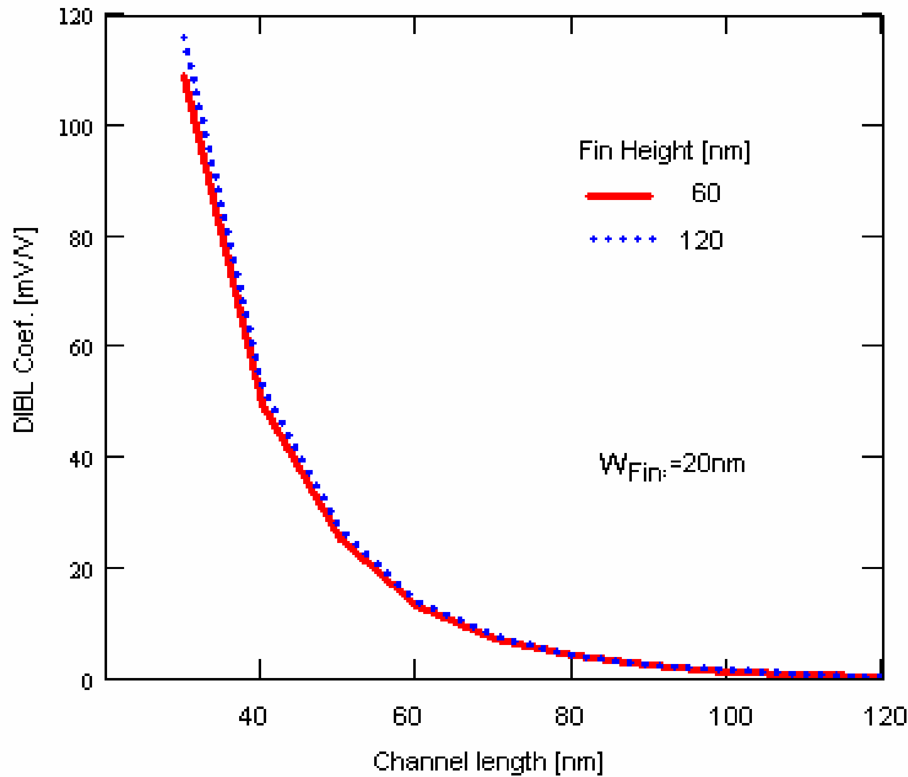
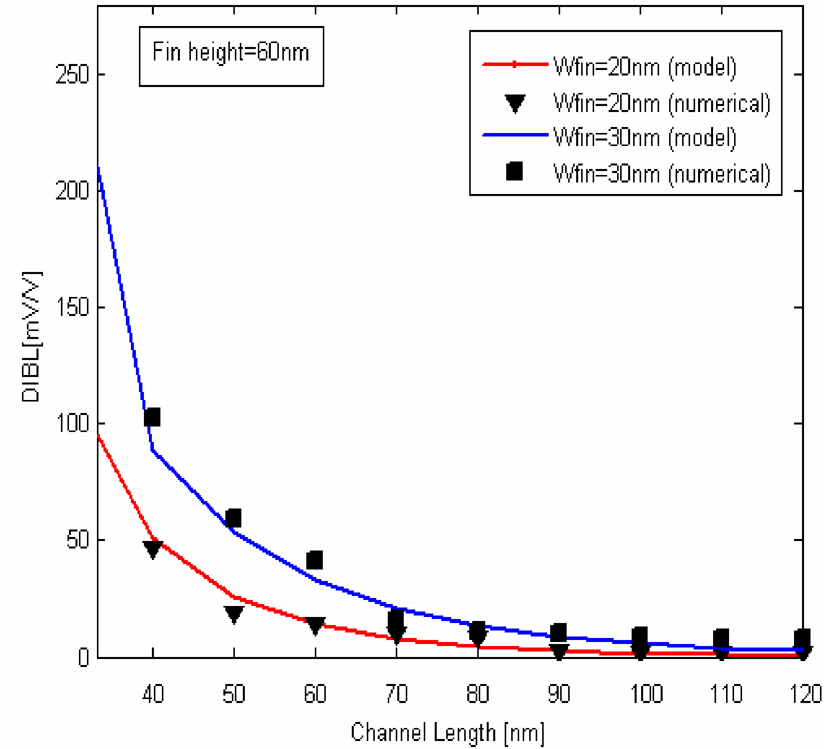
SCEs for the undoped FinFET

2C.3 DIBL result

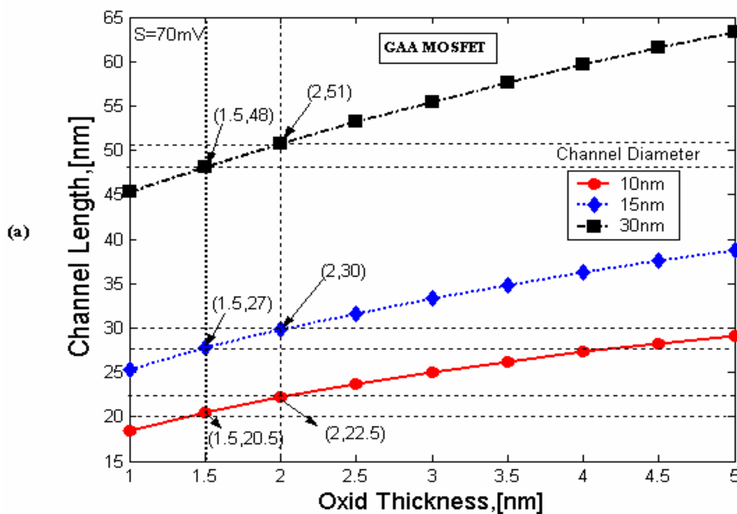


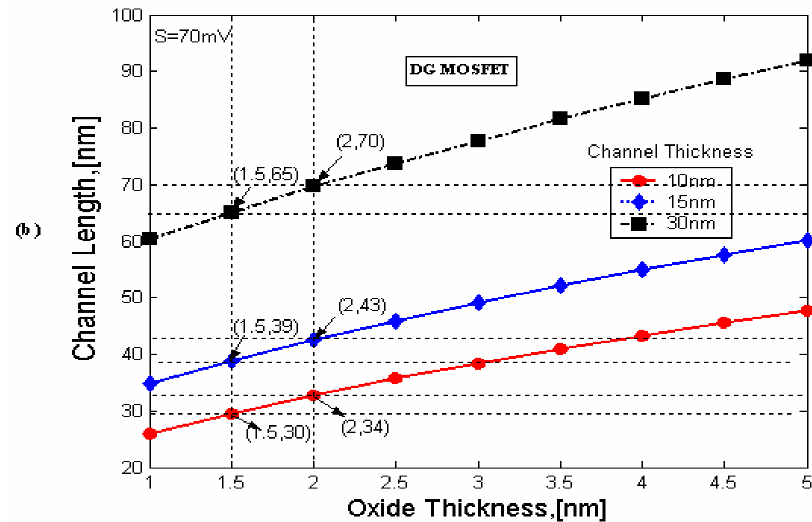


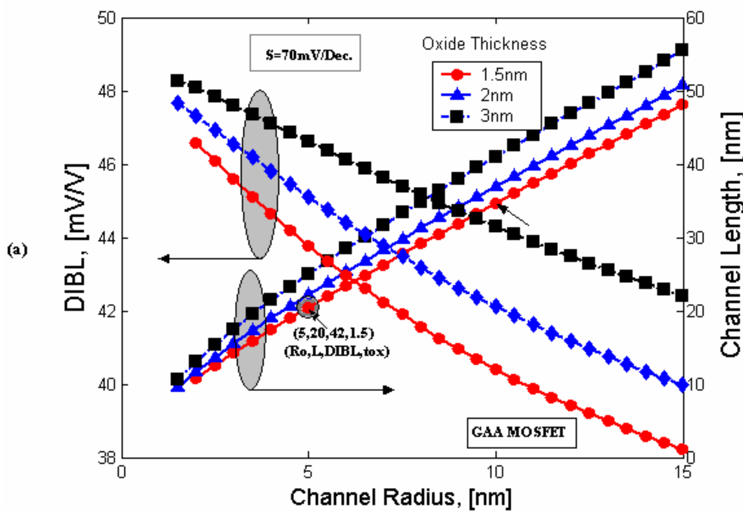
Hamdy et al, J. App. Phy., submitted, March 2007

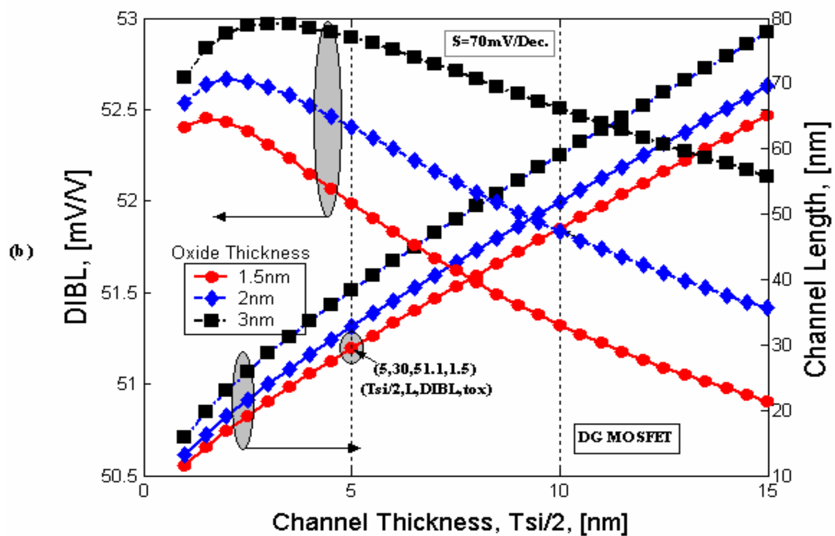
2D. Scalbility limits of Multiple Gate MOS devices

At S=70mV









Hamdy et al, Solid-State Electronics, Vol. 51, March 2007

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S=70mV

Channel Diameter, [nm]	Channel Length, [nm]	Oxide Thickness, [nm]	DIBL, [mV/V]
10	20	1.5	42
15	27	1.5	41.6
30	48	1.5	38
10	22.5	2	45
15	30	2	43.5
30	51	2	40

T. 1 GAA MOSFET device characteristics

Result

We have observed that to reach a given performance, the GAA MOSFET, can have a 33% longer channel length than the DG MOSFET.

Channel Thickness [nm]	Channel Length, [nm]	Oxide thickness, [nm]	DIBL, [mV/V
10	30	1.5	51.1
15	39	1.5	51.75
30	65	1.5	50.8
10	34	2	52.45
15	43	2	52.25
30	70	2	51.45

T. 2 GAA MOSFET device characteristics

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2. Short Channel Effects in undopded Multiple Gate MOS Devices
   1. SCEs in Cylindrical GAA MOS at low drain-source voltage
   2. SCEs in Cylindrical GAA MOS including DIBL Effect
   3. SCEs in DG MOSFET
   4. SCEs in FinFETs
3. **Current Transport in undoped Multiple Gate MOS Devices**
   1. **Current Models for Long channel Devices**
      1. **Explicit current Model for Long channel GAA MOSFETs**
      2. **Explicit current Model for Long channel FinFET**
      3. **Explicit current Model for Long channel DG MOSFETs**
   2. **Ballistic and quasi ballistic transport in multiple Gate MOS devices**
4. Summary

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ISBN: 978-84-690-8295-9 / D.L: T.1514-2007

3.A. Explicit Continuous Model For Long Channel Undoped Multiple Gate MOSFETs

3.1 GAA Model and results

Assuming the gradual channel approximation (GCA), in an undoped (lightly-doped) cylindrical *n*-type SGT-MOSFET, Poisson's equation takes the following form:

$$\frac{d^2\phi}{dr^2}+\frac{1}{r}\frac{d\phi}{dr}=\frac{kT}{q}\delta e^{\frac{q(\phi-V)}{kT}} \qquad \frac{d\phi}{dr}(r=0)=0, \qquad \phi(r=R)=\phi_{so}$$

Charge control model

$$\left.\begin{aligned}\phi(r)&=V+\frac{kT}{q}\log\left(\frac{-8B}{\delta(1+Br^2)^2}\right)\\ C_{ox}(V_{GS}-\phi_{ms}-\phi_{so})&=Q=\varepsilon_{Si}\left.\frac{d\phi}{dr}\right|_{r=R}\end{aligned}\right\}(V_{GS}-\phi_{ms}-V)-\frac{kT}{q}\log\left(\frac{8}{\delta R^2}\right)=\frac{Q}{C_{ox}}+\frac{kT}{q}\log\left(\frac{Q}{Q_0}\right)+\frac{kT}{q}\log\left(\frac{Q+Q_0}{Q_0}\right)$$

An approximate explicit solution

$$Q=C_{ox}(V_{GS}-V_0-V), \qquad Q=Q_0\exp\left(\frac{V_{GS}-V_0-V}{V_{th}}\right)$$

$$Q=C_{ox}\left(-\frac{2C_{ox}V_T^2}{Q_0}+\sqrt{\left(\frac{2C_{ox}V_T^2}{Q_0}\right)^2+4V_T^2\log^2\left(1+\exp\left(\frac{V_{GS}-V_0-V}{2V_T}\right)\right)}\right)$$

$$Q=C_{ox}\left(-\frac{2C_{ox}V_T^2}{Q_0}+\sqrt{\left(\frac{2C_{ox}V_T^2}{Q_0}\right)^2+4V_T^2\log^2\left(1+\exp\left(\frac{V_{GS}-V_{TH}+\Delta V_{TH}-V}{2V_T}\right)\right)}\right)$$

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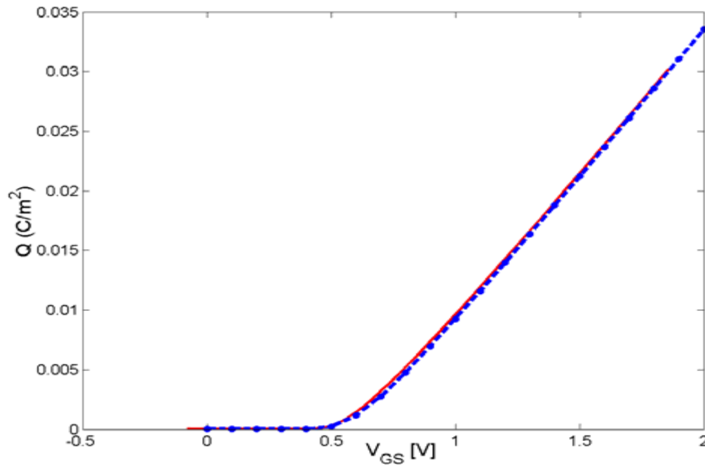
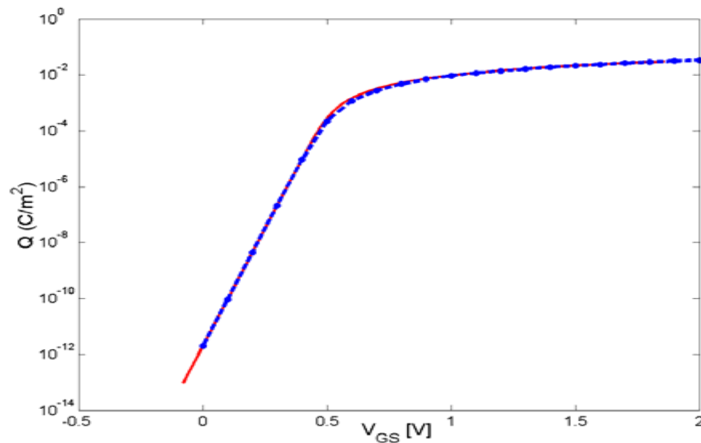
Charge density results





Channel charge density (per unit area)
gate working function of 4.61eV, L=1Micron, tox=1.5nm, R = 6.25 nm

The drain current calculations

$$I_{ds} = \mu \frac{2\pi R}{L} \int_0^{V_{ds}} Q(V)dV$$

From Charge control model Equation,

$$dV = -\frac{dQ}{C_{ox}} + \frac{kT}{q}\left(\frac{dQ}{Q} + \frac{dQ}{Q + Q_0}\right)$$

Now integrating between Q_s and Q_d

$$I_{ds} = \mu \frac{2\pi R}{L} \int_{Q_s}^{Q_d} Q \cdot dQ$$

$$I_{ds} = \frac{2\pi R}{L}\mu\left[2\frac{kT}{q}(Q_s - Q_d) + \frac{Q_s^2 - Q_d^2}{2C_{ox}} + \frac{kT}{q}Q_0 \log\left[\frac{Q_d + Q_0}{Q_s + Q_0}\right]\right]$$

Iñíguez et al, IEEE TED VOL. 52, AUGUST 2005

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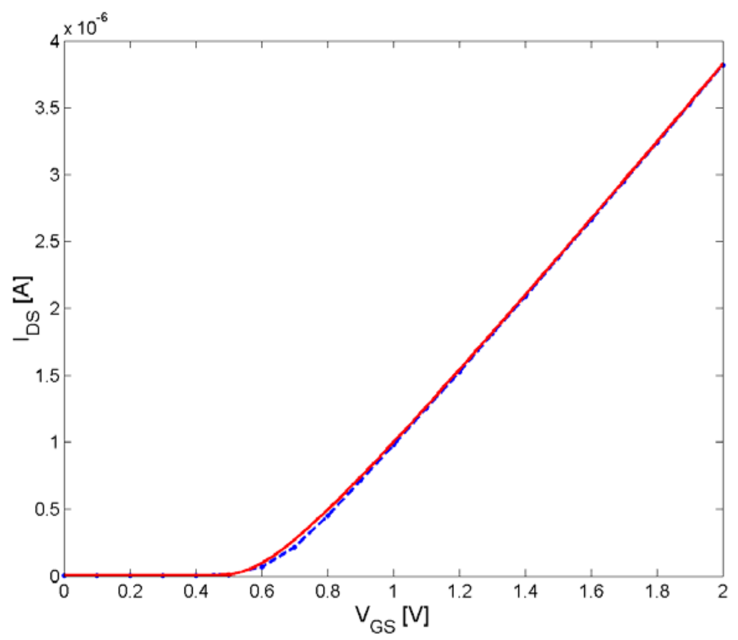
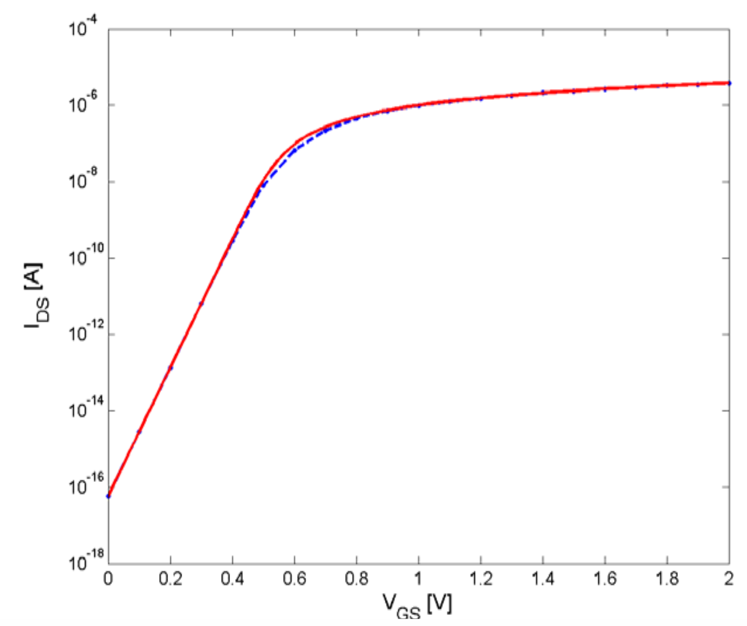
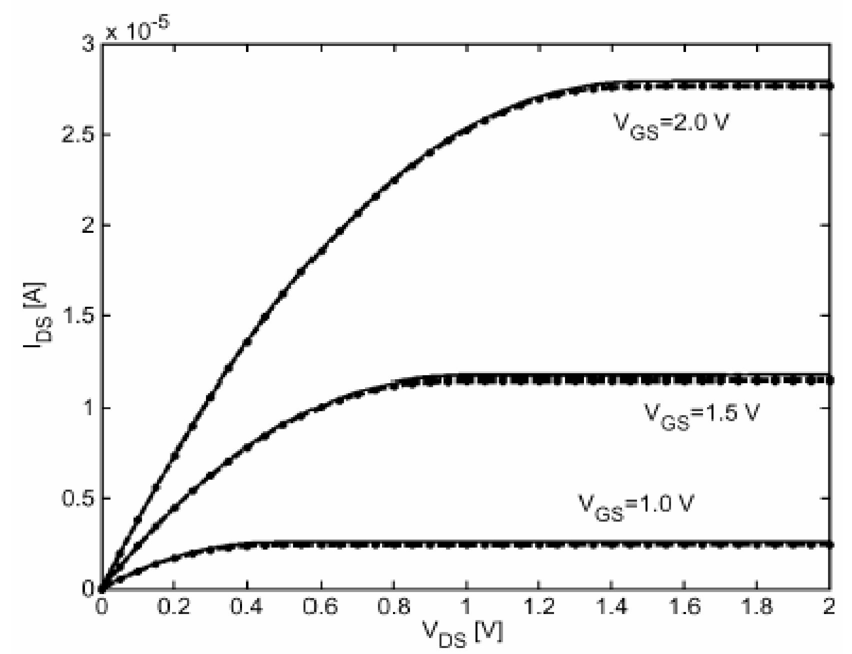
Current results





L=1Micron, tox=1.5nm, R = 6.25 nm, V_{ds}=0.1 V



Iñíguez et al, IEEE TED VOL. 52, AUGUST 2005

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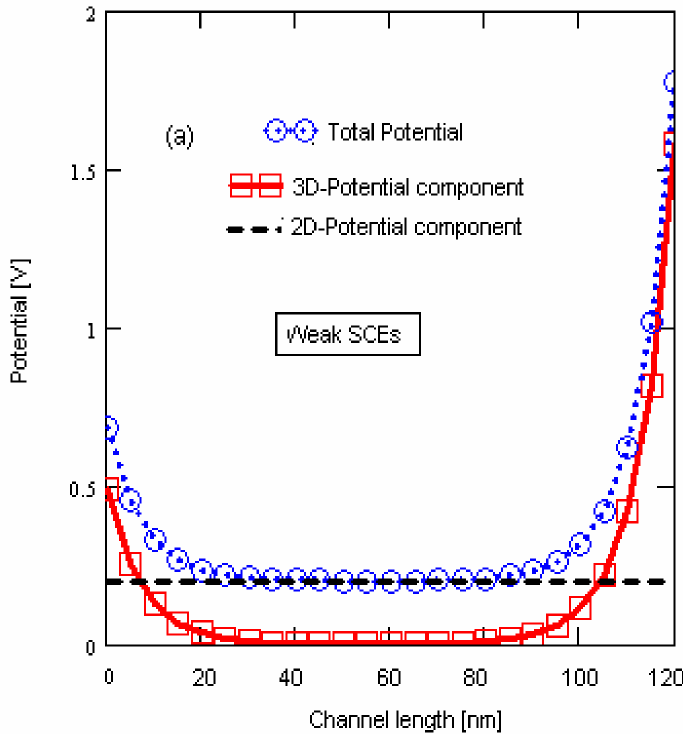
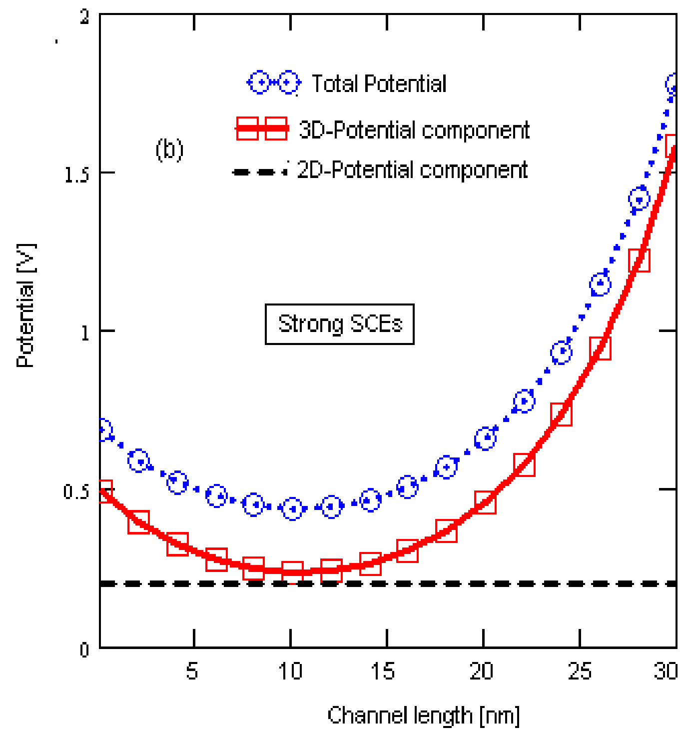
3.2 FinFET Model and results





$$Q = Q_0 \exp\left(\frac{\left(\Delta_{44} V_{GS1} - \Delta_{55} \cdot V_{GS2} - V_0 - V\right)}{V_T}\right) \approx Q_0 \exp\left(\frac{\left(V_{GS1} - V_0 - V\right)}{V_T}\right)$$

$$\mathrm{Q} = \mathrm{C_{ox}}' \cdot \left[\Delta_{44}\left(\mathrm{V_{GS1}}\right) - \Delta_{55}\left(\mathrm{V_{GS2}}\right) - V - V_0\right] \approx \mathrm{C_{ox}}' \cdot \left[\mathrm{V_{GS1}} - V - V_0\right]$$

Square GAA

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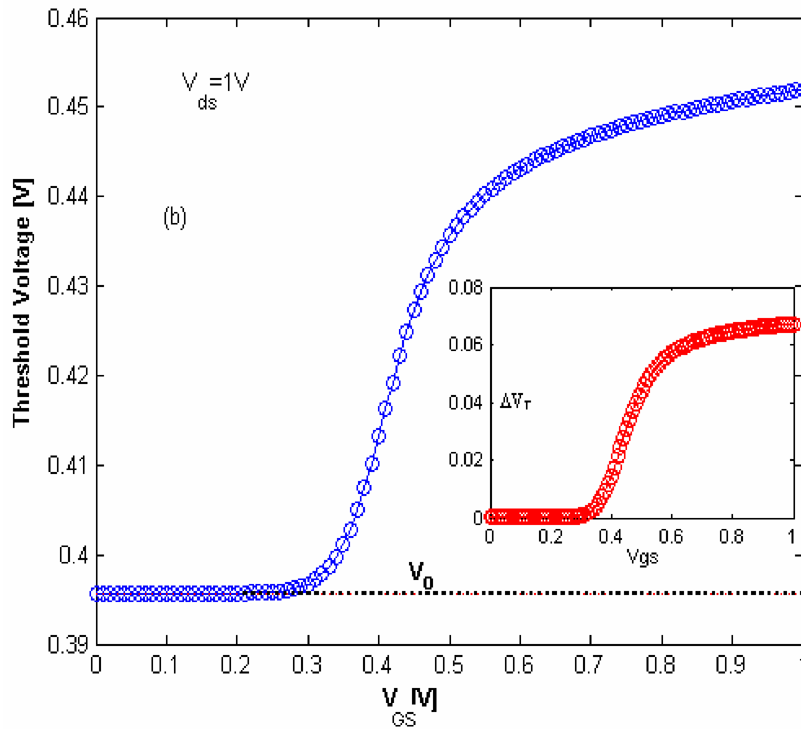
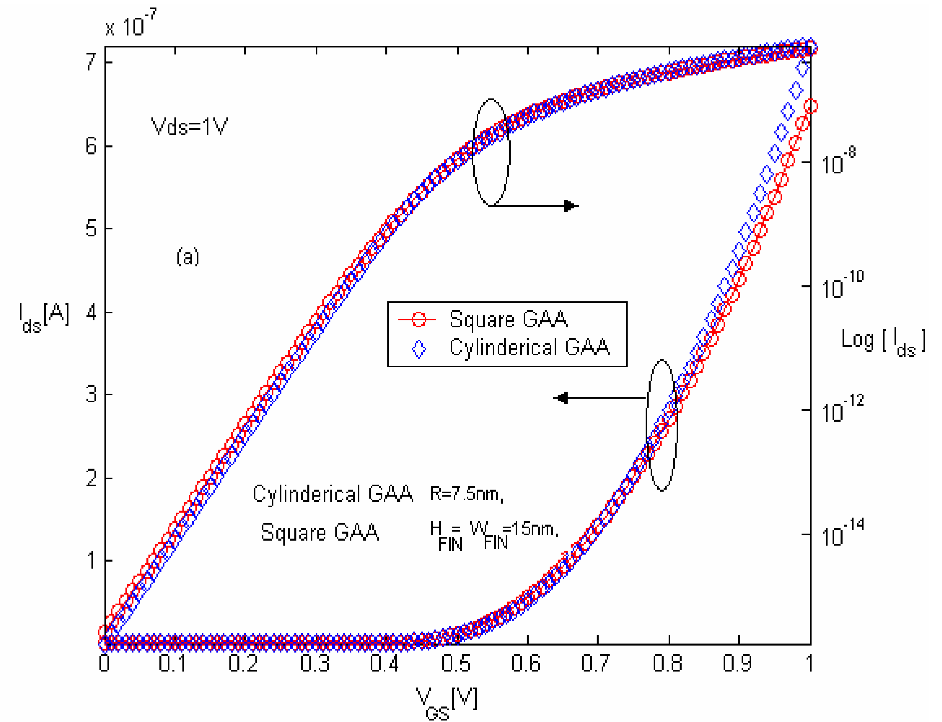
GAA Current results

$$I_{ds} = \frac{(2H_{FIN} + W_{FIN})}{L}\mu\left[2\frac{kT}{q}(Q_s - Q_d) + \frac{Q_s^2 - Q_d^2}{2C'_{ox}} + \frac{kT}{q}Q_0 \log\left[\frac{Q_d + Q_0}{Q_s + Q_0}\right]\right]$$

FinFET





GAA MOSFET model: Cylindrical and Square MOS comparison

gate working function of 4.61eV, L=10Micron, tox=1.5nm, t_{box}=150nm,

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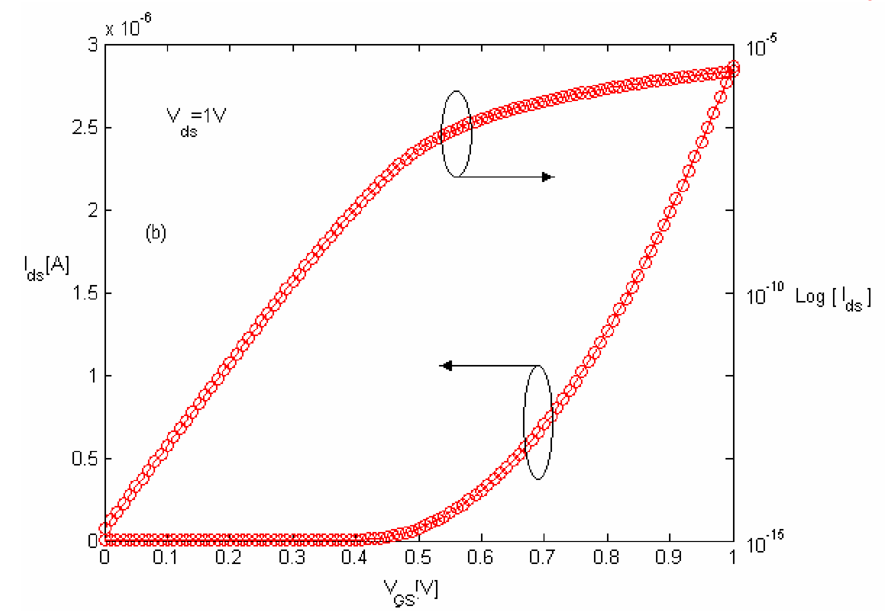
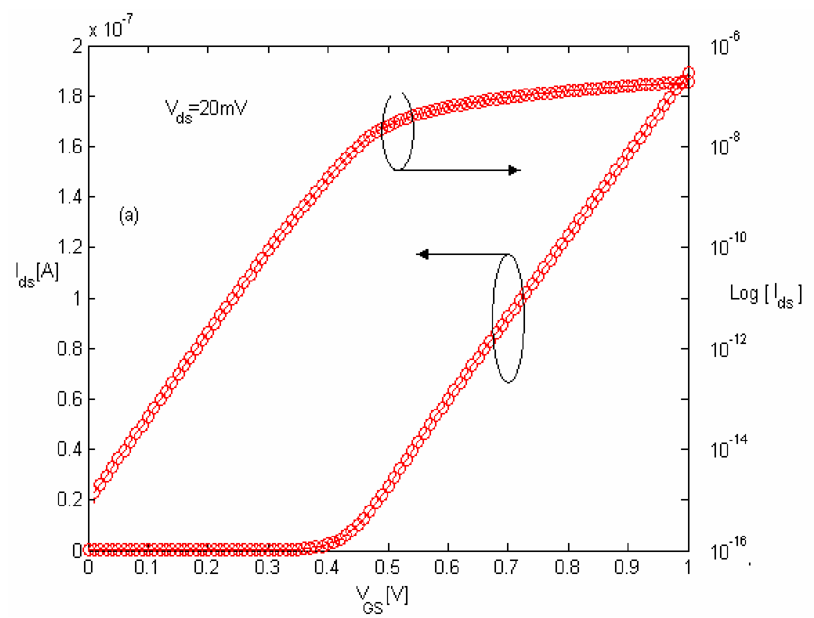
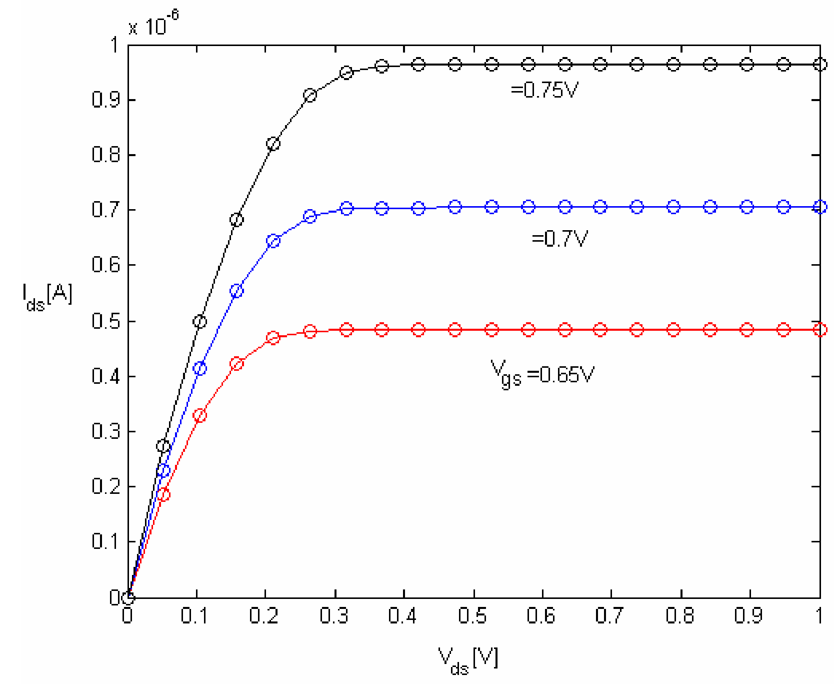
FinFET: current results







H_{FIN}=65nm, W_{FIN}=25nm, and L=10micron

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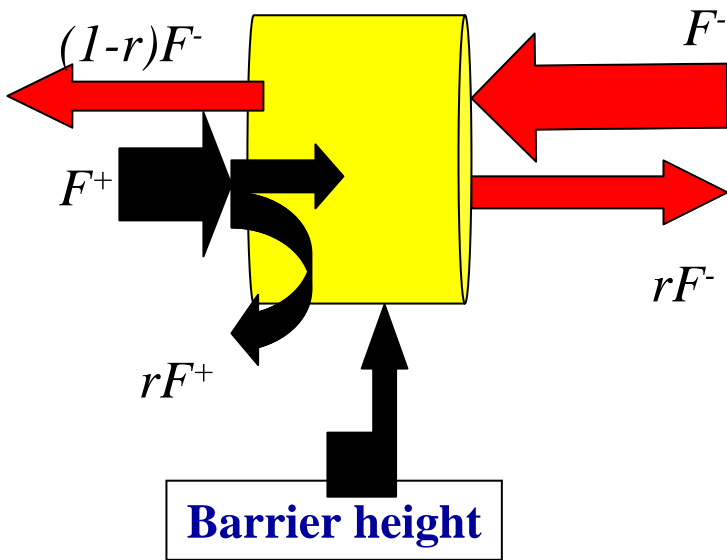
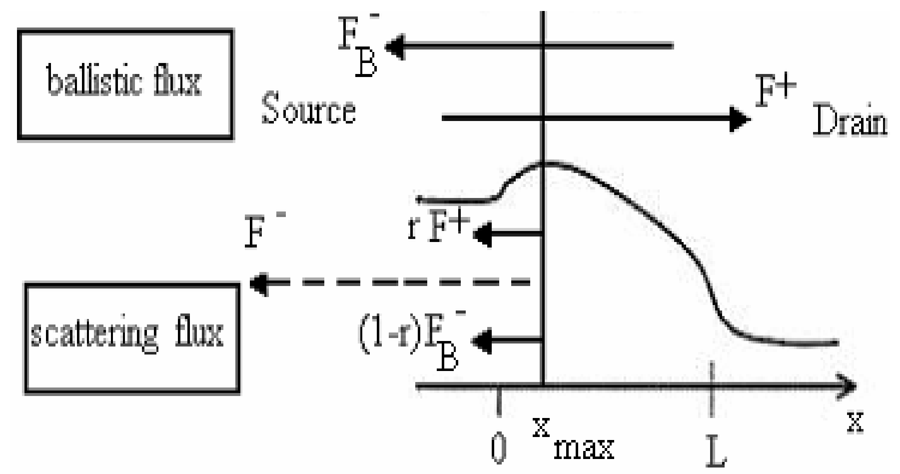
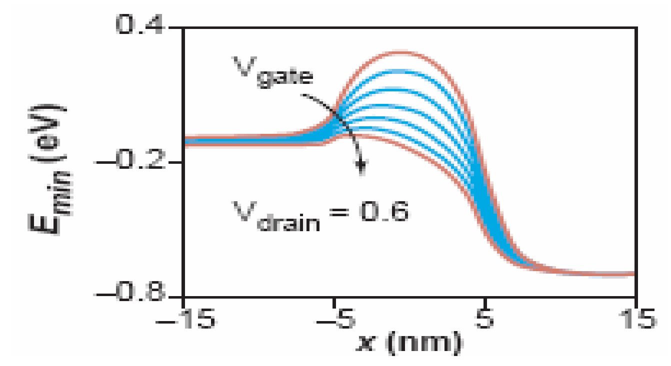
3.B. Ballistic and quasi ballistic transport

Channel Length are decreasing to below 50 nm where traditional compact models lose validity.







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3.B.1 DG Quasi Ballistic Transport

Ballistic Current

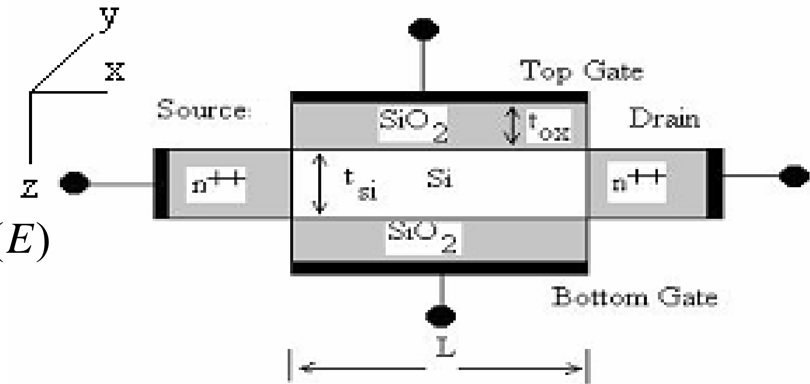
$$I = \frac{q}{L}\sum_{v}\sum_{k_z,k_y}\sum_{k_x>0} g_v\left(f_S(E)-f_D(E)\right)\left(\frac{\hbar k_x}{m_x^v}\right)T(E)$$

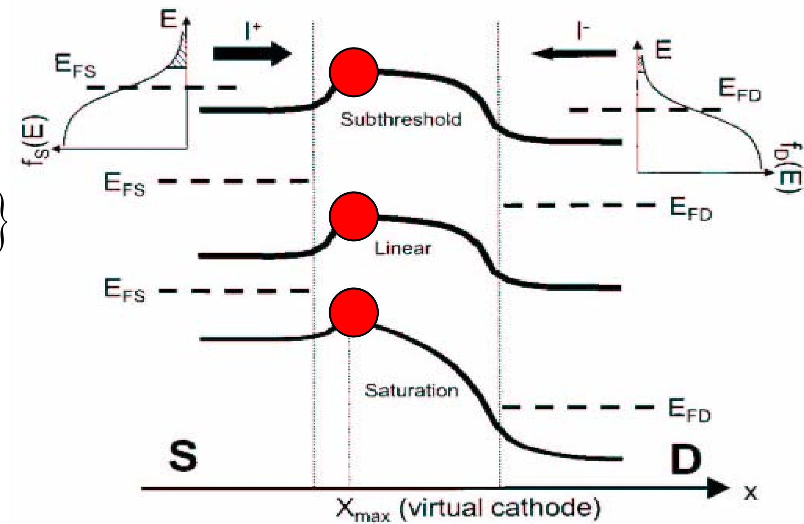
$$I_B = I^+ - I^- = W\ q\ (F^+ - F^-)$$

Ballistic Charge

$$Q = \sum_{v}\sum_{n}\left\{Q^+(E_{FS}-E_n^v(x_{max})) + Q^-(E_{FD}-E_n^v(x_{max}))\right\}$$

$$Q = \frac{q}{v}(F^+ + F^-)$$





Jimenez et al, Journal of Applied Physics, vol. 94, July 2003

ISBN: 978-84-690-8295-9 / D.L: T.1514-2007

3.B.2 DG Scattering Model

Backscattering Current

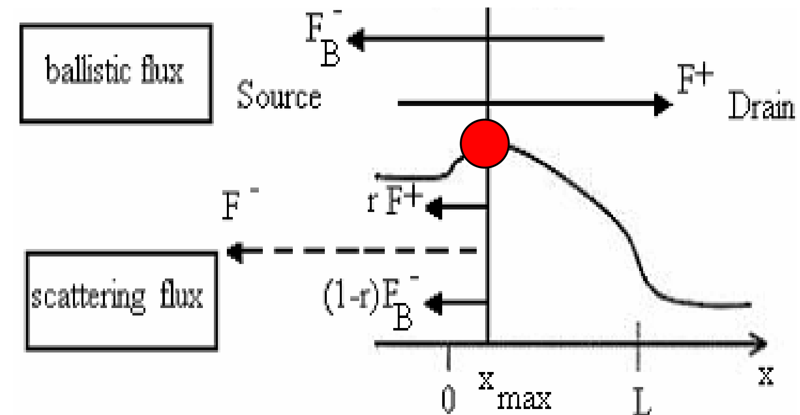
$$I = W\,q\,\left\{F^{+} - rF^{+} - (1-r)F_{B}^{-}\right\}$$
$$= W\,q\,(1-r)(F^{+} - F^{-}) = (1-r)I_{B}$$

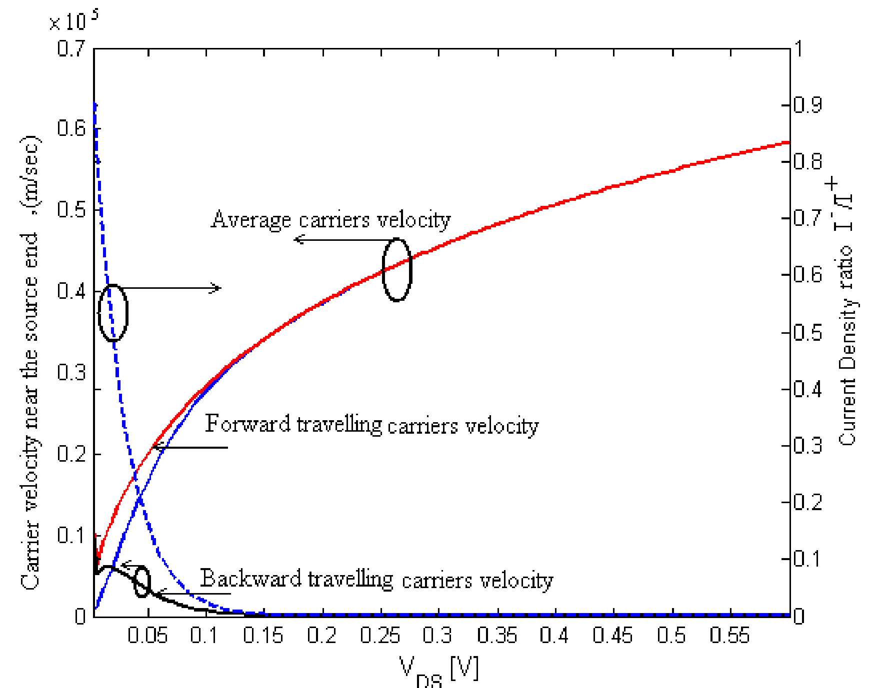
Backscattering Charge

$$Q = \frac{q}{v}\left\{F^{+} + rF^{+} + (1-r)F_{B}^{-}\right\} = (1+r)Q^{+} + (1-r)Q^{-}$$

Backscattering Coefficient

$$r = \frac{\ell}{\ell + \lambda}$$





Rahman, et al, IEEE TED, , Vol. 49, No. 3, March 2002

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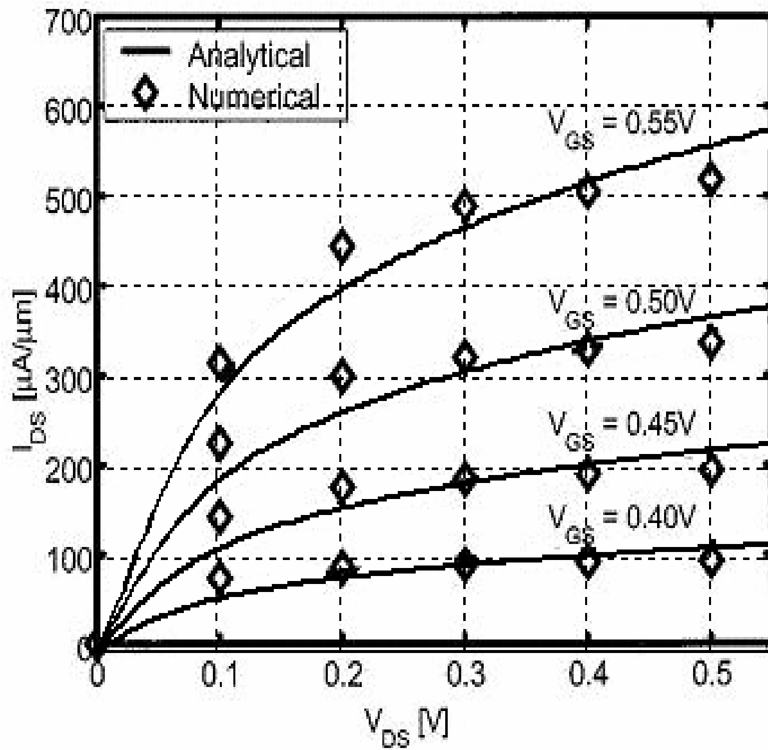
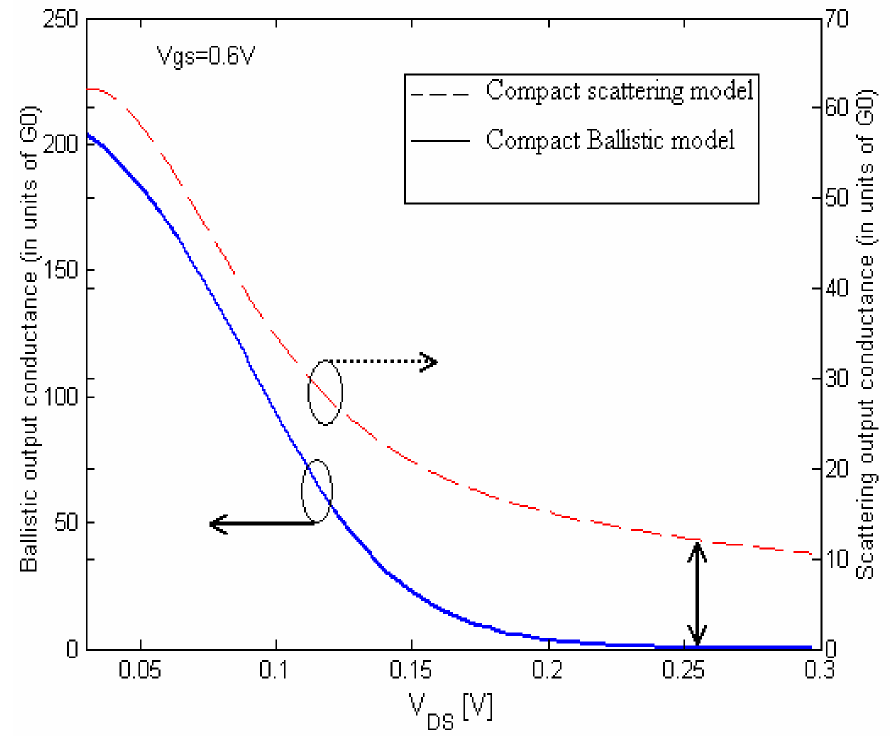
current results



The solid line results of our compact model, and the diamonds represents 2D numerical simulation of the same device.



Channel conductance for our compact scattering model ($r \neq 0$), and the solid line from the ballistic model ($r=0$).

Hamdy., et. al., physica status solidi, vol. 2, Issue 8, Date: May 2005

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3.B.3 FinFET Quasi Ballistic Transport

$$I_{ds_sat} = W \cdot v_{inj} \cdot \left[\frac{1-r_{sat}}{1+r_{sat}}\right] \cdot C_{ox} \cdot \left(V_{GS} - V_{T,sat}\right)$$

$$\frac{\partial I_{ds_sat}}{\partial T} = I_{ds_sat}\left[\frac{1}{v_{inj}}\frac{\partial v_{inj}}{\partial T} + \frac{1+r_{sat}}{1-r_{sat}}\frac{\partial}{\partial T}\left(\frac{1+r_{sat}}{1-r_{sat}}\right) + \frac{1}{V_{GS}-V_{T,sat}}\frac{\partial\left(V_{GS}-V_{T,sat}\right)}{\partial T}\right]$$

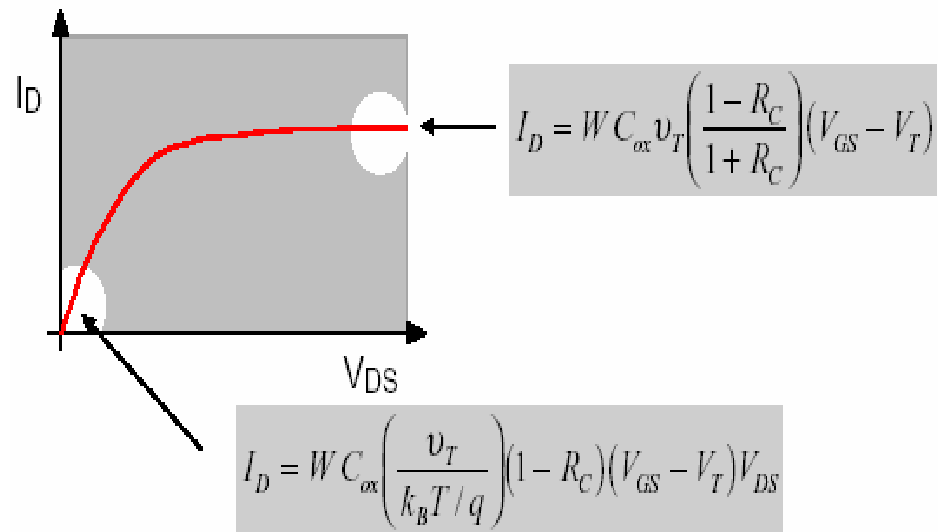
$$= I_{ds_sat}\left[\frac{1}{2T} - \frac{\partial r_{sat}}{\partial T}\left(\frac{1}{1+r_{sat}} + \frac{1}{1-r_{sat}}\right) - \frac{\eta}{V_{GS}-V_{T,sat}}\right]$$

$$= I_{ds_sat} \cdot \alpha$$

$$\eta = \left(V_{T-sat\,1} - V_{T-sat\,2}\right)/\left(T_1 - T_2\right)$$

$$\frac{\partial r_{sat}}{\partial T} = \left[2 r_{sat} \cdot \left(1 - r_{sat}\right)\right]/T$$

$$\alpha = \left(I_{ds-sat1} - I_{ds-sat2}\right)/\left[\left(T_1 - T_2\right)\right]$$



Lundstrom et al, IEEE *EDL*, vol. 18, 1997

Jer Chen et al, IEDM, 2002

Wee Ang, et al, ESSDERC, 2006, Switzerland (strained)

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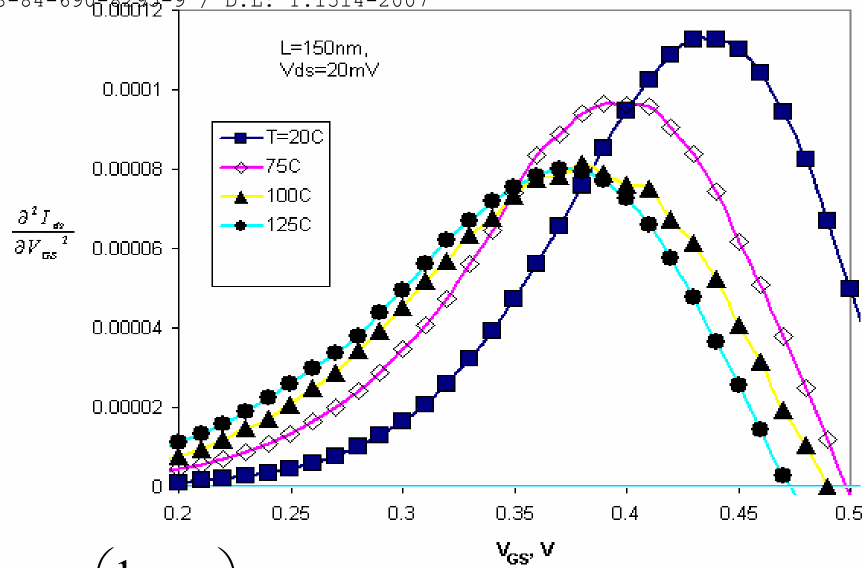
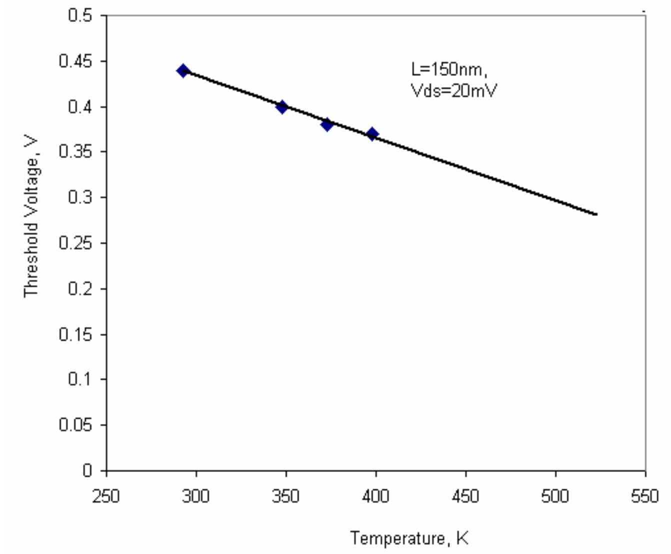
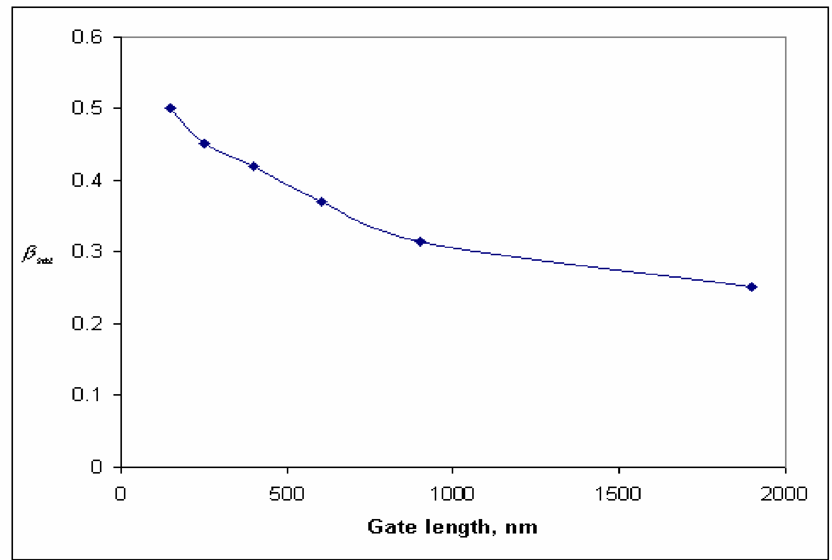
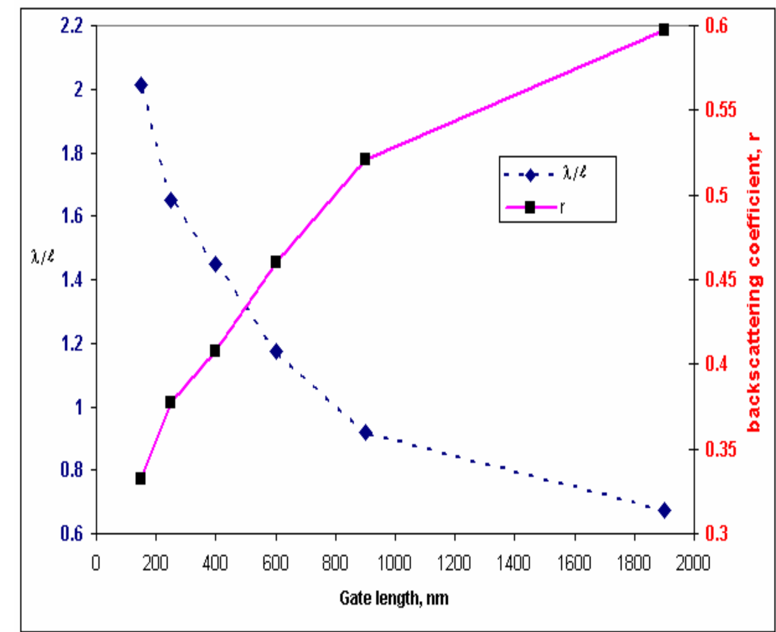
Quasi ballistic transport





$$\beta_{sat} = \left(\frac{1-r_{sat}}{1+r_{sat}}\right) \qquad I_{ds_with\,scattering} = \beta_{sat} \cdot I_{ds_without\,scattering}$$





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Conclusions

In this thesis we have studied the characteristics of the undoped multiple gate MOS devices.

- We have introduced compact models for the Short Channel Effects (SCEs) for three multiple gate devices (Surrounding Gate All Around, Double Gate, and FinFET).

- We did not introduce any fitting parameters to develop those models.

- The device electrostatics has been studied based on the device structures as: we consider 2D structures (like **Double Gate MOSFETs**), and 3D structures (like Gate All Around MOSFETs, and FinFETs).

- We have also proved that the devices with multiple gates have better performances than the devices with a single gate using our models.

- We have presented an analytical DC model for undoped multiple gate MOS devices. The model is based on a new unified charge control model

- The backscattering coefficient has also been studied through this thesis.

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Recommendations for the future work

- In the future we shall study the SCEs for the undoped multiple gate MOS devices with channel thickness thinner than 10nm, i.e. **the quantum effects should be included**

- We shall study the DC device characteristics for the devices with shorter lengths.

- We shall study the backscattering coefficient for the devices with new materials like SiGe, or carbon

- We shall study the devices with a strained Si, or SiGe

- System applications based on multiple Gate MOS devices also will be studied, e.g, **noise, amplification gain**

Publications

Journals

1- **Hamdy Abd-Elhamid,** Jaume Roig, Valeria Kilchytska, Denis Flandre, Benjamin Iñiguez ¨ A 3-D Analytical Physically-Based Model for SCEs in Undoped FinFETs,¨ **IEEE TRANSACTIONS ON ELECTRON DEVICES, submitted since Jan. 2007**

2- **Hamdy Abd-Elhamid,** Jaume Roig, , Valeria Kilchytska, Denis Flandre, Benjamin Iñiguez ¨ A 3-D Analytical Physically-Based Model for the Subthreshold Swing in Undoped FinFETs¨, **Journal app. physics, submitted since March 2007**

3- **Hamdy Abd-Elhamid,** Benjamin Iñiguez, and Jaume Roig ”Two-Dimensional Analytical Threshold Voltage and Subthreshold Swing Models of Undoped Symmetric Double Gate MOSFETs”,**IEEE TRANSACTIONS ON ELECTRON DEVICES, in press, May, 2007**

4- **Hamdy Abd-Elhamid,** Benjamin Iñiguez, and Jaume Roig, ”Scalability Limits Of Multiple Gate MOSFET Devices”, **Solid-State Electronics , Vol. 51, March 2007**

5 - **Hamdy Abd-Elhamid,** Benjamin Iñiguez, and Jaume Roig, ”Analytical Model of the Threshold Voltage and Subthreshold Swing of Undoped Cylindrical Gate All Around Based MOSFETs”, **IEEE TRANSACTIONS ON ELECTRON DEVICES, Vol. 54, No.3, March 2007**

6- **Hamdy Abd-Elhamid,** Benjamin Iñiguez, David Jiménez, Jaume Roig, Josep Pallarès, and Lluís F. Marsal, "Two-Dimensional Analytical Threshold Voltage Roll-Off and Subthreshold Swing Models For Undoped Cylindrical Gate All Around MOSFET," **Solid-State Electronics, Vol. 50, no. 5, pp. 805-812, May 2006..**

7- Benjamin Iñíguez, David Jiménez, Jaume Roig, **Hamdy Abd Elhamid**, Lluís F. Marsal, and Josep Pallarès *“EXPLICIT CONTINUOUS MODEL FOR LONG CHANNEL UNDOPED SURROUNDING GATE MOSFETS”*, **IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 52, AUGUST 2005**

8- **Hamdy Abd-Elhamid,** Benjamin Iñiguez, David Jiménez, Jaume Roig, Josep Pallarès, and Lluís F. Marsal *“A simple model of the nanoscale double gate MOSFET based on the flux method”* **physica status solidi (c) Vol. 2, Issue 8, Date: May 2005, Pages: 3086-3089**

•International conferences

9-(Invited) **Hamdy Abd-Elhamid**, Benjamin Iñiguez, and Jaume Roig "3-D Analytical Models for the Short-Channel Effect Parameters in Undoped FinFET Devices", **Workshop on compact modelling, WCM, May 20-24, 2007 Santa Clara Convention Center, California, U.S.A.**

10- **Hamdy Abd-Elhamid**, Benjamin Iñiguez, and Jaume Roig ¨A 2-D Short Channel Effects Model For Undoped Double Gate MOSFET , **Euro-SOI, Leuven, Belgium. 17-19 January, 2007**

11- **Hamdy Abd-Elhamid**, Benjamin Iñiguez, and Jaume Roig¨ NATO International Advanced Research Workshop *"Nanoscaled Semiconductor-on-Insulator Structures and Devices"* **15-19 October 2006, Sudak, Crimea, Ukraine**

12- **Hamdy Abd-Elhamid**, Benjamin Iñiguez, and Jaume Roig, MOS Modeling and Parameter Extraction Working **Group MOS-AK/ESSDERC/ESSCIRC Workshop Compact Modeling for Emerging Technologies, September 2006 Montreux Convention and Exhibition Center ¨scalability limits of multiple gate MOS devices¨**

13- **Hamdy Abd-Elhamid**, Benjamin Iñiguez, David Jiménez, Jaume Roig, Josep Pallarès, and Lluís F. Marsal*"Threshold voltage, and subthreshold swing for GAA MOSFET "*, **Euro-SOI, Grenoble, France. 19-21 March, 2006**

14- Benjamin Iñiguez , **Hamdy Abd-Elhamid**, ¨*Noise in SOI MOSFETs and Gate-All- Around Transistors*¨ 18th **International Conference on Noise and Fluctuations-ICNF 2005, Salamanca, Spain, 19-23 Sept. 2005**.

15- **Hamdy Abd-Elhamid**, Benjamin Iñiguez, David Jiménez, Josep Pallarès, and Lluís F. ¨*Compact Modelling for Surrounding Gate MOSFETs*¨ **International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES 2005), Krakow (Poland), June 2005**.

16- *(Invited)* Benjamin Iñiguez, **Hamdy Abd-Elhamid**, David Jiménez,*"Compact Model of Multiple-gate SOI MOSFETs"* ES 2005 **NSTI Nanotechnology Conference and Trade Show Nanotech, Workshop on compact modelling, WCM, 2005 May 8-12, 2005 Anaheim Marriott & Convention Center Anaheim, California, U.S.A.**

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17- **Hamdy Abd-Elhamid**, Benjamin Iñiguez, David Jiménez, Josep Pallarès, and Lluís F. *"Quasi Ballistic Model of double gate MOSFET"*, **First Workshop of the Thematic Network on Silicon on Insulator technology, devices and circuits Granada, SPAIN. 19-21 January, 2005**

National conferences

18- **Hamdy Abd-Elhamid**, Benjamin Iñiguez, David Jiménez, Josep Pallarès, and Lluís F. *"Double Gate MOSFET Compact Model Including Scattering"* **Conference on Electron Devices (CDE), Tarragona, Spain, 02-05 Feb., 2005**

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Professor **Denis Flandre**, and Dr. **Valeria Kilchytska**

Microelectronics Laboratory, Université catholique de Louvain, Belgium

--- And IMEC Group, Leuven, Belgium

Professor **Hall Steve**: **University of Liverpool, UK**

Professor **Tor A. Fjeldly** : UniK, Kjeller, Norway

Professor M. Jamal Deen of McMaster University

Dr. **David Jimenez** of Universitat Autonoma de Barcelona, Spain

Professors **Josep Pallares**, and **Lluıs F. Marsal** of Universitat Rovira i Virgili, Tarragona, Spain

Universitat Rovira i Virgili, Tarragona, Spain

Finally, thanks for your attentions