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Field effect in silicon nanostructure fabricated by atomic force microscopy nano lithography

ABSTRACT

The electrical property of silicon nano-structure is highly considered in nanoelectronics. In this context we investigate the field effect in nanostructure Junctionless p-type silicon nanowire transistor under the lateral gate voltage. The device fabricated by means of Atomic Force microscopy (AFM) nano lithography on Silicon on Insulator (SOI) wafer. I-V characteristic and the Drain/Source current under the lateral gate voltage investigated. The subthreshold swing measured and hysteresis effect observed for the old sample compared to new one.

Keyword: P-type silicon nanowire transistor; Atomic force microscopy nano lithography; Field effect; Silicon on insulator SOI; Local anodic oxidation