

Numerical study of side gate junction-less transistor in on state

ABSTRACT

Side gate p-type Junctionless Silicon transistor is fabricated by AFM nanolithography on low-doped (10^{15} cm^{-3}) SOI wafer. In this work, the simulation characteristic of the device using TCAD Sentaurus in on state will be studied. The results show that the device is the pinch off transistor, works in on state for zero gate voltage in depletion mode. Negative gate voltage drives the device into on state, but unable to make significant effect on drain current as accumulation mode. Simulation results for valence band energy, electric field and hole density are investigated along the active regions. The influence of the electric field due to the applied voltages of V_{DS} and V_G on charge distribution is much more when the device operates at the saturation region. The hole quasi-Fermi level has a positive slope showing the current flows from source to drain.

Keyword: Side gate junctionless transistors (SGJLT); Valence band energy; Hole density distribution