[ME09] Design and implementation of a digital front-end for multi-standard software defined radio receiver

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Introduction

Software defined radio (SDR) is an emerging technology, thought to realize flexible radio systems, multi-service, multi-standard, re-configurable and re-programmable by software (Buracchini,2000). A goal in SDR is to push the digitization point as close as possible to the antenna (Hentschel *et. al.*,1999).

An ideal SDR receiver architecture is to digitize signal at radio frequency (*RF*). But this ideal receiver is at the moment far from realizable since it is not reasonable to use a single *RF* stage for a multi-band system. This is due to the impossibility of building antennas and low noise amplifiers (LNAs) on a bandwidth ranging from hundreds of megahertz to units or tens of gigahertz. A realizable architecture will be to perform transformation of analogue *RF* signal to digital intermediate frequency (*IF*) signal. The ability to process signals corresponding to a wide range of frequency bands and channel bandwidths is a critical feature of multi-standard radios and impacts heavily on the design of both analogue and digital segments of the receiver.

Digital front-end (DFE) is a term introduced in (Hentschel *et. al.*,1999a). DFE is a hardware platform digitally realizing front-end functionalities that were formerly realized by analog signal processing. The DFE functionalities are channelization and sample rate conversion. The work presented in this paper realizes DFE design to meet the GSM and DECT standards specifications for a wideband multi-standard receiver.

Materials and methods

Design Methodology

This work is done with system level description of the DFE. The Xilinx System Generator 3.1 (XSG) is used to generate VHDL source code from Xilinx Blockset in the Matlab 6.5.1 environment. After simulating the model in Matlab, VHDL code, cores that are design entities of functions, and test vectors for verification help are generated by the XSG accordingly to the user defined system parameters. Using the generated VHDL code, the design flow is further be separated into three steps: simulation, synthesis, and implementation using Xilinx ISE 5.1.

Analog front-end consideration

In this work, the wideband fixed *IF* sub-sampling architecture (Figure 1) is considered because it eliminates the intrinsic disadvantages of the other receiver architectures, like dynamic offset, *RF* leakage and image rejection. The down-conversion of

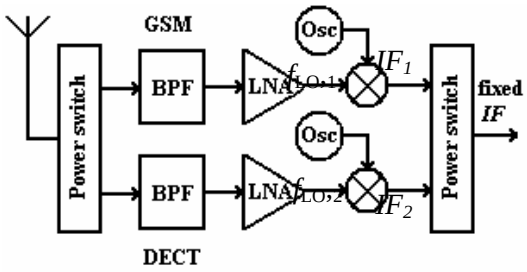

FIGURE 1 Wideband fixed *IF* receiver architecture.

RF signal to *IF* in this architecture can be done in a single stage or dual stage. This architecture also fulfills the SDR requirement by pushing the digitization point one step closer to the antenna, performing sampling at *IF*. In addition, the fixed frequency local oscillator (LO) can be integrated much easier than a tunable LO oscillator used in the other architectures. The following relationship between the sampling frequency, f_s, and the fixed *IF* holds (Karimi *et al.*,1997):

$$f_s = \frac{4}{2D-1} IF \quad D = 1,2,3,\ldots \qquad (1)$$

where *D* represents the integer for the Nyquist zone. The fixed *IF* signal sub-sampling is

performed in the 2nd Nyquist zone, D=2. This is to ensure suitable conditions for the digital signal processing in the baseband signal, giving f_s=4*IF*/3.

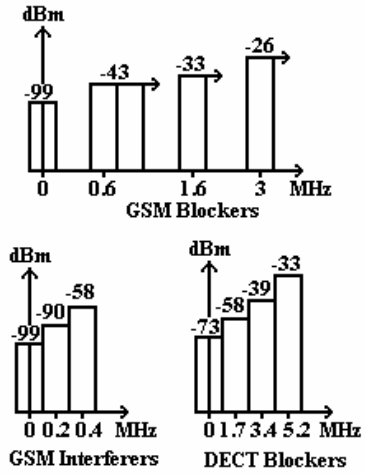

FIGURE 2 Worst case GSM and DECT blockers and interferers specifications.

Table 1 presents design specifications and considerations for GSM and DECT standard. The digitization with over-sampling ratio (OSR) is considered for a 4th order band pass sigma delta modulator (SDM). Using the specified OSR in Table 1, the dynamic range requirement of 98dB for GSM and 85 dB for DECT can be achieved (Ghazel *et al.*,2002). The over- sampling is based on symbol rate of the standards. For DECT, the final output rate will be twice its symbol rate in order to fulfill the Nyquist requirement. Final output of the over-sampled signal must match the required symbol rate or multiple of it.

The DFE must maintain a 10^{-3} bit error rate (BER) at the output of each DSP stage for both standards and this maps to an approximate carrier-to-noise ratio (CNR) of 9dB for GSM and 10.3dB for DECT at each stage output (Ghazel *et al.*,2002). Sensitivity power level is -102dB and -83dB for GSM and DECT respectively (Barrett,1998). Hence, the aliasing noise must maintain a minimum level of -111dB (-102dB-9dB) for GSM and -93.3dB (-83dB-10.3dB) for DECT. This requires all the distortions aliasing in the band of interest in every stage of DFE approach must remain below the sensitivity power level of the desired band of interest by its CNR requirement. To meet noise in signal of interest below the total allowable noise requirement, 24 bits would be needed, assuming 4 bits of accuracy, 2 bits for errors, and 18 bits for bits necessary at the output port to encompass the dynamic range of the filter output.

Digital front-end structure and design

The principal of DFE approach is shown in Figure 3. Quadrature down-conversion and multi-rate filtering are realized based on the channelization and sample rate conversion functionalities.

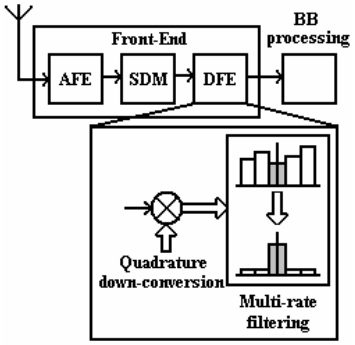

FIGURE 3 Digital front-end approach architecture

Quadrature Down-Conversion

Signal processing is almost always simpler and thus more efficiently performed at baseband. Thus the digitized *IF* signal need to be down-converted to baseband before further DSP. Down-conversion to baseband is a process of channelization with one main advantage compared to analog down-conversion which is the perfect I-Q matching and thus image rejection can be realized. As a result of sampling using equation (1), down-conversion can be done efficiently and more conveniently for signal centered around $3f_s/4$ to obtain in phase (I) and quadrature (Q) components.

TABLE 1 GSM and DECT standards specifications

	CNR (dB)	***IF* (MHz)**	**OSR**	**Symbol rate**	**Channel spacing**	**Peak to peak channel ripple**
GSM	9	13	64	270.833KSPS	100kHz	0.1dB
DECT	10.3	55.296	32	1.152MSPS	800kHz	0.5dB

The conventional and most flexible approach to quadrature down-conversion is to multiply the digitally sampled signal by a complex vector (e.g. numerically controlled oscillator) with periodic bit sequences [0 1 0 -1] and [1 0 -1 0] at f_s, representing sine and cosine carriers, respectively. The usage of multiplier and complex vector oscillator consumes high logic resources and power. Quadrature down-conversion can be efficiently implemented by using multiplexers producing 4 bit output in a sub-sampling architecture as shown in Figure 4, eliminating the use of two multipliers as in the conventional implementation. This approach is hardware and power efficient.

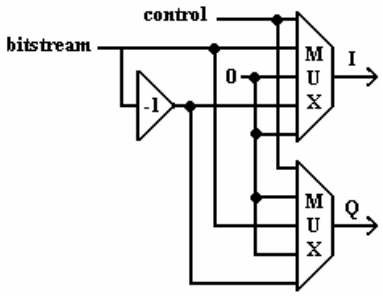

FIGURE 4 I/Q down-conversion implementation architecture.

Multi-rate Filtering

Multi-rate filtering was designed to reduce the number of computation needed to convert a wideband signal with high sampling rate to a single channel with reduced sampling rate. Instead of going straight away from the initial sampling rate to the final one, which can be very computationally expensive, the rate conversion is accomplished by dividing the process into several steps (block sets), with each step producing a different sampling rate from the initial one. The process is resumed until the intended sampling rate and channel bandwidth is achieved while maintaining the required CNR in each stage.

Multi-rate filtering applies channelization functionality to select the channel of interest and sample rate conversion functionality is applied to reduce the OSR to match the symbol rate of the standard. Cascaded comb filter, inverse sinc and generic FIR filters are designed to meet the CNR requirement for the worst case case blocking profile and adjacent channel interferers for GSM and DECT standards as shown in Figure 2 (Ghazel *et al*.,2002).

Comb filter

Comb filter is a very interesting first stage filter since it needs no multiplier. The comb filter is known to be an efficient way to down sample the output signal to four times the Nyquist rate (Candy,1986). This work is based on multiple of the standards symbol rate, so the comb filter is designed to give output with four times the final symbol rate.

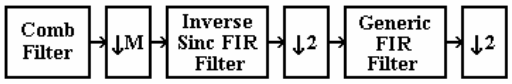

FIGURE 5 Multi-rate filters structure.

Since a band pass sigma delta modulator with order L=4 is considered, a cascade of N=5 (L+1) comb filter is necessary. So, a 5th order comb filter was designed with decimation ratio M=16 for the GSM standard and M=8 for the DECT standard, using equation (2) (Barrett,1998). The filter was designed for input sampled at f_s with differential delay R=1 for the GSM standard and R=2 for the DECT standard. Higher value of differential delay is applied for DECT since its decimation ratio is low because lower decimation ratio with differential delay of one gives lower attenuation.

$$H(z)=\left(\frac{1}{M}\cdot\frac{1-z^{-RM}}{1-z^{-1}}\right)^{N} \qquad (2)$$

According to its transfer function given in equation (2), the comb filter can be efficiently implemented as shown in Figure 6. The magnitude response, H(z), in equation (2) is separated into into integrator, $\left(\frac{1}{1-z^{-1}}\right)^{N}$, and denominator, $(1-z^{-RM})^{N}$, sections by moving

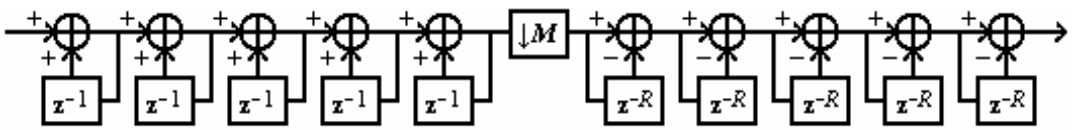

FIGURE 6 Comb filter implementation architecture.

the denominator section after the decimation operation. Hence, the filter can be implemented without multiplier. To avoid overflow problem, a 2's complement wrap-around arithmetic is used as long as the register width (Reg_Width) is greater or equal to value given by equation (3) (Ghazel *et al*.,2002), with B_{in} representing input data width.

$$\text{Reg\_Width} = N\log_2(RM) + B_{in} \qquad (3)$$

But the drawbacks of this filter are insufficient attenuation in stop band and distortion in passband. The stop band insufficient attenuation can be overcome by the attenuation in the follow up filters. To solve the inband attenuation problem, an inverse sinc filter is applied in the second stage of filtering to correct the droop caused by the comb filter.

Inverse sinc and generic FIR filter

The inverse sinc filter has a cubic response of the form $\left(\frac{x}{\sin x}\right)^N$, where N is the comb filter order (Xilinx,2002). This filter compensates the attenuation caused by the comb filter in the inband signal so that this band will be free from distortion. By referring to CNR requirement for the worst case blocking profiles and adjacent channel interferers, the second stage filter is designed by considering the out of band noise centered at the frequency of decimate by two which follows the inverse sinc filter. This is because the Nyquist bandwith surrounding this frequency will alias into the inband signal after decimation occurs. The filter is designed to attenuate out of band noise centered at the decimated frequency to a value below inband signal level by CNR of each standard.

Passband frequency of the inband signal is chosen equal to 82% of channel bandwidth resulting in a filter with 23rd order for GSM and 15th order for DECT. The filter is designed using constrained equiripple algorithm to determine the filter coefficients and does not give sharp cutoff at 100% of channel bandwidth. But, since the main idea of using an inverse sinc filter is to correct the droop in passband and also to attenuate out of band noise centered at the decimated frequency to CNR below inband signal level, this filter is applied. Sharp cutoff frequency of the passband is only considered most in the last stage. For GSM standard, the filter is designed to have passband of 82kHz and a stopband rejection of -60dB. For DECT standard, the filter is designed to have passband of 574kHz and a stop band rejection of -20dB.

For the last stage of filtering, a generic FIR filter is applied with a sharp passband cutoff frequency 82% of the signal channel bandwidth. This filter is designed to push out of band remaining undesired signal and also by considering the out of band noise centered at the frequency of decimate by two for the reason mentioned earlier. The transition band is from 82% to 100% channel bandwidth. When considering band of interest for DECT, only information bandwidth of 1.4MHz is considered as channel bandwidth in (Ghazel,2002), and (Barrett,1998), with passband taken as 82% of the information bandwidth. In this work, the information bandwidth for DECT is taken as 1.6MHz and the passband width is maintained as 82% of 1.4MHz. This will not affect DECT design requirement since 1.6MHz is still within the actual DECT bandwidth, 1.728MHz. This alteration is done to achieve a reduced order FIR filter to meet DECT specification.

The filter is designed using Remez algorithm to determine a 47th order the filter coefficients. By using this sufficient amount of order, a filter with passband frequency of 82kHz and a transition band ranging from 82kHz to 100kHz attenuating at -20dB is obtained for GSM standard. A 31st order filter is used to design the filter for DECT standard with passband frequency of 574kHz and a transition band ranging from 574kHz to 800kHz attenuating at -33.3dB.

For FIR filters in the second and last stage, three FPGA hardware efficient architectures have been envisaged. Two well-known method to save resources implementing DSP functions in FPGA are distributed arithmetic (DA) algorithm and multiply accumulate (MAC) algorithm. In the first solution, a DA FIR filter using Xilinx Core is considered. DA algorithm is a well known method to save resources implementing DSP functions. It performs the multiplication using LUT. The second and third solution is based on MAC engine to compute the sum of products. Using MAC, one implementation is a polyphase

TABLE 2 DFE implementation master clock requirement and FPGA memory usage report

	DFE Implementation FIR filters					
	Polyphase DA		**Polyphase MAC**		**Dual channel MAC**	
	GSM	**DECT**	**GSM**	**DECT**	**GSM**	**DECT**
Master clock (ns)	57.693	13.563	57.693	13.563	28.847	6.781
Memory (Kbytes)	342 744	288 856	256 572	255 096	171 516	169 528

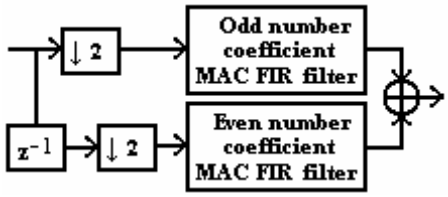

FIGURE 7 Polyphase MAC FIR filter implementation architecture.

MAC FIR filter implementation and the other one is a dual channel MAC FIR filter.

In an FPGA, a MAC type filter will occupy a fixed amount of logic resources for any *K* order of the filter, but will take additional clock cycles for each sample as orders are added. A DA filter runs in the same number of *K* clock cycles regardless of the number of filter order, but requires more logic resources as the filter order is increased.

Results and Discussion

Synthesis

The DFE design synthesis was performed for area constraint. Total memory usage and required master clock of each implementation in a FPGA is presented in Table 2. The target Xilinx FPGA was a Spartan 2E xc2s300e. And the speed grade -7 is chosen in order to achieve the best performance.

The best compromise between logic resources and master clock cycle, for GSM and DECT filters, is obtained with the polyphase MAC FIR filter implementation. The master clock frequency is the same as the input data sample frequency. So, SDM clock generator sharing can be applied in the polyphase MAC based implementation solution. Logic resources saving using MAC implementation are very much higher compared to DA implementation though not as low as the dual channel MAC FIR filter. Dual channel MAC implementation is avoided since it requires higher master clock frequency which consumes more power. In addition to this, high speed processing clock is more prone to violation error in the design due to asynchronous propagation..

Simulation

The input and output spectral results are analyzed in frequency domain using Matlab Simulink. The input from sigma delta modulator for simulation does not provide the required dynamic range for GSM and DECT. Work on SDM to provide ideal dynamic range is beyond the scope of this project so it is ignored. The idea of using SDM spectrum for simulation is only to prove that the filters final output gives the desired channel bandwidth at baseband together with desired sample rate. The effect of filtering based on blockers and interferers to provide required CNR is already considered in the filter design of multi-rate filtering.

After down-conversion, the signal around the 2nd Nyquist zone is split into I and Q phases and brought down to baseband for both GSM and DECT as in Figure 8 and 9 respectively. For GSM, the final output, f_{out}, is sampled at 270.833KSPS with a passband of 82KHz and transition band ranging from 82KHz to 100 KHz. The spectrum analysis in Figure 8 is within the range of $-f_{out}/2$ to $f_{out}/2$ which is -135.417KHz to 135.417KHz. For DECT, final output is sampled at 2.304MSPS with a passband of 574KHz and transition band ranging from 574KHz to 800 KHz. The $-f_{out}/2$ to $f_{out}/2$ range in Figure 9 is from -1.152MHz to 1.152MHz. The final output showing that there is no aliasing from adjacent spectrum and band is free from distortion.

Implementation

The B5-X300 FPGA board is used for hardware implementation and testing. The

clock input signal is generated by the programmable clock generator chip ICS525-01 available in the board. The chip is programmed to provide the required clock frequency, 17.333MHz and 73.728MHz. The FPGA device is tested by providing a constant 1 input using +5V DC power supply connected to the input port. Results observed using the logic analyzer give the required output results the 64 clock cycle and 32 clock cycle gives a time duration of 3692.305ns (270.833KHz) and 434.028ns (2.304MHz). Hence, the final output meet the design requirement. GSM output is 24 bit data sampled at 270.833KSPS and DECT's final 24 bit output data is sampled at 2.304MSPS.

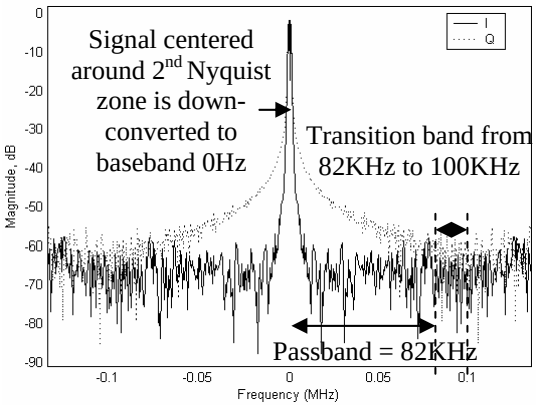

FIGURE 8 Experimental performance of GSM DFE.

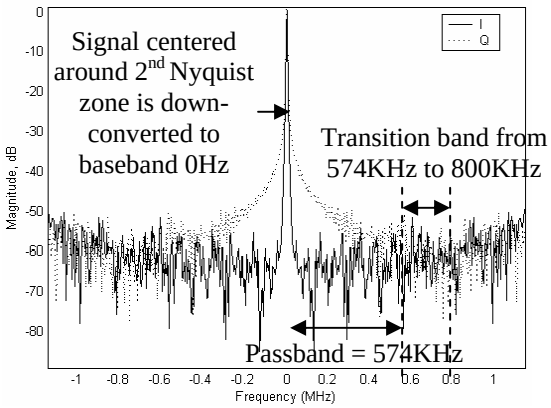

FIGURE 9 Experimental performance of DECT DFE.

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