[ME08] Development of silicon planar P-I-N photodiode

P Susthitha Menon a/p N V Visvanathan, Sahbudin Shaari

Photonics Technology Laboratory (PTL), Institute of Micro Engineering and Nanoelectronics (IMEN), Universiti Kebangsaan Malaysia, 43600 UKM, Bangi, Selangor, Malaysia.

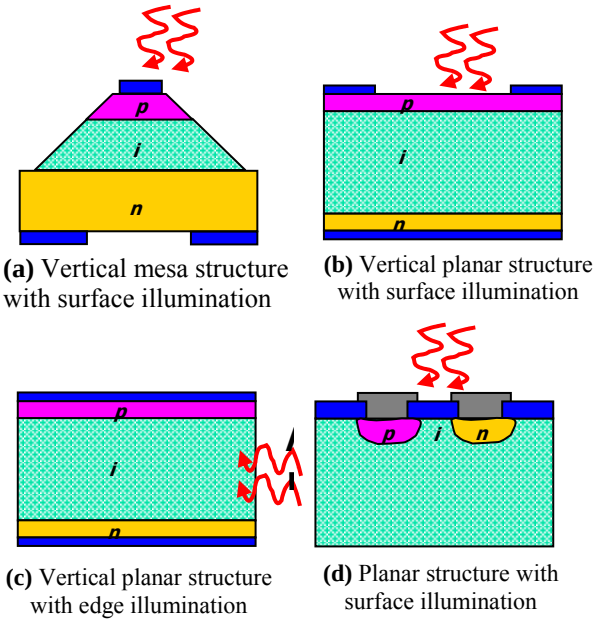
Introduction

Optical receivers are used to detect optical power and to extract the information that is being transmitted. The incident optical power is detected by a photo detector, usually a PIN or avalanche photodiode (APD). A PIN or APD is an amplitude modulation envelope photo detector, insensitive to phase or small changes in wavelength. It generates an electrical output that reproduces the envelope of the received optical signal (Li, 2000). The most widely deployed photodiode for all lightwave applications is the PIN photodiode where its performance and characteristics are well understood and documented (Campbell, 1995).

Silicon PIN photodiodes is still in high demand for applications operating up until the 1100nm wavelength range. The emergence of the *Fast Ethernet* and *Gigabit Ethernet* require the usage of silicon photodiodes operating at a wavelength of 770-860nm. Applications requiring photodiodes in array form are also driving factors towards the development of silicon planar PIN photodiodes which can be fabricated and integrated with ease. The low-cost, high reliability and established manufacturability process make silicon an attractive material for the fabrication of a planar PIN photodiode (Li, 2000). The success in the development of silicon based PIN photodiodes provides a stepping stone towards the development of PIN photodiodes using III-V materials such as GaAs, InGaAs and InGaAsP.

PIN Photodiode Structures

The structure of PIN photodiodes can be classified based on the location of the *p, i* and *n* regions arranged either vertically or in the same plane. A planar PIN photodiode is created in such a way that the *p, i* and *n* regions are all in one plane. Optical power is illuminated via the surface or the edge of the device. Figure 1(a)-(d) shows various structures of the PIN photodiode. The planar PIN photodiode (PD) has profound advantages compared to the vertical surface/edge illuminated PIN photodiode. Costly epitaxial layers are needed to form the *p, i* and *n* regions in a vertical structure using fabrication techniques such as MOCVD (*metalorganic chemical vapor deposition*) and MBE (*molecular beam epitaxy*). However, the planar PIN photodiode can be fabricated easily using standard CMOS processing techniques where the *p* and *n* regions are doped unto the substrate wafer using either diffusion or ion implantation techniques (Ehsan *et al*., 2001).



(a) Vertical mesa structure with surface illumination

(b) Vertical planar structure with surface illumination

(c) Vertical planar structure with edge illumination

(d) Planar structure with surface illumination

FIGURE 1 PIN photodiode structures

Theory

The current-voltage characteristic of a PIN photodiode with no incident light is similar to a rectifying diode. When the PIN photodiode is forward biased, as usual there is an exponential increase in the current. When a reverse bias is applied, a small reverse saturation current appears. It is related to the dark current as:

$$I_D = I_{SAT}(e^{\frac{qV_A}{k_BT}} - 1) \qquad (1)$$

where I_D is the PIN photodiode dark current, I_{SAT} is the reverse saturation current, q is the electron charge, V_A is the applied bias voltage, k_B=1.38 x 10^{-23} J/^{o}K, is the Boltzman Constant and T is the absolute temperature (273^{o}K=0^{o}C). Illuminating the photodiode with optical radiation, shifts the I-V curve by the amount of photocurrent (I_P). Thus:

$$I_{TOTAL} = I_{SAT}(e^{\frac{qV_A}{k_BT}} - 1) + I_P \qquad (2)$$

where I_P is defined as the photocurrent as in equation 2. As the applied reverse bias increases, there is a sharp increase in the photodiode current. The applied reverse bias at this point is referred to as breakdown voltage. This is the maximum applied reverse bias, below which, the photodiode should be operated (also known as maximum reverse voltage).

The internal quantum efficiency for a photodiode is defined as the number of hole-electron pairs generated per photon. The external quantum efficiency is defined as the ratio of generated carriers to the number of incident photons within the device taking into consideration optical loss due to surface reflections, electrode shadowing and other geometrical characteristics. The external quantum efficiency is given by equation 3 .

$$\eta = (1 - R) \cdot (1 - e^{-\alpha d}) \qquad (3)$$

where d is the thickness of the absorption region, R is the reflectivity at the air-semiconductor interface. The total quantum efficiency is obtained by multiplying the internal and external quantum efficiencies respectively.

The responsivity of a photodiode is the ratio of generated electrical current to the incident optical power and is defined in terms of the device's external quantum efficiency. This is given by equation 4.

$$R = \frac{I_{opt}}{P_{opt}} = \left(\frac{q}{h\nu}\right)\eta_{ext} \quad [\text{A/W}] \qquad (4)$$

The RC time constant for a photodiode is given by equation 5.

$$\tau_{RC} = \frac{1}{C_J(R_S + R_L)} \qquad (5)$$

where C_J is the junction capacitance, R_S is the series resistance and R_L is the load resistance. The bandwidth is defined as:

$$f_{3dB} = \frac{1}{2\pi\tau_{RC}} \qquad (6)$$

Materials and Methods

Simulation

The silicon planar PIN photodiode device modeling and simulation was performed using Silvaco ATHENA and ATLAS simulation softwares from Silvaco Incorporated. ATHENA simulates semiconductor material processes based on two-dimensional physical structures built into a defined grid format and ATLAS solves differential equations derived from the Maxwell laws in each node of the grid in order to obtain electrical and optical characteristics of the device. Silicon with resistivity of 1000 ohms/cm^2 and <100> orientation was used as the substrate material. An oxide layer of 0.6μm thickness was deposited for masking purposes. Next, successive etch steps followed by diffusion were used to define the p^+ and n^+ wells. The p^+ wells were formed by diffusing Boron for 120 minutes with a temperature of 1200^o Celsius and a dose of 8.19 x 10^{20} cm^{-3}. The n^+ wells were formed by diffusing Phosphorous for 50 minutes with a temperature of 1000^o Celsius and a dose of 2.02 x 10^{20} cm^{-3}. After the oxide-etching step, Aluminum with thickness of 3μm was deposited and etched to form electrodes; anode (p^+ well) and cathode (n^+ well). The simulated device has an intrinsic region width, d varying from 0.5mm to 2mm with p^+/n^+ well widths of 0.5mm.

Fabrication

Fabrication of the device involves 28 steps. Each prototype contains four devices with different intrinsic region widths ie 0.5mm, 1mm, 1.5mm and 2mm. The device photomask was designed using AutoCAD and Adobe Illustrator software and the structure was transferred to negative and positive polymer plates coated with chromium by an outsource vendor. The photolithography process in the fabrication of the device involves 5 photomasks ie the alignment mark, p+ well window, n+ well window, metal contact wind.

N-type <100> silicon with resistivity of 1-1000 ohms/cm^2 and bulk concentration of 3.64 x 10^{10} /cm^3 was used as the substrate material. Upon substrate cleaning the first photolithography was performed to transfer the alignment mark onto the substrate material using positive photoresist AZ 1500 from Clarient. A standard first spin speed of 800 rpm for 5 seconds and second spin speed of 4000 rpm for 30 seconds followed by softbake at 100 ^{0}C for 50 seconds was used to obtain a resist thickness of 0.5 µm.

Dash etchant solution was used to obtain a permanent marker on the substrate. After the etching and cleaning processes, dry oxidation using N_2 at 95 sccm and O_2 at 95 sccm for 240 minutes at 1200 ^{0}C was performed in order to obtain a diffusion masking oxide layer of 0.33µm. The second photolithography was carried out to obtain the p+ well openings. Spin-on diffusion technique using Boron B155 SOD from Filmtronics USA was utilized. Pre-diffusion first spin speed was at 400 rpm for 5 seconds and second spin speed was at 4000 rpm for 60 seconds. Next, hardbake at 200^{0}C for 20 minutes was followed by drive-in at 1200 ^{0}C for 120 minutes.

Subsequent etching and oxidation processes is followed by the third photolithography to create n+ wells using P509 SOD from Filmtronics USA. Pre-diffusion first spin speed was at 400 rpm for 5 seconds and second spin speed was at 4000 rpm for 60 seconds. Next, hardbake at 200^{0}C for 20 minutes was followed by drive-in at 1000 ^{0}C for 50 minutes. The fourth photolithography was carried out to create metal openings and lastly the *metal lift-off* technique was utilized after the fifth photolithography process to obtain metal contacts on the device. Thermal evaporation furnace using e-gun was used to deposit Al for 45 seconds in order to obtain a metal layer thickness of 700 – 1200 Å. Annealing at 500 ^{0}C for 15 minutes was performed in a dry oxidation furnace with the flow of nitrogen gas N_2 at 2000 ml/min. Finally the device was cut and polished at the edges to allow for lateral illumination.

Characterization

The prototype was characterized for dark/photo I-V and responsivity utilizing the smart semi-automatic probing system from Signatone and also *Metrics Interactive Characterization Software (ICS)* Version 3.5.0 at IMEN. The device was placed on a probing table while dark/photo I-V data was collected. Photo I-V data was obtained by illuminating the top of the device with red light (λ= 612nm) with three different optical powers; 0.2mW, 0.3mW and 0.5mW .

Results

Simulation Results

The current-voltage (IV), total quantum efficiency, responsivity, rise time and frequency response characteristics of the devices were simulated. The simulated structure for d=0.5mm is shown in Figure 2. The anode junction depth was at 11.2 µm, p+ sheet resistance was 0.68 ohm/square (at X.value=750), intrinsic region sheet resistance was 1706.24 ohm/square(at X.value=1250) and n+ sheet resistance was at 12.62 ohm/square(at X.value=1750).

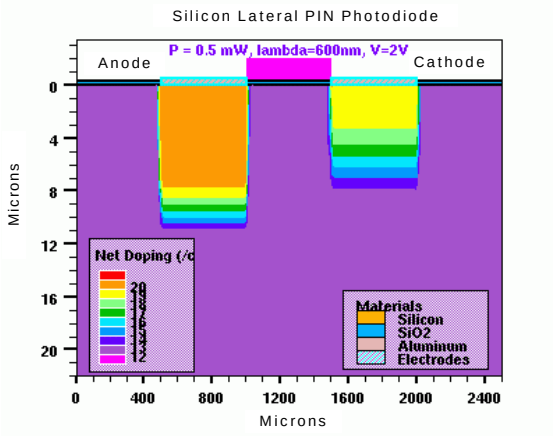


FIGURE 2 Si Planar PIN Photodiode (d=0.5mm) illuminated by optical beam

Figure 3(a)-(d) shows the reverse dark and photo I-V curves of the device for different intrinsic region widths. The breakdown voltage of –500V with equivalent dark current of 45.7pA was obtained for all the devices with different intrinsic region widths. Ideality factor of n=1, high dynamic resistance, (R_s= 10^6 Ω) and shunt resistances (R_D=10^{11} Ω) indicate that a ideal diode has been simulated. Illumination of the device with an optical spot power of P=0.5mW(V=-10V) generated an increased photocurrent in the devices (I_p=0.038mA). Increment in the incident optical power to P=2.5mW (I_p=0.164mA) and P=5mW (I_p=0.314mA) increased the

photocurrent as well respectively. However, devices with a larger intrinsic region width showed lesser photocurrent increment for a fixed optical power intensity.

The total quantum efficiency, η of the devices peaked at a wavelength of 200nm at 10.2% for d=0.5mm, 5.13% for d=1mm, 3.41% for d=1.5mm and 2.54% for d=2mm where

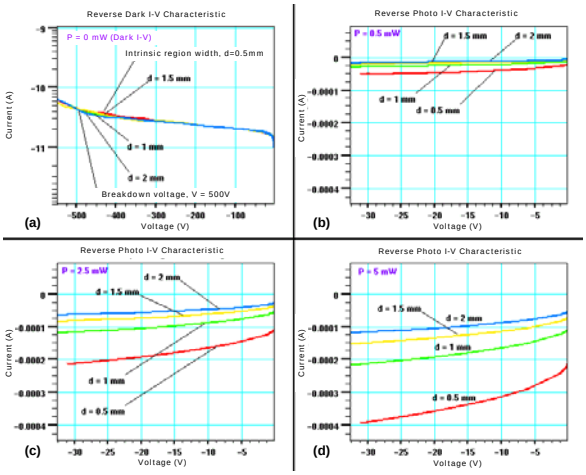


FIGURE 3 Reverse dark and Photo I-V curves for devices with different intrinsic region widths and incident optical power (a) dark, (b) P=0.5mW, (c) P=2.5mW and (d) P=5 mW.

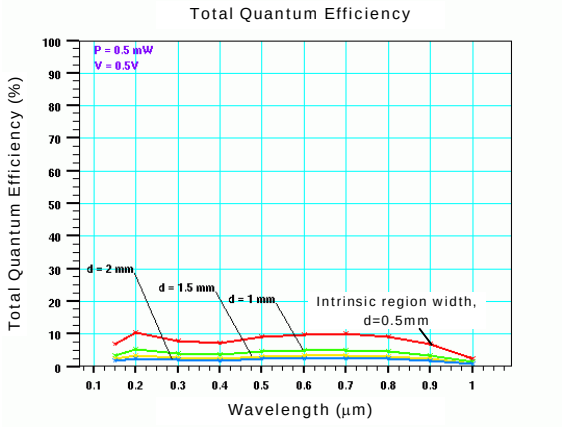


FIGURE 4 Total quantum efficiency for different intrinsic region widths.

increment in the intrinsic region width reduced the total quantum efficiency. The incident optical power was 0.5mW and applied reverse bias of 0.5V. This is shown in Figure 4.

The responsivity curves are exhibited in Figure 5. The wavelength of the optical spot power was increased gradually from 150nm till 1000nm and responsivity values at each wavelength was extracted. The highest responsivity of 0.059 A/W at λ=800nm was achieved for the PIN photodiode device with d=0.5mm. When the intrinsic region width is increased, the responsivity of the device decreased. This is due to the reduction in the generated photocurrent as a result of decreased electric field strength between electrodes which are placed further apart.

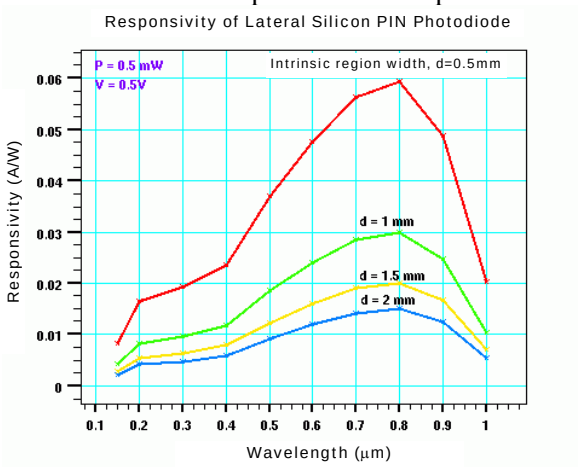


FIGURE 5 Responsivity of the devices with different intrinsic region widths

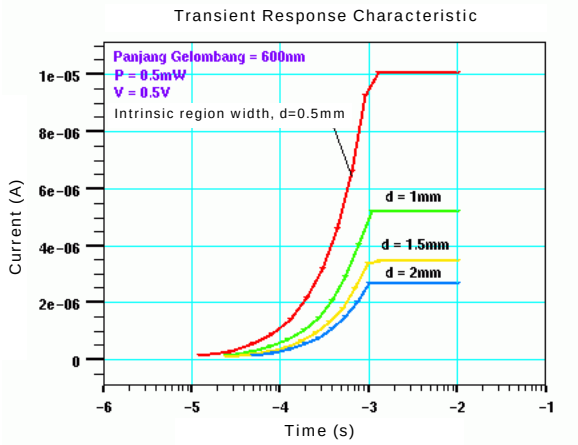


FIGURE 6 Rise time of the devices with different intrinsic region widths

Fig 6 and Fig 7 shows the rise time and frequency response of the devices respectively with the same optical spot power (P=0.5mW) and reverse bias voltage (0.5V). Referring to Fig 7, the planar PIN photodiode with intrinsic region width of d=0.5mm shows the fastest rise time of 0.66ms which is equivalent to a bandwidth of 0.5kHz. The graph clearly shows a decrease in the final available photocurrent in the device when the intrinsic region width is increased. Rise time values calculated from values taken from the graph indicates an increase in the rise time when intrinsic region width is increased. This is because the electrons and holes formed in a wider intrinsic region need to travel further in

order to reach the electrodes. Fig 8 shows the frequency response of the planar PIN photodiode devices. The frequency response of the devices with larger intrinsic region width is lower. The rise time and frequency response of the devices are shown in Table 1.

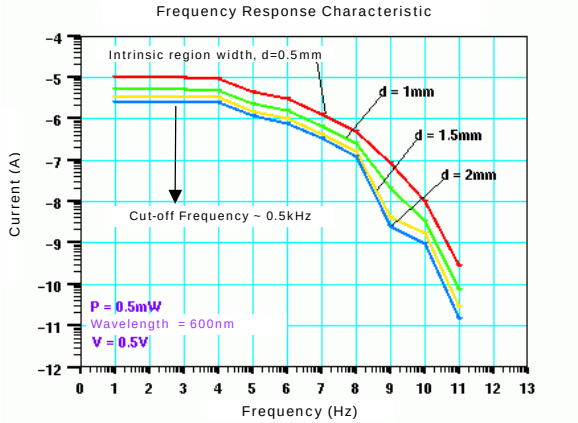


FIGURE 7 Frequency response of photodiode devices with different intrinsic region widths

TABLE 1 Rise time and frequency response values of PIN photodiode devices with different intrinsic region widths

Intrinsic Region Width (mm)	**Rise Time, t_r ($t_{90\%}$ - $t_{10\%}$) (s)**	**f_{3dB} (0.35/ t_r) (Hz)**
0.5	6.6189×10^{-4}	528
1	7.0548×10^{-4}	498
1.5	7.2468×10^{-4}	482
2	7.7554×10^{-4}	451

Fabrication Results

Figure 8 shows the photomasks that were used and Figure 9 shows the fabricated device. Each prototype contains 4 devices each with different intrinsic region widths ie d=0.5mm, 1mm, 1.5mm and 2mm. The junction depth obtained for the p+ and n+ wells were 1.09µm and 1.61µm respectively. Bulk dopant concentration for the p+ and n+ wells were 8.19 x 10^{20}/cm^3 and 2.02 x 10^{20}/cm^3 respectively. The measured resistivity was 2.02 ohms/cm^2 and 5.07 ohms/cm^2 for the p+ and n+ wells respectively.

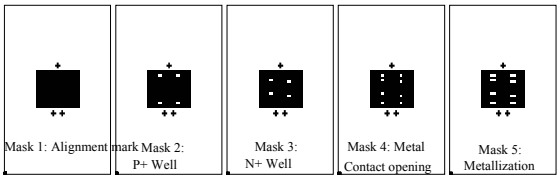


FIGURE 8 Device photomasks

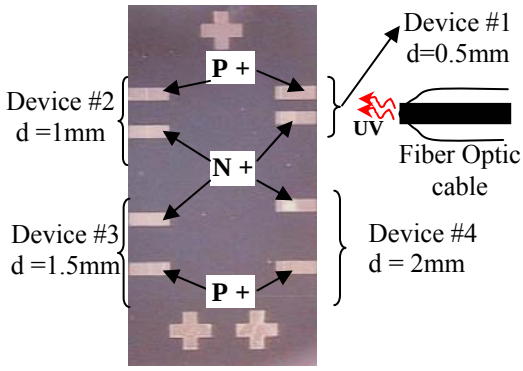


FIGURE 9 Fabricated PIN photodiode

Characterization Results

Figure 10 shows the reverse bias dark I-V data for all the four PIN photodiode devices. The trend is consistent with the trend obtained via simulation where increment in reverse bias current is observed when intrinsic region width is increased.

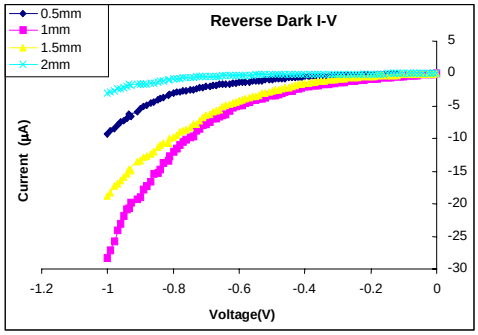


FIGURE 10 Reverse bias dark I-V

However, the breakdown voltage is extremely low at 0.8V at a reverse bias current of 0.77µA for device with d=2mm. Ideality factor approaching value of n=2, low dynamic resistance R_s in the range of 167-868 Ω and low shunt resistance, R_D=0.2-14 MΩ indicate the existence of generation-recombination currents in the prototype due to carrier tunneling through the intrinsic region.

When the device is illuminated with three different optical powers (λ= 612nm, V=-0.2V); P=0.2mW, 0.3mW and 0.5mW, there is only slight increment in the device photocurrent as shown in Figure 11 where I_p is 0.159µA, 13.4µA and 23.5µA respectively (for device with d=0.5mm). This is equivalent to a responsivity of 0.001A/W (η=0.16%), 0.044A/W (η=9.05%) and 0.047A/W (η=9.52%) respectively. The small

photocurrent is due to the high leakage current in the device.

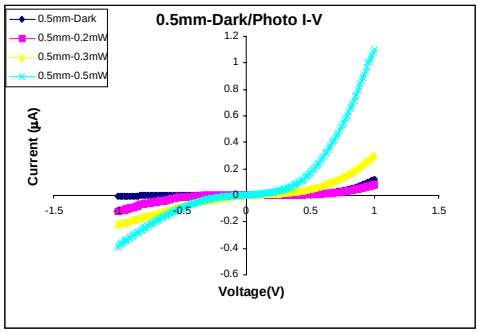


FIGURE 11 Dark/Photo I-V curve(d=0.5mm)

Discussion

A silicon planar PIN photodiode was successfully modeled and simulated using Silvaco Athena and Atlas software. Intrinsic region width of the device was varied and the effect on device characteristics were analysed. Based on the obtained data, when intrinsic region width is increased, there is a decrease in the generated photocurrent, total quantum efficiency and responsivity. The device rise time increases and thus the bandwidth is reduced significantly. Prototypes of the simulated devices were fabricated using standard CMOS technology. Low breakdown voltage as well as ideality factor approaching a factor of 2 indicates the presence of leakage current in the device. High dopant concentration measurements in the intrinsic region of the device indicated that impurities have been deposited either due to insufficient substrate cleaning or thin oxide diffusion masking layer. Further investigation is required to identify the exact rootcause.

Acknowledgements

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