[ME04] FPGA implementation of multi frequency continuous phase frequency shift keying (MCPFSK) modulation techniques for HF data communication

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Introduction

In HF (High Frequency) data communication systems [1,2], FSK (Frequency Shift Keying) digital modulation is widely used. The simplicity in the implementation is the main reason for its popularity. Since noncoherent detection is possible, additional components such as timing recovery circuits [3] are not necessary as required in PSK (Phase Shift Keying) modulation. In addition, FSK is robust to noise and phase synchronization error that present in a HF communication environment (ie. multipath fading)[4]. Existing implementation utilized DSP processor [1,2]. The use of hardware based design such as FPGA (Field Programmable Gate Array) can further miniaturize system size and add more features into existing systems. The importance of FPGAs in communication system application is described in[5,6]. This paper describes the implementation of a MCPFSK (Multi frequency Continuous Phase FSK) modem on the FLEX10K board EPF10K70RC240. Both transmitter and receiver modules are integrated into a single FPGA. This is achieved by adopting a multiplierless and parallel algorithm at the receiver module. Comparisons with conventional filtering or FFT detection techniques demonstrate significant reduction in components besides increasing the transmission rates.

Signal Model

A received signal within a bit-duration is given as

$$y(t) = x(t) + w(t) \qquad (1)$$

where $x(t)$ is the true signal, and $w(t)$ is the interference due to additive white Gaussian noise with zero mean and power σ_p^2. The true signal $x(t)$ is [7] generated by using multi frequency modulation where one baud or symbol will represent more than a bit. M frequencies are used to transmit n combination of bits that can be calculated as $M = 2^n$ [7]. For this project, 16 frequencies are used for a combination of 4 bit binary data per symbol. By using this method, the bit rate increases to 4 times of the baud rate.

For simulation purposes, the modulation parameters of the signal are as follows: subcarrier frequencies f_c at 1800Hz, frequency deviation f_{dev} at 100 Hz, bit-rate of 100 bits/sec and sampling frequency of 8000 Hz. The time and frequency domain representation of the signal for transmitting a character sequence '12345678' is shown in Fig. 4 and 5 with different index modulation.

A. Generation Of CPFSK

A conventional FSK signal can be expressed as

$$\begin{aligned} x(t) &= \cos 2\pi \left(f_c \pm f_{dev}\right)t \\ &= \cos 2\pi \left(f_c + \frac{h}{2T_b}\right)t \\ &= \cos\left(2\pi f_c t + \frac{\pi h}{T_b}t\right) \end{aligned} \qquad (2)$$

where h is the modulation index, f_{dev} is the deviation frequency, f_c is the center frequency and T_b is the baud duration. By assuming that $\varphi(t) = \pi h t / T_b$ Equation (2) can be derived as

$$\begin{aligned} x(t) &= \cos\left(2\pi f_c t \pm \varphi(t)\right) \\ &= \frac{1}{2}\cos\left(2\pi f_c t\right)\cos\left(\pm\varphi(t)\right) \\ &\quad - \frac{1}{2}\sin\left(2\pi f_c t\right)\sin\left(\pm\varphi(t)\right) \end{aligned}$$

$$= \frac{1}{2}\cos(2\pi f_c t)\cos(\varphi(t)) \mp \frac{1}{2}\sin(2\pi f_c t)\sin(\varphi(t)) \quad (3)$$

From Equation (3), a CPFSK signal can be produced by using 4 different signals with 2 frequencies. Consider f_c=1900Hz, h= 4 and T_b=1/100. The carrier frequency and modulation index derived from the modulation parameters in section 2.0 are

$$f_c = f_1 - f_0/2 = 1900$$

$$h = 2T_b f_{dev} = 2(1/100)(2000-1800)/2 = 2 \quad (4)$$

B. Multi Frequency CPFSK (MCPFSK)

Multi frequency modulation is an advanced modulation technique, allowing the increase of bit transmission rate of communication system without changing the baud rate. The combination of bit are organized in gray code and $x(t)$ is considered as the generated MCPFSK signal.

$$x(t) = \frac{1}{2}\cos(2\pi f_c t)\cos(\varphi_{dev}\varphi(t)) \mp \frac{1}{2}\sin(2\pi f_c t)\sin(\varphi_{dev}\varphi(t)) \quad (5)$$

where φ_{dev} is an integer number and depends on the amount of combination bit that will be used, and $\varphi(t) = 2\pi f_{dev} t$. φ_{dev} is an odd number that appears until $M = 2^n$. For this project, value of φ_{dev} is 15,13,11,9,7,5,3, and 1. Phase can be calculated as $\varphi_{dev} * 2\pi f_{dev} T_b$ with consideration that $f_{dev} = 100$, T_b =1/100, and f_c =1900 for this project.

C. Detection of CPFSK

In FSK modulation, the binary information is represented in frequency mode. This information can be extracted by calculating the power spectrum of the signal in frequency domain. The peaks of the power spectrum occur at the frequency of the signal. Spectrum based detection [9] utilizes the concept of the power spectrum. The BER (bit-error rate) performance is slightly lower than that of coherent detection but phase synchronization is not critical in spectrum based detection. The power spectrum can be expressed as

$$S_{XX}(f) = \frac{1}{T_b}|X(f)|^2 = \frac{1}{T_b}\left|\int_{t_0}^{t_0+T_b} x(t)b^*(t,f)\,dt\right|^2 \quad (6)$$

where $x(t)$ is the signal and $b(t,f)$ is the basis function. If a complex sinusoid is used as basis function, the resulting spectrum is the Fourier spectrum. The basis function based on the complex square wave defined within a period $T=1/f$ is

$$b(t,f) = 1 \quad -\frac{1}{4f} \le t \le \frac{1}{4f} \quad (7)$$
$$= -1 \quad \frac{1}{4f} \le |t| \le \frac{1}{2f}$$
$$= j1 \quad 0 \le t \le \frac{1}{2f}$$
$$= -j1 \quad -\frac{1}{2f} \le t \le 0$$

The square wave basis function is chosen to eliminate multiplication in the hardware implementation.

D. Detection of MCPFSK

For detecting 16 frequencies, the same sub module for detecting FSK signal is used. Instead of detecting 2 frequencies, 16 sub modules are designed in parallel to detect 16 frequencies. In multi-frequency modulation, each frequency of each symbol will have a different probability of error. Data bits are generated by using gray code, to minimize to only one bit error for each symbol. The probability of symbol error is the summation of each frequency's probability shown as

$$P_e = \frac{(16-1)}{16/2}\left(\frac{1}{2}\exp\left[-\frac{A^2}{2N_p}\right]\right) = \frac{15}{8}\left(\frac{1}{2}\exp\left[-\frac{A^2}{2N_p}\right]\right) \quad (8)$$

For the general case, the probability of symbol error for multi-frequency FSK can be expressed as

$$P_e = \frac{(M-1)}{M/2}P_{BFSK} \quad (9)$$

Implementation Methodology

The designed system is divided into 2 major parts, which is the transmitter and receiver part. Before the hardware of the

system is designed, each method is generated and tested using MATLAB.

A. Transmitter

The transmitter is designed using digital recursive generator, which is a multiplier based modulator. For this project, multi frequency CPFSK signal is generated at the modulator. Consider x(n) the generated CPFSK and can be expressed as

$$x(t) = \frac{1}{2}\cos\left(2\pi f_c t\right)\cos\left(\varphi(t)\right) \mp \frac{1}{2}\sin\left(2\pi f_c t\right)\sin\left(\varphi(t)\right)$$
$$= \frac{1}{2}\cos A\cos B \mp \frac{1}{2}\sin A\sin B \quad (10)$$

From equation (10), there are 4 different signals that should be generated to produce CPFSK. A Coupled standard quadrature oscillator structure can be used to generate sinusoidal A and B frequencies. This structure is chosen because it features both quadrature and equi-amplitude outputs. However, this oscillator requires four multipliers per iteration. A serial coupled standard quadrature oscillator structure is used to implement complex sinusoidal and CPFSK signal, which limits the used of only one multiplier in the system.

A coupled standard quadrature oscillator is capable of generating both sine and cosine wave which have same frequency simultaneously. Let $s_1[n]$ and $s_2[n]$ denote the two outputs of the generator given by

$$s_1[n] = \alpha\sin\left(n\theta\right)$$
$$s_2[n] = \beta\cos\left(n\theta\right) \quad (11)$$

Equation (11) can be expressed as equation (12) and (13) for $n=n+1$ and is used in the chosen oscillator structure.

$$s_1[n+1] = \alpha\sin\left((n+1)\theta\right)$$
$$= \alpha\sin\left(n\theta\right)\cos\theta + \alpha\cos\left(n\theta\right)\sin\theta \quad (12)$$
$$= \cos\theta s_1[n] + \alpha/\beta\sin\theta s_2[n]$$

$$s_2[n+1] = \alpha\cos\left((n+1)\theta\right)$$
$$= \beta\cos\left(n\theta\right)\cos\theta - \beta\sin\left(n\theta\right)\sin\theta \quad (13)$$
$$= \cos\theta s_2[n] - \beta/\alpha\sin\theta s_1[n]$$

The only difference between CPFSK and multi frequency CPFSK is the value of B, which is the frequency deviation value. Instead of 1 value in CPFSK, multi frequency CPFSK has 8 values and this value is stored in a buffer and is selected by using multiplexer according to bits transmission.

```
// pseudo code to generate MCPFSK signal
for ( n=0;n<nbit;n++)
{   // generate cosA & sinA
    SinA1=SinθA X CosA(n)
          SinA2=CosθA X sinA(n)
          SinA(n+1)=SinA1 + SinA2

          CosA1(n+1)=CosθA X cosA(n)
          CosA2(n+1)=sinθA X sinA(n)
          CosA(n+1)=cosA1- cosA2

   // generate cosB & sinB
          SinB1=SinθB X CosB(n)
          SinB2=CosθB X sinB(n)
          SinB(n+1)=SinB1 + SinB2

          CosB1(n+1)=CosθB X cosB(n)
          CosB2(n+1)=sinBA X sinB(n)
          CosB(n+1)=cosB1- cosB2


   //x[n]=1/2*cosA*cosB(+-)1/2*sinAsinB

   mult1=1/2 *cosA[n]*cosB[n];
   add3=mult1;
   mult1=1/2 *sinA[n]*sinB[n];
   x[n]=add3 ± mult1;
  //add/sub depends on generating the MSB bit
'1/0'
}
```

FIGURE 1 Pseudo code to generate MCPFSK signal.

B. Receiver

A square wave detector is designed and implemented as the receiver system to optimize implementation of hardware (such as using ASIC and FPGA) by avoiding the use of multipliers. A multiplier is required to calculate the signal-basis function product $x(t)b^*(t,f)$ in Equation (13). If the complex square wave is used as a basic function, then the multiplication function can be done by replacing the multiplier with a sign check and compliment module. The overall system is generated based on the pseudo code shows in Fig. 2.

```
// pseudo code to detection of MCPFSK;

   // freq[n,M] is basis function for each frequency
   // x[n] is input

for ( M=1;M<16,M++)
{
// for one bit sample
sum0=0;
sum1=0;
detect_bit=0;

for ( n=0;n<Nsample,n++)
  {
   if (freq[n,M]=1)
      { if ( x[n]>0)
          { sum[M]= sum[M] + x[n];}
            else  if ( x[n]<0)
                 { sum[M]= sum[M] - x[n];} }

  }

if (sum[M]>sum[M-1] )
     { detect_bit=M;}
     else detect_bit=detectbit;}
}
```

FIGURE 2 Pseudo code to generate parallel multi frequency square wave detection.

Results

There are several ways of designing multi frequency detectors such as filtering for noncoherent detection or using FFT module. Coherent structure is not considered in this project because of the complexity in designing its timing recovery circuit due to the nature of HF channel. Figure 3 shows the MATLAB simulation performance for different types of detectors and shows that a square wave detection performs with better results than using FIR filters in terms of BER performance. Table I lists the simulation results from MAXPLUS II tools for MCPFSK design, which is includes the startbit detection module for data synchronization and CRC16 for error detection. For comparison purposes, data from ALTERA megacore function for FFT and FIR filter module is used. From collected data, the FIR filter is not a good choice in terms of design area and speed performance to implement 16 CPFSK, where 16 filters is needed to detect 16 frequency simultaneously. FFT technique is much more reasonable for detection of 16 frequencies. Data from TABLE I and TABLE II shows that FFT module uses double the amount of logic cells than the proposed technique not including the RAM block for multiplier design.

The proposed technique has better performance in terms of BER and size of implementation design. It is also proposed for MSK modulation, which use the minimum frequency deviation. For noncoherent detection, a filter with larger length is required to implement MSK detection. But, with this proposed technique, no extra component is needed. Figure 5 shows the generated signal from modulator and have been used as input for the demodulator for index modulation, h= ½, which is a MSK signal.

TABLE I List of components for MCPFSK modulation technique for HF data transmission.

Module	Input Pin	Output Pin	Bidirection Pin	Memory		Chip size	
				Bit's	Utilized	LC's	Utilized
Modulator	6	46	16	128	0%	1578	42%
a)CPFSK	13	30				1001	26%
b)serialop(UART)	28	43				268	7%
c)CRC	12	20				98	2%
Demodulator	6	56	16	384	2%	3121	83%
a)Startbit	12	19				315	
b)square wave detection	16	22	256	256	1%	2275	60%
c)CRC	12	20				98	
d)serialop(UART)	28	43				268	7%
Modulator and demodulator(without UART)	64	117	16	384	2%	3583	96%

TABLE II List of streaming data flow performance and device utilization for the FFT MegaCore function in Stratix II devices.

Table 1: Streaming Architecture Performance and Device Utilization for Stratix II Devices

Device	Points	Width (1)	Logic Elements (LEs) (2)	18 * 18 Mults	M4K blocks used (3)	M-RAM blocks used	fMAX (MHz)	Clock Cycle Count	Transform Time (µs)
EP2S15F484C3	256	16	4,561	9	19	0	314.27	256	0.82
EP2S15F484C3	512	16	4,936	9	19	0	317.36	512	1.61
EP2S15F484C3	1,024	16	5,213	9	38	0	311.53	1,024	3.29
EP2S15F484C3	2,048	16	7,266	18	75/44	0/2	295.96	2,048	6.92
EP2S30F484C3	4,096	16	7,649	18	144/88	0/2	281.55	4,096	14.55
EP2S60F484C3	8,192	16	7,525	18	304/176	0/2	272.85	8,192	30.02

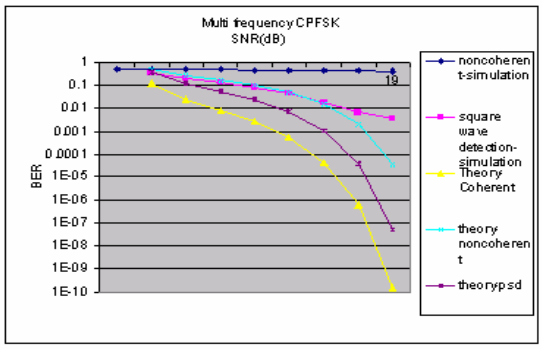
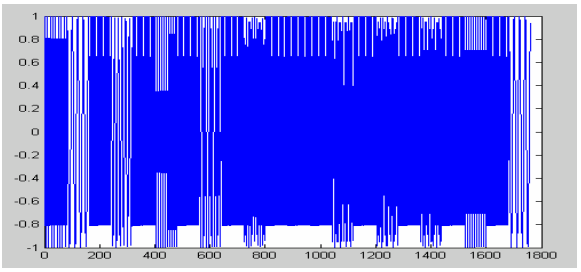


FIGURE 3 Probability of error for MCPFSK signal with different type of detection.



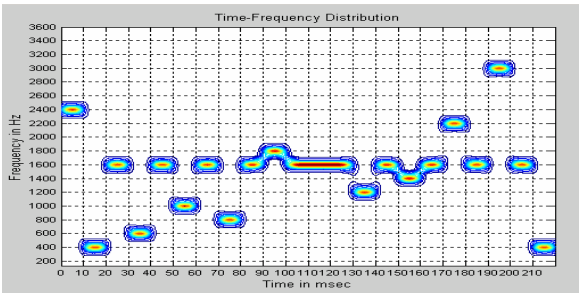
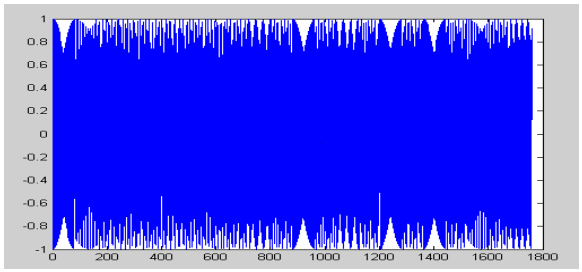


FIGURE 4 Time and frequency distribution for MCPFSK for index modulation,h=4.

Conclusion

This paper describes the design of an MCPFSK modem on FPGA. The hardware approach is adopted with the objective to miniaturize system size. The design module is compared to FFT and FIR ALTERA modules. The square wave detector has 50% less logic component because no multiplier is used in the algorithm. Thus, the modem designed with the square wave detectors can be made smaller. Besides that, it can also be used for MSK detection.



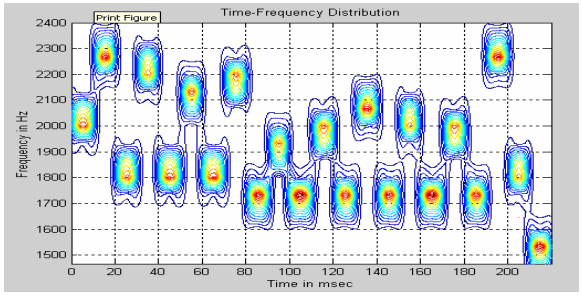


FIGURE 5 Time and frequency distribution for MCPFSK for index modulation,h=1/2.

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