# CREEP AND ISOTHERMAL FATIGUE BEHAVIOUR OF EUTECTIC SnPb, SnBi and SnZn SOLDERS FOR MICROELECTRONIC PACKAGING AT MILDLY ELEVATED TEMPERATURES

by

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# NOMENCLATURE

| | Symbol | unit |
|---|---|---|
| Coefficient of thermal expansion | $\alpha$ | ppm |
| Thermal conductivity | $\kappa$ | $Wm\ ^{o}K^{-1}$ |
| Surface tension | $\Gamma$ | $mNm^{-1}$ |
| Resistivity | $\Re$ | $\Omega$.cm |
| Modulus of elasticity | E | GPa |
| Tensile strength | | $Nm^{-2}$ |
| Strain rate | $\dot{\varepsilon}$ | $s^{-1}$ |
| Activation energy | Q | $KJ\ mol^{-1}$ |
| Boltzmann Constant | k | $Cal\ ^{o}K^{-1}$ |
| Temperature | T | $^{o}K$ |
| Stress exponent | n | |
| Burger vector | b | |
| Grain size | d | Å |
| Applied stress | $\tau$ | $Nm^{-2}$ |
| Shear modulus | G | $Nm^{-2}$ |
| Maximum applied stress | $P_{max}$ | MPa |
| Difference between fatigue and creep lifetime | $\Delta t_{sp}$ | s |
| Number of cycles to failure | $N_f$ | |
| Stress amplitude | $\sigma_f$ | $Nm^{-2}$ |
| Plastic strain range | $\Delta\varepsilon_p$ | |

| | | |
|---|---|---|
| Frequency of loading | f | Hz |
| Cycle per minute | CPM | |
| Ratio of minimum applied load to maximum applied load, $L_{min} / L_{max}$ | R | |

# PUBLICATIONS FOR CONFERENCES AND REFERRED JOURNALS

1. The following papers were published in the conference proceedings

(a) M.A.Hashim, K.Z.K.Ahmad & A.Isnin, *"Comparative Microstructure Observation of Eutectic Tin-Lead and Eutectic Tin-Magnesium Solder Alloy"* presented at PERFIK 2000 conference Organized by Universiti Kebangsaan Malaysia (UKM), September 20-22, 2000

(b) M.A.Hashim, K.Z.K.Ahmad, A.Isnin, *"Creep And Fatigue Interaction In Eutectic Tin-Lead Solder Interconnect"* presented at MASS 2000 conference Johor Bahru, November 20-22, 2000

(c) M.A. Hashim, K.Zarina K.A, W.M.N.W.Jaafar, A.Isnin, “Isothermal Fatigue Testing of Eutectic Tin-Lead Solder Alloy”, presented at the 3rd international Conference on recent Advances in Materials, Minerals and Environment [RAMM 2003]. 20-22 October 2003

(d) M.A.Hashim, N.M.Yusof, W.M.N.W. Jaafar, A.Isnin, “Comparative Microstructural Evolution of Eutectic SnPb and Hypoeutectic SnAgCu Interconnect Alloys”, Presented at 5th International Materials technology Conference and Exhibition, IMTCE 2006. Organized by Institution of Materials, Malaysia. Held at Mutiara Crowne Plaza Hotel, Kuala Lumpur from 17 – 20 July 2006

(e) M.A. Hashim and A.Rahmat,” Fractograhpy of Lead-Containing and Lead-Free Solder Alloys Under Static and Dynamic Loading”, 6th International materials and Technology Conference and Exhibition, 26 ~ 27 August 2008, Park Royal Hotel, Kuala Lumpur

(f) M.A.Hashim and A.Rahmat, ”Mechanical Cycling: An Alternative to Thermal Cycling for Reliability Testing of Interconnect Materials Used in Electronic Packaging” 4th RAMM and &ASMP Conference 2009, 1-3 June 2009, Bayview Hotel and Resort, Pulau Pinang

2. Publication in referred Journals

(a) M.A.Hashim, K. Zarina K.A, W.M.N. Wan Jaafar, A. Isnin, “ Fractography of Lead-containing and Lead-Free Solder Alloys Under Monotonic Uniaxial Tensile Loading”, Journal of Institute of Materials, Malaysia, Vol. 4(1). Jan 2003. Pgs: 25-35

(b) M.A.Hashim and A.Rahmat, “Stress Relaxation and Fatigue Characterisation of Eutectic SnPb Solder Alloy”, In-Press. Journal of Key Engineering Materials, Vol 462-463, 2011

# Rayap dan Perlakuan Isotermal Lesu terhadap Pateri Eutektik SnPb, SnBi dan SnZn dalam Pembungkusan Microelektonik pada Anjakan Suhu Sederhana


## Abstrak

Bahan penyambungan dalaman digunakan untuk menyambung komponen litar lekap, pasif dan diskrete keatas lapik kupram atau lapik lain, dan didalam lubang papan litar tercetak. Ketika ini, amalan industri adalah dengan menggunakan kitaran termal sebagai kaedah untuk pengujian keutuhan papan litar tercetak yang telah dipasang dengan komponennya. Spesimen pukal aloi pateri 63Sn37Pb diuji dengan isotermal lesu pada tiga suhu sederhana tinggi (30, 40 dan $50^{o}$ C), tiga beban frekuensi (6, 60 dan 600 kpm) dan dengan beban puncak terikan yang berlainan. Spesimen didapati gagal berleluasa secara rayap dengan tenaga aktivasi dalaman beranggaran 60 KJ $mol^{-1}$, dan eksponen ketegasan berubah diantara 1 dan 2, dan didalam keadaan eksperimen yang sama, pengujian rayap statik menunjukkan tenaga aktivasi sebanyak 85 KJ $mol^{-1}$ dan nilai purata eksponen ketegasan sebanyak 1.5. Ujian keterikan lesu kitar terkendali pada suhu, frekuensi, puncak keterikan dan nilai R berlainan menghasilkan nilai purata keterikan bergerak-balas mundur secara eksponential. Pada R=-1, nilai purata ketegasan bergerak-balas kesifar serta merta untuk semua terikan, frekuensi dan suhu yang diuji. Ujian isoterma lesu yang dijalankan pada R=-1, beban frekuensi 600 kpm dan pada dua suhu berlainan menunjukan mekanisma pembaikan kerosakan rayap dan memajukan fenomena interaksi “rayap-lesu” didalam bahan pukal aloi pateri. Fraktografi keatas spesimen retak menunjukan perubahan didalam mekanisma retak, dari mikro-lompang kepada mikro-retak. Meskipun, data kitaran termal tidak diperolehi untuk perbandingan dengan eksperimen yang telah dijalankan, pemerhatian dari eksperimen mengesyorkan kaedah yang sesuai dan wajar didalam melaksanakan pengujian isotermal lesu. Justeru, dalam perbandingan dengan kehadiran sebahagian data dari kitaran termal, pengujian isotermal lesu adalah cadangan alternatif untuk pengujian keutuhan bahan penyambung dalaman aloi pateri eutektik.

Creep and Isothermal Fatigue Behaviour of Eutectic SnPb, SnBi and SnZn Solders used in Microelectronic Packaging at Mildly Elevated Temperatures

## Abstract

Interconnect materials are used to connect surface mounting components and other passive and discrete circuit components on to copper pads or lands, and in holes on the printed circuit boards. Presently, the industrial practice is using thermal cycling as a method for reliability testing of circuit boards with assembled components. Bulk specimens of 63Sn37Pn solder alloy were subjected to isothermal fatigue at three mildly elevated temperatures (30, 40 and 50$^{o}$C), loading frequencies (6, 60 and 600 CPM) and at different applied peak stresses (ranging from 8.75 to 33.25 MPa). The specimens were found to fail predominantly due to creep with activation energy of about 60 KJ mol$^{-1}$ with stress exponents varying between 1 and 2, and under the same experimental conditions, static creep tests showed activation energy of 85 KJ mol$^{-1}$ and an average stress exponents of 1.5. Strain-controlled fatigue tests conducted at different temperatures, loading frequencies, three different applied peak strains and different R-values resulted in the mean stress responses to decay exponentially. At R=-1, the mean stress responses decayed instantaneously to zero value for all applied peak strains, loading frequencies and temperatures. Isothermal fatigue tests conducted at R=-1, 600 CPM frequency and at two different temperatures showed creep damage repair mechanism and enhances creep-fatigue interaction phenomenon in the bulk solder material during mechanical cycling. Fractography of fractured specimen showed a change in fracture mechanism, that is, from micro-voids to micro-cracks observations. Even though, thermal cycling data were unavailable for comparison with those from isothermal fatigue, observations obtained from the experiments conducted suggested suitable and appropriate methods in conducting isothermal fatigue tests. Hence, in comparison with presence of some thermal cycling data, the isothermal fatigue test is a proposed alternative test for reliability testing of eutectic interconnects.

# Chapter 1 Introduction

## 1.0 Low melting temperature solder alloys

Low melting temperature solders, particularly, eutectic tin-lead alloy had been in used for decades as interconnect alloy in integrated chips packaging. This alloy had been chosen due to factors such as low melting temperature (183$^{o}$C), acceptable wettability, and exhibited single eutectic temperature and the most important of all, a lot of research had been conducted on this specific alloy and that this alloy could be taken as a reference alloy if other lead-free solder alloy is to be considered as a substitution alloy. One of the major concerns in using this alloy is the reliability of the solder joint formed. Solder joints are subjected to mechanical loadings during handling and when the system is in used, the mechanical properties of solder joints such as their fatigue, creep and shear strength are important in determining packaging reliability and integrity.

## 1.1 Problem statements

1.1.1 Thermal cycling for reliability testing of solder alloys as interconnect materials has been cited to inherit the following problems, (i) It involves a long period of testing since this testing involves time to complete failure, (ii) it is costly and laborious in nature, (iii) Tested parts normally involve intricate

shapes of the IC chip packaging and therefore results obtained were not easily interpreted. Other promising techniques such as mechanical cycling [1, 2, 3] and drop test [1] were among others examined by various researchers as alternatives to thermal cycling.

1.1.2 The eutectic tin-lead solder alloy is a soft alloy, and is ductile in nature and some circumstances the alloy may exhibit super plasticity behaviour [4, 5]. This alloy has a melting temperature of 183$^{o}$C and at room temperature of 25$^{o}$C has homologous temperature of 0.45, which indicates that the alloy undergo creep deformation processes at room temperature [6, 7]. And, it is due to this behaviour which has made the evaluation of bulk property such as strength and young's modulus a difficult task.

1.1.3 Fatigue testing of eutectic tin-lead solder alloy will eventually result in the specimen to creep [7, 8]. The sample elongated and exhibited as specimen failure under creep test due internal tensile forces which developed in the bulk material during testing. In order to observe the internal tensile force, strain controlled fatigue tests were conducted at various applied strains, R-values and effect at mildly elevated temperatures.

## 1.2 Research objectives

The primary objectives of this research are,

1.2.1 To investigate creep phenomenon in as-received eutectic tin-lead solder alloy under tensile loads at mildly elevated temperatures (30, 40 and 50$^{o}$C)

1.2.2 To study the developed internal tensile stress in the bulk eutectic tin-lead solder sample under strain controlled fatigue at different applied strains, R-values, loading frequency and temperatures.

1.2.3 To study the effect of stress controlled fatigue on the standard dimension bulk eutectic tin-lead solder alloy at selected R-values, loading frequency and temperatures

## 1.3 Organisation of the thesis

Chapter two of this thesis gives the background theory and the relevant literature survey. Chapter three describes the materials and experimental method. Chapter four consists of detail results and chapter five on the discussion. Chapter six is on research conclusions, and suggestions on future work.

# Chapter 2 Literature review

## 2.1 Integrated Circuit Chips

### 2.1.1 Introduction

The electronic industry has been recognized as one of the most dynamic and important industry in this scientific age. Everyone accepts that electronics had improved the world we live in, tremendously. Two of the essential technologies which had improved our lives are electronic packaging and electronic assembly, respectively.

Integrated circuit (IC) chips and other circuit components are not isolated islands. They are connected and interconnected with other components for maximum performance. Packaged chips and other embedded circuit networks are delicate work pieces which require shelter and protection from hostile surrounding environment. IC chips packaging focuses on how silicon chip is packaged efficiently and reliably which form a powerful component of bigger electronic device. IC packaging is therefore an important technology to be developed for device efficiency and reliability. Further, according to Moore's law [9] which was formulated in the 1960s, stated that the transistor count on an integrated circuit doubles every 18 month. This has been the driving force for package miniaturization, light weight, efficient and low gadget cost.

The materials employed in the packaging of chips and connecting to other components on circuit board must be reliable and compatible, both

electrically and mechanically. For instance, solders are used as interconnecting media between packaged IC chips to printed circuit boards. In the real microelectronic joining, solders are expected to perform as structural alloys where the operating temperature (usually, 0.5 to 0.8 of melting temperature, in $^{o}$K) and the total strain (usually, greater than 11 percent) are considerably high. These working conditions are described as aggressive to assigned solder materials, as compared to most structural materials experiencing the same working environment [10, 11, 12].

The following pages reveal how different solder materials were employed in the designing of different chip packages, their physical and mechanical properties and solder materials behaviour while in applications.

### 2.1.2 Packaging of Integrated Circuit Chips

The concept of component miniaturization is to be achievable without sacrificing quality, reliability, increasing product cost or even power consumption. Packaging technology helps to make these devices possible, and this technology focuses on how a chip or many chips are packaged reliably and efficiently. Packaged IC chips are not isolated islands and must be connected to other board components through inputs and outputs interconnection system. It also requires protection from the harsh external environment. This is done by placing chip/s in a chip-carrier and thus forms the first level of IC chip packaging. Figure 2.1 illustrates the various level of packaging starting from chip level packaging, the second level of packaging (or printed circuit board packaging)

and the mother board packaging (or the third level packaging). Figure 2.2 shows schematic diagram of the first level of chip packaging.

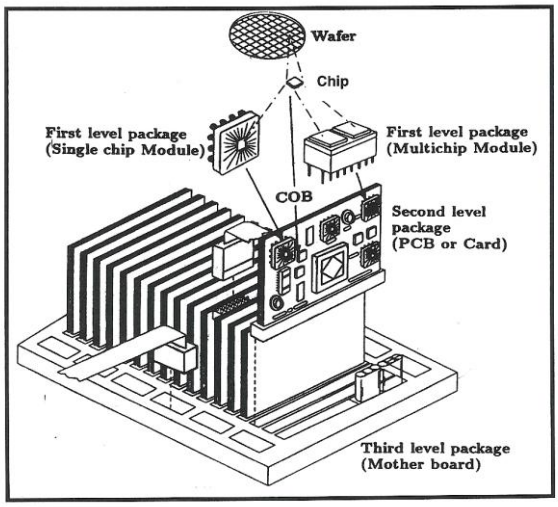


Figure 2.1: A schematic illustration of different packaging levels of IC chip and other circuit sub-components [13]

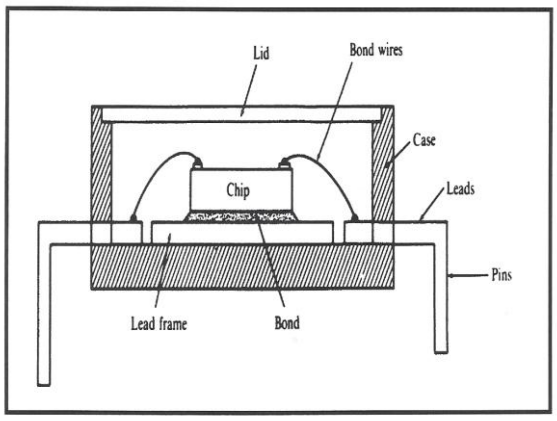


Figure 2.2: Schematic diagram showing the first level of IC packaging [14]

### 2.1.3 Types and construction of chip carriers

According to Dally [14], chip carriers are classified according to the materials used in their construction and the types of leads used for the input/output (I/O)

connections. The two common materials used are plastics and ceramics. Plastics cases, formed by injection molding are used for low and moderate cost electronic products, while ceramic cases are used for products that require stringent hermeticity. Military aircraft electronics and general avionics applications are some examples.

There are three types of chip to board interconnections which are currently in used. They are (i) pin in-hole, (ii) leads soldered to solder pads (e.g, J-leads and gull-wing, and (iii) metallised pads on chip carrier soldered to solder pads on circuit board. Schematic diagrams in Figures 2.3 to 2.5 show these constructions.

The dual in-line (DIP) type of chip packaging is an example of pin in-hole carrier. These carriers have two rows of pins that are arranged at 2.54-mm centres along the longer sides of the package, and are available in many different sizes.

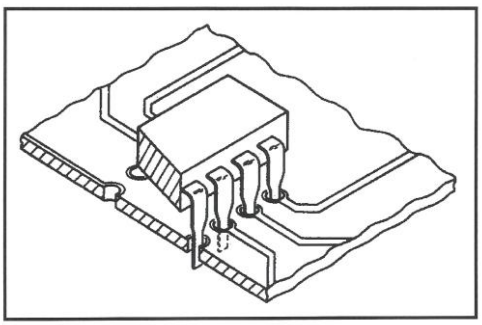

Figure 2.3: Pin-hole package [14]

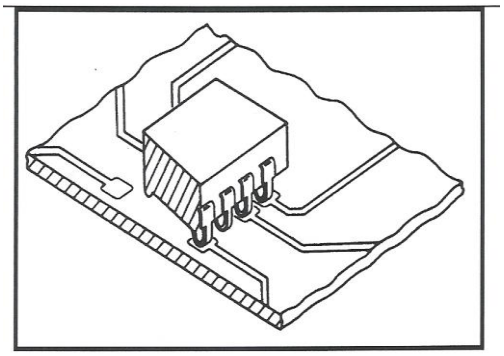

Figure 2.4: J-leaded package [14]

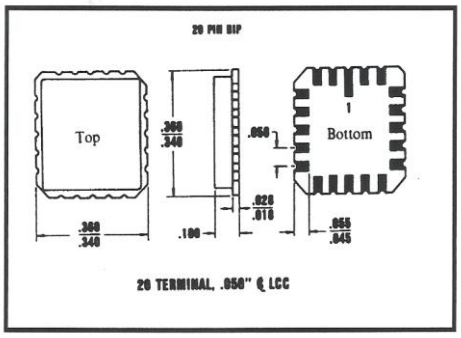


Figure 2.5: Metallised pads on chip carrier soldered to solder pads [14]

They are often used for power devices with 8 to 64 connecting pins. These pins are short and are relatively large in cross-sectional area; as such they are stiff and robust. They are inserted into holes in the circuit board by “pick and place” machines, and soldered on the underside of the board by passing through a standing wave of molten solder. The disadvantages of this type of chip carrier is its poor area efficiency which limits the number of I/O connections and due to its poor wire ability limits its usefulness in housing high density logic chips.

The pin grid array (PGA), as shown in Figure 2.6 is used as substitutes for DIPs when additional I/O connections are required or when a lower thermal resistance is also a requirement. The body of the package is fabricated from ceramic, with multilayer alumina and has a cavity for chip placement. Around

this cavity is a ledge which supports metallised pads used to bond wires that lead to the chip. The pins are about 20 to 25 mil in diameter are brazed into the ceramic substrate. When a chip is fixed in the cavity, a ceramic or kovar lid is placed over it and sealed using inorganic solders that do not out-gas.

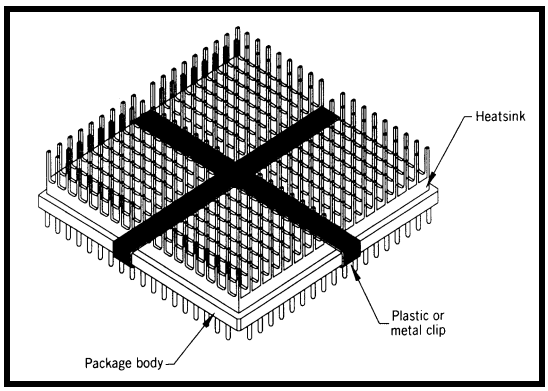


Figure 2.6: Pin-Grid Array packaging [14]

### 2.1.4 Leaded surface mounted chip carriers

When leads from chip carrier are soldered on to pads or lands on the surface of circuit board, they are known as “surface mounted” chips, as shown in Figures 2.4 and 2.5. The quad flat pack (QFP) is an example in which leads are deployed along all four sides of the package and are spaced at 1.27-mm centres. The leads are cut and shaped to gull wing configuration prior to mounting on the circuit board (Figure 2.4). The advantage of this type of packaging is its relatively small size compared to DIPs, with same number of I/O connections. However, the disadvantage of this packaging is due to fragile leads and the necessity to solder individual leads to the circuit board.

### 2.1.5 Leadless surface mounted chip carriers

Leads are fragile and can be deformed during shipping, so that their replacement with metallised pads (Figure 2.5) shows major advantages. The metallised pads are 1.27- mm centres and provide an area efficient chip carrier. These pads are connected to the corresponding pads or lands on the circuit board using solder paste.

## 2.2 Chip-to-chip carrier mounting

The silicon chip is bonded to the chip carrier to prevent any movement relative to its housing during the entire life of the product. The bonding methods vary depending on the quality of the chip carrier being produced. A high performance chip carrier has its body fabricated from ceramic and meets stringent hermetic requirement [13, 14]. It uses eutectic solder alloy of gold and silicon as the bonding materials. This alloy has a melting temperature of 390 $^{o}$C, does not out-gas with time and exhibits a high thermal conductivity (2126 W/m/$^{o}$C), aiding in the transfer of heat from the chip to the casing.

In contrast, the bonding of a chip to plastic carrier does not achieve “hermetic seal”, in part due to differences in coefficient of thermal expansion (CTE) between the plastic housing and the silicon chip. Silicon has a coefficient of thermal expansion (CTE) of 4.0 x $11^{-6}$ $^{o}C^{-1}$ compared to the epoxy encapsulation which has CTE of 27 x $11^{-6}$ $^{o}C^{-1}$ and the Bis-melamine triazine polymer (BT) which has CTE of 11 x $11^{-6}$ $^{o}C^{-1.}$ Direct bonding of a chip to plastic carrier would induce large thermal stresses due to temperature changes.

This problem is resolved by incorporating a ‘lead-frame” into the housing (Figure 2.7). The lead frame serves the following functions:

(i). The lead-frame is a copper alloy that has a coefficient of thermal expansion closed to that of silicon and so can be used as bonding interface.

(ii) It provides leads that are protrude/extend out of packages

(iii) It provides a surface to which connecting leads from the chip can be welded

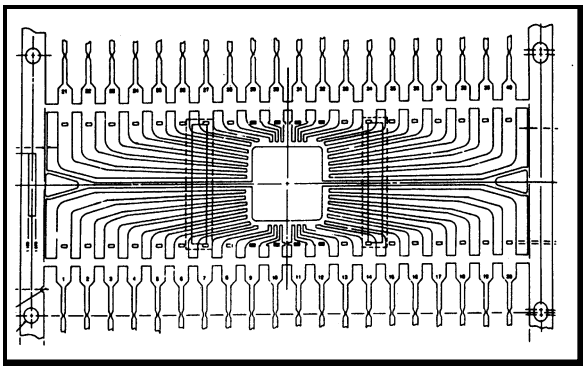

Figure 2.7: A typical lead frame used for chip bonding in a plastic DIP housing [14]

## 2.3 Chip-to-chip carrier connections

The input/output (I/O) connections from a chip consist of a number of bonding pads usually arranged around the top edge of the chip. The pads are miniature in size, each measuring about 0.127 $mm^2$ and placed at 0.254 mm apart. On a dense chip, the pad size is about 0.076 $mm^2$ and is spaced at 0.0112 mm apart. Connections are made between these bonding pads and the chip carrier through wire bonding. In application, there are three different methods of chip-to chip carrier connections, namely automatic wire bonding, tape automated

bonding and flip-chip bonding. These methods are described in detailed by Lau [13] and Dally [14].

## 2.4 Updates on integrated circuit packaging

Lau [9] had identified two main problems in IC packaging. They are termed as “on-chip signal delay” and “signal delay from packaged ICs”. The signal delay from packaged ICs has not been addressed as vigorously as on-chip signal delay. IC packages therefore experience “loss function” which need to be addressed. Packaging engineers proposed that the problem could be addresses by increasing the number of pin counts, which in-turn increases package performance. (The package performance is measured in terms of on-chip clock frequency. For instance, some microprocessors were designed with 1100 package pin count and 400 MHz device clock frequency)

Application specific integrated circuits (ASICs), static random access memory (SRAM), dynamic random access memory (DRAM) and other microprocessor chips are examples of devices which have been designed to run faster than 110 MHz, and their pin count had been increased to 1200. According to Lau [13], further improvement in chip performance is achievable if the present technology, known as the fine pitch technology, having a pitch of less than 650 μm could further be improved. In this way, the number of pin count could be increased which improves microprocessor performance by having a faster device clock frequency.

However, with the application of fine pitch technology and the concurrent reduction in packaging delays, the conventional chip packaging technology is

nearing its practical limitations. Problems which relate to these limitations and which resulted in highly undesirable effects are lead coplanarity, package cracking, fine pitch limitations and relatively long leads. Long leads are known to inherit stray inductance, resistance and capacitance. Figure 2.8 shows examples of conventional chip packages: they are plastic chip carrier (PLCC), plastic quad flat pack (PQFP) and thin small outline package (TSOP).

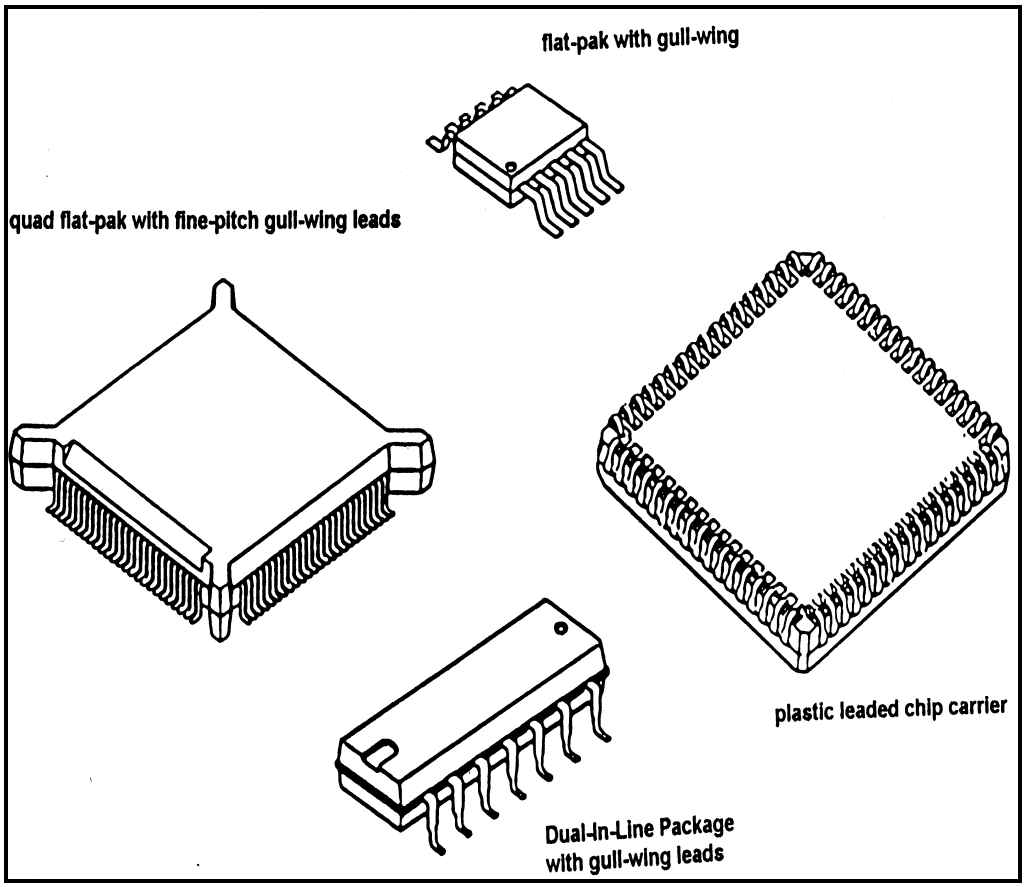


Figure 2.8: Some conventional chip packages [13]

Advanced IC packaging promises a more reliable performance than the conventional packages, in terms of finer lead pitches, thinner package profiles and smaller foots prints on the circuit board. Figure 2.12 shows some examples

of advanced IC packages. They are tape carrier packages (TCP), pin grid arrays (PGA), ceramic ball grid arrays (CBGA), plastic ball grid array (PBGA), tab ball grid arrays (TBGA)

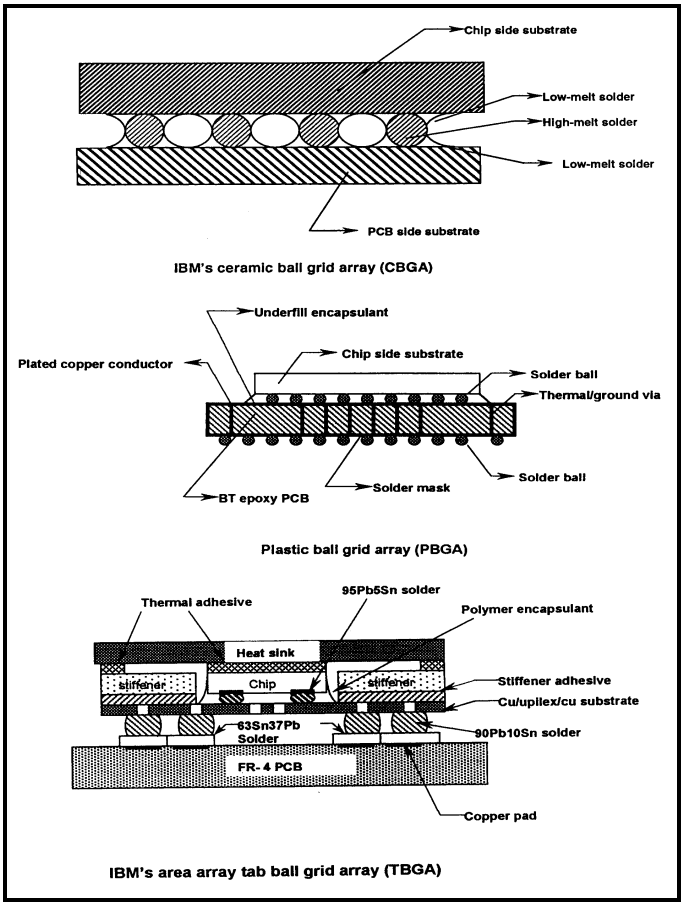


Figure 2.12: Some advanced chip packages [13]

## 2.5 Ball Grid Array – an overview

In the past decades, pin grid arrays (PGAs) and quad flat packs (QFPs) have been the electronic industry's major chip carrier packages. The ceramic pin grid array (CPGAs) packages were found versatile and flexible, since both the number of layers and size could be varied. Thus, CPGA chip carriers can satisfy a broad range of applications. However, the requirements for an

increasing performance and for providing additional functions require an ever-increasing integration. It is therefore, difficult for PGAs to remain cost effective since there is a practical limitation on the pin arrays and pin attachment cost is high. These limitations are partly solved by using ball gird arrays (BGAs). BGAs are not only cost effective and surface mount compatible, but are much smaller in physical size and exhibit superior electrical performance compared to PGAs and QFPs.

BGAs utilize an area array of solder balls which are mounted on the underside of the package to achieve an optimum solder joint to a printed circuit board (Figure 2.11). The Joint Electron Device Engineering Council (JEDEC) of the United States of America proposed that grid pitches of 1.0, 1.27 and 1.5 mm were suitable for BGAs. These pitches will provide I/O densities exceeding 2000 for a 50 mm BGA package.

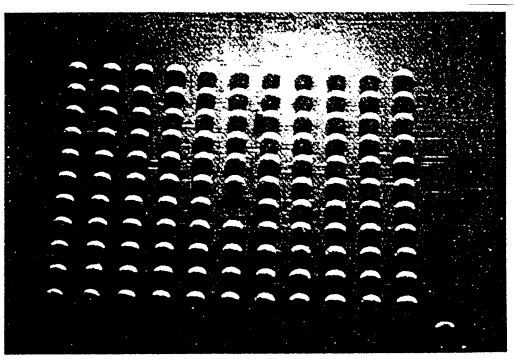

Figure 2.11: Solder spheres located on an area array of chip bonding pads [14]

Depending on the application and design, the AMKOR/ANAM BGA package is constructed using double-sided or multi-layer printed circuit laminate with the chip die or dies attached to it with a silver filled epoxy. A conventional plastic transfer moulding process is used to encapsulate the die for moisture resistance.

After further processing, the solder balls are then attached to the backside of the substrate. A schematic diagram representing the Amkor/Anam's cavity down super BGA is as shown in Figure 2.11

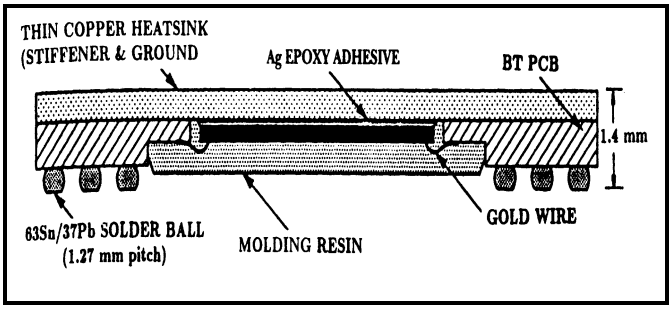


Figure 2.11: Amkor BGA package [13]

The composition of the BGA solder spheres alloys is governed by specification QQ-S-571, Revision F [15]. The typical lead-containing alloy compositions suggested by the specification are as shown in Table 2.1:

Table 2.1: Typical lead-containing solder spheres; diameters and tolerances [15, 16]

| Alloy composition | Sphere diameter, mm | Tolerance, mm |
|---|---|---|
| 63 Sn37Pb | 0.305 | ±0.013 |
| 63 Sn37Pb | 0.508 | ±0.025 |
| 63 Sn37Pb | 0.635 | ±0.025 |
| 63 Sn37Pb | 0.762 | ±0.025 |
| 62Sn36Pb2Ag | 0.762 | ±0.025 |
| 11.5Sn812.5Pb | 0.8812 | ±0.051 |

## 2.6 Advantages and drawbacks in application

The advantages of using BGAs over other types of packaging were highlighted by Lau [13] are as below.

(i) It represents as saving on precious printed circuit board (PCB) surface area. For example, typical package dimension of 31 mm x 31 mm with a pitch of 1.5 mm enables 400 input/output (I/O) connections to be made.

(ii) It eliminates problem of coplarity, skewness and bending associated with the use of leaded packages during PCB assembly

(iii) It improves assembly, electrical performances, IC package yield and board assembly yield.

(iv) It allows IC package to be self-centered when positioned on the PCB due to wide pad areas.

The disadvantages in the usage of BGAs are due to the followings:

(i) It is due to the softening of BGA spheres and cracking of interconnects had been reported during re-flow soldering and thermal cycling processes. Hence, there is a requirement for highly reliable solder interconnects

(ii) Inspection is difficult and expensive, and test methods are not well established. Inspection is only possible using X-ray or ultra-sonic technique

## 2.7 Interconnect and surface mounting materials

Both metallic and non-metallic solders had been used as interconnect or surface mounting materials for electronic devices. Table 2.2 shows candidates

of solder material with their approximate melting temperatures. The most widely used solders in the electronic assemblies are either eutectic or near eutectic tin-lead alloys. However, lead is also known to pose a risk to human health and recently a bill to control the use of lead was introduced in the United States Congress. This has stimulated in the use of lead-free solders, especially for the electronic industry. The bill also proposed banning of lead from a variety of uses, such as in the petroleum, automotive and other related chemical industry.

Glazer [17] and Vincent *et al*., [18] highlighted some interconnect materials that have potential as substitute for eutectic or near eutectic tin-lead alloy. Some eutectic or near-eutectic solder alloys, for example 58Bi42Sn, 1212.3Sn0.7Cu and SnBiAgCu were reported to be potentially viable lead-free solder alloys. Table 2.2 shows some lead containing, lead-free alloys as well as non-metallic adhesives used as surface mounting materials.

## 2.8 Desirable properties of surface mounting materials

Glazer [17] has identified some most important desirable properties and characteristics of interconnect and surface mounting materials. They can be grouped under three broad headings, namely physical and microstructure, corrosion and oxidation and mechanical properties.

### 2.8.1 Physical properties

Some important physical properties are melting temperature and melting temperature range, coefficient of thermal expansion, surface tension and electrical resistivity values. For example, the melting temperature and melting

temperature range determine both the maximum possible operating temperature of a component and the minimum short-term temperature

Table 2.2: Some typical interconnect and surface mounting materials [17]

| Lead-containing alloys | Melting temp., $^{o}$C | Lead-free alloys | Melting temp., $^{o}$C | Non-metallic solders | Softening temp., $^{o}$C |
|---|---|---|---|---|---|
| 63Sn37Pb | 183 | Sn0.7Cu | 227 | Metal-filled Thermoplastic / thermosets | Low curing temperature, that is, room temperature to about 140 $^{o}$C |
| Sn5Pb | 232 | Sn4Cu0.5Ag | 216 | | |
| InPb | …. | Sn2Mg | 200 | | |
| PbBi | ….. | Sn12Zn | 11212 | | |
| 11Sn88Pb2Ag | ….. | Sn58Bi | 138 | | |
| 62Sn36Pb2Ag | ….. | Sn52In | 120 | | |
| | | Bi32In | 1112 | | |
| | | Bi26In17Sn | 712 | | |
| | | Bi66In | 72 | | |
| | | 110Sn | 232 | | |
| | | Sn3.5Ag | 227 | | |
| | | Sn7.5Bi2Ab 0.5Cu | 207 | | |
| | | In3Ag | 143 | | |

a component has to survive. Table 2.2 shows some typical lead containing and lead-free solder alloys used as interconnect or surface mounting materials. In addition to alloy's low melting temperature, the ideal solder material for electronic application should also possess a narrow melting temperature range so that solidification occurs over a narrow temperature range. For this

application, a candidate material with eutectic or near eutectic composition is often chosen.

The surface tension of molten solder has an important role in determining its wetting behaviour. Flux is employed in soldering process to reduce surface tension at the solder/vapour interface and enhances the system's wetting behaviour. On the other hand, the relatively high surface tension of tin-lead solder influences the capillary flow of solders and self-alignment of surface mounted components. It also helps in retaining circuit components on to printed circuit board during second-side re-flow of surface mounted devices. Table 2.3 shows and compares surface tension values of eutectic tin-lead to lead-free solder alloys.

Table 2.3: Comparison of surface tension values at ($T_L$ + 50) $^oC$ [17]

| Alloy | $T_s$ /$^oC$ | $T_l$ /$^oC$ | Surface tension/mN $m^{-1}$ | |
|---|---|---|---|---|
| | | | Air | $N_2$ (<20 ppm $O_2$ |
| 63 Sn37Pb | 183 | … | 417 | 464 |
| 125Sn5Sb | 240 | …. | 468 | 4125 |
| 1212.3Sn0.7Cu | 227 | … | 4121 | 461 |
| 126.5Sn33.5Ag | 221 | … | 431 | 4123 |
| 125.5Sn4Ag0.5Cu | 207 | 212 | ……. | …. |
| 121Sn12Zn | 11212 | … | 518 | 487 |
| 42Sn58Bi | 138 | … | 3112 | 3412 |
| 110Sn | 232 | … | … | … |

The coefficient of thermal expansion (CTE) of the solder material influences the stress-strain distributions of a joint while in application and during product reliability testing. To eliminate large differences in the stress and strain of various parts in the whole packaging, it desirable to have parts CTE closely match to each other. As an illustration on the significance of coefficient of

thermal expansion of various materials used, a typical construction of plastic ball grid array (Figure 2.12) is cited as an example. The materials CTE is as shown in Table 2.4. In most packaging designs, a joint failure was observed in the interconnect/solder material.

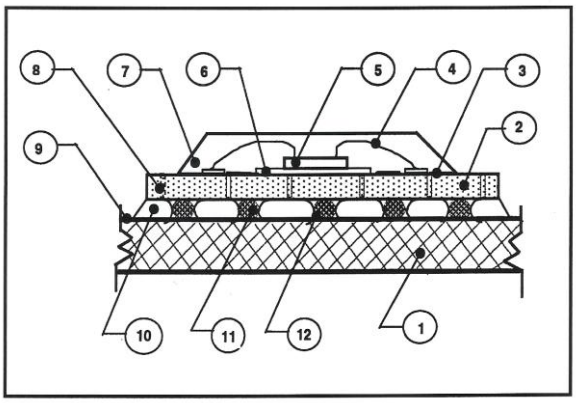


Figure 2.12: Plastic ball grid array with different materials of construction

Table 2.4: Materials of construction against coefficient of thermal expansion [17]

| Part No. | Material of construction | Coefficient of thermal Expansion x $10^{-6}$ |
|---|---|---|
| 1 | Epoxy glass, FR-4/FR-5 | 18.5 |
| 2 | Bis-melamine triazine polymer (BT) | 15.0 |
| 3 | Plated copper conductor (Chip side) | 17.5 |
| 4 | Connecting wire | …. |
| 5 | Silicon chip | 2.5 |
| 6 | Die pad | …. |
| 7 | Epoxy encapsulation | 27.0 |
| 8 | Thermal via (copper plated) | 17.5 |
| 9 | Plated copper conductor (PCB side) | 17.5 |
| 10 | Under-fill polymer material | …. |
| 11 | Solder spheres | …. |
| 12 | Interconnect material(**eutectic Sn-Pb)** | 21.0 |

### 2.8.2 Microstructure

Earlier workers like Glazer [17] defined microstructures as the combination of phases that are present in a material, which comprises of defects, its

morphology and distribution. The composition and microstructure of an alloy determine its properties and hence are important determinants of reliability of solder joints. Microstructure is a function of the composition of the material, thermal, mechanical and in some cases electromagnetic property.

Higher tensile strengths and lower melting temperatures are some reasons for the use of eutectic compositions. Eutectic alloys comprise of two phases, which solidify concurrently at the eutectic temperature. The solidified microstructure is usually lamella or may be fine or degraded lamella if the matrix is cooled rapidly. In this case, due to controlled diffusion process which occur within the microstructure. Interaction between substrate and molten solder causes the microstructure of the solidified solder to be sensitive to the time-temperature profile used in its solidification. These interactions not only influence the nature of the substrate/solder interface, but also influence the composition of the solder, and subsequently the resultant microstructure. Intermetallic particles, which are brittle and may initiate cracking while in service may also be present in the bulk solder, either because they form in the bulk during solidification or they break away from the interface layers.

The other fundamental property of solder materials is the material resistivity. It is very dependent on temperature, composition and microstructure. Resistivity values are normally low, and therefore its exact value is not significant to circuit functionality. Some typical values of electrical resistivity of materials of construction used in the construction of an IC packages are as shown in Table 2.5

Table 2.5: Comparison of electrical resistivity values of typical materials used in the construction of IC packages [17]

| Materials of construction | Typical resistivity values/ μΩ.cm |
|---|---|
| **Solder alloys** | |
| 63Sn37Pb | 11 (low) : 11 (high) |
| 126.5Sn3.5Ag | 11(Low): 12.3 (high) |
| 58Bi42Sn | 30(Low): 34.4 (high) |
| 50Sn50In | 14.7(low): 30 (high) |
| 48Sn52In | 14.7 |
| **Lead frame materials** | |
| Cu | 1.73 |
| Cu-0.6Fe-0.05Mg-0.02P-0.23Sn | 2.65 |
| Fe-52Ni | 43.2 |
| Fe-42Ni(Alloy 42) | 57 |
| **Pure metals** | |
| Ag | 1.512 |
| Bi | 111 |
| In | 8.8 |
| Pb | 20.6 |
| Sn | 11.1 |

### 2.8.2.1 Eutectic tin-lead

The eutectic tin-lead alloy is an example of a binary alloy, which was widely used as interconnect or surface mount material before a proposal was imposed for replacement material due to toxicity of lead. At atmospheric pressure (Figure 2.13), the three equilibrium phases exhibited are: (i) liquid (L), (ii) a lead-rich phase and centred cublic solid solution ($\alpha$) of tin in lead with maximum solubility of 112 wt % Sn, (iii) and a tin rich-phase with body centred cubic tetragonal ($\beta$) phase with maximum solubility of 2.5 wt. % lead.

During eutectic cooling (Figure 2.14), the liquid transformation occurs as:

$$L_{61.12\ wt\ \%\ Sn,\ 38.1\ wt\%Pb} \longrightarrow \alpha_{\ 112wt\%Sn\ 81wt\%Pb} + \beta_{\ 127.5\ wt\%\ Sn\ 2.5\ wt\ \%\ Pb} \quad \ldots.(2.1)$$

α and β are two solid solutions formed during the eutectic reaction. The compositions of these two solid solutions are 112 wt % Sn and 81 wt% Pb and 127.5 wt % Sn and 2.5 wt % Pb, respectively. The α-platelet nucleates and grows in the eutectic liquid due to inward diffusion of lead atoms and outward diffusion of tin atoms from nucleus to the adjacent regions, enhancing a lead-rich α-solid. The adjacent region continues to increase in tin content until the composition reaches 127.5 wt % Sn and solidifies as β platelets. This process of eutectic solidification continues until completion, and α and β micro-constituents are fully observed.

The lamella growth was cited as an example of a preferentially orientated plane-front steady-state growth by previous researchers like Wineguard [19], and cited by Askeland [4], Morris et al., [20] and Frear et al., [21]. The growth phenomenon was further described as a cooperative growth process since the solute rejected ahead of one phase became immediately incorporated in the adjacent region, and both phases grew simultaneously at the same rate. A distinct boundary between adjacent grains is observed when a lamellae grain grows continuously until contact is made with a mould wall or with similar growing grains. The lamellae spacing within the eutectic grain is determined by the cooling rate, a faster cooling rate results in fine lamellae.

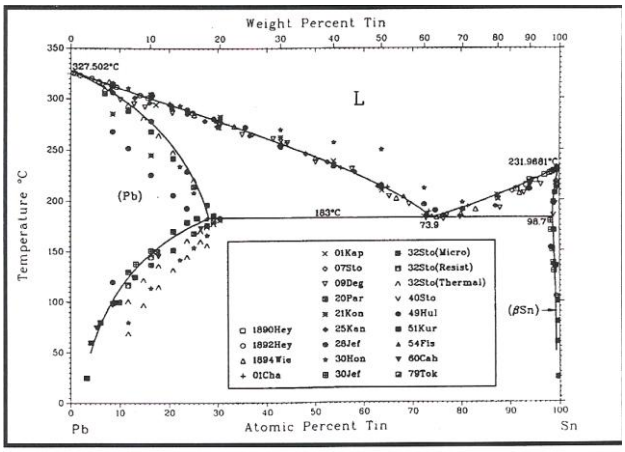


Figure 2.13: Tin-lead phase diagram (Harris et al., [22])

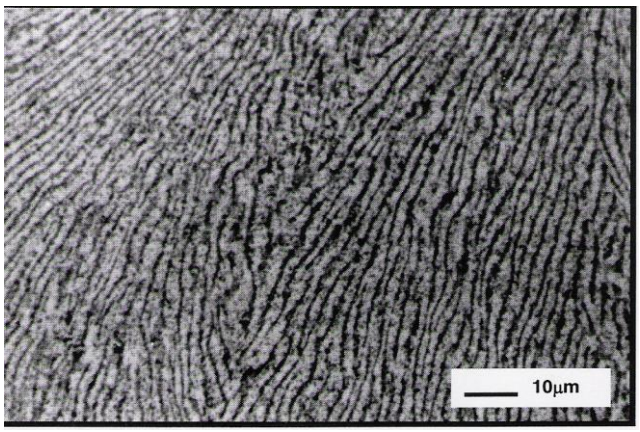


Figure 2.14: Formation of two distinguished lamella grains during cooling of eutectic tin-lead alloy (Morris et al., [20])

### 2.8.3 Mechanical properties

Solder joints formed both, electrical and mechanical connections in an electronic assembly. As metallic solders are good electrical conductors, their mechanical properties shall be reviewed. The mechanical properties of a material describe its response to an externally imposed stress and generated strains. Glazer [17] categorized conditions under which these stresses or strains were imposed, and they can be divided into three broad categories,