METHODOLOGIES FOR THERMAL ANALYSIS IN SINGLE DIE AND STACKED DIES ELECTRONIC PACKAGING

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METHODOLOGIES FOR THERMAL ANALYSIS OF SINGLE DIE AND STACKED DIES ELECTRONIC PACKAGING

by

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LIST OF SYMBOLS

SYMBOL	DESCRIPTION	UNIT
Q_x	Conduction heat flow rate at x direction	W
K_x	Thermal conductivity in x direction	W/mK
A_c	Cross section area perpendicular to the heat flow	m^2
dT	Temperature difference	K
dx	Distance difference	m
Q_{conv}	Convection heat flow rate	W
h	Convective heat transfer coefficient	W/m^2K
A_s	Surface exposed to convection	m^2
T_s	Surface temperature	µm
T_∞	Temperature of fluid or surroundings	K
$Q_{rad\ w}$	Heat flow due to radiation	W
ε	Surface emissivity	-
σ	Stephan-Boltzmann constant (5.67×10^{-8} $W/m^2.K^4$)	$W/m^2.K^4$
R_{ja}	Junction-to-ambient thermal resistance	K/W
R_{jc}	Junction-to-case thermal resistance	K/W
k_F	Thermal conductivity of FR4	W/mK
k_{cu}	Thermal conductivity of copper	W/mK
k_{eq}	Equivalent thermal conductivity	W/mK
A_{via}	Area of via	m^2
h_{nup}	Natural convection heat transfer coefficient for upper surface	W/m^2K
h_{ndn}	Natural convection heat transfer coefficient for bottom surface	W/m^2K

P	Dimensionless parameter where the surface area of one side of the flat plate divide by the surface perimeter	-
L	Length of the surface exposed to convection	m
W	Width of the surface exposed to convection	m
h_f	Forced convection heat transfer coefficient	W/m^{2}K
h_{rad}	Heat transfer coefficient due to radiation	W/m^{2}K
h_{total}	Sum of heat transfer coefficient	W/m^{2}K

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1 Thermal Performance Prediction of QFN Packages using Artificial Neural Networks 132

2 Application of artificial neural network in thermal and solder joint reliability analysis for stacked dies LBGA 132

KEADAH DALAM ANALISIS TERMA BAGI CHIP TUNGGAL DAN CHIP BERLAPIS PEMBUNGKUSAN ELEKTRONIK

ABSTRAK

Analisis terma bagi chip tunggal dan chip berlapis dalam pembungkusan elektronik adalah penting untuk peralatan komunikasi mudah alih disebabkan kekurangan ruang untuk kaedah penyejukan secara aktif. Penyelidikan masa kini lebih tertumpu kepada kaedah penyejukan aktif dan mengabaikan penyejukan pasif yang lebih ekonomikal melalui rekabentuk struktur pembungkusan elektronik and pemilihan bahan mentah. Chip berlapis pembungkusan elektronik merupakan inovasi yang berkos efektif dan mempunyai prestasi elektrikal yang tinggi. Namun, masalah terma yang disebabkan oleh terma crosstalk perlu diatasi. Kaedah eksperimen dan pengiraan berangka terkini adalah sangat rumit, mengambil masa yang lama dan berkos tinggi.

Untuk mengatasi masalah tersebut, kaedah unsur terhingga yang dipermudahkan dengan menggunakan ANSYS ® akan dibina dengan mengunakan pengaturcaraan APDL. Kaedah ini meringkaskan proses pembinaan model 3D, meshing dan mengurangkan masa penyelesaian masalah oleh komputer. Dua jenis kaedah pembungkuan elektronik yang terkenal iaitu Quad Flat No-lead (QFN) and stacked dies Low-profile Ball Grid Array (LBGA) telah dipilih untuk menguji kemampuan dan ketepatan kaedah ini. Kaedah baru ini mempunyai ketepatan yang tinggi untuk meramal suhu dan prestasi terma pembungkusan elektronik apabila dibandingkan dengan kaedah eksperimen. Perbezaan di antara ramalan suhu dan

prestasi terma menggunakan kaedah ini dengan eksperimen adalah sebanyak 8% untuk QFN dan sebanyak 12.4% untuk stacked dies LBGA.

Rangkaian saraf tiruan merupakan kaedah baru yang diperkenalkan untuk meramal prestasi terma pembungkusan elektronik secara tepat dan cepat. Kaedah unsur terhingga yang dibina digunakan untuk menghasilkan data untuk melatih jaringan saraf tiruan (ANN). ANN dibina dengan menggunakan perisian Matlab 6.5. ANN memberikan ketepatan ramalan yang tinggi dan mempunyai perbezaan sebanyak 5.9% dan 9.25% masing -masing untuk QFN dan stacked dies LBGA jika dibandingkan dengan eksperimen. Kaedah ANN dapat memudahkan kerja seseorang pereka pembungkusan elektronik kerana kaedah ini lebih ringkas, mudah, tepat dan memerlukan kos yang rendah.

ANN digunakan untuk membuat kajian parametrik ke atas prestasi terma untuk QFN dan stacked dies LBGA. Keputusan ANN telah merumuskan faktor yang perlu dititikberatkan untuk meningkatkan pretasi terma dalam QFN dan chip berlapis LBGA. ANN juga dapat menyelidik kesan terma crosstalk dalam chip berlapis LBGA dengan mudah dan berkesan.

METHODOLOGIES FOR THERMAL ANALYSIS OF SINGLE DIE AND STACKED DIES ELECTRONIC PACKAGING

ABSTRACT

Thermal analysis in single die and stacked dies electronic packaging for portable communication devices is very important due to lack of real estate for active cooling. Recent research had focused on active cooling and neglected the low cost passive cooling by optimizing the architecture of package structure and material selection. Stacked dies electronic package is an economical and good electrical performance innovation but inherent thermal problems which caused by thermal crosstalk. Recent methodology for numerical method and measurement method for thermal analysis in QFN and stacked dies LBGA is labor intensive, needs huge amount of investment and requires expert's knowledge.

To fill the gap above issue, 3D Finite Element method (FEM) using ANSYS ® with simplified and automated method by APDL language available in ANSYS ® had been established. This method had reduced 3D model building, meshing and computation time tremendously especially for stacked die electronic packaging. Two types of popular electronic packaging namely Quad Flat No-lead (QFN) and stacked dies Low-profile Ball Grid Array (LBGA) had been chosen to demonstrate the capability of the new methodology. The results from the FEM were compared with experimental result from open literature. The thermal performance and temperature predicted by this simplified pre-processing method in FEM have highest relative error of 8% for QFN compared to experiment result carried out. The highest relative error of simplified pre-processing method in FEM for stacked dies LBGA is 12.4%. After the result been verified, the simplified pre-processing method in FEM was used to generate huge

amount of data to train the back propagation feed forward artificial neural networks (ANN).

Artificial Neural Networks (ANN) had been introduced in this study. The ANN was built using Neural Network Toolbox in Matlab 6.5. The simplified pre-processing method in FEM was used to generate data to train the ANN. The highest relative error of prediction of thermal performance and temperature by ANN was less than 5.9% and 9.25% for QFN and stacked dies LBGA respectively. ANN can simplify the way package designers to evaluate their design's thermal performance with very minimum computational power, cost and time by eliminating the error prone model building, complexity of meshing and boundary condition settings.

ANN was used to do parametric study for thermal performance for QFN and stacked dies LBGA. Parametric study carried out by ANN had concluded the important parameters which can affect the thermal performance of QFN and stacked die LBGA. ANN can be used to evaluate the thermal crosstalk in stacked dies LBGA with ease.

CHAPTER 1
INTRODUCTION

1.0 Overview

In this section, an introduction to analysis and thermal prediction of single die and stacked dies in the electronic packaging using Finite Element Method (FEM) and Artificial Neural Network (ANN), along with the objectives and the outline of the thesis, will be presented. The main contents in this chapter are:

- Introduction to electronic packaging
- Quad Flat Non-lead (QFN) or Micro leadframe Packaging (MLP) electronic packaging
- Stacked dies Low-profile Ball Grid Array (LBGA) type of electronic packaging
- Thermal analysis of QFN type of electronic packaging
- Thermal analysis of stacked dies BGA type of electronic packaging
- Artificial Neural Network
- Problem Statement
- Project objectives
- Thesis outline

1.1 Introduction to electronic packaging

Electronic devices continue to find new application and innovation in personal, healthcare, automotive and environment systems. Electronic Packaging is one of the crucial stages in electronic devices manufacturing. Proper design of packaging will help to improve reliability and lifetime of the electronic devices but at the same time will increase the cost of the electronic components. Hence, choices of types of electronic packages, technology of implementation, power distribution, thermal analysis and reliability need to be

studied in details to ensure a good performance and minimize the cost. The electronic packaging trend involves reduction in form factor packages, reduction in cost, increase in functionality, integration and power. Hence, advancement in co-design tool such as CAD/CAE/CAM, reliable interconnects technologies and low cost material, will drive and evolve the packaging technologies to rally with the electronic packaging trend and meet the electronic devices' ever increasing demand on functionality, miniaturization and cost effective. Figure 1.1 shows the evolution trend of different types of electronic package platform for different system applications.

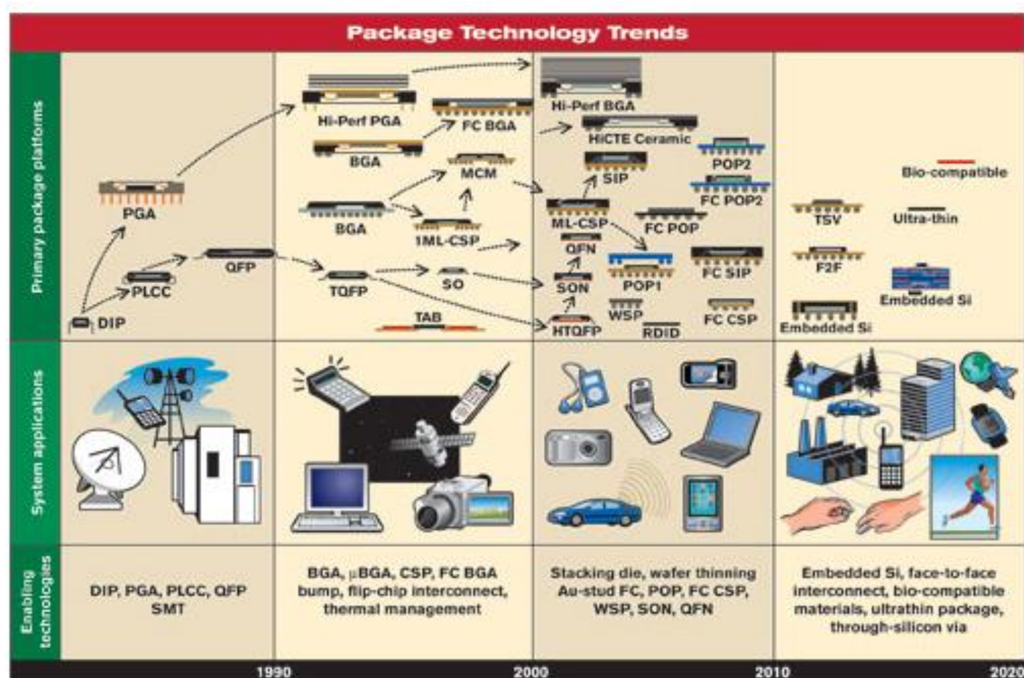


Figure 1.1: Packaging technology trends reflect application and end equipments (Mahadevan, 2009)

1.2 Quad Flat Non-lead (QFN) or Micro leadframe Packaging (MLP) Semiconductor Packaging

QFN is a near CSP (chip scale package) plastic encapsulated package with a copper lead frame as a base. The QFN packages use perimeter lands at the bottom of the package to have electrical contact with printed wiring board (PWB). QFN has short electrical path which provides excellent electrical performance. The paths include gold wire and terminals to PWB. QFN can be categorized as the thermal enhancement package since the major thermal dissipation path is through die attached epoxy and die attach pad to the PWB. The die attach pad is directly soldered to printed circuit board (PCB) to enhance the thermal performance of the package. Figure 1.2 shows the picture of QFN while Figure 1.3 illustrates the cut off view of the QFN structure.

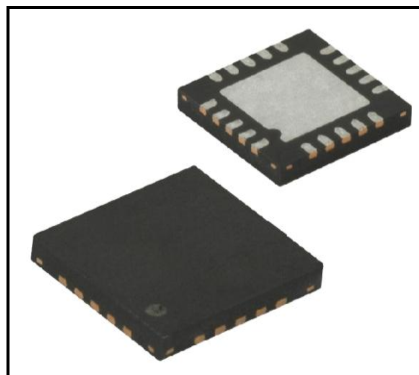


Figure 1.2: Photo of physical units of QFN with 25 leads. (http://www.asat.com)

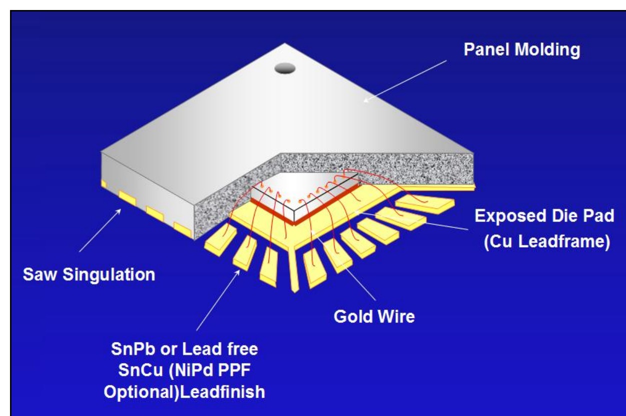


Figure 1.3: Cut off view of QFN (http://www.asat.com)

It is predicted that the demand on this package will be drastically increased (200% ~ 300%) due to its various advantages (Source: 2005 Electronic Trend Publication, Inc). QFN has smaller size and reduced package footprint by 50% or more compared to Quad Flat Plastic (QFP) and Thin Shrink Small Outline Package (TSSOP) packages as shown in Figure 1.4. QFN has low profile or thinner body (<1.0mm) because of its single-side molded construction. Smaller package footprint and thinner profile will help to save valuable board space. The small size and weight along with the excellent thermal and electrical performance makes QFN the ideal and favourite choice for handheld portable applications such as cell phone, PDAs and digital camera.

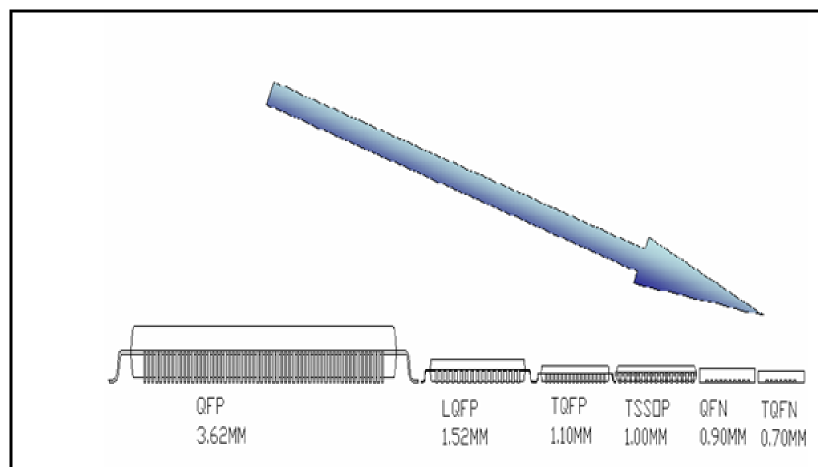


Figure 1.4: Profile of different leadframe based electronic packaging (Law et al., 2007)

The QFN package is cost effective as the existing equipment and process flow (Figure 1.5) can be utilized and implement for mass production. The map lead frame designs which increase the unit density of a strip help to reduce the cost per unit.

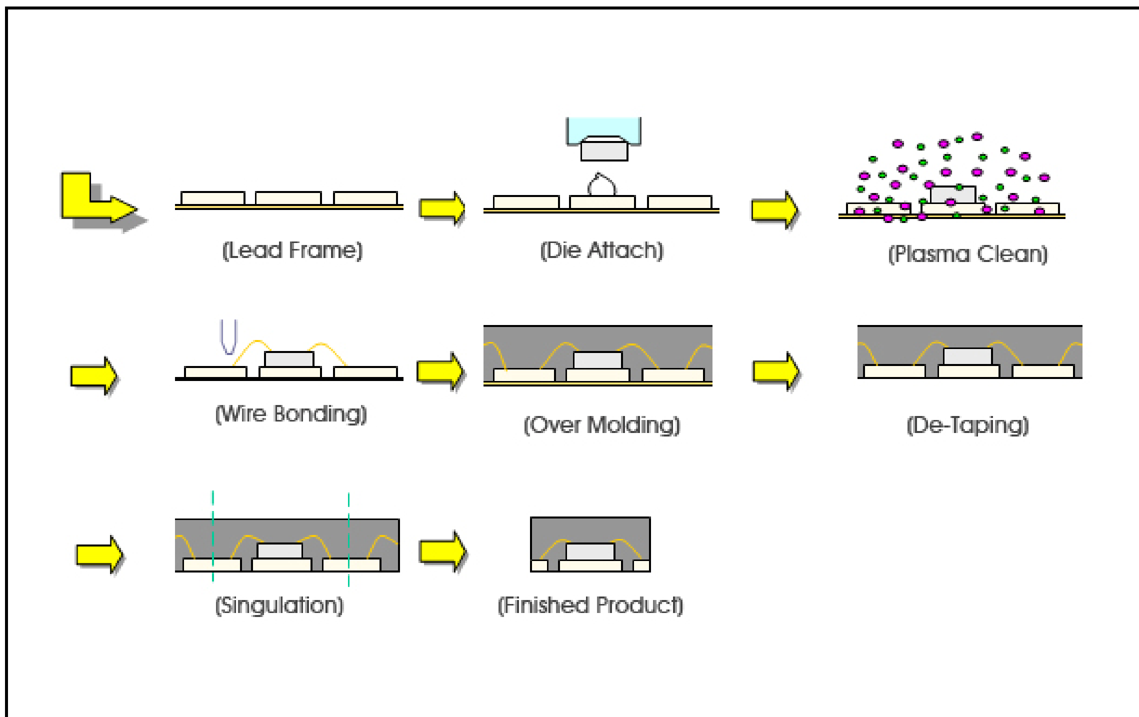


Figure 1.5: Assembly flow for QFN (http://advanpack.com)

1.3 Stack dies ball grid array (BGA) type of electronic packaging

The demand for more functionality in electronic system rapidly grows and forces researchers to work on the system-in- a-chip to minimize the cost. However, cost and yield become the issues preventing such integration to be economical feasible. Some of the die sets which are integrated together to form a system and subsystem are unable to be integrated into a single die due to difference of die material. For example, the fabrication of memory chip using Germanium telluride is not able to cooperate into microprocessor chip which is using silicon during wafer fabrication.

Hence, splitting a single die into multiple dies by stacking up into the same IC packaging as stacked dies has revolutionized the electronic industry and this technology can provide advantages in both performance and cost. In term of electrical performance, the signal will travel in shorter interconnects within the package compared to a longer distance through the traces on the printed circuit board to connect the single die packages from one to another. This will help to reduce the

electrical parasitic and increase the speed of electrical signal when dies are stacked within a package.

The vertically integration of two or more dies in an electronic packaging is called stacked dies packages. Stacked dies packages have become popular for applications that require increased functionality, smaller form factors and lighter weight. Stacked dies can help reducing the footprint and total cost of package and enable the integration of system in package. Hence, stacked dies packages are more common in handheld devices such as PDAs, cell phones and digital camera whereby incorporating the complex integration of different devices types such as logic devices (Digital Signal Processors (DSPs) and graphic devices) and memory device s (Flash, SRAM, PSRAM) is common. Figure 1.6 shows the overview of pyramid type of stacked die which requires very thin dies and tight loop height and profile control.

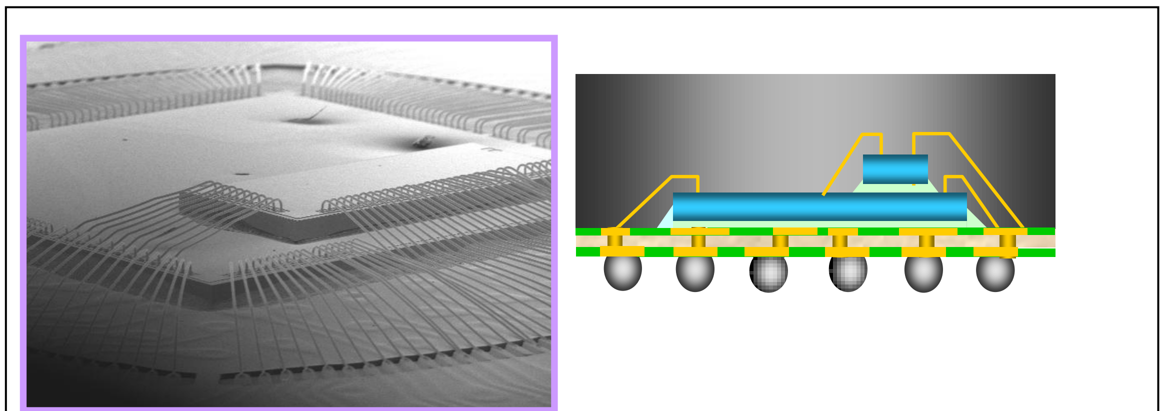


Figure 1.6: Pyramid type of stacked dies (Tong et al., 2006)

1.4 Thermal analysis of QFN type of electronic packaging

QFN gains popularity in automotive and telecommunication where the thermal performance of the package is crucial for the good reliability of the package. Shrinkage of dies and package size will prevent the heat dissipation to flow effectively. For high power application, proper optimization of QFN geometry such as pad size, die

size and package size must be carried out. Selection of materials such as high thermal conductivity mold compound and epoxy is needed to maintain the lower junction temperature of the die.

The thermal performance of QFN is measured by the thermal resistance of the package. QFN with lower thermal conductivity will have better thermal performance. To reduce the cost and cycle time of the design stage, Finite Element Analysis (FEA) is used as a tool to calculate the junction temperature of the die. The obtained junction temperature will then be used to calculate the thermal resistance of the package.

1.5 Thermal analysis of stacked dies Low-profile Ball Grid Array (LBGA) type of electronic packaging

With the complex architecture of stack dies, the thermal management becomes crucial, and integrated solution including PCB design, packages design, embedded and external cooling passives (such as heat slug, heat pipes and heat sink), active cooling (such as fan, liquid, micro pump and heat exchanger) is needed. However, with limited space and cost consideration in handheld devices, the thermal management becomes more challenging. The reliability of the die depends on the lower junction temperature of each die.

For years, IC companies and large packaging subcontractors have been publishing and maintaining their package offering thermal resistance. Most of the thermal resistance database of the offered package consists of the data for single die. In stack dies packages, the temperature rise at each individual chip is caused by multiple heat sources and difficulty is encountered when the calculation of thermal resistance is carried out. Conventional method to report a single thermal resistance of the package is not relevant. FEA is the common tools used to evaluate the

temperature rise of individual die in the stacked dies packages with different power distributions at each die. This will eliminate the tedious and costly way of experimental thermal measurement.

1.6 Artificial Neural Networks

Artificial neural network (ANN) is a neurocomputing approach loosely imitated function of human brain which solves complex problems through the learning from experiences. The field of neural network is enormous and interdisciplinary, attracting interest from researchers in many different areas such as engineering, physics, neurology, psychology, medicine, mathematic, computer science, chemistry and economics. The application of artificial neural network can be categorized into 5 major segments which are prediction, classification, data association, data conceptualization and data filtering.

The work on the artificial neural networks has reported some of the applications in real-life. In aerospace field, artificial neural networks have been used in high performance aircraft autopilot and aircraft component detection. ANN is widely used in medical for breast cancer cell analysis, EEG and ECG analysis and optimization of transplant times. Some of the novel ANN applications in handy gadgets such as 3G mobile phone, PDAs and smart devices such as speech recognition, image and data compression, bio sensor, characters recognition have boost the efficiency of data storage and data mining processes

ANN offers solutions for our ever increase demands in the area of super computer, data mining, business intelligence and robotic. Many researchers, realizing the importance of this technology, have invested their time and funds in this key technology. Hence, in this study, the potential of the ANN applications in thermal

management for electronic packaging will be explored where the modeling methods and experiment methods are complex, costly and time consuming.

1.7 Problem Statement

Thermal performance of electronic packaging becomes crucial during the design stage which involves material selection, packaging technologies and mechanical structure design. However, the vast capital investment in experiment tools, laborious experimental setup procedure, and thermal crosstalk of stack dies become bottlenecks of fast and accurate prediction of thermal performance in small scale package for package designers. Stacked dies LBGA is one of the most demanded three dimensional packages. Thermal analysis in stacked dies will not be straight forward. Thermal characterization of stacked dies is fairly complicated and currently there is no equivalent standard like single die packaging thermal evaluation which is deployed by JEDEC standard. The cross talk effects in stacked dies packaging is hard to be captured using conventional thermal characterization method. Computational Fluid Dynamic (CFD) techniques are widely used in thermal analysis for stacked dies as the thermal measurement required enormous time and large investment in equipment due to multiple power sources required. CFD simulate the flow field exist around the area near the package and board surfaces for both laminar and turbulence and predict convective heat transfer coefficients on those surfaces. However, CFD will require laborious task of 3D modeling, expertise in setting the accurate boundary condition and error prone material properties and long computational time. The motivation of the research is to provide the faster, more user friendly and accurate alternative tools to predict and analyze the thermal performance of popular small scale packages such as QFN and Stacked dies LBGA where thermal dissipation is generally inefficient.

1.8 Project objectives

For this project of *"Methodologies for Thermal analysis in single die and stacked dies electronic packaging",* there are three objectives to be achieved. These objectives are:

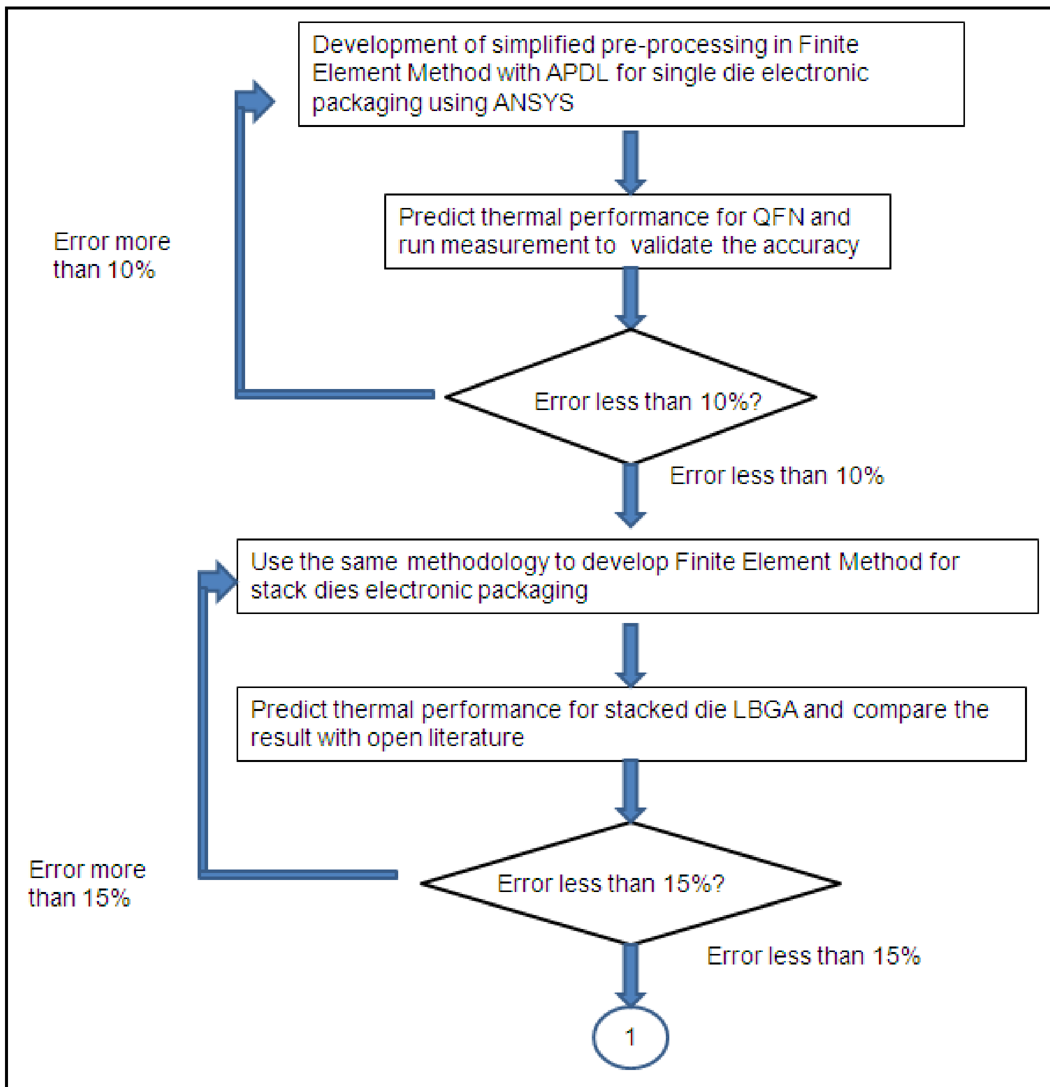
- To establish Finite Element Method (FEM) methodology and analysis to predict junction temperature of single die in electronic packaging and of each stacked dies in electronic packaging. The finite element method helps data collection for ANN training
- To predict thermal performance of single die and stacked dies in electronic packaging using ANN.
- To utilize the ANN to carry out parametric study for thermal performance in single die and stacked dies electronic packaging

1.9 Thesis outline

The thesis is organized in six chapters which include introduction, literature review, research methodology, result and discussion and lastly conclusion. The first chapter presents the brief introduction of single die and stacked dies in electronic packages specifically QFN and stacked dies LBGA which are the popular choice for current electronic market. This chapter also introduces the thermal analysis and artificial neural network. Finally this chapter outlines the objectives and structure of the thesis. The second chapter discusses the literature surveys regarding past and recent development of thermal modeling for single and stacked dies electronic packaging and application of artificial neural network in the industry. Chapter three discusses the research methodology using Finite Element Method in ANSYS® for single die type electronic packages. Simplified pre-processing method in Finite Element Method will be presented in this chapter. Chapter four discusses the research methodology using Finite Element Method in ANSYS® for stacked dies type of electronic packages. This

chapter will also cover the simplified way to predict the effects of thermal crosstalk in stack dies packages. Proceeding chapter which is chapter five discusses the application of artificial neural network built with Matlab® to predict thermal performance of single die electronic packages. The proven good ANN methodology in single die electronic packaging will used in stacked dies in electronic packages to evaluate the thermal crosstalk of multiple dies. Chapter six presents the result of the Finite Element Method and Artificial Neural Network in dealing with analysis and prediction of thermal performance in single die and stacked dies electronic packages. Result and discussion of parametric study on effects of package mechanical structural design, material selection and environment condition to the thermal performance using ANN will also be discussed. Finally, the thesis will end with conclusion in chapter seven.

Figure 1.7 shows the framework of the research methodology of the project.


Development of simplified pre-processing in Finite Element Method with APDL for single die electronic packaging using ANSYS
Predict thermal performance for QFN and run measurement to validate the accuracy
Error more than 10%
Error less than 10%?
Error less than 10%
Use the same methodology to develop Finite Element Method for stack dies electronic packaging
Predict thermal performance for stacked die LBGA and compare the result with open literature
Error more than 15%
Error less than 15%?
Error less than 15%
1

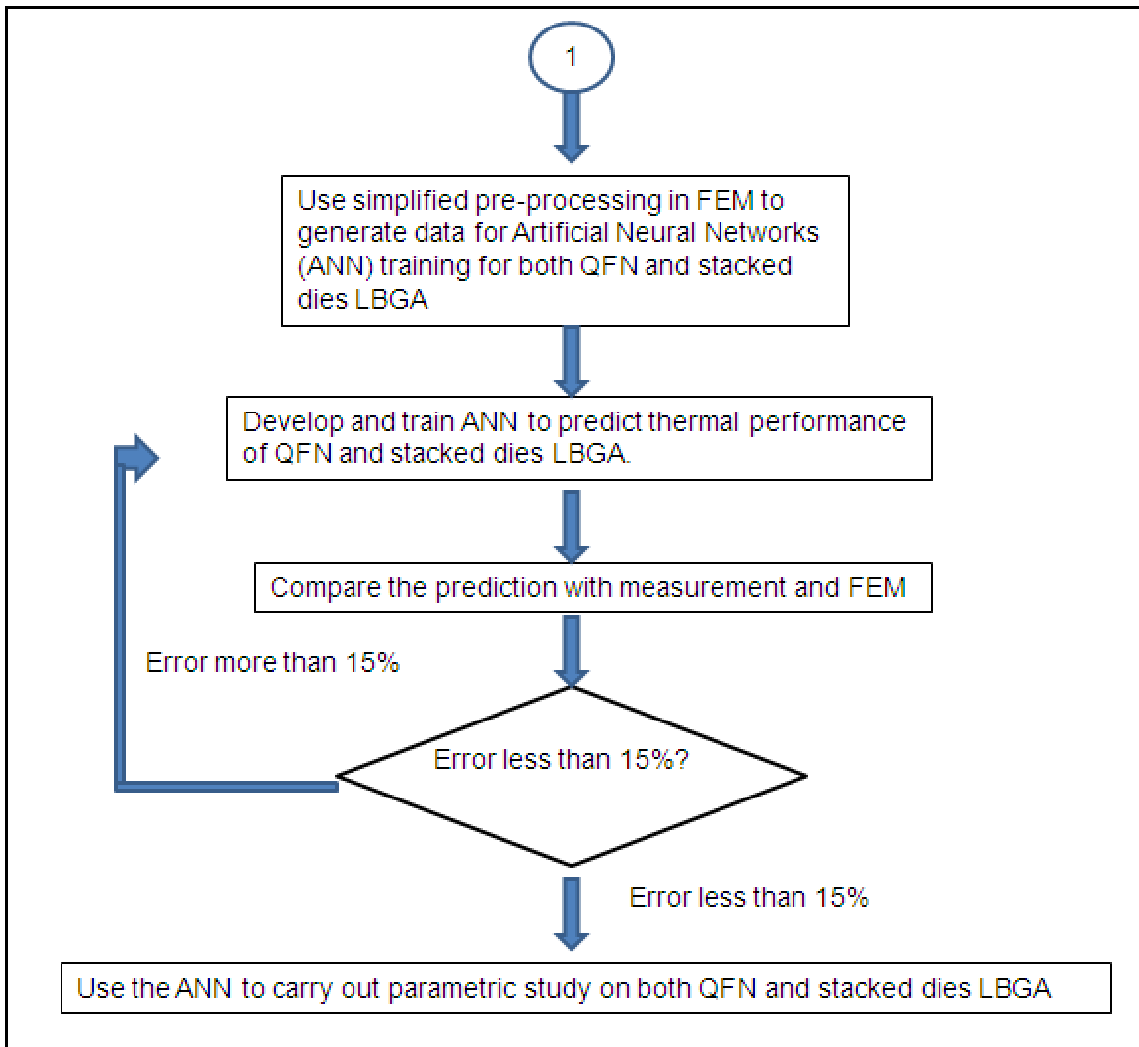


Figure 1.7: Flow chart of the framework of the project.

CHAPTER 2
LITERATURE SURVEY

2.0 Overview

In this section, literature survey and the summary of the literature survey will be presented in this chapter. The main contents in this chapter are:

- Overview of electronic packaging technology
- Overview of thermal management in electronic packaging
- Numerical method of thermal analysis for single die electronic packaging
- Numerical method of thermal crosstalk analysis for stacked dies electronic packaging
- Application of Artificial neural networks in electronic packaging

2.1 Overview of electronic packaging technology

2.1.1 Introduction

Electronic packaging is a technique of building electrical interconnects and mechanical structure to encase the electronic components such as integrated circuit so that they could reliably and functionally be integrated into electronic system and products. The functions of electronic packaging are providing physical isolation and protection of IC from mechanical shock and vibration, thermal cycling, moisture and corrosion which are exist in environment. Electronic packaging also offers integrity and distribution of signal to next level of electronic system. Heat dissipation and thermal management is also built within the package to ensure that IC is operating at suitable temperature.

2.1.2 Single die electronic packaging

There are various types of single die electronic packaging in the market and they are generally divided into leadframe packages, laminated packages, leadless

packages and chip scale packages. This section will discuss briefly on each of this common packages and their advantages and disadvantages.

Leadframe packages are one of the earliest techniques in electronic packaging. The chip is mounted inside the leadframe, and wirebond connects the chip to the long leads. There are 2 type of assembly of this package to the second level which are insertion mount (e.g. Dual In-line Package (DIP)) and surface mount (e.g. Quad-Flat-Package (QFP)). The long leads induce parasitic inductance and power losses. In high frequency applications, leads tend to cause impedance mismatch. Hence, in today complex hand held electronic devices, where space is limited and higher pin counts is mandatory, the leadfame packages popularity fade away. Figure 2.1 shows the leadframe family of electronic packages.

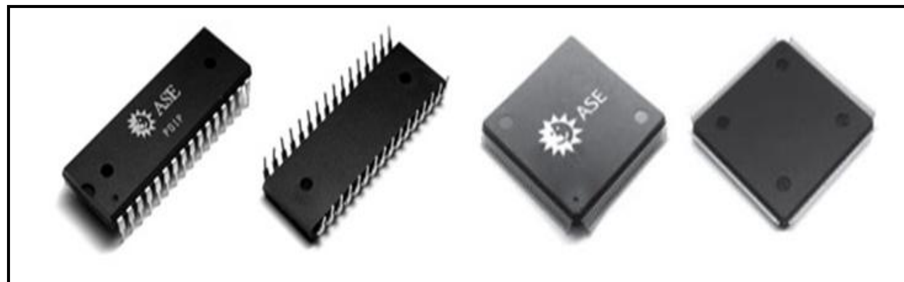


Figure 2.1: PDIP and QFP packages (www.asetwn.com.tw)

Laminate packages rapidly replaced leadframe packages in late 1980s due to leadframe packages' pin count limitation and electrical performance. The example of this type of electronic package is Ball Grid Array (BGA) which is a potential low-cost packaging solution to achieve miniaturization in electronics. Figure 2.2 shows the BGA type of electronic packages. BGA packages had been adopted easily into electronic system due to their high pin counts and flexibility for redistributions within the package. The die can be attached on the substrate and connected using wire bonding technology or flip chip bumps. Conductor layers, ground planes and power planes can

be structured within the BGA substrate which is important for high pin counts application where common supply of voltages distribution and current return path to the die need to be constructed. To connect different layers within substrate, vias are drilled and plated with thin copper. However, laminated packages are cost intensive package type which substrate alone consumes up to about 70% of all assembly cost. When cost is concern, leadframe packages and leadless packages will be costly effective for electronic packages with pin counts lowers than 250. Without proper design, BGA is not a suitable package for high frequency application because conductors on the substrate layers show high inductance.

Figure 2.2: Laminate type of packages BGA (www.amkor.com)

Leadless packages such as QFN (Quad Flat Non-lead) and LGA (Land Grid Array) are superb candidates for high frequency application (Scheuenpflug, 2003). The smallest available package size is 2mm x 2mm and the contact is thin which will decrease inductance, hence it can be used in high frequency application in the GHz range. In leadless packages like QFN, the chip can be directly attached to the paddle and act as heat sink and reduce the thermal resistance. Another advantage of this type of package is low cost with high manufacturing yield. However, the leadless packages are only suitable for low and medium pin count application. Figure 2.3 shows family of leadless packages.

Figure 2.3: Leadless packages (www.statchippac.com)

The demand of higher density and more functionality within a small area in mobile devices gave birth to new electronic packages. The innovation of chip-scale packages (CSP) had been emerged in late 1990s and resulted in reduction of real estate of board. CSPs are only 20% larger than the original die and can be mounted directly to the board. Thin film technology can be utilized to deposit the metallization or dielectric layer on the die during wafer level. The redistribution concept can be applied on CSPs and impedance matched transmission line can be realized for high frequency applications. The major advantages of this technology are the signal traces are very short, package dimension is small and the material cost is more cost effective. However, thermal management and long term solder joint reliability due to CTE mismatch is a culprit for the larger and high power applications. Figure 2.4 shows the CSP.

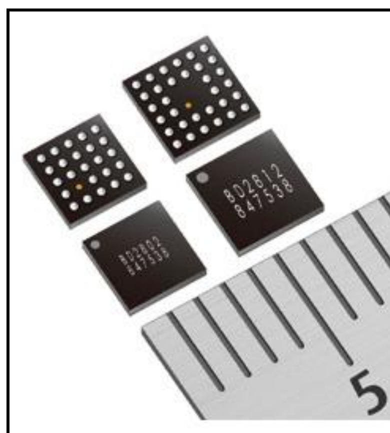


Figure 2.4: Chip-scale packages (www.rohm.com)

2.1.3 Stack dies electronic packaging

Stack dies electronic packaging is one of the product family of System in Package (SiP). INEMI define SIP as: “System in Package is characterized by any combination of more than one active electronic component of different functionality into a single standard package that provides multiple functions associated with a system or sub-system.” Over 85% of SiPs are used recently in mobile phone and the growth is about 10% through 2004 to 2010 (Mahadevan, 2009). The electronic packaging market moves towards SiPs due to its increase of functionality and in parallel with increase of miniaturization. The increasing trend of hand held portable mobiles drives the dramatic demand of the SiPs. Figure 2.5 show the main board of Apple Iphone 4 containing several of stacked dies packages.

Mixing flip chip technique and wirebonding has been used as the interconnection in the electronic packaging industry because this interconnection technology can be built using the existing conventional equipment and low cost manufacturing. Figure 2.6 shows the cross section of the stacked dies packages for combined flip chip and wirebond. Another industrialized electronic packages structure are pyramidal (top die smaller than bottom die or bottom die is smaller than top die) such as in Figure 2.7 and twin die (equal in size) such as in Figure 2.8. For the equal die size, a spacer or interposer is needed to separate the dies for the wire bonding clearance.

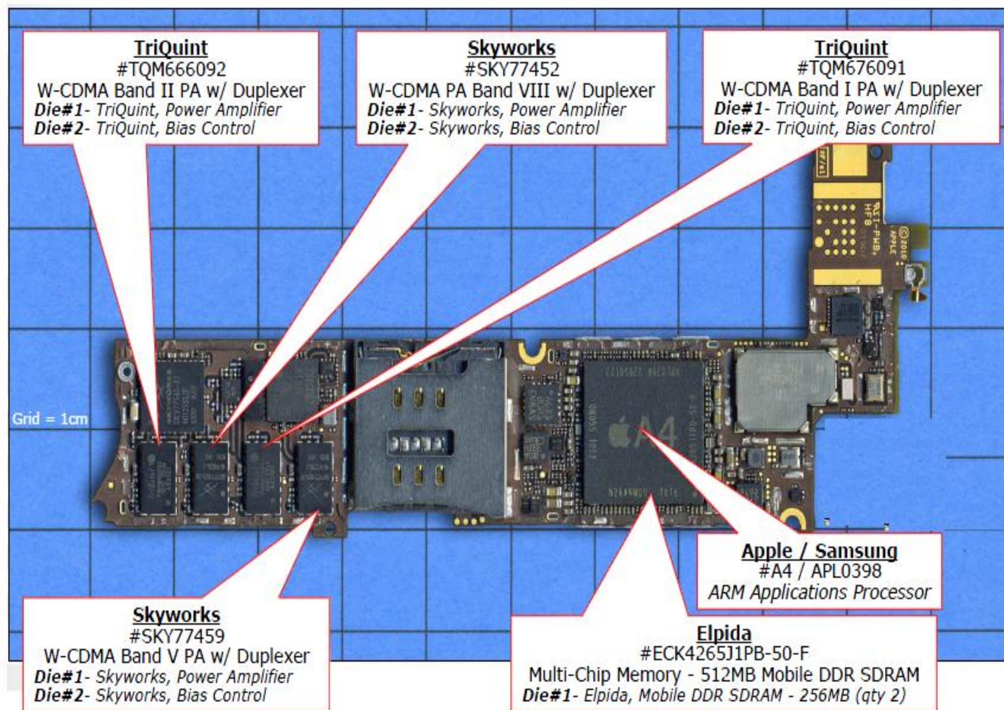


Figure 2.5: Apple iphone 4 main board. (www.teardown.com)

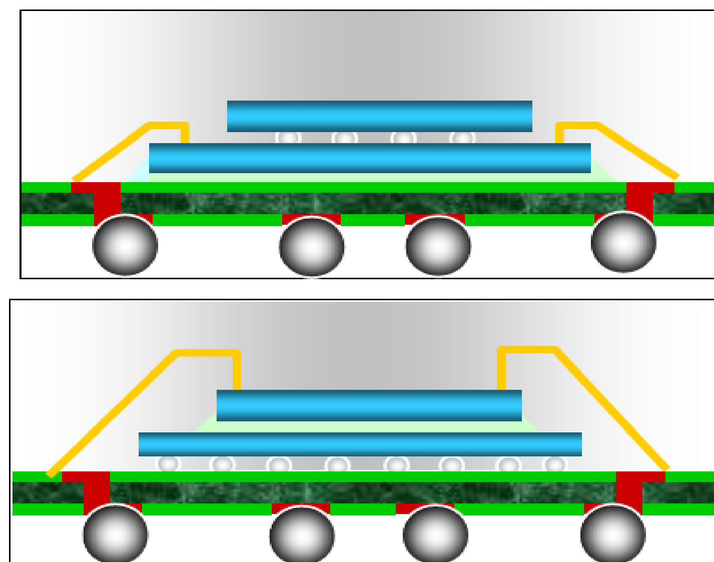


Figure 2.6: Stacked dies packages with mixed wire bonding and flip chip (Tong et al., 2006)

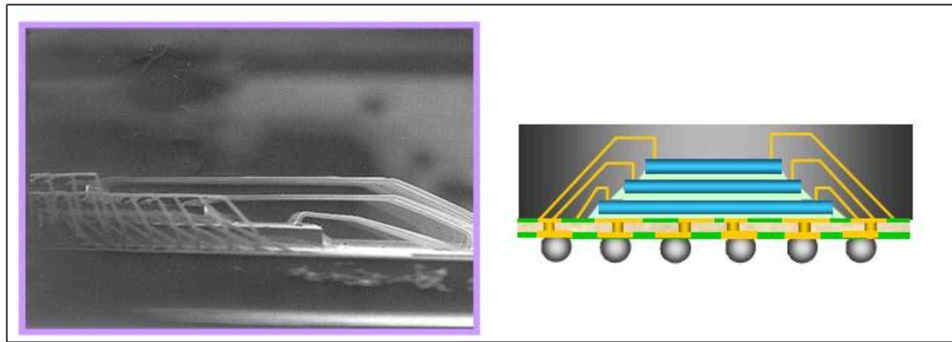


Figure 2.7: Pyramid type of stacked dies (Tong et al., 2006)

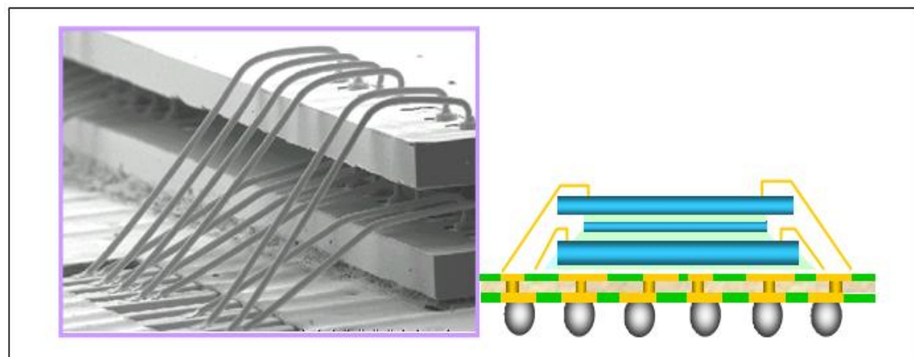


Figure 2.8: Twin stacked dies with spacer (Tong et al., 2006)

In today's electronic packaging industry, standard maximum package height for stacked die BGA ranges from 1.0 mm to 1.7 mm. To enable more dies to be stacked in a single package, the technology on wafer-thinning has been used. The challenge to reduce the die until 50 – 75 μm in thickness is critical in this package type. Hence, back grinding and handling process become the key success for stacking more dies. Some packaging houses proposed polishing process to further enhance the mechanical strength of the wafer.

2.2 Thermal management in electronic packaging

2.2.1 Introduction

Thermal management in electronic packaging is essential to ensure that the electronic package can operate reliably under its operating condition and environment.

To enable a good thermal design, the heat transfer mode in electronic packaging needs to be studied first. Then, in this section, characterization of thermal transfer and thermal measurement method will be discussed. Lastly this section will discuss the recent development in numerical method for thermal analysis for electronic packaging.

2.2.2 Heat transfer mode in electronic packages

Heat is generated when the electrical current passed through the active and passive devices. When the demand for higher frequency and higher power density for electronic devices is increasing, electronic package designer is forced to consider the efficiency of transferring the thermal energy away from the device or die. To enable the steady-state operating temperature of the device as low as possible, the understanding of heat transfer modes occurred in electronic packages is essential. The dominant modes of heat transfer in electronic packaging are conduction and convection. Therefore, radiation heat transfer mode will be neglected.

Conduction happens when heat energy transfer in a medium by random motion and vibrating molecules to the neighboring molecules from higher temperature to lower temperature. The molecules with higher energy due to higher temperature will transfer the energy to less energetic molecules. Fourier's law define that in any given direction, the rate of heat flow is proportional to the cross-sectional area (perpendicular to the direction of heat flow) and to the gradient of temperatures in that but inversely proportional to the distance between the temperature difference. Fourier's law can be expressed in mathematic formulae as below:

$$Q_x = -K_x A_c (dT/dx)$$

where Q_x is conduction heat flow rate at x direction; K_x is thermal conductivity of the medium in x direction; A_c is the cross section area which is perpendicular to the x direction and dT is temperature difference across the distance of dx

Convective heat transfer of convection occurs due to heat energy transfer from one place to another by random motion or bulk motion of particles in the fluid. Convection can be divided into natural or free convection and forced convection. Free convection happens when movement of the fluid occurs due to the changes of the fluid density when subjected to temperature difference. Warmer fluid when subjected to higher temperature with lower density will buoy and replaced by cooler fluid. Forced convection happens when heat from heated area transferred by the fluid movement mechanism which is caused by driving force. In convection, the heat flow is proportional to the temperature difference between the surface and fluid, and to the surface area. The mathematical expression for this Newton's law of cooling is given by

$$Q_{conv} = hA_s(T_s - T_\infty)$$

where Q_{conv} is heat flow rate due to convection, A_s is the surface area of the heat flow, T_s is temperature of the surface, T_∞ is the temperature of the fluid and h is the heat transfer coefficient. The heat transfer coefficient influenced by surface geometries, properties of fluid and velocity of the fluid around the surface subjected to the heat loss.

Radiation heat transfer occurs due to the emission of electromagnetic waves by the body or matter. Unlike conduction and convection, radiation heat transfer mechanism does not require physical medium between two bodies. Only electromagnetic wavelength in the range of 0.1μm to 100μm contributes to thermal energy transport (Remsburg, 2001). The net rate heat flow for a small surface exchanging radiation with large surroundings at a uniform temperature can be represented with mathematical expression:

$$Q_{rad} = \varepsilon \sigma A_s (T_s^4 - T_\infty^4)$$

Where ε the surface emissivity, σ is is Stephan-Boltzmann constant (5.67 x 10^{-8} W/m^2.K^4), A_s is surface area , T_s is the surface temperature and T_∞ is the temperature of surroundings.

2.2.3 Thermal characterization of overall heat transfer

Figure 2.9 shows typical heat transfer in the electronic packaging. The heat energy will be conducted through the chip to the electronic package body. Then the heat will be transferred from the package body to the heat sink through conduction and converted from heat sink or external board to environment through convection and radiation. Heat will also be transferred through top chip to the top package and converted or radiated to ambient environment.

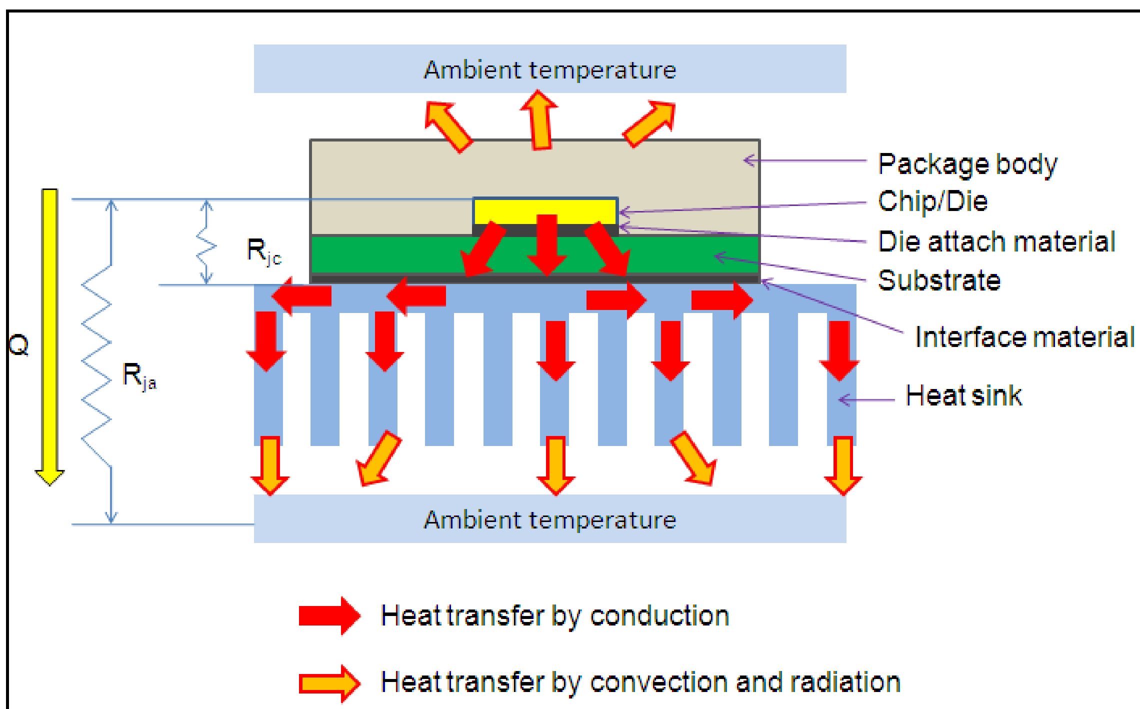


Figure 2.9: Overall characterization of electronic package

The two parameters that are typically used to characterize heat transfer in single die electronic packages are the junction-to-case resistance, R_{jc} or Θ_{jc}, and the junction-to-ambient resistance, R_{ja} or Θ_{ja}. R_{jc} is defined as the difference between the

source (chip) temperature and the average package casing temperature, per unit of heat *Q* that is conducted through the package. R_{ja} is the difference between the source (chip) temperature and the ambient temperature, per unit of heat dissipated by the package.

2.2.4 Thermal measurement method

Many IC packaging failure have been traced to the rate of temperature change, temperature cycle magnitude or absolute temperature. Some of the circuit performance is highly sensitive to the operating temperature. Hence, thermal measurement and characterization have become essential during the development of electronic packaging. There is standard way of thermal measurement for single die electronic packaging which has been outlined by JESD51 series. However, stacked dies electronic packaging induces complexity and difficulty using conventional standard in JESD51.

Altet et al. (2002) had investigated four different approaches for the measurement of IC surface temperature, which are scanning thermal microscope, laser reflectometer, laser interometer and electronic built in differential sensors. All the techniques are able to detect the hot spot of the defective die and the paper concluded that these techniques can be automated or partially automated and they achieved remarkable sensitivity which is not reach by conventional IC temperature testing.

Zahn (2004), Zhang et al (2004), and Krishnamoorthi et al. (2007) had extended the measurement method to be used in stacked dies electronic packaging. Krishnamoorthi et al. (2007) performed thermal evaluation of two die stacked FBGA (D2-FBGA) with identical die structure. Experiment had been carried out to measure the temperature rise of top and bottom dies by activating one die in a time. The linear super position matrix formulation is generated using the experimental data to identify

the changes of temperature rise between the dies when the various temperature distributions are applied on each die.

Thermal measurement and experiment setup to measure thermal resistance and temperature gradient need huge investment and intensive labor time. Hence, numerical method had been used to estimate these variables. Over a decade, the virtual prototyping of thermal design has been progressed from basic analytical and semi-empirical to predict the thermal performance of simple system to complex numerical for system level of electronic devices. The numerical method will be further discussed in section 2.3 which will have advantages compared to measurement and experiment.

2.3 Numerical method in thermal analysis for single die electronic packages

The thermal characterization using experiment needs significant amount of investment and labour time. There are readily available standardized procedures for thermal measurement in JEDEC. However, due to computational power increased, there are numerical tools which permit the simulation of standardized procedures. These numerical simulations help to reduce physical prototyping to verify the optimized packaging solutions. Most of the software in the market are built around using 2 popular numerical methods which are finite element method FEM and Computational Fluid Dynamic (CFD).

The approach of finite element method is restricted for solid modeling of conductive heat transfer. To enable approximation of heat transfer through convection, heat transfer convective or natural coefficients are applied on the cooling surfaces of electronic packaging which are derived from flat plate correlations. Ellisons (1989) published the correlations to obtain free and forced convection for electronic package. Zahn et al. (1997) developed isothermal and Isoflux natural convection coefficient