DESIGN OF TUNABLE SINGLE BAND AND CONCURRENT LOW NOISE AMPLIFIER

by

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TABLE OF CONTENTS

CHAPTER 3: LITERATURE REVIEW

CHAPTER 4: DESIGN METHODOLOGY

CHAPTER 5: RESULT AND DISCUSSION

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS

AC	Alternating-Current
ADC	Analog to Digital Converter
AI	Active Inductor
BiCMOS	Bipolar Complementary Metal Oxide semiconductor
BPF	Band-Pass Filter
BW	Bandwidth
CG	Common-Gate
CMOS	Complementary Metal-Oxide-Semiconductor
CNM	Classical Noise Matching
CS	Common-Source
dB	Decibel
DC	Direct-Current
GHz	Gigahertz
GPAPU	General Purpose Analog Programmable Unit
GSG	Ground-Signal-Ground
GSM	Global System for Mobile
HBT	Heterojunction Bipolar Transistor
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
IF	Intermediate-Frequency
IIP2	Input-Referred Second-Order intermodulation point
IIP3	Input-Referred Third-Order Intermodulation Point
IM	Inter-Modulation
ISD	Inductive Source Degenerated
LNA	Low Noise Amplifier

LO	Local Oscillator
LPF	Low-Pass Filter
MHz	Megahertz
NF	Noise Figure
NMOS	N-Metal Oxide Semiconductor
OIP3	Output-Referred Third-Order Intermodulation Point
PCNO	Power-Constrained Noise Optimization
PCSNIM	Power-Constrained Simultaneously Noise and Input Matching
PDK	Process Design Kit
PLS	Post-Layout Simulations
PMOS	P-Metal Oxide Semiconductor
PSS	Periodic Steady State
Q-factor	Quality Factor
RC	Resistor-capacitor
RF	Radio-Frequency
RLC	Resistor-inductor-capacitor
SiGe	Silicon Germanium
SNIM	Simultaneous Noise and Input Matching
SOC	System-on-Chip
S-parameters	Scattering Parameters
UWB	Ultra Wide Band
VLSI	Very Large-Scale Integration
WCDMA	Wide-band Code Division Multiple Access
WLAN	Wireless Local Area Network

REKA BENTUK JALUR TUNGGAL BOLEH TALA DAN SEREMPAK PENGUAT HINGAR RENDAH

ABSTRAK

Penguat hingar rendah (LNA) merupakan kunci utama binaan blok rantaian penerimaan kerana ia bertujuan untuk menguatkan isyarat sambil menambah hingar seminima yang mungkin. Sehubungan itu, beberapa jenis teknik bagi meminimumkan hingar LNA diperkenalkan. PCSNIM (kuasa terhad dengan hingar dan input sepadan serempak) dilihat antara teknik yang banyak diberikan perhatian. Namun, berdasarkan kepada kajian sebelum ini, ia menghadkan keupayaan gandaan LNA. Bagi menyelesaikan permasalahan ini dan menyokong keperluan pelbagai jalur, tesis ini mempersembahkan empat jenis rekaan LNA (LNA1 hingga LNA4) berdasarkan sumber induktif merosot (ISD) untuk meliputi jalur tunggal (contoh: IEEE802.11.b/g, Bluetooth) dan serempak (contoh: WIFI). LNA1 disasar untuk menyelesaikan isu gandaan yang rendah bagi jalur tunggal LNA dengan penambahbaikan pada keluarannya. Bagi mendapatkan penerimaan serempak untuk dua jalur frekuensi (24.5/5.2 GHz piawaian WIFI), LNA3 direka berasaskan topologi yang sama untuk LNA1. LNA ini dilaksanakan dalam struktur penuh-bersepadu untuk menyahkan penggunaan komponen luaran cip. Rekaan LNA2 dan LNA4 terhasil daripada masalah anjakan frekuensi selepas proses fabrikasi LNA1 dan LNA3. Bagi menangani isu ini, struktur boleh tala menggunakan varaktor digunakan pada padanan masukan/keluaran LNA2 dan sistem baru GPAPU (unit analog boleh program kegunaan umum) diperkenal dan dilaksana kepada struktur penguat boleh tala-serempak (LNA4). Kesemua kaedah dibuktikan secara simulasi dan pengukuran. LNA1, LNA2 dan LNA3 difabrikasi menggunakan teknologi 0.13 µm CMOS manakala LNA4 direka hanya pada tahap pra susun atur simulasi. Untuk LNA1, pengukuran gandaan hadapan dan hingar memberikan nilai 19.84 dB dan 2.59 dB. Bagi masukan/keluaran sepadan, nilai diperolehi adalah -9.39 dB dan -39.23 dB. LNA1 menggunakan arus terus 4 mA daripada bekalan kuasa 1.2 V. Sementara itu, terdapat

anjakan frekuensi sebanyak 260 MHz pada keluaran LNA1. Ini disebabkan proses toleransi semasa fabrikasi. Nilai pengukuran bagi gandaan hadapan dan hingar bagi LNA2 adalah 14.62 dB dan 3.73 dB dengan kuasa arus terus 5 mW. Untuk julat talaan, 140 MHz pada masukan dan 50 MHz pada keluaran berjaya dicapai untuk padanan masukan/keluaran. Berdasarkan kepada struktur talaan varaktor pada masukan dan keluaran LNA2, nilai dapatan (terutamanya NF) berubah-ubah bergantung kepada padanan masukan/keluaran. Ini bertujuan untuk mencapai fungsi boleh tala jika dibandingkan dengan LNA1. Nilai pengukuran yang diperoleh bagi gandaan hadapan LNA3 ialah 17.11 dB pada 2.45 GHz dan 10.42 dB pada 5.2 GHz dengan kuasa arus terus 4.8 mW. Nilai pengukuran bagi padanan masukan dan keluaran pula adalah -19.48 dB dan -39.23 dB bagi jalur rendah manakala -25.51 dB dan -10.46 dB bagi jalur tinggi. Nilai hingar yang diukur untuk LNA3 ialah 4.09 dB pada jalur rendah dan 10.47 dB untuk jalur tinggi. Nilai yang diperoleh bagi bacaan gandaan dan nilai hingar berbeza daripada jangkaan awal. Ini kerana, terlihatkan anjakan frekuensi sebanyak 1 GHz pada jalur atas yang dipengaruhi oleh proses perubahan semasa fabrikasi. Daripada hasil simulasi, LNA4 menunjukkan gandaan hadapan yang dicapai bagi jalur rendah ialah 21 dB dan jalur tinggi 18 dB. Untuk nilai hingar, 2.53 dB diperolehi bagi jalur rendah dan 2.96 dB bagi jalur tinggi dengan kuasa arus terus 5.5 mW. Bagi rangkaian keluaran untuk LNA4, julat nilai boleh tala yang diperolehi ialah 300 MHz. Kesimpulannya, kaedah penambahbaikan gandaan yang digunakan bagi LNA1 berfungsi dengan jayanya dan isu nilai gandaan yang rendah berasaskan teknik PCSNIM dapat diselesaikan. Begitu juga masalah anjakan frekuensi dalam penguat jalur tunggal diatasi menggunakan struktur boleh tala LNA2. Tambahan pula, penguat PCSNIM serempak penuh-bersepadu (LNA3) yang direka dan dilaksanakan berjaya menerima frekuensi-frekuensi bagi piawaian WIFI secara serempak. Akhir sekali, struktur boleh tala yang baru (GPAPU) diperkenalkan dan terbukti berfungsi berdasarkan kepada keputusan simulasi LNA4.

DESIGN OF TUNABLE SINGLE BAND AND CONCURRENT

LOW NOISE AMPLIFIER

ABSTRACT

Low noise amplifier (LNA) is one of the key building blocks in receiving chain as they aimed to amplify the signal while adding minimum possible noise to it. Thus, several noise optimization techniques were proposed by researchers to minimize the noise of LNAs. Among these techniques, the PCSNIM (power constrained simultaneous noise and input matching) is found to be a popular approach; however, it limits the gain of the LNA according to literature. Therefore, to tackle the mentioned issue and to support the requirement for multi-band, this thesis presents the design of four LNAs (LNA1 to LNA4) based on inductive source degenerated (ISD) to cover single-band (e.g. IEEE 802.11.b/g, Bluetooth) and concurrent (e.g. WIFI) applications. LNA1 is targeted to solve the reduced-gain issue of single-band LNA by utilizing a gain-enhancer at the output of LNA. To obtain the concurrent reception of two frequency bands (2.45/ 5.2 GHz in WIFI standard), LNA3 is designed based on the same topology of LNA1. This LNA is implemented in fully-integrated structure to eliminate the off-chip components. Meanwhile, the design of LNA2 and LNA4 are resulted from the problem of frequency shift that occurred after the fabrication of LNA1 and LNA3. Hence, to tackle the issue, a tunable structure using varactors is used at the input/output matching of LNA2 and a new system (GPAPU-general purpose analog programmable unit) is introduced and implemented to the concurrent structure to obtain the tunable-concurrent amplifier (LNA4). For this work, LNA1, LNA2, and LNA3 were fabricated in 0.13 µm CMOS technology while LNA4 was designed only up to pre-layout simulation level. The measured forward gain and noise figure (NF) values for LNA1 are 19.84 dB and 2.59 dB respectively, while achieving the input/output return losses of -9.39 dB and -39.23 dB. LNA1 consumes 4 mA of dc current from 1.2 V supply. Meanwhile, 260 MHz frequency-shift was observed at the output of LNA1 due to the process tolerances

during fabrication. The measured forward gain and NF values of LNA2 are 14.62 dB and 3.73 dB respectively, while consuming 5 mW of dc power. Moreover, the tuning ranges of 140 MHz at the input and 50 MHz at output are accomplished by LNA2 for the input/output matching. Due to the varactor-based tuning structure at the input and output of LNA2, the gain (and respectively NF) was traded-off with input/output matching to achieve tunable function comparing to LNA1. LNA3 is measured with the forward gain values of 17.11 and 10.42 dB at 2.45 and 5.2 GHz frequencies respectively, while consuming 4.8 mW of dc power. Also, the obtained values for input and output return losses are -19.48 and -39.23 dB respectively at the lower band and -25.51 and -10.64 dB respectively at upper band. The measured NF of this LNA3 is 4.09 dB at the lower-band and 10.47 dB at the upper band. The achieved gain and NF are different from the expected simulation results due to the observed 1 GHz frequency-shift at upper-band due to process variation during fabrication. From the simulation results of LNA4, the forward gain values obtained for lower and upper bands are 21 and 18 dB respectively. Also, the achieved NF values are 2.53 and 2.96 dB respectively in the mentioned bands while consuming 5.5 mW of dc power. In addition, the output network of the LNA4 can be tuned in range of 300 MHz. In conclusion, the implemented method of gain-enhancer in LNA1 works perfectly and the reduced-gain issue of PCSNIM technique is solved. Also, the problem of frequency-shift in single-band amplifier was tackled using the tunable structure of LNA2. Furthermore, a fully-integrated concurrent PCSNIM amplifier (LNA3) is designed and implemented successfully to receive simultaneous frequency bands of WIFI standard. Finally, a new tunable structure (GPAPU) was introduced and theoretically proved to be functional based on the simulation results of LNA4.

CHAPTER 1

INTRODUCTION

This chapter provides an introduction to this research work and explains the motivations and challenges on the state of the art in LNA design. Then, the problem statements, objectives, scope and contributions of this work are discussed. Finally, an overview of the thesis organization ends this chapter.

1.1 Introduction to Wireless Standards

The history of radio communication starts from early 20th century when Guglielmo Marconi successfully established the first radio contact over the Atlantic Ocean (Vidojkovic, 2008). The prospect of this demonstration predicted an exciting future for telecom industry by replacing the wired telegraph and telephone communication with radio waves. The developments of Shannon's information theory and the concept of cellular systems along with the invention of transistor, paved the way for low-cost wireless communications. Furthermore, due to the computer-aided design and powerful IC design tools (e.g. Cadence IC design suite) and utilizing new techniques (e.g. photolithography); the dream of very large-scale integration (VLSI) of the transistors on a tiny piece of silicon die became true. These developments lead to cost-effective mass production of the electronic components and system on-chips (SOCs) that allows people to enjoy low-cost wireless communication (Razavi, 1998; Tasić, Serdijn, & Long, 2007).

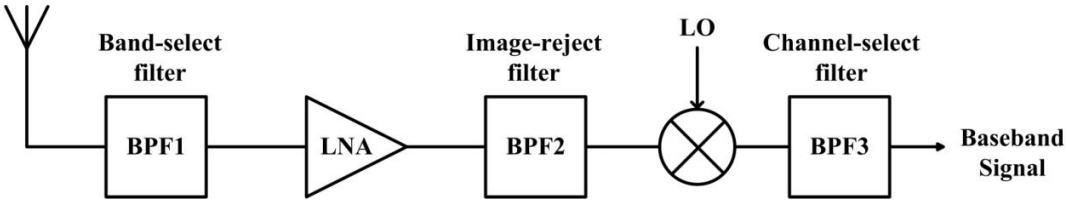
According to the increasing market demands for wireless services and the variety of wireless applications, many standards have been developed to fulfill the user's requirements by the standardization committee. Table 1.1 shows some of the famous standards with their specifications as: centre frequency, bandwidth, duplex type, data rate, modulation and the receiver architecture. For instance, Bluetooth standard is defined to work at 2.44 GHz centre frequency and it needs to cover a bandwidth range of 80 MHz (from 2.4 to 2.48 GHz). It

uses TDD (Time Division Duplexing scheme) and GFSK (Gaussian Frequency Shift Keying) modulation. In addition, the data rate of Bluetooth is 0.723 Mb/s and it can be down-converted using both low-IF and zero-IF architectures.

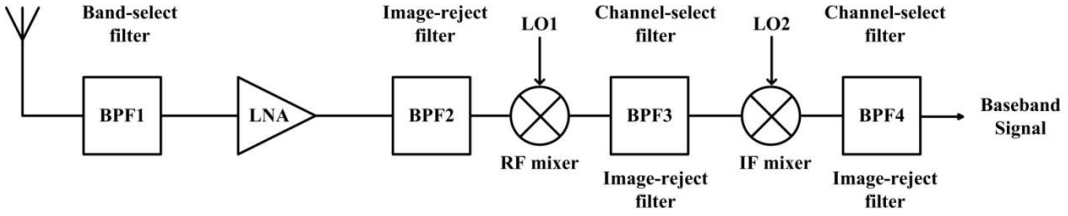
Table 1.1: Wireless standards (Tasić, Serdijn, & Long, 2007).

Standard	**Freq (GHz) /BW (MHz)**	**Duplex**	**Data Rate**	**Modulation**	**Architecture**
GSM	0.947 / 25	FDD	14.4 kb/s	GMSK	zero-IF/high-IF/low-IF
DCS1800	1.842 / 75	FDD	14.4 kb/s	GMSK	zero-IF/low-IF/high-IF
IS-95	1.96 / 60	FDD	14.4 kb/s	QPSK, OQPSK	high-IF
WCDMA	2.14 / 60	FDD,TDD	2-10 Mb/s	QPSK, 16QAM,	zero-IF
WCDMA 3GPP	1.967 / 115	TDD	2-10 Mb/s	QPSK, 8PSK	zero-IF
DECT	2.44 / 80	TDD	1.152 Mb/s	GFSK	low-IF zero-IF/high-
Bluetooth	2.44 / 80	TDD	0.723 Mb/s	GFSK	low-IF/zero-IF
802.11b(g)	2.44 / 80	TDD	11(54)Mb/s	BPSK, QPSK (OFDM)	zero-IF low-IF/high-IF
802.11a	5.15-5.825	TDD	54 Mb/s	BPSK, QPSK	zero-IF low-IF/high-IF
UWB	3-10 / NA	-	600 Mb/s	BPSK, QPSK, OFDM	-
ZIGBEE	2.44 / 80	-	250 kb/s	QPSK	-

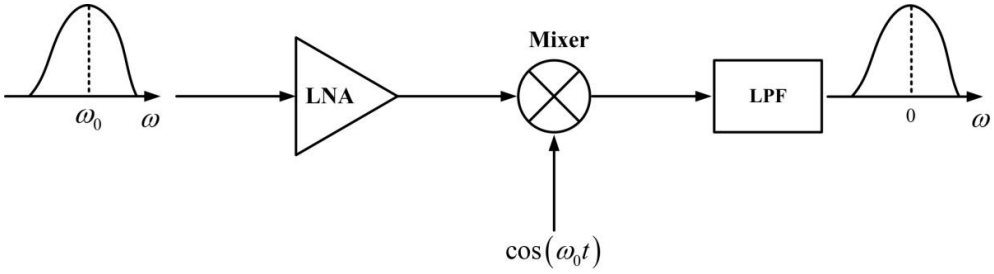
Based on the mentioned wireless standards, many receiver structures (Figure 1.1), including but not limited to, heterodyne, super-heterodyne, homodyne and concurrent have been introduced to respond to the user's requirements in both single-band and multiband applications.



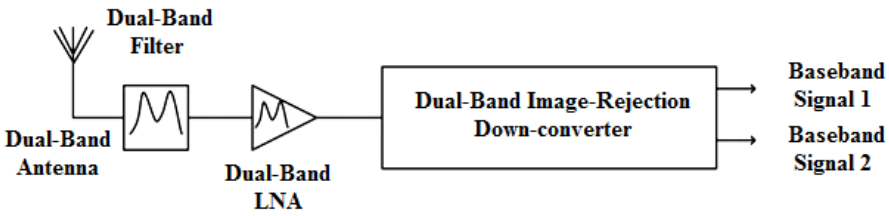
(a)



(b)



(c)



(d)

Figure 1.1: Receiver structures; (a) Heterodyne (Tasić, et al., 2007), (b) Super-heterodyne (Tasić, et al., 2007), (c) Homodyne (Razavi, 1998), (d) Concurrent (Hashemi & Hajimiri, 2002).

Generally, the receiving process of the RF signal can be divided into two main tasks as: amplification and down-conversion. According to Figure 1.1, in most of the proposed topologies, low noise amplifier (LNA) is the first active block after the antenna in receiving path. Therefore, the main role of the LNA is to amplify the RF signal while adding as less as

possible noise to it. In some structures (e.g. heterodyne), LNAs are followed by a band-selection filter at the input and an image-rejection filter at the output. The former enables LNA to select and amplify the desired range of frequency and the latter helps to suppress the unwanted interferences from the adjacent channels (Tasić, et al., 2007). Then, the received signal is passed to down-converter which is usually consists of a mixer and local-oscillator. Depending on the used architecture, one or few down-conversion steps are carried out (by receivers) to prepare the signal for baseband section.

In this research work, the interest is on first task of the receiver (low-noise amplification of the RF signal), therefore, some design methodologies are presented in order to investigate the existed issues in amplification step.

1.2 Motivations on LNA Design

Typically, the first active block (after antenna) in receiving chain is a low noise amplifier (LNA) and its main duty is to amplify the received signals without adding any noise to them. Also, the level of amplification (gain of the LNA), should be high enough to overcome the noise of subsequence stages.

Undoubtedly, the noise figure (NF) is the most important parameter in LNA design procedure, as it contributes to the overall noise performance of the receiver. In addition, the sensitivity of the receiver is also determined by the NF and gain of LNA (Lee, 2004).

According to the receiver's architecture (such as super heterodyne), it is necessary to implement some filters at the input and output of LNA (for instance, band-selection and image-rejection filters). Therefore, it is essential to consider the impedance matching requirements in order to maximize the transferred power from source to load (Li, 2012). On the other hand, the optimum noise impedance point is different from proper input matching point. Hence, important trade-offs between noise matching and input matching of LNA

should be taken into the account during the design optimization process (Nguyen, Kim, Ihm, Yang, & Lee, 2004).

LNA also plays an important role in the linearity performance of the system (Lee, 2004), it should accommodate large signals without distortions. Meanwhile, it needs to maintain high stability and isolation to prevent oscillations.

Finally, the power consumption and the size of the LNA should be accounted during the design procedure; as the former determines maximum swing (linearity), gain and noise performance of the LNA (Razavi, 1998) and the latter impacts the costs of implementation.

From above discussion, it can be inferred that LNA is one of the most interesting and challenging circuits as its performance parameters involved with critical trade-offs (e.g. gain, noise, matching, linearity and power consumption).

1.3 Problem Statement

Inductive source degenerated (ISD) cascode is one of the popular LNA topologies that used in both single-band and multiband applications. Although the LNAs based on this topology achieve high-gain, but their noise performance needs further improvements. Thus, several optimization techniques (see Section 2.5.2) have been proposed by researchers to minimize the noise factor of these LNAs. The PCSNIM (power constrained simultaneous noise and input matching) method is found as an appropriate approach compared to the other techniques for this work. But, the gain performance of LNA is degraded utilizing this technique, because of the additional components at the input of the LNA (Hashemi & Hajimiri, 2002) as well as the generated parasitic after the physical implementation. Therefore, it is important to modify the topology in order to alleviate this gain issue while maintaining the simultaneous noise and input matching under the power constraint.

Another prevalent problem in single-band LNAs is the shift of frequency from desired operating point. The main reason of this issue is not pointed clearly in available literatures; but, the PDK (process design kit) model uncertainties, fabrication process variations and in-complete modeling of parasitic (especially at high frequencies) can be named as the culprits of this issue in single-band amplifiers. Furthermore, this problem is not only affecting the single-band LNAs but also degrades the performance of concurrent structures. Therefore, it is essential to implement a mechanism to enable frequency tuning post fabrication while maintaining the performance parameters of both LNAs.

Finally, based on the limited number of fixed-air probes during the measurement of the tunable-LNA, it was not feasible to connect as many as desired control voltages to tune the circuit at the desired mode. This issue is highlighted more, when a capacitor (or resistor) switch-bank is implemented into the LNA as it requires more control bits. Therefore, it is necessary to design a tunable structure with minimum number of tuning voltages with no penalty on noise, gain and power consumption of the LNAs.

1.4 Research Objectives

- To design and implement a single-band PCSNIM LNA with enhanced gain performance for IEEE 802.11.b/g (2.45 GHz) applications.
- To design and implement a fully-integrated PCSNIM concurrent LNA for WIFI (2.45/5.2 GHz) applications.

1.5 Scope of the Work

In this research, after a brief review on background knowledge of LNA design and related literature, the design methodologies of four LNAs for single-band and concurrent applications are presented. Three of the LNAs (single-band, tunable and concurrent) are targeted for fabrication and measurements while the new tunable-concurrent LNA is designed (up to pre-layout step only) as a theoretical proof of the idea. Also, for each design,