A 0.13-µm CMOS RECONFIGURABLE POWER CONSTRAINED SIMULTANEOUS NOISE AND INPUT MATCHING (PCSNIM) LOW NOISE AMPLIFIER (LNA) FOR MULTI-STANDARD 0.9, 1.8 AND 2.1 GHz MOBILE APPLICATION

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by

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DECLARATION

I hereby declare that the work in this thesis is my own except for quotations and summaries which have been duly acknowledged.

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LIST OF ABBREVIATIONS

2G	Second-generation wireless telephone technology
3G	Third generation of mobile telecommunications technology
CEDEC	Collaborative Microelectronic Design Excellence Centre
CMOS	Complementary metal oxide semiconductor
CR	Current Reuse
C	Correlation coefficient
CC	Coupling capacitor
dB	Decibel
DCS	Digital Cellular System
DUT	Device Under Test
DRC	Design Rule Check
F	Noise Factor
FC	Folded Cascode
GPS	Global Positioning System
G-S	Gate-Source
GSM	Global System for Mobile
I	Current
IC	Integrated Circuits
IDCS	Inductively-degenerated common source
IP_{1dB}	Input 1-dB Compression Point
IIP_3	Input-Referred Third-Order Intermodulation Point
IM	Inter-Modulation
ISS	Impedance Standard Substrate
LNA	Low Noise Amplifier

MOS	Metal Oxide Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect-Transistor
NF	Noise Figure
NF_{min}	Minimum Noise Figure
NMOS	N-Metal Oxide Semiconductor
OP_{1dB}	Output 1-dB Compression Point
OIP_3	Output-Referred Third-Order Intermodulation Point
P_{1dB}	1-dB Compression Point
P_{in}	Input Power
PCSNIM	Power-Constrained Simultaneously Noise and Input Matching
PMOS	P-Metal Oxide Semiconductor
P_{out}	Output Power
R	Resistance
R_{on}	Output resistance of the MOSFET
RF	Radio Frequency
USM	Universiti Sains Malaysia
V	Voltage
W	width of MOSFET
W-CDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Networks

LIST OF SYMBOLS

α	alpha
δ	delta
γ	gamma
Ω	Ohm
χ	Chi
μ	micron
r	Resistivity
log	Logarithm
G	Transducer gain
C_c	Coupling capacitor
C_{eq}	Equivalent capacitance
C_1	Capacitor 1
C_2	Capacitor 2
c_{gs}	Gate-source capacitance
c_{gd}	Gate-drain capacitance
C_{d1}	Drain capacitor 1
C_{ex1}	External capacitor 1 at the input
C_{ex2}	External capacitor 2 at the input
C_{ex3}	External capacitor 3 at the input
C_{Msw3}	Switch 3 capacitance
C_{Msw4}	Switch 4 capacitance
C_o	Output capacitor
C_{ox}	Oxide capacitor
C_t	Total capacitance

C_{tot}	Total capacitance
f	Frequency (Hz)
F	Noise factor
G	Transducer gain
G_a	Available gain
g_m	Transconductance
I	Current (A)
I_{DC}	Current flow through a device
I_h	Current handling constant
L	Length of the transistor/material
L_{d1}	Drain inductor 1
L_{d2}	Drain inductor 2
L_s	Source inductor
L_g	Gate inductor
M_1	Transistor 1
M_2	Transistor 2
M_{SW1}	Transistor switch 1
M_{SW2}	Transistor switch 2
M_{SW3}	Transistor switch 3
M_{SW4}	Transistor switch 4
N_a	Noise added by the amplifier
N_i	Noise power levels at the input to the amplifier
N_o	Noise power levels at the output to the amplifier
P	Power
Q_s	Quality factor
$Q_{s,opt}$	Optimum quality factor

R	Resistance
R_1	Resistor 1
R_s	Sheet resistance
S_{11}	Input reflection coefficient
S_{21}	Forward transmission coefficient
S_{12}	Reverse transmission coefficient
S_{22}	Output reflection coefficient
S_i	Signal at the input to the amplifier
S_o	Signal at the output to the amplifier
T	Thickness of the material
V_{BIAS_1}	Bias volatage 1
V_{BIAS_2}	Bias volatage 2
V_{DS}	Drain-Source voltage
V_{GS}	Gate-Source voltage
V_{in}	Input voltage
V_{ov}	Overdrive voltage
V_{th}	Threshold voltage
W	Width of transistor
W_{M1}	Width of transistor 1
W_{M2}	Width of transistor 2
W_{MSW1}	Width of transistor switch 1
W_{MSW2}	Width of transistor switch 2
W_{MSW3}	Width of transistor switch 3
W_{MSW4}	Width of transistor switch 4
ω_o	Omega
ω_T	Transition frequency

Z_{in}	Input impedance
Z_{Msw}	Impedance switch
Z_{Msw1}	Impedance of switch 1
Z_{Msw2}	Impedance of switch 2
Z_{Msw3}	Impedance of switch 3
Z_{Msw4}	Impedance of switch 4
Z_{opt}	Input noise

SATU 0.13-µm CMOS PADANAN MASUKAN DAN HINGAR SERENTAK DENGAN KEKANGAN KUASA PENGUAT HINGAR RENDAH BOLEH KONFIGURASI SEMULA BAGI APLIKASI MUDAH ALIH BERBILANG PIAWAIAN 0.9, 1.8 DAN 2.1 GHz

ABSTRAK

Industri komunikasi tanpa wayar sedang mengalami pertumbuhan yang luar biasa. Sebelum ini, penerima berbilang piawaian telah direka dalam seni bina yang selari untuk menampung berbilang piawai. Walaubagaimanapun, untuk setiap laluan, kawasan bentangan yang besar membuatkan kos fabrikasi meningkat. Sebagai tindakbalas terhadap permintaan untuk bahagian hadapan tanpa wayar yang berkos rendah dan berprestasi lebih tinggi, banyak kajian intensif pada CMOS frekuensi radio (RF) litar bahagian hadapan telah dijalankan. Projek ini menggabungkan laluan-laluan selari tersebut kepada kaedah penerima tanpa wayar laluan tunggal. Matlamat utama adalah untuk meminimumkan “trade-off” atau mencapai keseimbangan antara prestasi tinggi, saiz yang lebih kecil dan kos rendah pada reka bentuk penggunaan kuasa yang rendah. Sasaran projek ini adalah untuk mereka bentuk penguat hingar rendah (LNA) berbilang piawaian bagi tiga piawai operasi jalur frekuensi. Bagi mendemonstrasi keberkesanan teknik, satu reka bentuk LNA laluan tunggal berbilang piawaian menggunakan konsep pensuisan telah dilaksanakan. Reka bentuk boleh memilih jalur frekuensi operasi dengan mengalihkan suis yang digunakan di rangkaian padanan masukan dan keluaran. Satu LNA berbilang piawaian dengan topologi Padanan Masukan dan Hingar Serentak dengan Kekangan Kuasa (PCSNIM) telah dilaksanakan bagi tujuan ini. LNA beroperasi pada frekuensi 0.9 , 1.8 dan 2.1 GHz. Oleh itu, reka bentuk piawai tanpa

wayar adalah bagi aplikasi GSM900 , DCS1800 dan W-CDMA. Reka bentuk ini telah dilaksanakan pada proses CMOS 0.13-µm 8-lapisan logam. LNA berbilang piawaian mempamerkan nilai angka hingar (NF) serendah 1.72 dB pada 1.8 GHz dan 1.85 dB pada 2.1 GHz. Gandaan adalah dalam julat 10 ke 11 dB. Titik pintasan tertib ketiga (IIP3) adalah setinggi 0.2 dBm (pada 1.8 GHz), -1 dBm (pada 2.1 GHz) dan -2 dBm (pada 0.9 GHz). Manakala titik mampatan 1 dB pula adalah -12.2 dBm (pada 0.9 GHz), -11.5 dBm (pada 1.8 GHz) dan -11 dBm (pada 2.1 GHz). Jumlah penggunaan kuasa untuk reka bentuk ini adalah 7.42 mW dengan bekalan voltan sebanyak 1.2 V.

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ABSTRACT

The wireless communication industry is experiencing tremendous growth. Previously, multi-standard receivers were designed using parallel architecture to accommodate multiple standards. However, for each path, the area consumption is high which increases cost of fabrication. Responding to the demand for a low-cost and high performance wireless front-end, many intensive researches on CMOS radio-frequency (RF) front-end circuits have been carried out. This project merges the parallel paths into a single path wireless receiver. The ultimate goal is to minimize the trade-off between high performance, smaller size and low-cost at low power consumption design. The target of this project is to design a multi-standard low noise amplifier (LNA) for three standards frequency bands. To demonstrate the effectiveness of the design technique, an LNA design is presented for multi-standard single path LNA with the switching concept. The design can select operating frequency band by switching the switches which are adopted at the input and output matching network. A multi-standard Power Constrained Simultaneous Noise and Input Matching (PCSNIM) topology was implemented. The multi-standard LNA is operated at 0.9, 1.8 and 2.1 GHz frequencies. The design covers wireless standards of GSM900, DCS1800 and W-CDMA applications. The design was implemented on 0.13-µm 8-metal CMOS process. The multi-standard LNA shows the noise figure (NF) as low as 1.72 dB at 1.8 GHz and 1.85 dB at 2.1 GHz. The gain is in the range 10 up to 11 dB. The third order intercept point (IIP_3) is 0.2 dBm (at 1.8 GHz), -1 dBm (at 2.1

GHz) and -2 dBm (at 0.9 GHz) while IP_{1dB} compression point is -12.2 dBm (at 0.9 GHz), -11.5 dBm (at 1.8 GHz) and -11 dBm (at 2.1 GHz). The power consumption of the design is 7.42 mW with 1.2 V power supply.

CHAPTER 1

INTRODUCTION

1.1 Introduction

In the past decade, wireless communication systems have been evolving increasingly, growing rapidly and has high demand in market. The functionality of RF transceiver increase as RF designers pursue cost-effective multi-standard transceivers. Recent developments in wireless communication have new requirements on wireless transceivers. It is desirable to provide multi-band transceiver where wireless standards can operate simultaneously to extend its functionalities (Hashemi, 2002). Various communication standards have to be adopted to accommodate different needs depending on their data rate, bandwidth, operating range and carrier frequency. The key block of a multi-band multi-standard receiver is the low-noise amplifier (LNA). The easiest way is to employ several parallel passages to accommodate the different communication standard. There are different architectures that have been proposed to realize the goal. However, the requirement for a very large design area if the receiver is to be implemented on a single chip. The major drawback would also result in higher production cost. A block diagram of parallel architecture is shown in Figure 1.1.

The parallel architecture, shown in Figure 1.1, utilizes several single-band architectures that are placed in parallel. Each LNA is designed to receive one of the desired bands. The advantage of this architecture is low power consumption. However, for each path, the area consumption is high, which increases the cost of the chip for fab-

rication. One of the challenges for the parallel architecture design is to reduce the area.

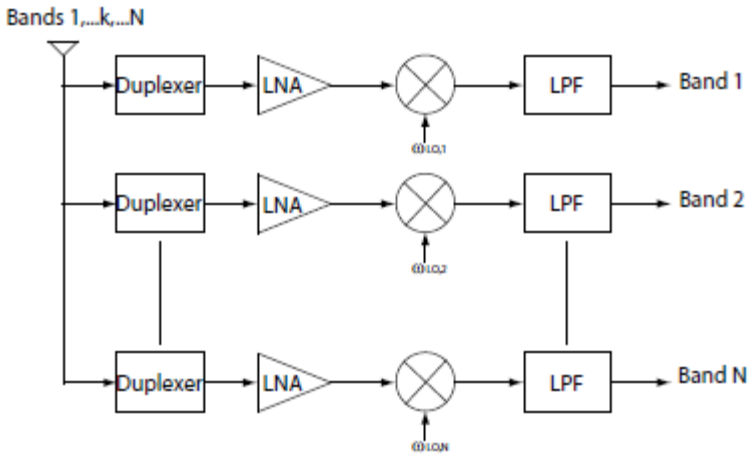

Figure 1.1: Block diagram of a multi-band receiver using parallel architecture. (El-Nozahi, 2010).

To overcome the large consumption problem, an architecture that should be more desirable with parallel architecture multi-standard receiver. This architecture can cover various standards with just one single LNA, compared to the previous architecture that uses one LNA for each single standard. Less number of devices leading to a system with less complexity, less area and most importantly, less power consumption.

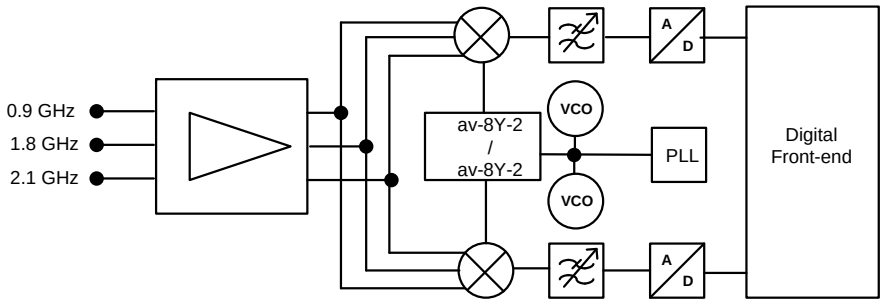

Figure 1.2: Block diagram of a multi-standard receiver with single LNA (Gustafsson, 2006)

1.2 Motivation

In a multiband LNA, the RF front-end has to cover a huge range of different carrier frequencies to incorporate all the standards. Some front-end needs either wideband LNA (Knapp, 2001), a narrowband LNA with multiple passbands or known also as concurrent LNA (Hashemi, 2002), concurrent with two stages design and wideband multimode (Aravint, 2015) or a tunable LNA (Andersson, 2002).

Concurrent LNAs with multiple passbands are only suitable where the passbands are well separated and not more than two. Tunable LNAs are very attractive but hard to design for a large tuning range (Andersson, 2005). The wideband LNA can receive multiple bands of interest, however, it requires higher consideration on the tradeoff between power, area and sensitivity. The high linearity requirement make it unattractive. Concurrent with two stages; common-gate (CG) and common source (CS) and wideband miltimode can achieve good matching, gain and compression point but the NF is too high up to 8.5 dB (Aravint, 2015).

Tunable LNA which is also known as reconfigurable LNA, can dynamically change its configuration to achieve a different band. By tuning the switches ON/OFF, the LNA can alter between two operating frequencies bands. For this LNA architecture, the number of switchable or tunable components should be limited; otherwise, the performance of the LNA may be deteriorated because of the parasitic parameters introduced by CMOS switches. Furthermore, this topology is generally suitable for narrow band applications. Band selection of the LNA is realize by an inductor tuning circuit. Compared with concurrent LNAs, it can be continuously tuned and is preferred for applications with a large number of frequency bands.