# LOW NOISE AND LOW POWER ECG AMPLIFIER USING CMOS 0.13µm TECHNOLOGY

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*Specially dedicated*
*to every person who is behind*
*me through the highs and lows.*

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## ABSTRACT

Through the scaling down of modern VLSI technologies, the realization of CMOS based electrocardiogram (ECG) device becoming wearable to its user is possible. Yet, this transition introduces more constraints to its analog circuits. This is due to the measured electrical signal of ECG devices, or known as ECG signal possessed characteristics that are low in frequency (0.1 to 150Hz) and amplitude (<5mV), thus it lead to every ECG devices suffered from flicker noise for low frequency cardiac signal acquisition at the front-end of its sensor, 50 Hz power line electromagnetic interference, and the large unstable input offsets due to the improper attachment of electrode-skin interface. Therefore, to encounter this problem, the front-end of ECG devices, which is amplifier needed to be enhance so it able to accurately detect the ECG signals. Besides that, the amplifier must able to operate at low voltage and less power consumption so that it can be used in wearable device. In this work, a high performance CMOS amplifier for ECG sensors that improves the noise issue and suitable for low power wearable cardiac screening is designed. The designed circuit adopts the folded cascode topology to achieve high gain and less susceptible to noise. This work uses 0.13 µm CMOS process technology from Silterra and Mentor Graphics Pyxis as the design tool. This successfully achieve high CMRR which is 160dB. Besides that, this work also able to reduce the noise at the front-end amplifier system down to 1.28nV/$\sqrt{}$Hz. The power consumption of the designed amplifier is 3 µW, which is low and suitable to be implemented on design for wearable ECG devices.

# ABSTRAK

Kemajuan dalam teknologi VLSI moden telah membolehkan peranti elektrokardiogram (EKG) yang berasaskan CMOS menjadi satu sistem mudah alih. Namun begitu, peralihan sistem EKG kepada peranti mudah alih akan membebankan litar analognya. Hal ini kerana signal elektrik yang diukur oleh peranti EKG, atau lebih dikenali sebagai signal EKG mempunyai ciri-ciri signal yang berfrekuensi dan amplitud yang rendah. Ini menyebabkan setiap peranti EKG mengalami gangguan kerlipan pada frekuensi rendah pada bahagian hadapan penguat EKG ketika meperoleh signal EKG, gangguan elektromagnet daripada 50 Hz talian kuasa, dan ketidakstabilan masukan ofset yang besar disebabkan oleh penyambungan antara muka elektrod dan kulit yang tidak sempurna. Untuk mengatasi masalah ini, bahagian hadapan peranti ECG iaitu penguat perlu di pertingkatkan untuk memperoleh signal EKG dengan tepat. Selain itu, penguat tersebut hendaklah beroperasi dalam kadar voltan dan kuasa yang rendah supaya ia boleh digunakan dalam peranti mudah alih. Dalam projek ini, Di dalam projek ini, penguat yang mampu untuk mengatasi masalah gangguan signal dan berkuasa rendah untuk peranti EKG dicadangkan. Penguat ini mengadaptasi topologi kaskod terlipat yang mempunyai daya stabil yang tinggi. Dengan menggunakan teknologi CMOS 0.13 µm daripada Silterra, keputusan simulasi menunjukkan bahawa bahagian hadapan litar ini berupaya mencapai nisbah penolakan mod sepunya (CMRR) yang tinggi iaitu 160 dB. Selain itu, penguat ini mencapai tahap gangguan isyarat masukan yang rendah iaitu 1.28nV/$\sqrt{}$Hz. dan jumlah lesapan kuasa penguat ini hanyalah sebanyak 3 µW yang mejadikan ia sesuai digunakan bersama bahagian belakang yang memproses dan mengklasifikasi isyarat lanjutan untuk peranti mudah alih EKG.

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# LIST OF ABBREVIATIONS

| | | |
|---|---|---|
| AA | - | Arrhythmia, Amyloid |
| AgCl | - | Silver Chloride |
| AL | - | Amyloid Light-Chain |
| BSIM4 | - | Berkeley Short-channel Insulated Gate Field-Effect Transistor Model version 4 |
| BW | - | Baseline Wander |
| CMRR | - | Common Mode Rejection Ratio |
| DC | - | Direct Current |
| ECG | - | Electrocardiogram |
| EM | - | Electrode Motion |
| HRV | - | Heart Rate Variability |
| MA | - | Muscle Artifacts |
| PLI | - | Power Line Interference |

# LIST OF SYMBOLS

| | | |
|---|---|---|
| A | - | Ampere |
| Ad | - | Differential Gain |
| Ac | - | Common Gain |
| $C_{ox}$ | - | Oxide Capacitance |
| dB | - | Decibel |
| $f$ | - | Frequency |
| gm | - | Transconductance |
| Hz | - | Hertz |
| V | - | Volt |
| $V_{TH}$ | - | Threshold Voltage |
| W | - | Watt |
| $\mu_n$ | - | Mobility |

# CHAPTER 1

# INTRODUCTION

This thesis presents the ECG signal amplifier design using folded cascode operational amplifier topology. This chapter discusses the overview of the knowledge of the project, problem statement, project objective, scope, and thesis organization respectively.

## 1.1 Introduction

The rapid growth in medical technology, alongside with advancement in semiconductor industry, make it possible for traditional biomedical instrument, which usually bulky in size to be redesign to become smaller and even portable and wearable. Therefore, many efforts have been done to perform continuous yet comfortable health monitoring in daily life through a wearable system [1]. There are various biomedical signal such as body fat, heart rate, electromyogram, and electroencephalogram are now available to be monitored in commercialized wearable biomedical devices [1]. Among these, the most vital biomedical instrument is ECG monitoring device as

cardiovascular diseases are the major cause of death worldwide [2]. This have led to increase of the need to have wearable ECG monitoring in homecare and clinical setting to prevent cardiovascular disease or detect symptomatic signs for patients with uncommon events.

To realise wearable ECG monitoring device, a lot of things needed to be put into consideration. The main concern on wearable ECG monitoring device is the device is battery operated [3], thus it inherently require very low power circuitry to operate as good as conventional ECG monitoring device. This show that every block in wearable ECG monitoring device should be optimize, especially the most important block which is ECG front end amplifier, which require high signal to noise ratio output for further processing of subsequent block in the device.

## 1.2 Problem Statement

Currently, battery operated devices, suffered various constrain in its analog circuitry due to more complex digital circuit and clock frequency introduced to the system. The portable ECG signal acquisition system is not excluded in this matter. The analog circuitry in portable ECG signal is the front end amplifier. This front end amplifier is the most important part in the system because the degree of reliability of ECG signal acquisition system heavily rely on the quality of the signal been produce by this front end amplifier.

In portable ECG monitoring system, low power front end ECG amplifier are very prone to noisy environment. The noisy environment are contributed by several factors. First factor is powerline magnetic field interference ranging in 50Hz, [3, 14-17]. Second factor is flicker noise. Flicker noise is very dominant in low-frequency band due to its fluctuations in carrier mobility. This two noises can easily interfered

with ECG signal obtain from the electrode feed to front end ECG amplifier because ECG signal is typically in range of amplitude and frequency less than 5mV and 250Hz respectively. Besides that, DC offset created by skin-electrode interface also contributed to noisy environment. The DC offset can reach as high as ±100mV. This noise can easily saturate the amplifier and lead to limited amount of gain can be applied to ECG amplifier. These noise and offset is should not happened in portable ECG monitoring system because it can compromise the system quality.

This issues greatly challenge the design of precise ECG front end amplifier. The, designing process must feature high common mode rejection ratio (CMRR), high signal to noise ratio, high input impedance, DC offset suppression and low power consumption in order to realize the single-chip portable ECG monitoring system.

## 1.3 Objective

As the noisy environment and low frequency noise is the main problem in portable ECG signal acquisition system, therefore the main objective of this project is to design the most impacted block by this problem which is ECG signal amplifier. In addition to that, as the nature of trade-off in analog amplifier design, some amplifier parameter will put to top priority in trade of others parameter. Those parameter are CMRR and amplifier gain. This is due to accuracy and precision are very important aspect in handling medical application, therefore by prioritizing this parameter will help to achieve it [4]. Besides that, the amplifier design must be low power as it will be uses in wearable devices. In a nutshell, in this project the ECG signal amplifier is designed to have low power, high CMRR, and low noise one lead ECG signal amplifier by using 0.13 µm CMOS process technology.

## 1.4 Scope

This project scope is limited only to amplifier design, without considering other backend components of ECG signal acquisition system such as filter, analog to digital converter, and digital processing unit. The ECG amplifier design in this project are based on one of the low noise amplifier design which is folded cascode amplifier. The technology node used for this project is BSIM4 0.13 µm CMOS transistor process technology. The tool being used for the circuit design are Pyxis Schematic and the simulation are done through ELDO simulation software. Figure 1.1 depicted scope of this project, which is highlighted in green colour.

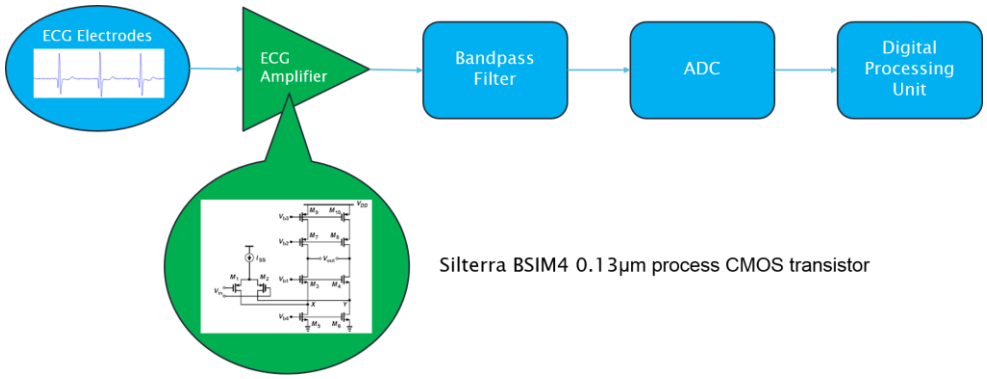


**Figure 1.1:** Project Scope

## 1.5 Organization

The content of this report is organized into a total of five chapters. The first chapter consists of the background and information of this project, the problem statement, project objectives and the project scope. Chapter 2 consists of the literature review which includes the discussion of the background and the works from other researchers that are related to this project. The Chapter 3 is discussing about the

methodology that is the method, hardware, tools, software and the design algorithms that are used to develop this project. While the Chapter 4 is discussing about the project design simulated result and output. The last chapter which is Chapter 5 discussing the conclusion and future works that are required to further enhance the current design.

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