FACE DETECTION HARDWARE ACCELERATOR USING C-BASED HIGH-LEVEL SYNTHESIS

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A thesis submitted in fulfilment of the
requirements for the award of the degree of
Master of Philosophy

Faculty of Electrical Engineering
Universiti Teknologi Malaysia

FEBRUARY 2018

Dedicated to my beloved parents, supervisor, seniors and friends.

ACKNOWLEDGEMENT

First of all, I would like to express the highest gratitude to my supervisor, Professor Dr. Mohamed Khalil bin Mohd. Hani for his invaluable support, sharing of his philosophy of life and continuous motivation which lead to the successful completion of this work.

My sincerest appreciation goes to my co-supervisor and mentors, Dr. Hau Yuan Wen, Liew Shan Sung and Syed Omid Ayat for their support and advice throughout my research journey.

My warmest regards to my parents, brother and friends for their seamless caring and moral supports.

My sincerest, greatest and deepest appreciation goes to Tan Lay Peng who always support me, encourage me, and listen to me on my hardship journey.

ABSTRACT

Research has shown that Field Programmable Gate Array (FPGA) based implementation of image processing system results in high computational speed and energy efficiency. However, FPGA design has relatively long development time compared to alternative implementation platforms, such as those based on Central Processing Unit, Graphical Processing Unit or Digital Signal Processor. Designing digital hardware at a higher level of abstraction is an effective way to shorten the development time. High-level synthesis (HLS) raises the abstraction level for designing digital circuit and translates a C-based description of the desired design into Hardware Descriptive Language. However, C-based HLS techniques are still lacking some maturity. In particular, existing works on applying C-based HLS to design hardware that accelerates window-based image processing algorithms are generally done in a trial and error manner, and usually results in non-optimal designs. Hence, there is a need for an effective procedure in applying C-based HLS that can lead to an optimized accelerator design. Therefore, the key contribution of this research is to present a systematic C-based HLS technique to be used in the design of hardware that accelerates image processing algorithm. The proposed C-based HLS design procedure is illustrated with a case study of the Sobel filter. The effectiveness of the proposed design technique is demonstrated by the case study of a Viola-Jones face detection accelerator targeted for implementation in FPGA. The proposed face detection hardware applies a pipelined architecture with task-level parallelism that allows concurrent execution on every sub-module. Experimental results show that the resulting accelerator module achieves a speed performance improvement of up to 12 times when compared to that of existing works. Tested on CMU+MIT database, the proposed accelerator achieves high detection accuracy of 88% and 46 false positives. Experimental results also show that the proposed design achieves up to 61 frames per second detection speed. This work demonstrates that the proposed C-based HLS design methodology is effective for image processing hardware accelerator development.

ABSTRAK

Penyelidikan telah menunjukkan bahawa pelaksanaan sistem pemprosesan imej Tatasusunan Get Boleh Aturcara Medan (FPGA) menghasilkan kelajuan pengiraan yang tinggi dan kecekapan tenaga. Walau bagaimanapun, reka bentuk FPGA mengambil masa pembangunan yang agak lama berbanding platform pelaksanaan alternatif, seperti Unit Pemprosesan Pusat, Unit Pemproses Grafik atau Pemproses Isyarat Digital. Merekabentuk perkakasan digital pada tahap pengekstrakan yang lebih tinggi adalah cara yang berkesan untuk memendekkan masa pembangunan. Sintesis Aras Tinggi (HLS) meningkatkan tahap pengekstrakan untuk mereka bentuk litar digital dan menerjemahkan deskripsi berasaskan C pada reka bentuk yang dikehendaki kepada Bahasa Takrifan Perkakasan. Walau bagaimanapun, teknik HLS yang berasaskan C masih kurang matang. Khususnya, kerja-kerja yang sedia ada untuk menggunakan HLS berasaskan C untuk mereka bentuk perkakasan yang mempercepatkan algoritma pemprosesan imej berasaskan tetingkap umumnya dilakukan dengan kaaedah cuba-cuba, dan biasanya menghasilkan reka bentuk yang tidak optimum. Oleh itu, terdapat keperluan untuk prosedur yang berkesan untuk menggunakan HLS berasaskan C yang boleh membawa kepada rekaan pemecut optimum. Oleh itu, sumbangan penting dalam penyelidikan ini adalah untuk mempersembahkan teknik HLS berasaskan C yang akan digunakan dalam reka bentuk perkakasan yang mempercepat algoritma pemprosesan imej. Prosedur reka bentuk HLS berasaskan C yang dicadangkan telah digambarkan dengan didorong oleh kajian kes penapis Sobel. Keberkesanan teknik reka bentuk yang dicadangkan telah ditunjukkan oleh kajian kes reka bentuk pemecut pengesanan wajah Viola-Jones di FPGA. Perkakasan pengesanan wajah yang dicadangkan menggunakan senibina talian paip dengan keselarian aras tugas yang membolehkan pelaksanaan serentak pada setiap sub-modul. Keputusan eksperimen menunjukkan bahawa modul pemecut yang dihasilkan mencapai peningkatan prestasi kelajuan sehingga 12 kali ganda berbanding dengan kerja yang sedia ada. Diuji pada pangkalan data CMU+MIT, pemecut yang dicadangkan mencapai ketepatan pengesanan setinggi 88% dan serendah 46 positif palsu. Hasil eksperimen juga menunjukkan bahawa reka bentuk yang dicadangkan mencapai kelajuan pengesanan 61 bingkai per saat. Kerja ini menunjukkan bahawa kaedah HLS berasaskan C yang telah dicadangkan adalah berkesan untuk pembangunan pemecut perkakasan imej pemprosesan.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

AP SoC	-	All Programmable SoC
CPU	-	Central Processing Unit
DFG	-	Data Flow Graph
DSP	-	Digital Signal Processor
FPGA	-	Field Programmable Gate Array
fps	-	Frames per Second
GDB	-	GNU Debugger
GPU	-	Graphical Processing Unit
HW/SW	-	Hardware-Software
HDL	-	Hardware Descriptive Language
HLS	-	High-level Synthesis
IDE	-	Integrated Development Environment
I/O	-	Input/Output
RTL	-	Register Transfer Level
SDK	-	Software Development Kit

LIST OF APPENDICES

CHAPTER 1

INTRODUCTION

1.1 Background

Field Programmable Gate Arrays (FPGA) is an ideal platform for image processing application because of its potential to perform highly-parallelized computations for performance speed-up and high energy efficiency [1]. However, a hardware implementation for such algorithm consumes more time and human resources than a equivalent software development. Moreover, for FPGA SoC design of image processing system which is the implementation of embedded SoC on FPGA platform facing even more challenges and further increase the development time. There are handshaking issue between hardware module and complicated interface design for CPU to FPGA communication,

Hence, an efficient way to tackle this issue is by design at a higher abstraction level. At higher abstraction level, hardware design is created at algorithmic level by using C/C++/System C/Matlab as a programming language. This movement does not only help to improve productivity but also slightly lower the barrier for more software designers to get access to FPGA platform. High-level synthesis tool is required to interpret the algorithmic description of a user-specific behaviour and create digital hardware that implements that behaviour. HLS tool also facilitates the handshaking between hardware module and interface design which can ease the FPGA SoC design process. There is a wide selection of tools available in the market that can be used for high-level synthesis. Conventionally hardware and software designers prefer using high-level languages such as C/C++ for algorithm developments, and Vivado high-level synthesis (HLS) is one of the most popular C-based HLS that is capable of synthesis C/C++ code into Register-Transfer Level (RTL) for hardware implementation.

Users require restructuring the high-level implementations to make them synthesizable and suitable for specific hardware architecture. Without such restructuring, the HLS tools can still derive a hardware realisation, but the resulting hardware can be bloated and suffer from poor performance [3]. It becomes necessary to apply hardware design knowledge during restructuring for the HLS tool to synthesizing an efficient hardware with high performance and reasonable resource usage. Therefore FPGA-based hardware design using HLS tools is fundamentally a hardware design process [4] that requires a good knowledge of digital logic circuit as well as digital logic design. In this work, an algorithm for face detection is selected as the case study for C-based HLS hardware design.

Nowadays face detection plays an important role in the modern world since images of human faces are central to intelligent human-computer interaction(HCI) [5]. Face detection is the key process in HCI for smart systems as face detection is the first stone for all facial analysis algorithms such as face recognition, face tracking and facial expression recognition. In advertisement industry, it is used for data collection like audiences' watch time, gender and age range for targeted billboard advertisement [6]. The face detection is defined as a process of determining the availability of faces in an image and return image location and extent of each face [7]. The face localization is a simplified detection process which assumes that there is only one face in an input image and aims to determine the image position of a single face [7].

There are various types of face detection algorithms that are typically grouped into four categories: knowledge-based, feature invariant, template matching and appearance-based methods [7]. The knowledge-based method is developed based on knowledge of researchers on deriving a set of rules that describe the feature and their relationship that build up a human face. The feature invariant method focuses on finding invariant features and use them to locate the face. The invariant feature is the feature that invariant under different pose and lighting condition. The template matching method is developed based on a predefined standard face pattern (template) which is applied to the input image to find their correlation. The correlation value determines the existence of face. The appearance-based method is developed based on learning algorithm that could identify/learn the characteristics of a face from a set of training images. These characteristics form a discriminant function that is used for the detection process. Face detection can be attributed to many circumstances, such as variation in scale, location, pose and lighting condition.

In 2001, Viola and Jones [8, 9] proposed their face detection framework based

on Haar features that are capable of processing images rapidly, with high detection rate and low false positive. The Viola-jones face detector is an appearance-based detection developed by using Adaboost learning algorithm. AdaBoost is a machine learning boosting algorithm capable of constructing a strong classifier through a weighted combination of weak classifiers. The Viola-Jones face detector contains three main ideas that make it run at a higher speed which is the Integral Image representation, the simple and efficient classifier built with AdaBoost learning and the cascade classification process. The Viola and Jones approach is primarily developed for face detection, but the algorithm can detect any object by using different training data. Even though Viola-Jones Face Detector was not the most accurate detector available but it has received considerable attention and probably being the highest impact face detection algorithm in the 2000s [10], because of its good speed-accuracy trade-off [11]. However, for embedded real-time processing there is still a need for FPGA hardware acceleration.

1.2 Problem Statement

FPGAs have become increasingly popular as a configurable computing platform targets for high-performance image processing applications due to its advantages of high computational speed and power efficiency. Implementing such algorithm in software would suffer from poor execution speed. FPGA speed up an image processing application by offloading computational workload from Central Processing Unit (CPU). However, RTL design has relatively long development time compared to alternative implementation platforms, such as CPU and GPU [12]. An effective way to improve design productivity is to raise the level of design abstraction beyond RTL. Existing research work of window-based image processing hardware accelerator design at higher level abstraction [13,14] did not effectively map algorithm into efficient hardware. They did not report on their precise design direction, design goal and desire hardware architecture but rather a trial and error design approach for getting a better result. The architecture of their proposed design is also not clearly presented. In summary, the existing work with trial and error approach does not generate an optimal or real-time performance hardware design. Although C-based HLS design for image processing is a good solution on shorten development time however effectively map the algorithm into efficient hardware is still a challenge.

In this work, Viola-jones face detection algorithm is selected as the case study for presenting the effectiveness of improved technique of mapping window-based

image processing functions into hardware accelerator. The compute intensive cascaded Haar classifier, integral image and image normalization is mapped into hardware using C-based HLS design method. A cascaded Haar classifier consists of thousands of Haar classifiers that calculate Haar-like features from the integral images. To achieve a real-time performance face detection system, Haar classifier needs to highly optimized because this module is the most frequently and repeatedly used module in the detection process. The Haar classifier has no data dependency among each other, potentially to be executed in parallel to obtained better speed-up. The integral image process is consisting of two stages, the pixels accumulation of the horizontal axis of the sub-window and the pixels accumulation of the vertical axis of the sub-window. Serial processing integral image is time-consuming. Hence, executing integral image in pipeline is required. Existing literature does not discuss hardware architecture of the Integral Image module in depth. Viola-Jones face detection algorithm applied image normalization toward sub-window to minimize lighting effect during detection [8, 9]. Existing hardware implementation of Viola-Jones [15–17] does not have an in-depth discussion on normalization which might the possible reason for their accuracy degradation. Floating-point representation in image normalization is not suitable to apply during hardware implementation due to higher resource consumption and lower execution speed. Therefore, fixed-point representation is required. However, it is important to ensure that it is minimal in information loss in image normalization to maintain the appropriate detection accuracy.

1.3 Objective

This thesis focuses on enhancing the C-based HLS hardware accelerator design methodology for window-based image processing. Viola-Jones face detection algorithm is used as case study to prove the effectiveness of this methodology. In detail, the objectives of this research are:

1. To develop an improved C-based HLS hardware accelerator design technique that effectively maps window-based image processing algorithms into efficient hardware with a shorter development time. The improved methodology is illustrated by using Sobel filter, and its effectiveness is proven by using Viola-Jones algorithm
2. To propose a hardware accelerated Viola-Jones face detection design with C-based HLS that guarantees to have shorter development time, good detection

accuracy, low false positives and high-speed performance. The proposed hardware has the following features:

(a) Parallel design for Cascaded Haar Classifier

(b) Pipelining for Integral Image

(c) Fixed point resource saving for Image Normalization

(d) Task-level parallelism for proposed hardware accelerator.

1.4 Scope of Work

The scope of work in this thesis is limited to some restrictions as follows:

1. A systematic technique of C-based HLS design using window-based image processing is presented. The algorithm is first transformed into Data Flow Graph (DFG) and schedule diagram/ pipeline datapath to facilitate more effective and efficient C-based HLS design. The C-based description is written according to the schedule diagram/ pipeline datapath.
2. The software model of the proposed face detection hardware accelerator implements the Viola-Jones algorithm is developed in C/C++ based on the work of [8, 9]. It is compiled with GCC compiler under Window 10.
3. The software model of the proposed face detection hardware accelerator is tested on the MIT-CMU frontal face test set. The aim is to achieve comparable detection accuracy and false positive as in [8, 9] to prove the correctness of the algorithm. Matlab is used to ease the output verification and analysis process. It is used for image-to-text conversion, image displaying and graph plotting.
4. C-based HLS tools and high-level programming language C are used to model the proposed face detection hardware accelerator. The design targeted to run on Xilinx Zynq7000 ZC-706 development board running at 125MHz and with Arm Dual-core processor running at 666MHz for executing the embedded software.
5. The entire C-based HLS design is verified and analyzed in Vivado Simulator using C/C++ testbench in C simulation and C/RTL co-simulation.
6. The system-level integration is using Vivado IP Integrator, a new IP-centric design flow for accelerating the time-to-system integration.
7. The proposed design methodology for window-based image processing is illustrated by designing Sobel filtering accelerator and the effectiveness of this

methodology is presented by designing Viola-Jones face detection accelerator.

8. This face detection system aims to perform face detection mainly on grayscale image of size 320x240 and 640x480 and it is flexible to be modified for handling different size of input images.

1.5 Contribution

The proposed face detection hardware accelerator using Viola-Jones algorithm in this thesis has been improved over existing work. The contributions of this thesis are:

1. A state of the art and systematic technique of designing window-based image processing hardware accelerator using C-based HLS is presented. Case studies applied are Sobel filter and Viola-jones face detection algorithm. Various optimization and the trade-off for speed and resource utilization were discussed. Interface management, memory mapping and arbitrary precision data type also being discussed.
2. A proposed face detection hardware accelerator that runs on Xilinx Zynq7000 ZC-706 development board using Vivado HLS tools for C-based HLS design is presented. A detection rate of 88% and 46 false positives is achieved on hardware implementation. It achieved 61fps and 14fps for an input image of size 320x240 and 640x480 pixels respectively which is up to 206 times speed-up compared to software implementation that executed in the same board. By applying proposed C-based HLS design technique, hardware accelerated face detection system improved the speed performance by double of similar work on [13].

1.6 Thesis Organization

This thesis is divided into seven chapters. The first chapter includes the research background, problems statement, research objectives, limitations of the proposed system as well as the contributions of this research work. Chapter 2 contains the theoretical background and related existing works and the previous work. C-based HLS design method and the description of simulation tools and design platform of this

work are included in Chapter 3. Chapter 4 presented a motivational case study using C-based HLS on designing Sobel filter.

Chapter 5 presented the design of proposed face detection hardware accelerator. Chapter 6 presented the experimental results and performance analysis in term of speed and accuracy as well as benchmarks on the performance of the proposed design with other related works. Verification of the proposed algorithms is included as well.

The last chapter, Chapter 7 concludes the presented proposed face detection accelerator and gives a suggestion for the future work.

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