CHARGE-BASED COMPACT MODEL OF GATE-ALL-AROUND FLOATING GATE NANOWIRE WITH VARIABLE OXIDE THICKNESS FOR FLASH MEMORY CELL

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To my beloved family and friends.

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ABSTRACT

Due to high gate electrostatic control and introduction of *punch* and *plug* process technology, the gate-all-around (GAA) transistor is very promising in, and apparently has been utilized for, flash memory applications. However, GAA Floating Gate (GAA-FG) memory cell still requires high programming voltage that may be susceptible to cell-to-cell interference. Scaling down the tunnel oxide can reduce the Program/Erase (P/E) voltage but degrades the data retention capability. By using Technology-Computer-Aided-Design (TCAD) tools, the concept of tunnel barrier engineering using Variable Oxide Thickness (VARIOT) of low-*k*/high-*k* stack is utilized in compensating the trade-off between P/E operation and retention characteristics. Four high-*k* dielectrics (Si_3N_4, Al_2O_3, HfO_2 and ZrO_2) that are commonly used in semiconductor process technology are examined with SiO_2 as its low-*k* dielectric. It is found that by using SiO_2/Al_2O_3 as the tunnel layer, both the P/E and retention characteristics of GAA-FG can be compensated. About 30% improvement in memory window than conventional SiO_2 is obtained and only 1% of charge-loss is predicted after 10 years of applying gate stress of -3.6V. Compact model of GAA-FG is initiated by developing a continuous explicit core model of GAA transistor (GAA Nanowire MOSFET (GAANWFET) and Juntionless Nanowire Transitor (JNT)). The validity of the theory and compact model is identified based on sophisticated numerical TCAD simulator for under 10% maximum error of surface potential. It is revealed that with the inclusion of partial-depletion conduction, the accuracy of the core model for GAANWFET is improved by more than 50% in the subthreshold region with doping-geometry ratio can be as high as about 0.86. As for JNT, despite the model being accurate for doping-geometry ratio upto 0.6, it is also independent of fitting parameters that may vary under different terminal biases or doping-geometry cases. The compact model of GAA-FG is completed by incorperating Charge Balance Model (CBM) into GAA transistor core model where good agreement is obtained with TCAD simulation and published experimental work. The CBM gives better accuracy than the conventional capacitive coupling approach under subthreshold region with approximately 10% error of floating gate potential. Therefore, the proposed compact model can be used to assist experimental work in extracting experimental data.

ABSTRAK

Oleh kerana kawalan elektrostatik get yang tinggi dan pengenalan kepada teknologi proses *tebuk* dan *plak*, transistor get-silinder-menyeluruh (GAA) sangat meyakinkan, dan telah digunakan dalam aplikasi memori *flash*. Walaubagaimanapun, GAA get terapung (GAA-FG) masih memerlukan voltan program yang tinggi yang mungkin terdedah kepada gangguan *cell-to-cell*. Pengecilan-skala terowong oksida dapat mengurangkan voltan program/padam (P/E) tetapi menyebabkan kemerosotan kepada daya-pengekalan datanya. Dengan menggunakan perisian rekabentuk-berbantukan-teknologi-komputer (TCAD), konsep Kejuruteraan Terowong Penghadang Oksida Boleh-ubah (VARIOT) *k*-rendah/*k*-tinggi telah digunakan dalam konteks mengimbangi kurang-lebih antara operasi program/padam dan daya-pengekalan data. Empat dielektrik *k*-tinggi (Si_3N_4, Al_2O_3, HfO_2, ZrO_2) yang kebiasaannya terdapat dalam industri semikonduktor dianalisa dengan SiO_2 sebagai dielektrik *k*-rendah. Hasil simulasi menunjukkan gabungan SiO_2/Al_2O_3 sebagai lapisan terowong GAA-FG dapat mengimbangi kurang-lebih antara operasi program/padam dan daya-pengekalan data. Sebanyak 30% peningkatan jendela memori berbanding SiO_2 dan hanya 1% kehilangan cas dijangkakan selapas 10 tahun dikenakan voltan-get setinggi -3.6V. Model kompak bagi GAA-FG dimulai dengan penghasilan model eksplisit berterusan untuk transistor GAA (GAANWFET dan JNT). Kesahihan antara teori dan model kompak dipastikan berdasarkan perisian simulasi TCAD bagi ralat maksimum beza-upaya permukaan sebanyak 10%. Hasil menunjukkan, dengan mengambil kira kesan konduksi separa-habis dapat meningkatkan ketepatan model-teras GAANWFET sebanyak lebih daripada 50% dalam kawasan sub-ambang untuk nisbah dopan-geometri sehingga 0.86. Bagi JNT pula, disamping model kompaknya tepat untuk nisbah dopan-geometri sehingga 0.6, ia juga tidak bergantung kepada parameter-cubaan yang mungkin berubah-ubah bagi voltan-terminal atau nisbah dopan-geometri yang berbeza. Model kompak GAA-FG disempurnakan hasil gabungan model pengimbang-cas (CBM) dan model kompak transistor GAA yang mana ketepatannya teruji baik dengan simulasi TCAD dan hasil eksperimen yang sudah diterbit. CBM memberikan ketepatan yang lebih baik berbanding kaedah kapasitif-gandingan konvensional pada bahagian sub-ambang dengan ralat beza-upaya get-terapung sebanyak 10%. Oleh itu, model kompak yang dihasilkan dapat digunaakan untuk membantu kerja-kerja eksperimen bagi mengekstrak nilai parameter.

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LIST OF ABBREVIATIONS

ACM	-	Adcanced Compact MOSFET
ALCVD	-	Atomic Layer Chemical Vapor Deposition
AT	-	Above Threshold
BiCS	-	Bit-Cost Scalable
BIOS	-	Basic Input Output Storage
BT	-	Below Threshold
BSIM	-	Berkeley Short-Channel IGFET Model
CBM	-	Charge Balance Model
CCCM	-	Capacitive Coupling Coefficient Model
C-FG	-	Conventional-Floating Gate
CD-ROM	-	Compact-Disk Read-Only-Memory
CLM	-	Channel Length Modulation
CMOS	-	Complementary Metal-Oxide-Semiconductor
CT	-	Charge Trapping
CTCI	-	Cell-to-Cell Interference
DC-SF	-	Dual-Control Gate Surrounding-Floating Gate
DIBL	-	Drain Induced Barrier Lowering
DRAM	-	Dynamic Random Access Memory
DVD-ROM	-	Digital-Versatile-Disc Read-Only-Memory
DQT	-	Direct Quantum Tunneling
EEPROM	-	Electrically Erasable Programmable Read-Only-Memory
EKV	-	Enz-Krummenacher-Vittoz
EPROM	-	Erasable Programmable Read-Only-Memory
EOT	-	Effective Oxide Thickness
ETOX	-	EPROM Tunnel Oxide
FG	-	Floating Gate
FD	-	Fully-Depleted
F-N	-	Fowler-Nordheim
GAA	-	Gate-All-Around
GAANWFET	-	Gate-All-Around Nanowire Field-Effect-Transistor

GCA	-	Gradual Channel Approximation
GCR	-	Gate Capacitance Ratio
HDD	-	Hard-Disk Drive
HiSIM	-	Hiroshima-University STARC IGFET Model
IGFET	-	Insulated Gate Field-Effect-Transistor
IPD	-	Inter-Poly Dielectric
ITRS	-	International Technology Roadmap for Semiconductor
JNT	-	Junctionless Nanowire Transistor
LPCVD	-	Low-Pressure Chemical Vapour Deposition
MLC	-	Multi-Level Cell
MM11	-	MOS Model 11 Philips
MOS	-	Metal-Oxide-Semiconductor
MOSFET	-	Metal-Oxide-Semiconductor Field-Effect Transistor
MOS-C	-	Metal-Oxide-Semiconductor Capacitor
MONOS	-	Metal-Oxide-Nitride-Oxide-Silicon
NVM	-	Non-Volatile Memory
PD	-	Partially-Depleted
PROM	-	Programmable Read-Only-Memory
PSP	-	Philips's MM11 and Surface Potential
RAM	-	Random-Access-Memory
ROM	-	Read-Only-Memory
SCP	-	Sidewall Control Pillar
SOI	-	Silicon-on-Insulator
SONOS	-	Silicon-Oxide-Nitride-Oxide-Silicon
SPICE	-	Simulation Program with Integrated Circuit Emphasis
SRAM	-	Static Random-Access-Memory
SS	-	Subthreshold Slope
SSD	-	Solid-State Drive
STARC	-	Semiconductor Technology Academic Research Center
TBE	-	Tunnel Barrier Engineering
TCAD	-	Technology Computer Aided Design
TCAT	-	Terabit Cell Array Transistor
TLC	-	Tri-Level Cell
UCCM	-	Unified Charge Control Model
USB	-	Universal Serial Bus
VARIOT	-	Variable Oxide Thickness

VCVS	-	Voltage-Controlled Voltage-Source
XiP	-	Execute-in-Place

LIST OF SYMBOLS

A_{FN}	-	F-N coefficient
A_W	-	cross-section area
A_{gate}	-	gate area
B_{FN}	-	F-N coefficient
C_{ox}	-	gate oxide capacitance
C_{IPD}	-	inter-poly oxide capacitance
C_{eff}	-	effective gate capacitance
C_{gg}	-	gate-gate capacitance
C_{gs}	-	gate-source capacitance
C_{gd}	-	gate-drain capacitance
C_{dd}	-	drain-drain capacitance
C_{dg}	-	drain-gate capacitance
C_{ds}	-	drain-source capacitance
C_{ss}	-	source-source capacitance
C_{sg}	-	source-gate capacitance
C_{sd}	-	source-drain capacitance
D_{it}	-	interface trap charge density
E	-	electric field
E_s	-	surface field
E_G	-	band gap
g_m	-	transconductance
g_d	-	conductance
m^*	-	effective mass
m_0	-	electron effective mass
N_A	-	acceptor doping
N_D	-	donor doping
n_i	-	intrinsic concentration
n_0	-	center concentration
t_{ret}	-	retention time
T_{ox}	-	silicon dioxide thickness

T_{hk}	-	high-k dielectric thickness
T_{tun}	-	tunnel oxide thickness
T_{FG}	-	floating gate thickness
I_{ds}	-	drain current
I_{dC}	-	complementary drain current
I_{dDP}	-	depletion drain current
J_g	-	gate current density
L_g	-	gate length
Q_{fg}	-	floating gate charge
Q_m	-	mobile charge density
Q_C	-	complementary mobile charge density
Q_{DP}	-	depletion mobile charge density
Q_{eff}	-	effective charge density
Q_{dep}	-	depletion charge density
Q_{ch}	-	channel charge
Q_{bulk}	-	bulk charge
Q_g	-	gate charge
Q_d	-	drain charge
Q_s	-	source charge
Q_f	-	fixed oxide charge
Q_{sc}	-	semiconductor charge
R	-	radius
V_{fn}	-	F-N voltage
V_{tr}	-	transition voltage
V_g	-	gate voltage
V_{cg}	-	control gate voltage
V_{fg}	-	floating gate potential
V_{FB}	-	flat-band voltage
V_d	-	drain voltage
V_s	-	source voltage
V_{prog}	-	program voltage
V_{ers}	-	erase voltage
$V_{read-dist}$	-	read disturb voltage
V_{ret}	-	retention voltage
V_T	-	threshold voltage
α_{cg}	-	gate capacitance ratio

α_d	-	drain capacitance ratio
α_s	-	source capacitance ratio
μ	-	effective mobility
ΔV_T	-	threshold shift
$\Delta\varphi$	-	workfunction difference
ϕ	-	potential distribution
ϕ_c	-	correction potential
ϕ_s	-	surface potential
ϕ_0	-	center potential
ϕ_{dep}	-	full-depletion potential
ϕ_{pert}	-	perturbation potential
ϕ_f	-	fermi potential
ϕ_t	-	thermal voltage
ϕ_B	-	barrier height
ϕ_{ox}	-	silicon dioxide barrier height
ϕ_{hk}	-	high-k barrier height
ϵ_0	-	vacuum permittivity
ϵ_{Si}	-	silicon permittivity
ϵ_{ox}	-	silicon dioxide permittivity
ϵ_{hk}	-	high-k permittivity
ϵ_r	-	dielectric constant
η	-	interface trap parameter
χ	-	electron affinity
γ	-	body coefficient

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CHAPTER 1

INTRODUCTION

1.1 Research Background

Moore's law has led to the advancement of high-speed logic computing, increasing number of electronic consumer and information technology that urge for higher data storage capability. Memory as one of the constituent of electronic devices has been continuously developed for providing massive data storage and high-speed applications. It is used in many consumer electronic appliances where encoded data is to be stored and retained as digital information inside a memory device. Memory can be divided into two main categories, which are volatile and non-volatile memory (NVM) as shown in Figure 1.1.

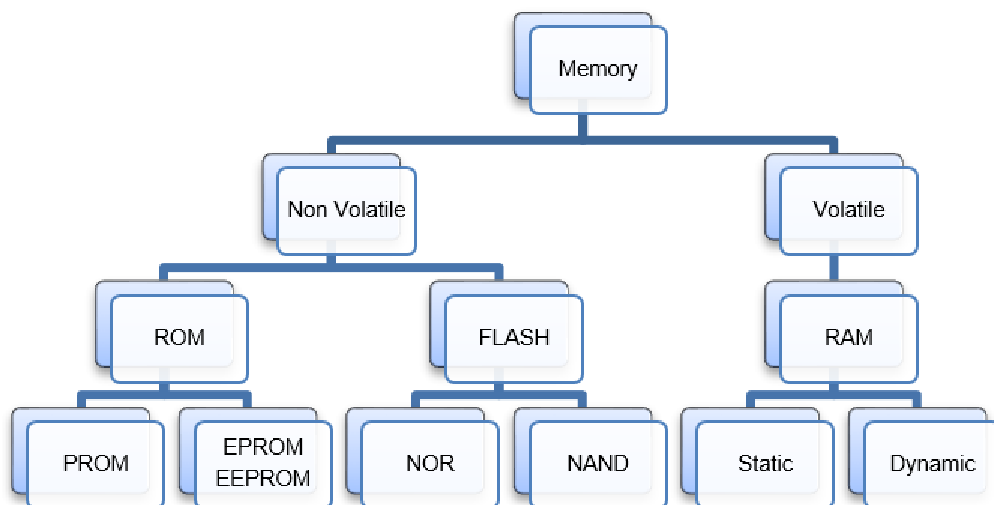
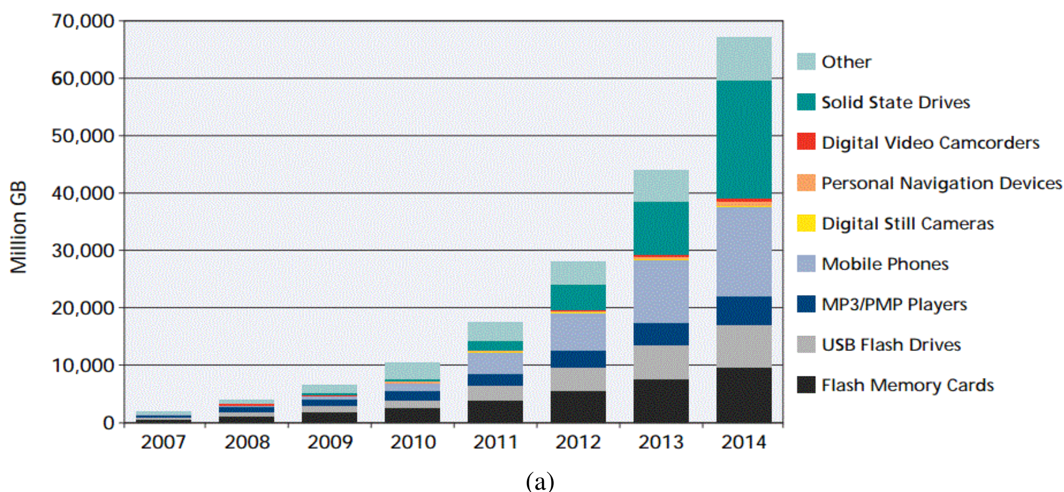


Figure 1.1: The memory device based on Complementary Metal-Oxide-Semiconductor (CMOS) technology divided into two categories, which are volatile and non-volatile.

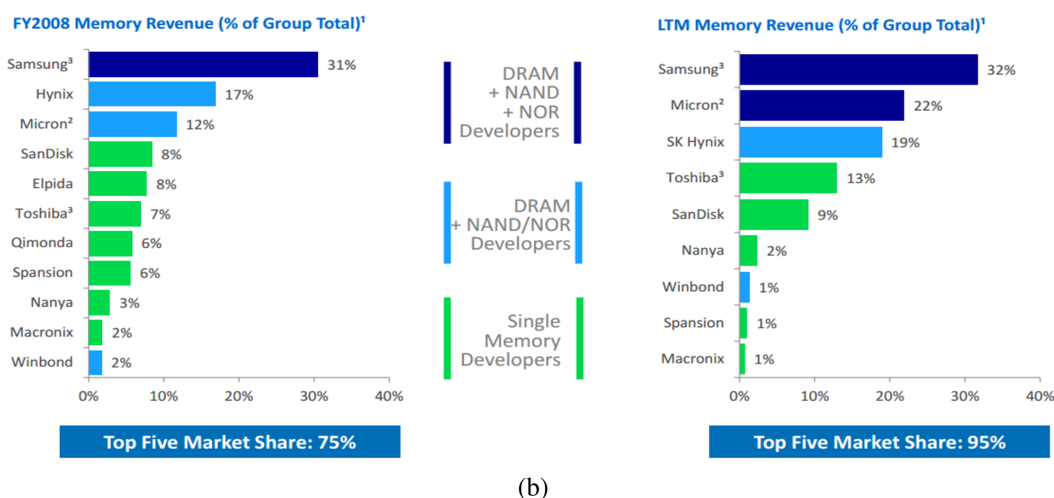
Volatile memory is a form of memory that loses data when the power is off. It is

also referred as Random-Access-Memory (RAM) with very fast read and erase time. Dynamic-RAM (DRAM) and Static-RAM (SRAM) are the commonly known volatile memory. Whereas, non-volatile memory is a form of memory that preserves the data even when the power is off. It is also known as Read-Only-Memory (ROM). NVM can retain massive amount of data but at lower write and read speed than the volatile memory. Mask ROM, Programmable ROM (PROM), Erasable PROM (EPROM), Electrically Erasable-Programmable ROM (EEPROM) and Flash Memory are the types of NVM. All of these memory devices are based on metal-oxide-semiconductor (MOS) technology. There are also other technologies that have been used to store data. Optical devices such as compact-disk ROM (CD-ROM), digital-versatile-disc RAM (DVD-RAM) and ferroelectric technology such as the well-known hard-disk drive (HDD) are employed as dominant secondary memory, in which all of these are commonly used to store digital information.

EEPROM provides with a practical usage of data storage device where the Program/Erase (P/E) operation is performed by applying electric field to the transistor cell's terminals. Furthermore, it also provides with byte-wise random access capability that made EEPROM a key figure for data storage application and to perform execute-in-place (XiP) operation. However, each of EEPROM's transistor cell or memory cell is form by two-transistor (2T), which made the device highly expensive and consumes very large circuit layout for massive storage application [1]. Flash memory is another type of NVM that had been developed from EEPROM. Instead of having 2T per cell, flash memory only consists of one-transistor (1T) per cell and has been a revolution in directing the course of memory industry into sub-20nm half-pitch scaling [2]. Because of its 1T per cell structure, the relative bit cost can be greatly reduced compared to EEPROM and it has been vastly used in many today's electronic appliances ever since. This has been proven based on a statistical study as shown in Figure 1.2(a) that the memory storage capacity exponentially increased within almost a decade (2007-2014). The emergence of mobile smart phone and solid state drive (SSD) have rapidly increased the storage capacity from 10,000 million GB to 70,000 million GB in a short span of four years (2010-2014). This has led to over 20% market share increment from the consolidation of some of the top semiconductor manufacturers such as Samsung, Micron, Hynix, Toshiba and SanDisk in which all of these companies hugely contribute to the manufacturing of mobile smart phone and SSD (refer Figure 1.2(b)).



(a)



(b)

Figure 1.2: (a) Number of storage capacity exponentially increase throughout the years with storage application devices is the highest. (Source from Forward Insight). (b) Memory revenue on some of the companies manufacturing various memory devices and the top five companies consolidation in memory industry, majorly dominated by companies that sold flash memory (source from Micron 2014 Winter Analyst Conference).

1.2 Flash Memory Scaling Challenges and Motivation

For more than two decades, floating gate (FG) memory cell has been commonly utilized in many flash memory devices. To increase the storage capacity of flash memory and to continue the exponential growth of the industry, scaling of FG cell is inevitable. However, downscaling of the FG cell has reached its bottleneck as the cell encounter physical limitations that degrade its memory performances. Figure 1.3 summarizes the issues for each component of the gate stack of the FG cell (i.e.: poly-Si FG, poly-Si control gate, inter-poly dielectric and tunnel oxide) in understanding the interrelation and the trade-off in their performances. These issues becoming more

and more severe due to oppression in gate capacitance ratio (GCR) which was caused by capacitive coupling between adjacent cells that subsequently decreases the gate electrostatic control. In order to improve the gate control while scaling its P/E voltages, the floating gate need to be wrap-around by the control gate and the thickness of dielectric layers need to be reduced but at the expense of its reliability (i.e.: retention and endurance) and add stronger coupling effect with neighboring cells. Therefore, it has been very challenging to sustain the GCR$\geq$0.6 as well as to scale its P/E voltages while maintains its high-speed operation, especially for sub-20nm half-pitch.

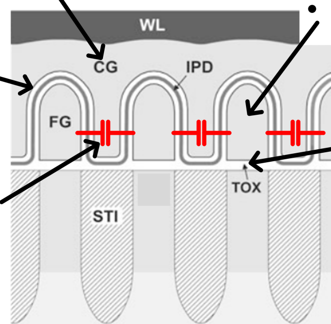
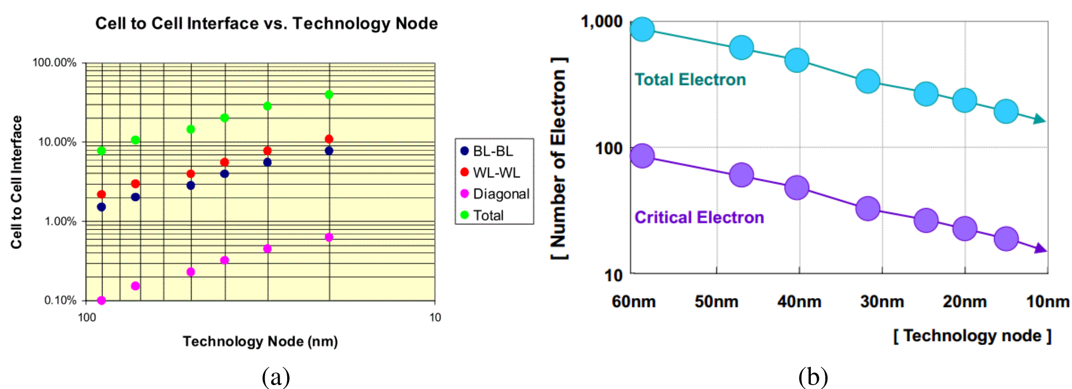


Figure 1.3: Summarized the downscaling issues in term of performance related to the gate stack of the conventional wraparound FG cell in NAND flash memory.

As shown in Figure 1.3, each component of the gate stack contributes to the reduction of GCR that affect the P/E performances of the FG cell. One of the major concerns of GCR reduction has been the scaling of its dielectric layers. An ideal dielectric material in FG cell is to provide fast P/E operation as well as scalable P/E voltages and to avoid from any electron leakage during program and retention, thus, granting the non-volatile capability. International Technology Roadmap for Semiconductor (ITRS) predicted that both the thickness of inter-poly dielectric (IPD) and tunnel oxide layers are restrained at 10nm and 6-7nm respectively while maintained the $4F^2$ cell size. This signifies the end of conventional symmetric scaling of 2F×2F at 20nm half-pitch given the floating gate distance along the same word-line (WL) only provides enough space for the IPD layer [2]. Continue scaling down the IPD thickness means the distance between FG cells in the same WL is

getting cramped; as a result, the GCR will be reduced prior to stronger coupling with neighboring floating gates. Moreover, to maintain the $4F^2$ cell size also implies that the distance between FG cells across the bit-line (BL) must be reduced creating fringing capacitance not only across the BL but also with diagonal FG cells as well [3]. This has added the variability to the threshold voltage of the selected cell and led to abnormal cell-to-cell interference (CTCI) effects. Such effects are the unstable bit states of FG cell that caused disturb during P/E and read operations, and also reducing its speed [4, 5]. Therefore, with continuous downscaling the CTCI effects are exponentially increased towards the 20nm half-pitch as shown in Figure 1.4(a). Other issue in scaling has been the floating gate itself as the electron charges continue to decrease with downscaling as shown in Figure 1.4(b). The figure also depicts the amount of critical electron charges before severe threshold voltage disturbance start to occur leading to unstable bit-state. In the case of tunnel oxide scaling, the high-field stress during P/E operation has caused severe wearing of the dielectric layer due to the introduction of negative trapped charges [6]. With frequent P/E cycles the negative trapped charges will steadily piled up and increases the threshold voltage, which subsequently degrades its dc (e.g.: Sub-threshold slope (SS), threshold voltage variation) and transient performances (i.e.: retention) [7].



(a) (b)

Figure 1.4: Scaling limitation of 2-D NAND flash. (a) Increments in cell-to-cell interference of a victim cell across BL, WL and diagonal FGs [4] and (b) decrements in number of electron in floating gate.

Due to restraints and limitations in FG cell dielectric thickness, it is difficult to effectively scale the 2-D NAND flash memory. Figure 1.5 shows the scaling projection from some of the top flash memory manufacturers. In mid-2012, SanDisk defies the symmetric $4F^2$ scaling of the FG cell and introduced the asymmetric 19nm×26nm per cell to provide enough space for IPD layer and retain the wrap-around poly-Si control gate technology. As flash memory continue to scale, it will only be a matter of time

before it reaches the horizon and stops at 10-12nm half-pitch due to the statistical limits of charge stored inside the floating gate for beyond 10nm node. Therefore, an indefinite increase of memory storage may not be possible through device scaling. Instead, it has been increased by stacking multiple layers of planar NAND array to form three-dimensional (3-D) NAND flash architecture [8]. However, stacking the conventional planar structure to form 3-D NAND flash requires additional photolithography process depending on the number of layers, which is technically challenging and can be very expensive.

NAND Flash Process Roadmaps (for Volume Production)

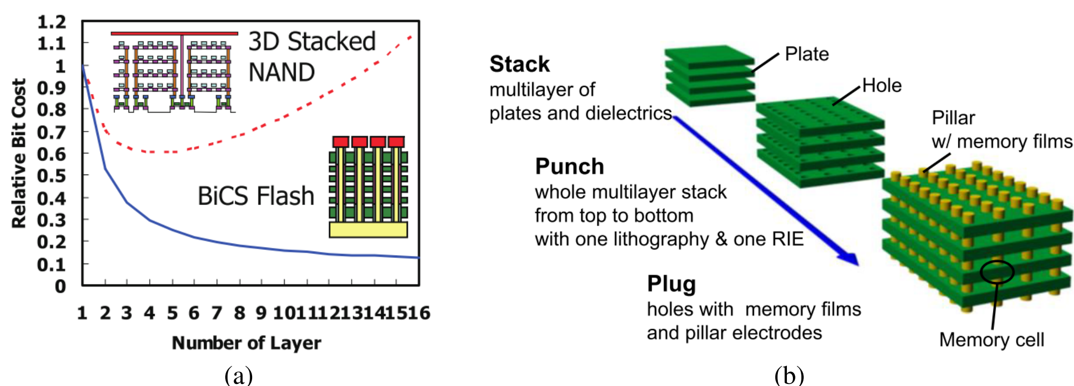
	2011–2017
IM Flash	20nm, 16nm, 10-12nm (2D); Gen 1, Gen 2 (3D)
Samsung	21nm, 16nm, 10-12nm (2D); 24L, 32L, Gen 3 (48L) (3D)
SK Hynix	20nm, 16nm, 10-12nm (2D); Gen 1, Gen 2 (3D)
Toshiba/SanDisk	19nm, 15nm, 10-12nm (2D); Gen 1, Gen 2 (3D)

Figure 1.5: Roadmap from top semiconductor foundries for scaling 2-D and 3-D NAND flash architectures (source from ICinsight, 2014).

The emergence of Bit-Cost Scalable (BiCS) technology using '*punch*' and '*plug*' process offers cheaper and higher number of vertical stack than conventional planar NAND flash memory [9]. Figure 1.6(a) depicts cheaper relative bit-cost for higher number of stack compared to 3-D stacked planar NAND. The '*punch*' and '*plug*' terms refer to the fabrication method that *punch* through multi-layer of electrodes and insulators with single lithography process before *plug* holes with channel films to form Gate-All-Around (GAA) transistor (refer Figure 1.6(b)). There are various types of 3-D NAND flash being manufactured nowadays, in which all of these architectures implemented the GAA structure as their cell transistor and employed either floating gate (FG) or charge-trapping (CT) as their memory element. Samsung and Toshiba have adopted the CT cell for their 3-D NAND namely the Terabit Cell Array Transistor (TCAT) and pipe-shaped Bit-Cost Scalable (p-BiCS) respectively [10, 11]. However, 3-D CT NANDs are known to be susceptible to charge-spreading in the nitride-trapping layer that led to poor distribution of cell-state and degrades the retention characteristics [12]. Therefore, some of the top semiconductor companies, such as Hynix and Intel/Micron Flash Technologies (IMFT) preferred FG cell for their 3-D

NAND flash [13,14]. The reasons for maintaining floating gate as the memory element in 3-D vertical NAND architectures are due to:

1. The 3-D stacked architecture with surrounding FG can circumvent the lateral charge spreading that occurs in the charge trapping layer along the BL.
2. The poly-Si FG provides high energy barrier (3.15eV) from electron tunneling during retention.



(a) (b)

Figure 1.6: (a) Comparison of relative bit cost of 3-D architecture NAND flash between the stacking of conventional 2-D planar NAND and Bit-Cost Scalable (BiCS) NAND technology as the number of layer increases. (b) BiCS fabrication method [9].

SK Hynix has been actively developing their 3-D FG NAND flash. Various form of 3-D FG cells was proposed such as the Dual-Control Gate Surrounding-Floating Gate (DC-SF), the Separated-Sidewall Control Gate (S-SCG) and the Sidewall Control Pillar (SCP). The most notable has been the SCP cell due to its capability of suppressing the interference effects, cell disturbances, fast P/E operation and accommodate downscaling to 20nm half-pitch. However, in early 2016, it was IMFT that caught the attention of computer consumers by announcing their first generation 3-D vertical NAND [14]. The 3-D NAND cell is based on Conventional-Floating Gate (C-FG) structure that uses the double poly-Si technology and conventional P/E schemes. Due to its large physical cell size compared to the 20nm NAND, better performance can be achieved. The wide memory window of approximately >10V is obtained indicating a greater number of electron stored in the floating gate. This gives a good indication for Multi-Level Cell (MLC) and Tri-Level Cell (TLC) applications, where 256Gbit (MLC)/384Gbit (TLC) data per die is expected to be stored in 32-layers vertical stack. The GAA structure also plays an important role in giving strong electrostatic gate control to improve the coupling

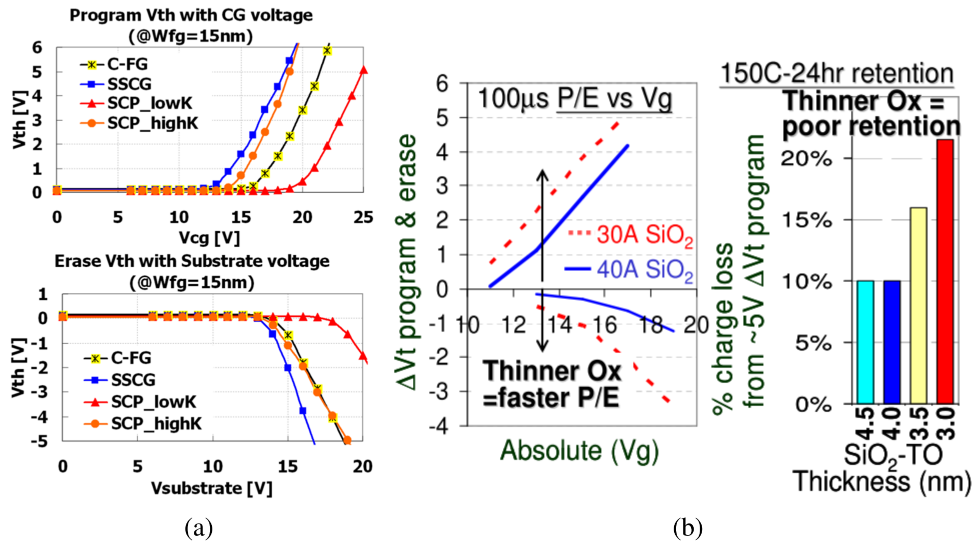
effects by aggressively reducing the total interference effects and threshold voltage distribution in planar 20nm 2-D NAND by ~80% and ~50% respectively [14]. Larger gate width/length ratio also added to its gate control capability to compensate the low mobility of polysilicon channel and increases the string on-current. In addition, it is reported that the IMFT 3-D cell with 32-layer vertical stack has the highest bit density of 1.52Gb/mm^2 compared to Samsung CT cell of 1.01 Gb/mm^2.

1.3 Problem Statements

Although the 3-D FG cell possesses relevant number of reliability advantages and high bit density compared to the 3-D CT cell, it also co-exists with cell-to-cell interference causes by poor coupling at the floating gate and become more severe when it comes to 3-D stacked architecture that led to higher programming voltage than its CT counterpart [15]. As can be seen from Figure 1.7(a), C-FG cell requires higher program voltage to yield wide threshold shift compared to SCP and S-SCG cells. Applying high program voltage on a select cell can induce high-field at channel interface and speedup the programming time, but this may eventually cause over-programming to its neighboring cells. Thinning the tunnel oxide thickness can also boost the programming speed and provides scalable P/E voltages but increases the rate of electrons tunneling back into the channel during retention. Figure1.7(b) depicts dramatic charge-loss in planar CT cell for tunnel oxide thickness below 4nm. As for the case of FG cell, the tunnel oxide can hardly be scaled below 6-7nm to prevent from severe charge loss [2]. Therefore, there has been a trade-off between scaling the tunnel oxide for scalable program voltage with data retention.

Nonetheless, given its conventional P/E schemes and less number of variability issues, the C-FG cell with GAA structure seems has been utilized as 3-D NAND flash memory [14]. In order to provide fast program operation and 10 years data retention, the tunnel dielectric layer must be scaled. A tunnel barrier engineering concept known as Variable Oxide Thickness (VARIOT) has been proposed through combinations of low-k/high-k stack to deal with the trade-off of P/E characteristics performance without severely jeopardizing the data retention capability [16, 17]. Govoreanu *et. al.,* (2003) have shown that by stacking the high-k material such as ZrO_2 on top of the low-k SiO_2 can increase the gate tunneling current while very low current is observed at low gate bias due to its thick physical thickness [16]. However, this method has yet to be utilized in 3-D FG cell leaving question marks to what combination of low-k/high-k that is suitable for boosting the P/E operation speed and retention characteristics.

Considering the characteristics of VARIOT that yield high electric field in its layer and thicker physical thickness than SiO_2, it is expected that the performances of P/E and reliability of GAA-FG can be compensated.



(a) (b)

Figure 1.7: (a) Comparison of threshold voltage shift after program with control gate voltage (Vcg) and after bulk erase between C-FG, S-SCG and SCP 3-D NAND cells [18]. (b) Trade-off between P/E scalability and retention characteristics for differents tunnel oxide thickness [19].

Computer Aided Design (CAD) tools have been vital for Integrated Circuit (IC) design. Circuit simulator is one of the CAD tools that have been widely used by designers in understanding circuit behavior and details of its operation. It allows quick evaluation of circuit performance without costly having to fabricate the integrated prototype. However, one should bear in mind that the accuracy of the results computed by the simulator depends on the quality of discrete device models. Thus, to acquire an accurate compact model, serve as the critical component for circuit designers in assessing the performance of mixed analog-digital circuit and play a crucial role in chip design productivity for semiconductor foundries.

A physics-based compact model is indispensable for device characterization, optimization and circuit simulation. A good compact model should meet several requirements, which are [20]:- the model is physically accurate, independent of fitting parameters, and also to ensure numerical convergence in Simulation Program with Integrated Circuit Emphasis (SPICE) simulator, the models must be described by an explicit and continuous expression over the entire operating regions [21]. Therefore, in order to accommodate experimental works for parameter extraction and to allow for

quick evaluation of circuitry or even discrete device performances, it is essential to develop a compact model for GAA-FG.

To model the electrical behaviour of GAA-FG cell, the GAA nanowire-FET (GAANWFET) core models must be comprehended. There are two types of GAANWFET which are the conventional GAANWFET and the most recent, junctionless-based GAANWFET or known as Junctionless Nanowire Transistor (JNT). Although there have been numerous works on compact modeling of GAANWFETs, especially for the conventional one, there are opportunities for further refinement. It can be described as follows;

For conventional GAANWFET:-

1. Several attempts are made to explicitly solve the arbitrary body-doped GAANWFET [22–24]. But the models are limited for dopant concentration up to 5×10^{18} cm^{-3} despite having empirical parameters being used [23] and neglected the importance of trap states along the channel for a realistic compact model. Furthermore, some of the models have also assumed zero flat-band voltage to fit the numerical TCAD simulation, which is physically unreasonable [24, 25].
2. Another important feature in GAANWFET is the partial-depletion conduction in highly-doped condition. Most of the models developed for GAANWFET invoked the full-depletion approximation to simplify the nonlinearity of Poisson's equation so that it can be integrated across the channel length. Thus, the model is accurate only for fully-depleted device and limited to doping-geometry ratio up to 0.45 [23, 26–31] that can lead to misinterpretation of its subthreshold performance. An attempt to include the partial-depletion conduction and to extend the validity of doping-geometry ratio only results in poor accuracy to its low-doped body condition [32].

For Junctionless Nanowire Transistor (JNT):-

1. Most models reported for JNT are regional, and the current expressions are piecewise continuous, where additional smoothing functions that rely on fitting parameters are required to unify between regions [33–38]. In addition, there are other JNT models that are continuous but took an implicit form [39–41]. The implicit form solution requires iterative numerical method, which either

converges very slowly or does not converge due to imaginary value [42]. Therefore, a nonpiecewise continuous and explicit model is required for JNT.

2. Quasi-static terminal charges and capacitance are essential for ac and transient simulation. As far as this work is concerned, there are very few works that provide with analytical solution of terminal charges and capacitnace for JNT [20, 43]. The developed solution for these parameters involves additional smoothing functions and rely on fitting parameters to fit the graph despite suffering in terms of accuracy as much as 16% [43]. While other, requires demanding derivation processes using partial derivative in solving the capacitance [20].

1.4 Research Objectives

The mutual target of this research is to design and enhance the performance of GAA-FG cell by implementing the concept of VARIOT and to develop its compact model using charge-based explicit expression. Based on the limitations and trade-offs in C-FG cell, also considering the performance expectation of VARIOT as the tunnel oxide layer, and the modeling issues in GAANWFET devices, the objectives are summarized as follow:

1. To optimize and determine a suitable VARIOT combination of low-k/high-k stack for GAA-FG cell in compensating the trade-off between P/E and retention characteristics.
2. Compact model of conventional GAANWFET:-
   (a) To explicitly solve the mobile charge density for arbitrary body doping including the trap state effects.
   (b) To analytically model the partial-depletion conduction.
3. Compact model of Junctionless Nanowire Transistor:-
   (a) To explicitly solve the mobile charge density that is continuous for all operating regions.
   (b) To obtain a continuous drain current, terminal charges and capacitance expressions.
4. To model the floating gate potential of GAA-FG.

1.5 Research Scopes

The scopes of this research will be confined as follows:

1. *GAA-FG Design*: The dimension and physical parameters of GAA-FG are based on experimental work performed by Lee *et al.*, (2013) [44]. Although the experimental data by Lee *et al.*, (2013) has used triangular nanowire as the channel, but in order to comply with vertical channel fabrication process the cylindrical channel has been used in this simulation work. In addition, the physical transport between triangular and cylindrical channels remain the same. Barrier Engineered of VARIOT tunnel oxide is limited to asymmetric combinations of low-k/high-k stack given the relevance for enhancing program operation and retention performances.
2. *Simulation Work*: Technological-Computer-Aided-Design (TCAD) simulation work is divided into two parts; parameters optimization and device simulation of GAA-FG. Based on MOS capacitor (MOS-C) structure and for a given flash memory constraint, extensive parameter optimization is conducted to obtain optimum parameter settings. Device simulation is performed to observe and analyze the transfer characteristics and transient memory performances of a discrete single-cell/transistor GAA-FG. Under this condition, the effects from neighbouring cell are omitted.
3. *Analytical Modeling*: Device compact modeling of GAA-FG, which involves obtaining the explicit expression of mobile charge densities for GAA nanowire-FET, and the floating gate potential model. The compact model is limited to the essence of core model, which are long-channel and constant mobility. Therefore, the compact model does not include advanced physical effects. The accuracy of the explicit expression is discussed based on the accuracy of previously published works and 3-D device simulation over practical terminal voltages.

1.6 Research Contribution

The significant contribution of this work can be highlighted as follow:-

1. *Optimization of VARIOT*: The optimization of VARIOT tunnel layer that consists of low-k/high-k stack is performed for various high-k materials in order to determine their optimum thickness and to extract its tunneling properties. The

extracted optimum thickness for various low-k/high-k stack can be used as a tunnel oxide layer in a memory cell devices. Given the nonlinear behaviour of tunnel barrier engineering, the tunneling properties of VARIOT such as Fowler-Nordheim (F-N) coefficients can be exploited by circuit designer in analyzing the P/E performances of a memory cell or even to analyze the effect of gate leakage in a MOSFET device that uses VARIOT as its gate oxide.

2. *GAA-FG with VARIOT tunnel layer*: Subsequent to the optimization of VARIOT, the optimized thickness of low-k/high-k stacks are employed as a tunnel layer in GAA-FG cell to improve its P/E characteristics as well as its data retention.

3. *Explicit and continuous compact model of GAA devices*: To the relevance of GAA-FG cell that adopted nanowire structure, the compact model of nanowire devices, which are the GAANWFET and the JNT are developed. In this study, due to the importance of highly-doped body of GAANWFET, the partial-depletion conduction is considered in improving the accuracy of the compact model. For the sake of avoiding numerical convergence and piecewise model, an explicit nonpiecewise and continuous compact model of JNT is developed.

1.7 Thesis Organization

Chapter 1 is the foundation of this research. A brief background on memory devices and its development throughout the years in highlighting on memory storage demand due to rapid technology advancement that prompt to the importance of flash memory. Then, scaling challenges and motivations of flash memory are highlighted that deduced the problem statements. Based on the problem statements, research objectives are identified. The scope of work has been clarified depending on the existing experimental and tools provided. Finally, the contributions of this work are highlighted.

Chapter 2 covers broad overview on 3-D NAND cell structures, where advantages and disadvantages from each structure are being highlighted. In conjunction with VARIOT tunnel layer, the concept of barrier engineering is discussed based on the types of dielectric stacking as well as its physical transport. Device modeling is briefly described before in-depth review on modeling approach of GAA nanowire-FET and floating gate potential modeling are discussed.

Chapter 3 discusses the research method of this work starting from general flow

and technical works that are being conducted in achieving the objectives. The tools that were used in this research are also highlighted. Furthermore, details on the approach taken in simulation work such as dielectric material, optimization method and physical models, and also compact modeling work such as model-flow and approximation techniques are presented in the form flowchart and discussed.

In Chapter 4, all the simulation results are presented, which includes optimization of VARIOT and characterization of GAA-FG in determining which VARIOT combination is the most prowess for its application as memory cell in providing fast P/E operation as well as 10 years data retention. As a consequent to simulation work of GAA-FG, Chapter 5 provides with a comprehensive explanation on analytical modeling with regards to all the issues highlighted in the research problem, until the compact model for GAA-FG is concluded.

Finally, Chapter 6 summarizes all the findings in this research and the contributions are highlighted. In addition, to ensure the continuation of this research and to add more promising contributions to compact model society, future works are provided.

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APPENDIX A

PARAMETER OPTIMIZATION OF ASYMMETRIC VARIOT

Table A.1: Parameters and data for SiO_2/Si_3N_4 extracted from TCAD simulation.

EOT (nm)	T_{ox}(nm)	T_{hk}(nm)	V_{prog}(V)	V_{read_dis}(V)	V_{ret}(V)	V_{tr} (V)	V_{fn} (V)
4	1	5.8	3.7	2.1	-2.3	8.0	12.8
	2	3.8	3.6	1.9	-1.5	4.0	6.4
	3	1.9	4.8	1.8	-0.8	2.7	4.3
	4	0.0	4.7	1.7	0	2.0	3.2
5	1	7.7	4.5	2.5	-3.2	10.0	16.0
	2	5.8	4.5	2.4	-3.9	5.0	8.0
	3	3.8	6.0	2.3	-3.9	3.3	5.3
	4	1.9	6	2.5	-3.2	2.5	4.0
	5	0.0	5.9	3.2	-1.7	2.0	3.2
6	1	9.6	5.4	3.0	-3.4	12.0	19.2
	2	7.7	5.3	2.9	-4.0	6.0	9.6
	3	5.8	7.2	2.8	-4.5	4.0	6.4
	4	3.8	7.1	3.0	-4.6	3.0	4.8
	5	1.9	7.0	3.8	-4.5	2.4	3.8
	6	0.0	7.0	3.8	-4.2	2.0	3.2
7	1	11.5	6.3	3.5	-3.8	14.0	22.4
	2	9.6	6.2	3.3	-4.0	7.0	11.2
	3	7.7	8.4	3.3	-4.2	4.7	7.5
	4	5.7	8.3	3.5	-5.1	3.5	5.6
	5	3.8	8.1	4.4	-5.2	2.8	4.5
	6	1.9	8.2	4.4	-4.9	2.3	3.7
	7	0.0	8.2	4.4	-4.6	2.0	3.2
8	1	13.5	7.2	4.0	-4.3	16.0	25.6
	2	11.5	7.1	3.8	-4.2	8.0	12.8
	3	9.6	9.6	3.7	-4.3	5.3	8.5
	4	7.7	9.5	4.0	-4.6	4.0	6.4
	5	5.8	9.3	5.0	-5.7	3.2	5.1
	6	3.8	9.4	5.0	-5.8	2.7	4.3
	7	1.9	9.4	5.0	-5.5	2.3	3.7
	8	0.0	9.4	5.0	-5.1	2.0	3.2

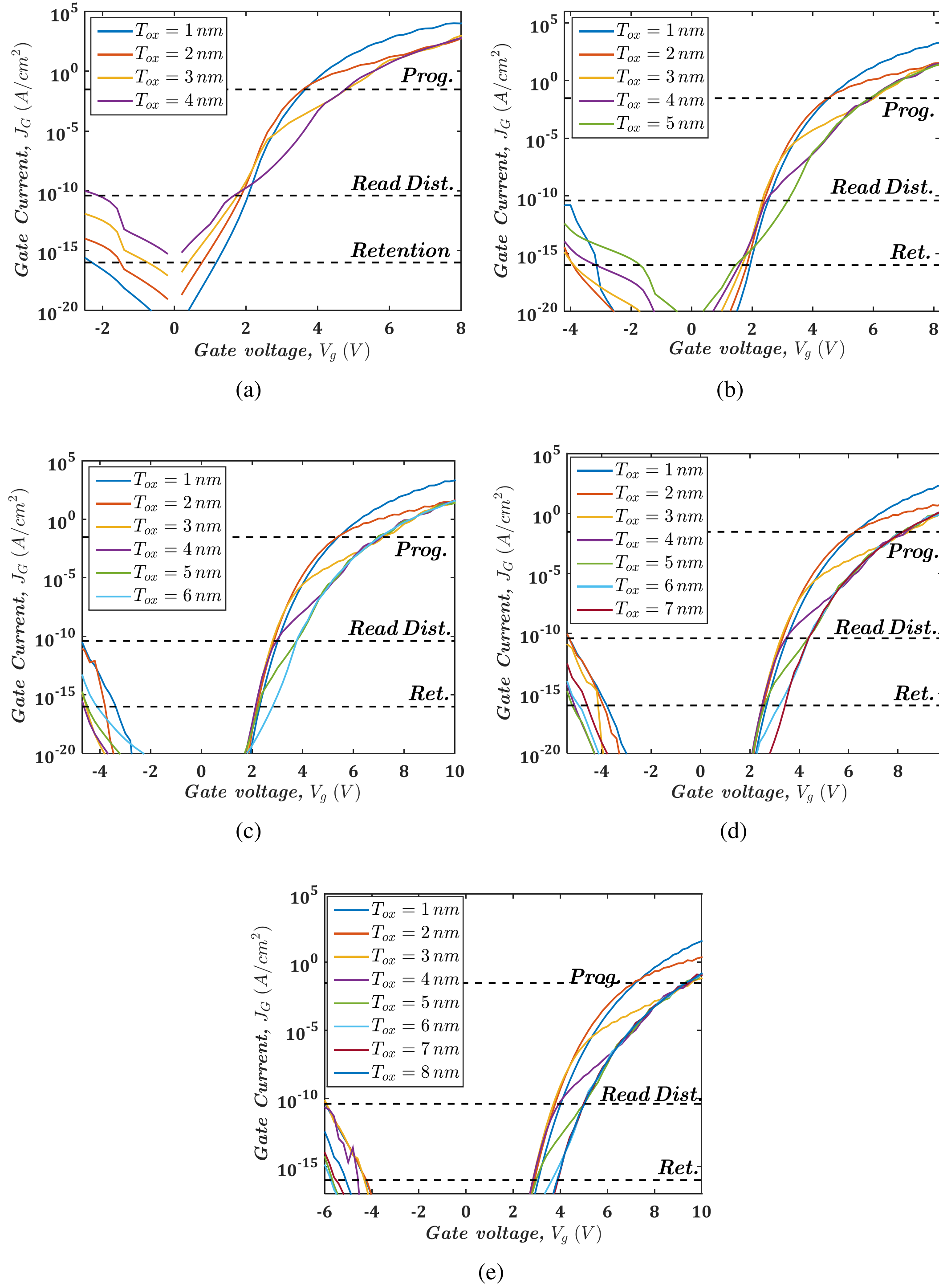

Figure A.1: $J_g - V_g$ characteristics of SiO_2/Si_3N_4 for EOT (a) 4nm (b) 5nm (c) 6nm (d) 7nm and (e) 8nm.

Table A.2: Parameters and data for SiO_2/Al_2O_3 extracted from TCAD simulation.

EOT (nm)	T_{ox}(nm)	T_{hk}(nm)	V_{prog}(V)	V_{read_dis}(V)	V_{ret}(V)	V_{tr} (V)	V_{fn} (V)
4	1	7.2	5.5	3.1	-4.6	9.6	12.8
	2	4.8	4.7	2.9	-4.1	4.8	6.4
	3	2.4	4.8	2.5	-1.8	3.2	4.3
	4	0.0	4.8	1.7	0	2.4	3.2
5	1	9.5	6.7	4.1	-5.3	12.0	16.0
	2	7.2	5.8	3.3	-5.3	6.0	8.0
	3	4.8	6.0	3.1	-5.0	4.0	5.3
	4	2.4	6.0	2.8	-4.3	3.0	4.0
	5	0.0	5.9	3.2	-1.8	2.4	3.2
6	1	11.9	8.2	4.9	-6.1	14.4	19.2
	2	9.5	6.9	4.3	-6.0	7.2	9.6
	3	7.2	7.2	4.0	-6.2	4.8	6.4
	4	4.8	7.2	3.7	-5.6	3.6	4.8
	5	2.4	7.2	3.8	-4.9	2.9	3.8
	6	0.0	7.1	3.8	-4.2	2.4	3.2
7	1	14.3	9.4	5.7	-6.9	16.8	22.4
	2	11.9	8.1	5.0	-6.9	8.4	11.2
	3	9.5	8.3	4.6	-6.9	5.6	7.5
	4	7.2	8.4	4.3	-7.0	4.2	5.6
	5	4.8	8.2	4.4	-6.5	3.4	4.5
	6	2.4	8.3	4.4	-5.5	2.8	3.7
	7	0.0	8.2	4.4	-4.6	2.4	3.2
8	1	16.7	10.8	6.5	-7.7	19.2	25.6
	2	14.3	9.2	5.7	-7.7	9.6	12.8
	3	11.9	9.5	5.2	-7.7	6.4	8.5
	4	9.5	9.5	4.9	-7.7	4.8	6.4
	5	7.2	9.4	5.0	-7.8	3.8	5.1
	6	4.8	9.4	5.0	-7.2	3.2	4.3
	7	2.4	9.4	5.0	-6.2	2.7	3.7
	8	0.0	9.5	5.0	-5.1	2.4	3.2

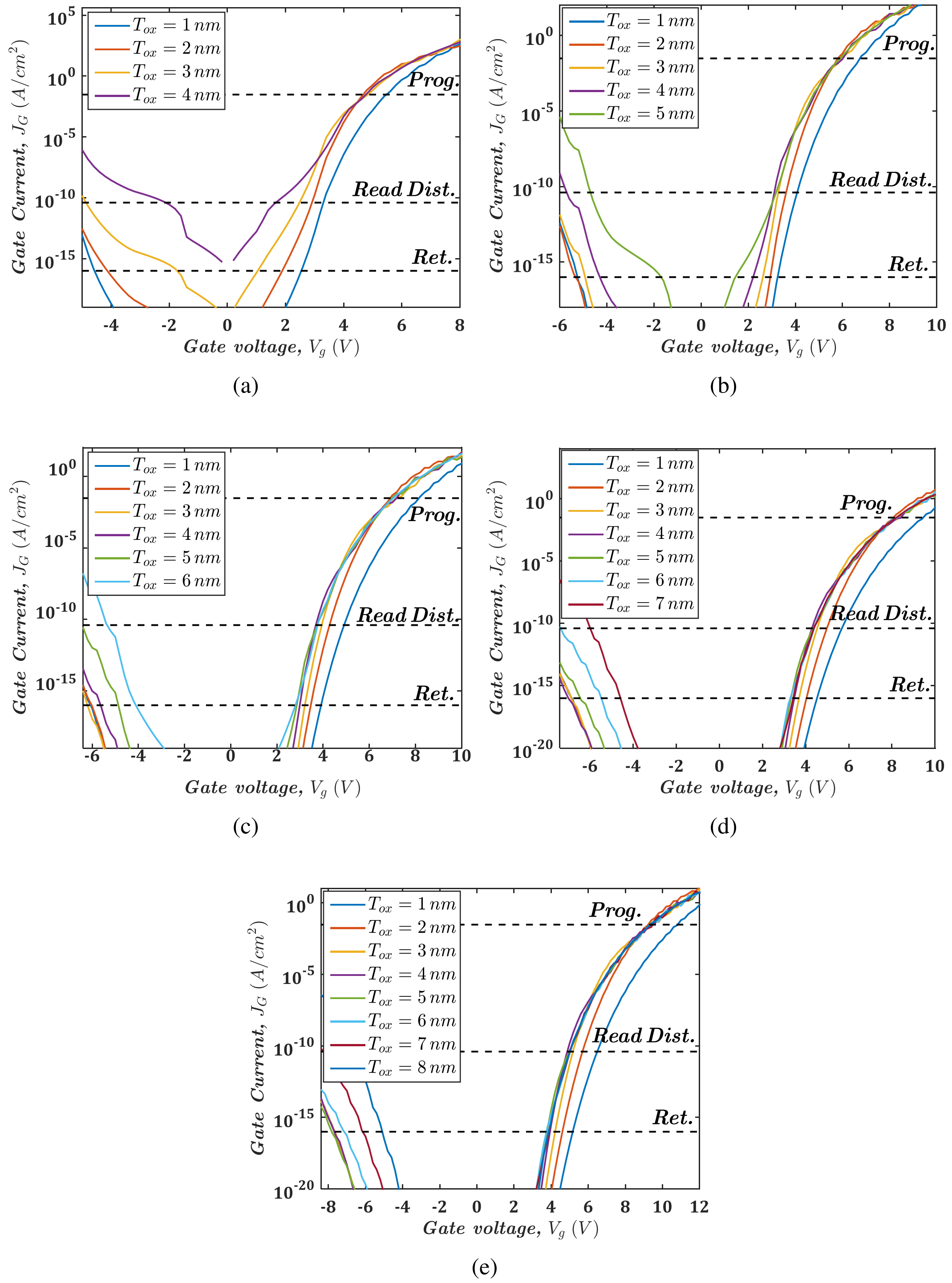

Figure A.2: $J_g - V_g$ characteristics of SiO_2/Al_2O_3 for EOT (a) 4nm (b) 5nm (c) 6nm (d) 7nm and (e) 8nm.

Table A.3: Parameters and data for SiO_2/HfO_2 extracted from TCAD simulation.

EOT (nm)	T_{ox}(nm)	T_{hk}(nm)	V_{prog}(V)	V_{read_dis}(V)	V_{ret}(V)	V_{tr} (V)	V_{fn} (V)
4	1	14.6	3.0	1.7	-2.2	6.0	12.8
	2	9.7	2.8	1.5	-3.5	3.0	6.4
	3	4.9	4.9	1.5	-3.1	2.0	4.3
	4	0.0	4.8	1.7	0.0	1.5	3.2
5	1	19.5	3.8	2.1	-2.7	7.5	16.0
	2	14.6	3.5	1.8	-3.5	3.8	8.0
	3	9.7	6.4	1.8	-4.1	2.5	5.3
	4	4.9	6.3	2.2	-4.5	1.9	4.0
	5	0.0	5.9	3.2	-1.7	1.5	3.2
6	1	24.4	4.5	2.5	-3.2	9.0	19.2
	2	19.5	4.2	2.2	-3.5	4.5	9.6
	3	14.6	7.5	2.2	-3.7	3.0	6.4
	4	9.7	7.3	2.7	-4.8	2.3	4.8
	5	4.9	7.0	3.9	-4.9	1.8	3.8
	6	0.0	7.0	3.8	-4.1	1.5	3.2
7	1	29.2	5.2	2.9	-3.5	10.5	22.4
	2	24.4	5.0	2.6	-3.6	5.3	11.2
	3	19.5	8.7	2.5	-4.0	3.5	7.5
	4	14.6	8.4	3.1	-4.4	2.6	5.6
	5	9.7	8.0	4.5	-5.4	2.1	4.5
	6	4.9	8.2	4.4	-5.6	1.8	3.7
	7	0.0	8.2	4.4	-4.6	1.5	3.2
8	1	34.1	5.9	3.3	-3.9	12.0	25.6
	2	29.2	5.6	2.9	-3.9	6.0	12.8
	3	24.4	9.9	2.9	-3.9	4.0	8.5
	4	19.5	9.6	3.5	-4.5	3.0	6.4
	5	14.6	9.2	5.0	-5.1	2.4	5.1
	6	9.7	9.2	5./0	-6.0	2.0	4.3
	7	4.9	9.5	5.0	-6.6	1.7	3.7
	8	0.0	9.4	5.0	-5.2	1.5	3.2

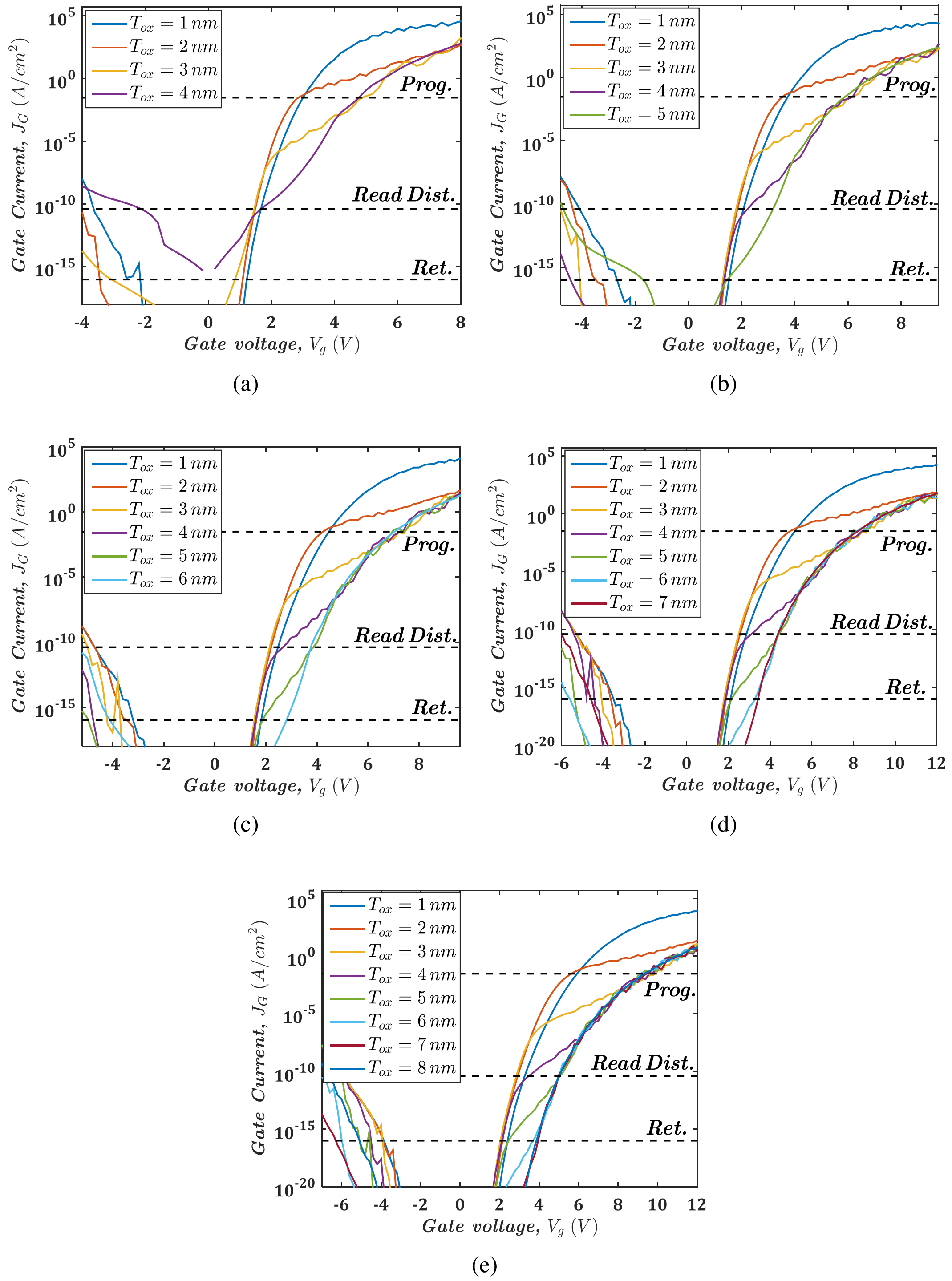

Figure A.3: $J_g - V_g$ characteristics of SiO_2/HfO_2 for EOT (a) 4nm (b) 5nm (c) 6nm (d) 7nm and (e) 8nm.

Table A.4: Parameters and data for SiO_2/ZrO_2 extracted from TCAD simulation.

EOT (nm)	T_{ox}(nm)	T_{hk}(nm)	V_{prog}(V)	V_{read_dis}(V)	V_{ret}(V)	V_{tr} (V)	V_{fn} (V)
4	1	19.2	3.0	1.7	-2.6	5.6	12.8
	2	12.8	2.8	1.4	-3.5	2.8	6.4
	3	6.4	4.9	1.4	-4.0	1.9	4.3
	4	0.0	4.8	1.7	0.0	1.4	3.2
5	1	25.4	3.7	2.1	-3.2	7.0	16.0
	2	19.2	3.4	1.8	-3.8	3.5	8.0
	3	12.8	6.2	1.7	-4.4	2.3	5.3
	4	6.4	6.1	2.2	-4.8	1.8	4.0
	5	0.0	5.9	3.2	-1.7	1.4	3.2
6	1	32.1	4.5	2.5	-3.6	8.4	19.2
	2	25.6	4.1	2.1	-3.9	4.2	9.6
	3	19.2	7.2	2.1	-4.4	2.8	6.4
	4	12.8	7.3	2.6	-5.0	2.1	4.8
	5	6.4	7.1	3.8	-5.5	1.7	3.8
	6	0.0	7.2	3.8	-4.1	1.4	3.2
7	1	38.5	5.2	2.9	-4.0	9.8	22.4
	2	32.1	4.8	2.5	-4.0	4.9	11.2
	3	25.6	8.5	2.4	-4.3	3.3	7.5
	4	19.2	8.4	3.1	-4.9	2.5	5.6
	5	12.8	8.2	4.5	-5.3	2.0	4.5
	6	6.4	8.3	4.4	-6.2	1.6	3.7
	7	0.0	8.2	4.4	-4.6	1.4	3.2
8	1	44.9	5.7	3.3	-4.4	11.2	25.6
	2	38.5	5.4	2.8	-4.4	5.6	12.8
	3	32.1	9.8	2.7	-4.4	3.7	8.5
	4	25.6	9.6	3.5	-4.9	2.8	6.4
	5	19.2	9.4	5.1	-5.4	2.2	5.1
	6	12.8	9.4	5.0	-6.2	1.9	4.3
	7	6.4	9.4	5.0	-7.0	1.6	3.7
	8	0.0	9.4	5.0	-5.1	1.4	3.2

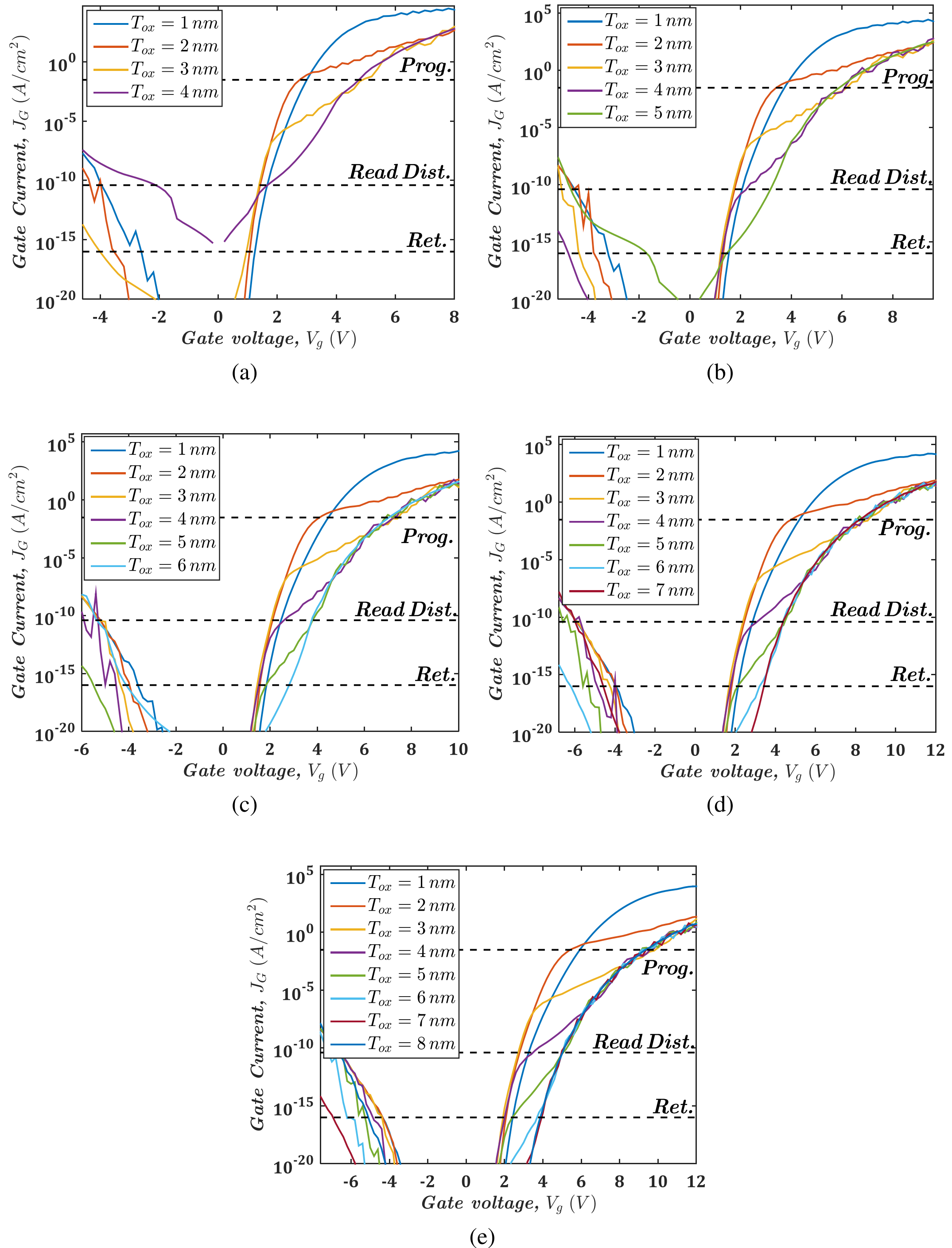

Figure A.4: $J_g - V_g$ characteristics of SiO_2/ZrO_2 for EOT (a) 4nm (b) 5nm (c) 6nm (d) 7nm and (e) 8nm.

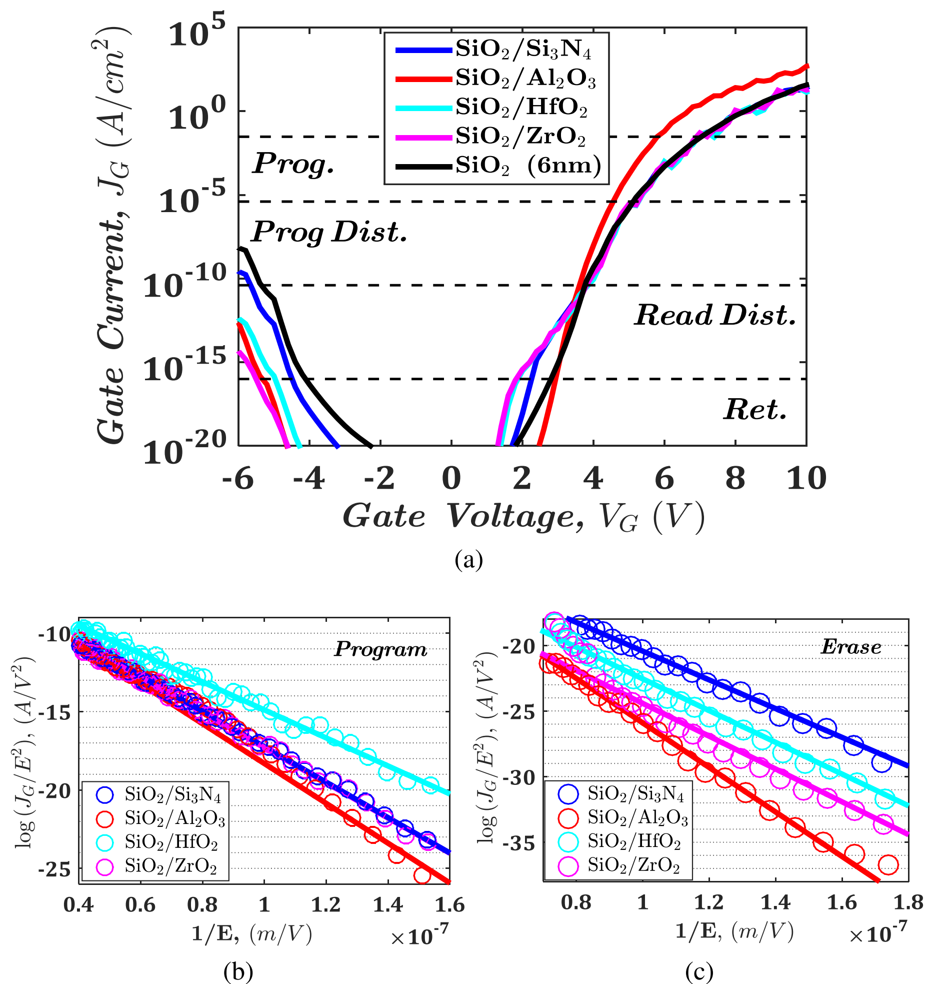

Figure A.5: (a) JV characteristics for the optimized parameters of all asymmetric VARIOTs conducted. F-N plot of all asymmetric VARIOTs conducted for (b) programming and (c) erase operations.

APPENDIX B

DERIVATION OF CHARGE-BASED COMPACT MODEL

B.1 Charge-Based Compact Model for Partially-Depleted GAANWFETs

Derivation for UCCM Expression;

Poisson's equation in 1-D for a semiconductor system given as

$$\nabla^2\phi = -\frac{\rho}{\epsilon_{si}} = -\frac{q\left(p - n + N_D^+ - N_A^-\right)}{\epsilon_{si}} \tag{B.1}$$

$$\frac{1}{r}\frac{d}{dr}\left(r\frac{d\phi\left(r\right)}{dr}\right) = \frac{qN_A}{\epsilon_{si}}\left(1 + \exp\left(\frac{\phi\left(r\right) - 2\phi_f - V}{\phi_t}\right)\right) \tag{B.2}$$

$$r\frac{d\phi\left(r\right)}{dr} = \frac{qN_A r^2}{2\epsilon_{si}} + \int_0^r \left(\frac{qN_A}{\epsilon_{si}}\exp\left(\frac{\phi_0 - 2\phi_f - V}{\phi_t}\right)\right) r \cdot dr \tag{B.3}$$

given the boundary condition in GAANWFET as

$$\left.\frac{d\phi}{dr}\right|_{r=0} = 0,\ \phi\left(r = 0\right) = \phi_0,\ \phi\left(r = R\right) = \phi_s \tag{B.4}$$

The Poisson has no analytical solution due to potential being dependence to r. In order to integrate the expression, Following [26], it need to be initially solved for weak

inversion and fully-depleted case before latter the moderate and the strong inversion are included. In weak inversion the potential at the surface and the center body is same ($\phi_0 = \phi_s$), similar goes to its carrier concentration ($n_0 = n_s$).

$$\frac{1}{r}\frac{d}{dr}\left(r\frac{d\phi\left(r\right)}{dr}\right) = \frac{qN_A}{\epsilon_{si}}\left(1+\exp\left(\frac{\phi_0 - 2\phi_f - V}{\phi_t}\right)\right) \tag{B.5}$$

Perform the 1st integral for any value of r

$$r\frac{d\phi\left(r\right)}{dr} = \int_0^r \frac{qN_A}{\epsilon_{si}}\left(1+\exp\left(\frac{\phi_0 - 2\phi_f - V}{\phi_t}\right)\right) r\cdot dr \tag{B.6}$$

$$\frac{d\phi\left(r\right)}{dr} = \frac{qN_A r}{2\epsilon_{si}} + \frac{qn_0 r}{2\epsilon_{si}} \tag{B.7}$$

Multiply with R/R

$$\frac{d\phi\left(r\right)}{dr} = \left(\frac{qN_A R}{2R\epsilon_{si}} + \frac{qn_0 R}{2R\epsilon_{si}}\right)\cdot r \tag{B.8}$$

By replacing $Q_{dep} = qN_A R/2$ and $Q_m = qn_0 R/2$

$$d\phi\left(r\right) = \left(\frac{Q_{dep}+Q_m}{R\epsilon_{si}}\right) r\cdot dr \tag{B.9}$$

Replace $r\cdot dr$ into Poisson equation without the weak inversion assumption

$$r\frac{d\phi\left(r\right)}{dr} = \frac{qN_A r^2}{2\epsilon_{si}} + \int_{\phi_0}^{\phi}\left(\frac{qN_A}{\epsilon_{si}}\exp\left(\frac{\phi\left(r\right) - 2\phi_f - V}{\phi_t}\right)\right)\left(\frac{R\epsilon_{si}}{Q_{dep}+Q_m}\right)\cdot d\phi\left(r\right) \tag{B.10}$$

Solve for RHS from $\phi\left(r=0\right)=\phi_0$ to $\phi\left(r=r\right)=\phi$ and using the boundary condition of $\left.\frac{d\phi}{dr}\right|_{r=R}=-E_s$, the Poisson can be obtained as

$$\begin{aligned}\left.\frac{d\phi}{dr}\right|_{r=R} &= \frac{Q_{dep}}{\epsilon_{si}}+\frac{\phi_t}{R}\left(\frac{2Q_{dep}}{Q_{dep}+Q_m}\right)\left(1-\exp\left(\frac{\phi_0-\phi_s}{\phi_t}\right)\right) \\ &\quad\times\exp\left(\frac{\phi_s-2\phi_f-V}{\phi_t}\right)\end{aligned} \tag{B.11}$$

The second term is actually the total mobile charge, Q_m at the channel interface

$$\frac{Q_m}{\epsilon_{si}}=\frac{\phi_t}{R}\left(\frac{2Q_{dep}}{Q_{dep}+Q_m}\right)\left(1-\exp\left(\frac{\phi_0-\phi_s}{\phi_t}\right)\right)\cdot\exp\left(\frac{\phi_s-2\phi_f-V}{\phi_t}\right) \tag{B.12}$$

Using full-depletion approximation of $\left(\phi_0-\phi_s\right)/\phi_t=qN_AR^2/4\epsilon_{si}$. Taking logarithm to both side and solve for ϕ_s

$$\begin{aligned}\phi_s &= 2\phi_f+V+\phi_t\ln\left(\frac{R}{2\phi_t\epsilon_{si}}\right)-\phi_t\ln\left(1-\exp\left(-\frac{RQ_{dep}}{2\phi_t\epsilon_{si}}\right)\right) \\ &\quad+\phi_t\ln\left(Q_m\right)+\phi_t\ln\left(1+\frac{Q_m}{Q_{dep}}\right)\end{aligned} \tag{B.13}$$

However, Q_{dep} in the last term will results in overestimation of the surface potential in strong inversion region due to the weak inversion approximation. Therefore, following [26], parameter Q_{dep} is changed to $C_{ox}\phi_t/H$.

$$\begin{aligned}\phi_s &= 2\phi_f+V+\phi_t\ln\left(\frac{R}{2\phi_t\epsilon_{si}}\right)-\phi_t\ln\left(1-\exp\left(-\frac{RQ_{dep}}{2\phi_t\epsilon_{si}}\right)\right) \\ &\quad+\phi_t\ln\left(Q_m\right)+\phi_t\ln\left(1+H\frac{Q_m}{C_{ox}\phi_t}\right)\end{aligned} \tag{B.14}$$

Replacing the surface potential expression into Gauss's law that enclosed across the gate stack

$$C_{ox}\left(V_g-\Delta\varphi-\phi_s\right)=Q_{dep}+Q_m-Q_f+qD_{it}\phi_s \tag{B.15}$$

$$V_g-V_{th}-\Delta V_{th}-\eta V=\frac{Q_m}{C_{ox}}+\eta\phi_t\ln\left(\frac{Q_m}{Q_0}\right)+\eta\phi_t\ln\left(1+\frac{Q_m}{Q_0}\right) \tag{B.16}$$

where $Q_0 = C_{ox}\phi_t/H$ with

$$V_{th}=\Delta\varphi+2\eta\phi_f+\frac{Q_{dep}}{C_{ox}}-\frac{Q_f}{C_{ox}}-\eta\phi_t\ln\left(\frac{4\phi_t\epsilon_{si}Q_{dep}}{RQ_0}\right) \tag{B.17}$$

and

$$\Delta V_{th}=-\eta\phi_t\ln\left(\frac{1}{Q_0}\right) \tag{B.18}$$

Derivation for partial-depletion conduction;

$$\frac{1}{r}\frac{d}{dr}\left(r\frac{d\phi_2\left(r\right)}{dr}\right)=\frac{qN_A}{\varepsilon_{si}} \tag{B.19}$$

In partial-depletion conduction, the boundary conditions are given as

$$\frac{d\phi_2\left(r=r_{dep}\right)}{dr}=0,\ \phi_2\left(r=r_{dep}\right)=0,\ \phi_2\left(r=R\right)=\phi_2\,. \tag{B.20}$$

Solving for its first derivative

$$\frac{1}{r}\frac{d}{dr}\left(r\frac{d\phi_2\left(r\right)}{dr}\right)\left(\frac{d\phi_2\left(r\right)}{dr}\right)=\frac{qN_A}{\varepsilon_{si}}\left(\frac{d\phi_2\left(r\right)}{dr}\right) \tag{B.21}$$

$$\frac{1}{r}\frac{d}{dr}\left(r\frac{d\phi_2\left(r\right)}{dr}\right)\left(\frac{d\phi_2\left(r\right)}{dr}\right)=\frac{qN_A}{\varepsilon_{si}}\left(\frac{d\phi_2\left(r\right)}{dr}\right) \tag{B.22}$$

$$\left(\frac{d\phi_2\left(r\right)}{dr}\right)^2=\int_{r_{dep}}^{R}\frac{qN_A}{\varepsilon_{si}}\cdot d\phi_2\left(r\right) \tag{B.23}$$

$$\left.\frac{d\phi_2}{dr}\right|_{r=R}=\sqrt{\frac{qN_A}{\varepsilon_{si}}\cdot\phi_2}=\sqrt{\frac{qN_A}{\varepsilon_{si}}\cdot\phi_c}; \tag{B.24}$$

Solution for channel charge;

$$Q_{ch}=-2\pi R\int_0^L Q_m\,dy=-\mu\frac{\left(2\pi R\right)^2}{I_{ds}}\int_0^{V_d}Q_m^2\,dV \tag{B.25}$$

$$\begin{aligned} Q_{ch} \; = \; & \mu\frac{\left(2\pi R\right)^2}{I_{ds}}\left[\frac{Q_m}{3C_{ox}}+\frac{\eta\phi_t Q_m^2}{2}+\right. \\ & \left.\left.\eta\phi_t\left(Q_0^2\ln\left(Q_m+Q_0\right)+\frac{Q_m^2}{2}-Q_0Q_m\right)\right]\right|_{Q_{m0}}^{Q_{mL}} \end{aligned} \tag{B.26}$$

Solution for drain charge;

$$Q_d=-2\pi R\int_0^L\frac{y}{L}Q_m\,\frac{dy}{dQ_m}dQ_m \tag{B.27}$$

from current continuity equation

$$I_{ds} = 2\pi R\mu Q_m \frac{dV}{dy} = 2\pi R\mu Q_m \frac{dV}{dQ_m} \cdot \frac{dQ_m}{dy} \tag{B.28}$$

replacing dy/dQ_m of the current continuity equation into Q_d with dV/dQ_m is differentiate from UCCM expression

$$Q_d = -\frac{(2\pi R)^2}{I_{ds}} \int_0^L \frac{y}{L} Q_m^2 \left[-\frac{1}{C_{ox}} - \eta\phi_t \left(\frac{1}{Q_m} + \frac{1}{Q_m + Q_0}\right)\right] dQ_m \tag{B.29}$$

the distance along channel y is again obtained from current continuity equation by rearranging it to be in a function of dy as

$$dy = \frac{2\pi R\mu}{I_{ds}} Q_m \left[-\frac{1}{C_{ox}} - \eta\phi_t \left(\frac{1}{Q_m} + \frac{1}{Q_m + Q_0}\right)\right] \cdot dQ_m \tag{B.30}$$

integrating y from 0 to distance of y and Q_m from Q_{m0} to Q_m, distance y is obtained

$$y = \frac{2\pi R\mu}{I_{ds}} \left[\frac{Q_m^2 - Q_{m0}^2}{2C_{ox}} + \eta\phi_t \left(2\left(Q_m - Q_{m0}\right) - Q0 \cdot \log\left[\frac{Q_m + Q_0}{Q_{m0} + Q_0}\right]\right)\right] \tag{B.31}$$

replace y into expression Q_d

$$\begin{aligned} Q_d \quad = \quad & \int_{Q_{m0}}^{Q_{mL}} -\frac{((2\pi R)^3\mu^2)}{I_{ds}^2 L} \cdot \\ & \left[Q_m^2 \left(\eta\phi_t \left(2(Q_m - Q_{m0}) - Q_0 \log\left(\frac{Q_m + Q_0}{Q_0 + Q_{m0}}\right)\right) + \frac{Q_m^2 - Q_{m0}^2}{2C_{ox}}\right)\right. \\ & \left.\left(\eta\phi_t \left(\frac{1}{Q_m + Q_0} + \frac{1}{Q_m}\right) + \frac{1}{C_{ox}}\right)\right] dQ \end{aligned} \tag{B.32}$$

Solution to integration

$$\begin{aligned}
Q_d &= \frac{-4\pi^3 R^3 \mu^2}{C_{ox}^2 I_{ds}^2 L}\left[\frac{Q_{m0}}{90}\left(12Q_{m0}^4 + 30\eta C_{ox} Q_0^3 \phi_t + 75\eta C_{ox} Q_{m0}^3 \phi_t\right]\right. \\
&+40\eta C_{ox} Q_{m0}^2 \phi_t \left(-2Q_0 + 3\eta C_{ox}\phi_t\right) - 15\eta C_{ox} Q_0 Q_{m0} \phi_t \\
&(Q_0 + 18\eta C_{ox}\phi_t)) + \frac{1}{90} Q_{mL}\left(18Q_{mL}^4 + 135\eta C_{ox} Q_{mL}^3 \phi_t - 10Q_{mL}^2\right. \\
&\left(3Q_{m0}^2 + 12\eta C_{ox} Q_{m0}\phi_t + \eta C_{ox}\phi_t(Q_0 - 24\eta C_{ox}\phi_t)\right) + \\
&30\eta C_{ox} Q_0 \phi_t(-Q_0^2 + 3Q_{m0}(Q_{m0} + 4\eta C_{ox}\phi_t)) - 15\eta C_{ox} Q_{mL}\phi_t \\
&\left.(-Q_0^2 + 6\eta C_{ox} Q_0 \phi_t + 6Q_{m0}(Q_{m0} + 4\eta C_{ox}\phi_t))\right) \\
&-\frac{1}{3}\eta C_{ox} Q_0^2 \phi_t(-Q_0^2 + 3Q_{m0}(Q_{m0} + 4\eta C_{ox}\phi_t))\log\left(Q_0 + Q_{mL}\right) \\
&+\frac{2}{3}\eta C_{ox} Q_0 Q_{mL}\phi_t(-Q_{mL}^2 + 3\eta C_{ox} Q_0\phi_t - 3\eta C_{ox} Q_{mL}\phi_t)\cdot \\
&\log\left(\frac{Q_0 + Q_{mL}}{Q_0 + Q_{m0}}\right) - \eta^2 C_{ox}^2 Q_0^3 \phi_t^2 \log\left(\frac{Q_0 + Q_{mL}}{Q_0 + Q_{m0}}\right)^2 \\
&+\frac{1}{3}\eta C_{ox} Q_0^2 \phi_t \cdot (-Q_0^2 + 3Q_{m0}(Q_{m0} + 4\eta C_{ox}\phi_t)) \\
&\log\left(Q_0 + Q_{m0}\right)) \qquad \text{(B.33)}
\end{aligned}$$

B.2 Charge-Based Compact Model for Junctionless Nanowire Transistor

Derivation for UCCM Expression;

Poisson's equation in 1-D for a semiconductor system given as

$$\nabla^2\phi = -\frac{\rho}{\epsilon_{si}} = -\frac{q\left(p - n + N_D^+ - N_A^-\right)}{\epsilon_{si}} \qquad \text{(B.34)}$$

$$\frac{1}{r}\frac{d}{dr}\left(r\frac{d\phi\left(r\right)}{dr}\right) = -\frac{qN_D}{\epsilon_{si}}\left(1 - \exp\left(\frac{\phi\left(r\right) - V}{\phi_t}\right)\right) \qquad \text{(B.35)}$$

$$r\frac{d\phi\left(r\right)}{dr} = -\frac{qN_D r^2}{2\epsilon_{si}} + \int_0^r \left(\frac{qN_D}{\epsilon_{si}}\exp\left(\frac{\phi_0 - V}{\phi_t}\right)\right) r \cdot dr \qquad \text{(B.36)}$$

given the boundary condition in JNT as

$$\left.\frac{d\phi}{dr}\right|_{r=0} = 0,\ \phi\left(r=0\right) = \phi_0,\ \phi\left(r=R\right) = \phi_s \tag{B.37}$$

The Poisson has no analytical solution due to potential being dependence to r. In order to integrate the expression, Following [26], it need to be initially solved for weak inversion and fully-depleted case. In weak inversion the potential at the surface and the center body is same ($\phi_0 = \phi_s$), similar goes to its carrier concentration ($n_0 = n_s$).

$$\frac{1}{r}\frac{d}{dr}\left(r\frac{d\phi\left(r\right)}{dr}\right) = -\frac{qN_D}{\epsilon_{si}}\left(1 - \exp\left(\frac{\phi_0 - V}{\phi_t}\right)\right) \tag{B.38}$$

Perform the 1st integral for any value of r

$$r\frac{d\phi\left(r\right)}{dr} = \int_0^r \frac{qN_D}{\epsilon_{si}}\left(-1 + \exp\left(\frac{\phi_0 - V}{\phi_t}\right)\right) r \cdot dr \tag{B.39}$$

$$\frac{d\phi\left(r\right)}{dr} = -\frac{qN_A r}{2\epsilon_{si}} + \frac{qn_0 r}{2\epsilon_{si}} \tag{B.40}$$

Multiply with R/R

$$\frac{d\phi\left(r\right)}{dr} = \left(-\frac{qN_A R}{2R\epsilon_{si}} + \frac{qn_0 R}{2R\epsilon_{si}}\right) \cdot r \tag{B.41}$$

By replacing $Q_{dep} = qN_D R/2$ and $Q_m = qn_0 R/2$

$$d\phi\left(r\right) = \left(\frac{-Q_{dep} + Q_m}{R\epsilon_{si}}\right) r \cdot dr \tag{B.42}$$

Replace $r \cdot dr$ into Poisson equation without the weak inversion assumption

$$r\frac{d\phi\left(r\right)}{dr} = -\frac{qN_D r^2}{2\epsilon_{si}} + \int_{\phi_0}^{\phi}\left(\frac{qN_D}{\epsilon_{si}}\exp\left(\frac{\phi\left(r\right)-V}{\phi_t}\right)\right)\left(\frac{R\epsilon_{si}}{-Q_{dep}+Q_m}\right)\cdot d\phi\left(r\right) \tag{B.43}$$

Solve for RHS from $\phi\left(r=0\right)=\phi_0$ to $\phi\left(r=r\right)=\phi$ and using the boundary condition of $\left.\frac{d\phi}{dr}\right|_{r=R} = -E_s$, the Poisson can be obtained as

$$\begin{aligned}\left.\frac{d\phi}{dr}\right|_{r=R} &= -\frac{Q_{dep}}{\epsilon_{si}} + \frac{\phi_t}{R}\left(\frac{2Q_{dep}}{-Q_{dep}+Q_m}\right)\left(1-\exp\left(\frac{\phi_0-\phi_s}{\phi_t}\right)\right) \\ &\quad\times\exp\left(\frac{\phi_s-V}{\phi_t}\right)\end{aligned} \tag{B.44}$$

The second term is actually the total mobile charge, Q_m at the channel interface

$$\frac{Q_m}{\epsilon_{si}} = \frac{\phi_t}{R}\left(\frac{2Q_{dep}}{-Q_{dep}+Q_m}\right)\left(1-\exp\left(\frac{\phi_0-\phi_s}{\phi_t}\right)\right)\cdot\exp\left(\frac{\phi_s-V}{\phi_t}\right) \tag{B.45}$$

The potential relation is replaced by using parabolic potential profile of $\phi\left(r\right) = \left(\phi_s-\phi_0\right)r^2/R^2+\phi_0$, where $\left(\phi_s-\phi_0\right)/\phi_t = \left(-Q_{dep}+Q_m\right)/Q_{sc}$. Taking logarithm to both side and solve for ϕ_s

$$\begin{aligned}\phi_s &= \phi_t\ln\left(\frac{-Q_{dep}+Q_m}{Q_{dep}Q_{sc}}\right)+\phi_t\ln\left(Q_m\right)+V \\ &\quad -\phi_t\ln\left(1-\exp\left[-\left(\frac{-Q_{dep}+Q_m}{Q_{sc}}\right)\right]\right).\end{aligned} \tag{B.46}$$

Given Gauss's law at channel interface as

$$C_{ox}\left(V_g - V_{FB} - \eta\phi_s\right) = -Q_{dep} + Q_m \tag{B.47}$$

where η is the interface trap parameter and by substituting the surface potential into the Gauss's law, the UCCM expression for JNT is finally deduced as

$$V_g - V_{th} - \eta V = \frac{Q_m}{C_{ox}} + \eta\phi_t \ln\left(\frac{Q_m}{Q_{sc}}\right) - \eta\phi_t \ln\left(\frac{Q_{dep}\left[1 - \exp\left(-Q_T/Q_{sc}\right)\right]}{Q_T}\right) \tag{B.48}$$

The total charge, Q_T is inferred as $-Q_{dep} + Q_m$ and threshold voltage, $V_{th} = V_{FB} - Q_{dep}/C_{ox}$.

Solution to drain charge Q_d

$$Q_d = Q_{dDP} + Q_{dC} \tag{B.49}$$

$$Q_d = -2\pi R \int_0^L \frac{y}{L} Q_{DP} \frac{dy}{dQ_{DP}} dQ_{DP} - 2\pi R \int_0^L \frac{y}{L} Q_C \frac{dy}{dQ_C} dQ_C \tag{B.50}$$

Solution to integration of Equation (5.73)

$$\begin{aligned} Q_{dDP} \quad = \quad & -\frac{\left(Q_{DPL} - Q_{DP0}\right)^2\left(12Q_{DPL}^3 + 24Q_{DPL}^2 Q_{DP0} + 16Q_{DPL}Q_{DP0}^2 + 8Q_{DP0}^3\right)}{120Q_{eff}^2} \\ & -\frac{Q_{eff}\left(Q_{DPL} - Q_{DP0}\right)^2\left(45Q_{DPL}^2 + 50Q_{DPL}Q_{DP0} + 25Q_{DP0}^2\right)}{120\mathrm{QEQ}^2} \\ & -\frac{\left(Q_{DPL} - Q_{DP0}\right)^2\left(40Q_{DPL} + 20Q_{DP0}\right)}{120} \end{aligned} \tag{B.51}$$

Solution to integration of Equation (5.75)

$$
\begin{aligned}
Q_{dC} &= -\frac{\left(Q_{CL}-Q_{C0}\right)^{2}\left(6Q_{CL}^{3}+12Q_{CL}^{2}Q_{C0}+8Q_{CL}Q_{C0}^{2}+4Q_{C0}^{3}\right)}{60C_{C}^{2}\eta^{2}\phi_{t}^{2}} \\
&\quad -\frac{\eta\left(Q_{CL}-Q_{C0}\right)^{2}\left(45C_{C}\phi_{t}Q_{CL}^{2}+50C_{C}\phi_{t}Q_{CL}Q_{C0}+25C_{C}\phi_{t}Q_{C0}^{2}\right)}{60C_{C}^{2}\eta^{2}\phi_{t}^{2}} \\
&\quad -\frac{\left(Q_{CL}-Q_{C0}\right)^{2}\left(80C_{C}^{2}Q_{CL}\phi_{t}^{2}+40C_{C}^{2}Q_{C0}\phi_{t}^{2}\right)}{60C_{C}^{2}\phi_{t}^{2}} \qquad \text{(B.52)}
\end{aligned}
$$

APPENDIX C

PUBLICATION LIST

C.1 International Journal

1. Afiq Hamzah, N. Ezaila Alias and Razali Ismail, Low-Voltage High-Speed Programming Gate-All-Around Floating Gate (GAA-FG) Memory Cell with Tunnel Barrier Engineering, (2018). Japanese Journal of Applied Physics, 57(6S3), pp. 06KC02-1–06KC02-8 [Q3, IF=1.384].
2. Afiq Hamzah, M. A. Hilman, N. Ezaila Alias and Razali Ismail, “Scaling Challenges of Floating Gate Non-Volatile Memory and Graphene as the Future Flash Memory Device: A Review”, Journal of Nanoelectronics and Optoelectronics, (2018) [Q4, IF=0.45]. (Accepted)
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