

CLUSTERED TWO-DIMENSIONAL MESH TOPOLOGY FOR LARGE-SCALE
NETWORK-ON-CHIP ARCHITECTURE

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NETWORK-ON-CHIP ARCHITECTURE

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Dedication to my parents, my wife, and my kids.

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ABSTRACT

Driven by the continuous scaling of Moore's law, the number of processing cores in chip multiprocessors and systems-on-a-chip are expected to grow tremendously in the near future. Connecting the different components of a multiprocessor chip in a scalable and efficient way has become increasingly challenging. Current network-on-chip (NoC) topologies are adequate for small-size networks but are not optimized for large-scale networks. Transmitted packets inside a large NoC require longer route to reach their destinations, resulting in an increase in certain performance parameters such as latency and power consumption. Thus, it is necessary to develop a new topology appropriate for large-size NoCs. In this research, we proposed a cost-effective network topology for large-size NoCs that improves performance in terms of end-to-end latency. The topology, called RaMesh, consists of clusters of mesh networks. A routing algorithm suitable for this topology was also proposed. The RaMesh architecture together with mesh, torus, and clustered 2D-mesh were simulated using Noxim (NoC simulator), C for software NoC models, and Altera ModelSim for Verilog hardware models. Simulations were conducted under different network traffic and for a variety of network sizes. Experimental results showed that RaMesh performed better than equivalent 2D-mesh and torus topologies. RaMesh topology was also benchmarked against a clustered mesh topology. Average hop count in the proposed topology was at least 22.7% lower compared to the mesh and torus. Average latency was also decreased by at least 24.66% as compared to the mesh and torus. Finally, the saturation point for the proposed topology increased by at least 15% as compared to mesh and torus.

ABSTRAK

Didorong oleh peningkatan berterusan dalam Hukum Moore, bilangan teras pemprosesan dalam multiprosesor cip dan sistem dalam satu cip dijangka berkembang dengan pesat dalam masa terdekat. Menyambung komponen yang berlainan dalam multiprosesor cip dengan cara yang cekap dan berskala tinggi telah menjadi semakin mencabar. Topologi Rangkaian-atas-Cip (NoC) semasa adalah cukup untuk rangkaian saiz kecil tetapi bukan teroptimum untuk rangkaian berskala besar. Paket-paket yang dihantar di dalam NoC besar mungkin mempunyai laluan yang panjang untuk sampai ke destinasi. Ini menyebabkan peningkatan dalam parameter tertentu seperti kependaman dan penggunaan kuasa. Oleh itu, adalah perlu untuk menghasilkan topologi baharu sesuai untuk NoC bersaiz besar. Dalam kajian ini, kami mencadangkan satu topologi rangkaian kos-berkesan untuk NoC bersaiz besar yang memperbaiki prestasi dari segi pendaman hujung-ke-hujung. Topologi yang dinamakan RaMesh, terdiri daripada kelompok rangkaian jejaring. Algoritma penghalaan yang sesuai untuk topologi ini juga dicadangkan. Seni bina RaMesh bersama-sama dengan jejaring dan torus disimulasi menggunakan Noxim (NoC Simulator), C untuk model NoC perisian, dan Altera ModelSim untuk model perkakasan Verilog. Simulasi dilakukan di bawah lalu lintas rangkaian yang berbeza dan untuk aneka saiz rangkaian. Hasil uji kaji menunjukkan prestasi RaMesh lebih baik daripada topologi jejaring-2D setara dan torus. Topologi RaMesh juga ditanda aras dengan topologi jejaring berkelompok. Kiraan hop purata dalam topologi yang dicadangkan adalah sekurang-kurangnya 22.7% lebih rendah berbanding dengan jejaring dan torus. Kependaman purata juga diturunkan sekurang-kurangnya 24.66% berbanding dengan jejaring dan torus. Akhirnya, titik tepu bagi topologi yang dicadangkan bertambah sekurang-kurangnya 15% berbanding dengan jejaring dan torus.

TABLE OF CONTENTS

CHAPTER	TITLE	PAGE
	DECLARATION	ii
	DEDICATION	iii
	ACKNOWLEDGEMENT	iv
	ABSTRACT	v
	ABSTRAK	vi
	TABLE OF CONTENTS	vii
	LIST OF TABLES	xi
	LIST OF FIGURES	xiii
	LIST OF ABBREVIATIONS	xvii
	LIST OF APPENDICES	xix
1	INTRODUCTION	1
	1.1 Network-on-Chip	1
	1.2 Problem Statement	2
	1.3 Objective	4
	1.4 Scope	4
	1.5 Contribution of Study	5
	1.6 Thesis Outline	5
2	LITERATURE REVIEW	7
	2.1 Network-on-Chip	7
	2.1.1 Network Topology	8
	2.1.2 Routing Algorithm	9
	2.1.3 Router Design	11
	2.1.4 Flow Control	13
	2.2 Related Work on NoC Topology	13
	2.2.1 1D and 2D Topology	14
	2.2.1.1 Direct Topologies	15
	2.2.1.2 Indirect Topologies	17

	2.2.1.3 Irregular Topologies	19
	2.2.1.4 Hybrid Topologies	25
	2.2.2 3D Topology	30
	2.2.3 Investigating Current Topologies for Large-Scaled NoCs	32
	2.2.4 Routing Algorithm	35
	2.2.4.1 TRANC Routing Algorithm	36
	2.2.5 Switching Techniques	38
	2.2.6 Traffic Models	41
2.3	Simulation Models of NoC Topology	43
	2.3.1 Cycle Accurate Model	43
	2.3.2 FPGA-based NoC Emulators	43
	2.3.3 RTL NoC Modeling	44
2.4	Open Source Router	44
2.5	Router Architecture	45
2.6	Summary	47
3	RESEARCH METHODOLOGY	49
3.1	Topologies Comparison Metrics	49
	3.1.1 Load Handling Performance	49
	3.1.2 Zero-Load Latency	49
	3.1.3 Maximum Saturation Throughput	52
	3.1.4 Maximum Clock Frequency of Router (FMAX)	53
	3.1.5 Area Overhead	54
3.2	Research Approach	55
3.3	Software Tools and Design Environment	56
	3.3.1 Noxim Simulator	56
	3.3.2 Developing Zero-Load Latency Model of New Topology and Routing Algorithm using C	56
	3.3.3 Modeling of the Topologies in C/C++ Using Visual Studio Software	57
	3.3.4 Verilog Modeling of Proposed Large- Scale NoC	57
	3.3.5 Verilog Modeling and Synthesis with Quartus II and Simulation with ModelSim	58
3.4	Experimental Work	58

3.4.1	Experimental Work 1: Simulation in Noxim	59
3.4.2	Experimental Work 2: Simulation of C Software Model	59
3.4.3	Experimental Work 3: Hardware Simulation	61
3.4.4	Experimental Work 4: Hardware Simulation	62
3.5	Summary	64
4	EVALUATION OF MESH TOPOLOGY FOR LARGE NOC	65
4.1	Characteristics of Mesh Topology	65
4.2	Evaluation Setup	66
4.2.1	Test 1 of Experimental work 1: Performance of Mesh Topology under Different Buffer Size and Different Routing Algorithm for Random and Transpose Traffics	68
4.2.2	Test 2 of Experimental work 1: Performance of Mesh Topology under Different Injection Rates and Routing Algorithms for Random and Transpose Traffics	73
4.3	Summary	78
5	PROPOSED TOPOLOGY AND ROUTING ALGORITHM	82
5.1	Introduction	82
5.2	Proposed Topology - RaMesh1	83
5.3	Proposed Topology - RaMesh2	85
5.4	Proposed Topology - RaMesh3	86
5.5	Proposed Topology - RaMesh4	89
5.6	Addressing in RaMesh	93
5.6.1	Equivalent Router Locations Between Different Topologies	96
5.7	RaMesh Routing Algorithm	97
5.8	Modification Setup	107
5.8.1	Modify Reference Router Design	108
5.8.2	Construction of NoC	110

5.9	Summary	111
6	RESULTS AND DISCUSSIONS	112
6.1	Result of Experimental Work 2	112
6.2	Result of Experimental Work 3.1 (with Random Traffic and Zero Load Injection Rate)	115
6.3	Result of Experimental Work 3.2 (with Different Traffic Models and Different Injection Rates)	116
6.3.1	Simulation with Different Injection Rates of Random Traffic	117
6.3.2	Simulation with Different Injection Rates of Transpose Traffic	117
6.3.3	Simulation with Different Injection Rates of Hotspot Traffic	119
6.3.4	Simulation with Different Injection Rates of Uniform Distribution Traffic	119
6.4	Result of Experimental Work 3.3 (Determination of Hardware Cost)	119
6.5	Result of Experiment Work 4 (Evaluation of RaMesh with Different Sizes of the Cluster)	125
6.6	Summary	129
7	CONCLUSION	134
7.1	Conclusions from Results of the Experiments	134
7.2	Contributions	136
7.3	Future Works	137
	REFERENCES	138
	Appendices A – B	150 – 151

LIST OF TABLES

TABLE NO.	TITLE	PAGE
2.1	One-dimensional topology	15
2.2	Two-dimensional direct topology	17
2.3	Two-dimensional indirect topology	19
2.4	Two-dimensional irregular topology	23
2.5	Hybrid and cluster based topology	29
2.6	Maximum number of hops between source and destination. Some entries are blank because the architecture does not support the corresponding network size.	30
2.7	Three-dimensional topology	32
3.1	Summary of experiments	60
4.1	Critical point for different sizes of mesh topology under uniform random and transpose traffics	67
4.2	Evaluation result for mesh topology around critical point under random traffic, different buffer sizes and different routing algorithms	69
4.3	Evaluation result for mesh topology around critical point under transpose traffic, different buffer sizes and different routing algorithms	70
4.4	Global average delay for mesh topology under random traffic	77
4.5	Global average delay for mesh topology under transpose traffic	80
4.6	Injection rate saturation point for each routing algorithm	80
5.1	Number of switches (N) and number of links (Ch) for RaMesh topologies	92
5.2	Address for RaMesh	93
5.3	Conversion of RaMesh3 and RaMesh4 addresses to mesh (and torus) addressess	97
6.1	Average hop count comparison for clustered 2D-mesh, mesh, torus, and RaMesh architectures for different size of NoC	113

6.2	RaMesh4 advantage compared to other topologies (in percent) in terms of average hop count	113
6.3	Maximum number of hops between source and destination for mesh, torus, norma, corona, hybrid ring/mesh, and RaMesh4 topologies	114
6.4	Simulation result to compare average latency between RaMesh, mesh, torus, and clustered 2D-mesh topologies under random traffic with constant injection rate	116
6.5	Hardware utilization summary for NoC implementation with 144 IP cores for Stratix V Altera FPGA	123
6.6	Summary of performance comparison for <i>RaMesh</i> _{4×4} over <i>RaMesh</i> _{6×6} and mesh	131
6.7	Critical injection rate and the average latency at the critical injection rate for mesh, torus, clustered 2D-mesh, <i>RaMesh</i> _{6×6} , and <i>RaMesh</i> _{4×4}	132
6.8	Injection rates (packets/cycle/node) at saturation point under different traffic models for different size of topologies	133

LIST OF FIGURES

FIGURE NO.	TITLE	PAGE
1.1	Examples of multi-core chips with on-chip networks [1, 2]	2
2.1	Network-on-Chip	8
2.2	NoC topologies	10
2.3	Summarizes various NoC topologies	14
2.4	A 4×4 DMesh network	17
2.5	Indirect topologies	18
2.6	Flattened butterfly topology	18
2.7	A regular (mesh) topology and a custom topology for a video object plane decoder (VOPD)	21
2.8	Adding long-range links to a 4×4 standard mesh network [3]	21
2.9	Norma-I topology with 16 and 32 IP cores [4]	22
2.10	Norma-II topology with 16 and 32 IP cores [4]	23
2.11	Corona topology (Number of IP core =24) [5]	24
2.12	Ring Road NoC Architecture [6]	24
2.13	Hybrid mesh architecture using hierarchical rings for global interconnect [7]	26
2.14	Hierarchical routing architectures in clustered 2D-mesh NoC[8]	26
2.15	Hybrid connection-based mesh topology for NoC	27
2.16	Low-latency cluster topology for local traffic NoCs	28
2.17	Heterogeneous and hybrid clustered topology	28
2.18	Proposed topology and routing algorithm	34
2.19	IRN map and graph for routing in a 4×4 torus NoC [9]	37
2.20	The proposed IRN Map representing the TRANC routing algorithm in an $n \times n$ torus [9]	38
2.21	Packet, or worm, format for a wormhole routed network	40
2.22	Routing two packets from $P \rightarrow Q$ over a wormhole routed mesh. A worm can span several switches	40
2.23	Router architecture [10]	47
3.1	Latency versus throughput for an on-chip network [11]	50

3.2	Research approach	55
3.3	Snippets of routing information and communication for each node by using C	61
3.4	Snippets of testbench	63
4.1	NoC interconnection using mesh topology	66
4.2	Latency versus throughput for an on-chip network [11]	67
4.3	Global average delay (cycles) around critical point for mesh topology under random traffic, different buffer size and different routing algorithm. The pir means packet injection rate	71
4.4	Global average throughput (flits/cycle) around critical point for mesh topology under random traffic, different buffer size and different routing algorithm	72
4.5	Global average delay (cycles) around critical point for mesh topology under transpose traffic, different buffer size and different routing algorithm	73
4.6	Global average throughput (flits/cycles) around critical point for mesh topology under transpose traffic, different buffer size and different routing algorithm	74
4.7	Global average delay (cycles) for different size of mesh topology, routing algorithm and injection rate for random traffic	75
4.8	Global average throughput (flits/cycle) for different size of mesh topology, routing algorithm and injection rate for random traffic	76
4.9	Global average delay (cycles) for different size of mesh topology, routing algorithm and injection rate for transpose traffic	78
4.10	Global average throughput (flits/cycles) for different size of mesh topology, routing algorithm and injection rate for transpose traffic	79
5.1	A mesh cluster in RaMesh topology	83
5.2	RaMesh1 with 144 IP cores (2×2 cluster of 6×6 mesh)	85
5.3	Switches in RaMesh1 and RaMesh2, (a) local switch (LS), (b) interface switch slave (ISS), (c) interface switch master (ISM)	86
5.4	RaMesh2 with 144 IP cores (2×2 cluster of 6×6 mesh)	87
5.5	RaMesh3 with 144 IP cores (2×2 cluster of 6×6 mesh)	88
5.6	RaMesh4 with 144 IP cores (2×2 cluster of 6×6 mesh)	90

5.7	(a) ES switch for external layer in RaMesh3, (b) ES switch for external layer in RaMesh4	91
5.8	Switch positions with their port names in RaMesh4 topology	91
5.9	Address for RaMesh1 and RaMesh2	94
5.10	Address for RaMesh3 and RaMesh4	95
5.11	The specifications of sides and edges for each layer	100
5.12	The lines a and b are as a divider for each cluster	101
5.13	Example 1: source and destination address are 0.0.0.0 and 2.2.1.0 respectively	105
5.14	Example 2: source and destination address are 2.0.1.1 and 0.1.1.7 respectively	105
5.15	Path of example1 (red path) and example2 (violet path)	106
5.16	Router architecture [10]	108
5.17	Modification of input port module for reference router	109
5.18	Process to modify routing algorithm	109
5.19	Snippets of the routing algorithm in Verilog	110
5.20	NoC connection in Verilog	111
6.1	Average hop count comparison between mesh, torus, clustered 2D-mesh, and RaMesh topologies for different size of NoC	114
6.2	Average latency for RaMesh, clustered 2D-mesh, mesh, and torus for different size of NoC for random traffic under constant injection rate	115
6.3	Average latency (cycles) of RaMesh, mesh, torus and clustered 2D-mesh under different injection rates of random traffic for different size of topologies	117
6.4	Average latency (cycles) of RaMesh, mesh, torus, and clustered 2D-mesh under different injection rates of transpose traffic for different size of topologies	118
6.5	Average latency (cycles) of RaMesh, mesh, torus, clustered 2D-mesh under different injection rates of hotspot traffic for different size of topologies	120
6.6	Average latency (cycles) of RaMesh, mesh, torus, and clustered 2D-mesh under different injection rates of uniform distribution traffic for different size of topologies	121
6.7	clustered 2D-mesh topology with 144 IP cores	123

6.8	Timing analysis result showing: average latency in ns for <i>RaMesh</i> _{6×6} , <i>RaMesh</i> _{4×4} , clustered 2D-mesh, mesh, and torus under different injection rates for various traffic models for 144 IP cores	125
6.9	RaMesh topology for 144 cores with 2 × 2 cluster of 6 × 6 mesh	126
6.10	RaMesh topology for 144 cores with 3 × 3 cluster of 4 × 4 mesh	127
6.11	Average latency (cycles) of <i>RaMesh</i> _{4×4} and <i>RaMesh</i> _{6×6} under different injection rates of random traffic for two sizes of network	127
6.12	Average latency (cycles) of <i>RaMesh</i> _{4×4} and <i>RaMesh</i> _{6×6} under different injection rates of transpose traffic for two sizes of network	128
6.13	Average latency (cycles) of <i>RaMesh</i> _{4×4} and <i>RaMesh</i> _{6×6} under different injection rates of hotspot traffic for two sizes of network	128
6.14	Average latency (cycles) of <i>RaMesh</i> _{4×4} and <i>RaMesh</i> _{6×6} under different injection rates of uniform distribution traffic for two sizes of network	129
6.15	Average latency (cycles) of <i>RaMesh</i> _{6×6} , <i>RaMesh</i> _{4×4} , and mesh under different injection rates of hotspot traffic for different percentage of traffic at hotspot nodes for 144 IP cores	130
B.1	Conventional VC router Architecture	153
B.2	Router or switch architecture	155
B.3	The functional block diagram look-ahead routing module in reference design	156

LIST OF ABBREVIATIONS

bps	-	Bit per second
BPSF	-	Bypass Forward
BPSR	-	Bypass Reverse
CMP	-	Chip multiprocessors
CPU	-	Central Processing Unit
DNLY	-	Down Layer
DOR	-	Dimension Ordered Routing
DyAD	-	Dynamical Adaptive and Deterministic routing
FPGA	-	Field Programmable Gate Array
FRWD	-	Forward
GAD	-	Global Average Delay
GAT	-	Global Average Throughput
GS	-	Global Switch
HDL	-	Hardware Description Languages
IC	-	Integrated Circuit
IDE	-	integrated development environment
IP	-	Intellectual Property
ISM	-	Interface Switch Master
ISO	-	International Organization for Standardization
ISS	-	Interface Switch Slave
IVC	-	Input Virtual Channel
LS	-	Local Switch
MPSoC	-	Multiprocessor System-on-Chip
NoC	-	Network on Chip
OVC	-	Output Virtual Channel
PE	-	Processor Element
QoS	-	Quality-of-service
RaMesh	-	Ring-based Mesh
ROMM	-	Randomized Oblivious Multi-phase Minimal routing
RTL	-	Register transfer level

RVRS	-	Reverse
SoC	-	System on Chip
UCDB	-	Unified Coverage Database
UPLY	-	Up Layer
VC	-	virtual channel
VHDL	-	VHSIC Hardware Description Language
XML	-	Extensible Markup Language

LIST OF APPENDICES

APPENDIX	TITLE	PAGE
A	Publications	150
B	Low Latency Router	151

CHAPTER 1

INTRODUCTION

1.1 Network-on-Chip

Multi-processor system-on-chip (MPSoC) is capable of accommodating many processing resources for high-performance computation [12, 13]. On-chip communication is the main bottleneck of MPSoC. Conventional bus-based on-chip interconnect cannot provide efficiency and scalability to connect many cores on one chip. Network-on-chip (NoC) has been proposed to meet on-chip interconnect challenges. NoC consists of interconnected routers based on certain topology (e.g., a mesh), that integrates memories, computational processors or the Intellectual Property (IP) components. The method of communication among IPs within an NoC-based system is through packet transmission via routers instead of circuit switching in bus-based interconnect.

Designing an efficient high performance and low latency NoC is still an open area of research. According to [14, 15], MPSoC size with hundreds or thousands of cores are likely to be common-place today. The increase of on-chip cores requires a high-bandwidth and scalable communication fabric [16, 17]. To satisfy these requirements, NoCs have been presented and has very quickly emerged as the preferred interconnection fabric.

As example, there exists real chips with 80 cores by Intel [1, 18], 100 cores by Tileria [19], and even a research prototype with 1000 cores by University of Glasgow [20]. While increased core count has allowed processor chips to scale without experiencing complexity and power dissipation problems inherent in larger individual cores, challenges still exist. NoC has been utilized to solve this problem. Figure 1.1 shows an example of a 80-core research prototype from Intel [1] (Figure 1.1a) and a commercial 64-core chip for embedded applications from Tileria (Figure 1.1b) that

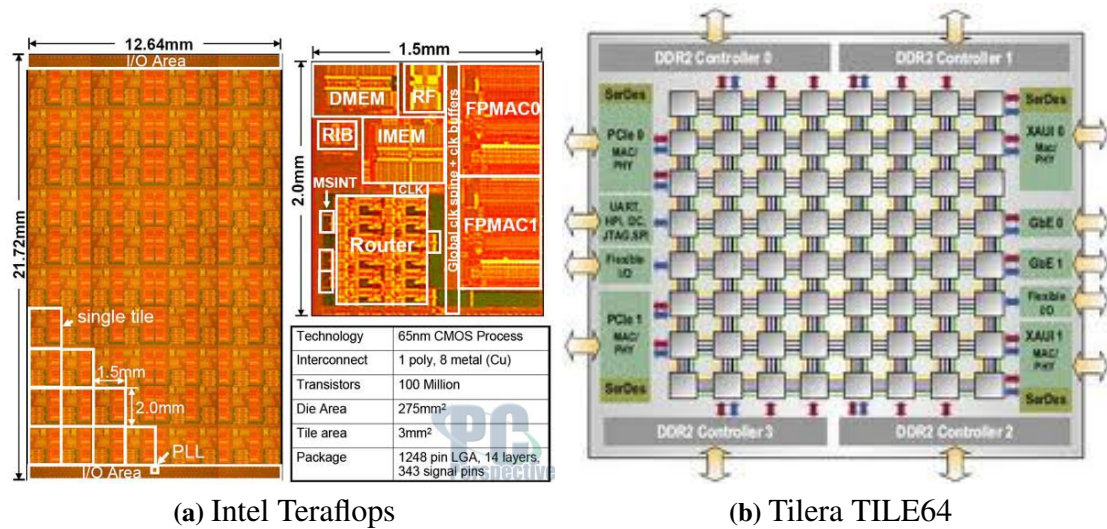


Figure 1.1: Examples of multi-core chips with on-chip networks [1, 2]

employs an on chip network for inter-tile communication [2].

1.2 Problem Statement

NoC topology defines how routers are connected together with network endpoints (i.e. IP cores). The performance and cost of NoC are greatly affected by the topology in large-scale MPSoC. Large-scale NoC topology is referred to as the one that has more than 100 IP cores [21]. An NoC topology is characterized by number of hop and network latency [22, 23]. The main issue with a large-scale NoC is the large number of hops that packets have to pass through to reach their final destination, hence creating significant network latency. A large number of hops also has a direct impact on the energy consumed in the interconnect for buffering, transmission, and control.

There are several critical outstanding problems of large-scale NoCs. Due to increasing number of the nodes inside the NoC and also the increase in the transaction between nodes, the rate of data transmission in the links rises. Thus, some links are used more excessively than other links which can lead to difficulty in load balancing inside the NoC. This imbalance makes some packets to take longer paths to reach the destination [24]. The long route results in increase latency, hop count, packet loss and power consumption, and decrease in throughput.

One of the ways to remove the aforementioned problems is to use routing

algorithm. Many routing algorithms were created to solve these problems, but perfect solution is still elusive. The topologies currently used are good for small size networks only. Thus it is necessary to design and develop a new topology which is appropriate for large size NoCs. Besides, an optimized routing algorithm suitable for the suggested topology must be developed. Nychis et al. in [25] have evaluated large NoCs of up to 4,096 cores, and they have shown two important issues with existing topologies in a large-scale NoC, which are high latency and low throughput.

Topologies are increasingly becoming the bottleneck that is limiting the performance of NoC [26, 27]. Indeed, for a large-scale NoC, the topology has a key impact on the performance and cost of the network [5, 7]. It is responsible for 60% to 75% of the miss latency [28].

The classical NoC topology is the two-dimensional mesh [17, 29]. It is preferred over other topologies. Since its simple implementation and the overall layout is very regular [22]. However, in spite of its advantage, the two-dimensional mesh topology is disadvantaged with congestion, high hop count, and high communication latency for large-scale NoC. Indeed, a significant disadvantage of the mesh topology is in its large communication radius which induces long path for packet delivery [7, 30, 24]. For small-scale network (up to 64 nodes [25]), mesh topology is proven to be efficient [23, 7, 25]. However, for large-scale NoC network, the performance of mesh topology degrades significantly [7, 31]. The performance of mesh topology does not scale well with network size.

The torus is also a favored topology for NoCs [32]. There are many long-range links in torus topology that may create problems in terms of performance and cost. A packet that uses a long-range link takes longer time to reach the next hop than when a packet uses a normal link [33]. In addition, each long link imposes a minimum latency and is a potential point of contention [3]. However, long-range links may improve performance by reducing number of hops [3].

Based on aforementioned disadvantages, there is a need to develop a topology with low network latency and hop count [3, 30]. The combination of mesh and ring topology have a potential to address latency and hop count and avoidance of congestion for large-scale networks [7, 8, 34].

1.3 Objective

The main goal of our research is to develop a topology with a suitable routing algorithm for large-scale NoC. The objectives in this thesis are:

- To propose a topology based on mesh clusters that reduces the number of switches, the number of hops, and latency in large-scale NoC. This thesis proposes a new NoC topology called RaMesh. RaMesh is designed based on clusters and it is suitable for large-scale NoCs that have more than 100 IP cores. Each cluster is a mesh topology. However, internal communication between IP cores inside the cluster uses the rule of ring topology. The target performance metrics include a low hop count and low average network latency, and congestion avoidance.
- To propose a routing algorithm to cater for the proposed topology. The proposed routing algorithm is a combination of three existing routing algorithms, which are ring, XY, and TRANC [13] to avoid congestion and deadlock problems.

1.4 Scope

The proposed topology is a hierarchical network topology based on mesh clusters suitable for large scale NoCs with more than 100 IP cores. The structure of each cluster is the mesh topology, but the rule of the ring topology is used for internal communication among IP cores.

In this thesis, the proposed topology was evaluated for different NoC sizes, different traffic models, and different traffic ratios. The proposed topology is benchmarked in terms of average hop count and latency with clustered 2D-mesh [8], mesh, and torus under the same experimental conditions.

The proposed topology was implemented using Verilog and simulated using ModelSim. To characterize the proposed topology, we have used random, transpose, hotspot, and uniform distribution traffic models to obtain average hop count and average latency for four sizes of network with 144, 324, 576, and 900 IP cores.

The proposed routing algorithm is based on deterministic routing. We used XY

and TRANC [9] routing algorithms for mesh and torus topology respectively as they are deadlock free. The switching technique for these routing algorithms is wormhole switching.

The hardware evaluation to compare hardware cost (in terms of number of adaptive logic modules (ALM)) and estimate maximum hardware operating frequency was done based on Stratix V 5SEEBF45I4 FPGA using Quartus II software for 144 IP cores. The NoC code was written in C and translated to Verilog HDL and compiled using Quartus II version 13 software. The code was verified using Altera Modelsim. This process is explained in more detail in section 3.4.3.

1.5 Contribution of Study

This thesis proposed a topology called RaMesh, which is suitable for a large-scale NoC. A routing algorithm for RaMesh that minimizes congestion and deadlock is also proposed. The proposed topology is based on mesh clusters, is hierarchical, and has long-range links to help reduce the hop count. The performance of RaMesh is superior in terms of network latency compared to existing topologies such as clustered 2D-mesh, mesh and torus. In summary, the main contributions of this thesis are:

- The proposed NoC topology improves significantly the average hop count compared to clustered 2D-mesh, mesh and torus topologies. For example, RaMesh on average has 42.1% lower hop count compared to clustered 2D-mesh topology in tests done for various network sizes.
- In tests using RTL model for each topology, RaMesh also has superior end-to-end average latency compared to other topologies. Compared to clustered 2D-mesh, mesh, and torus topologies, Ramesh has 31.2%, 49.5%, and 41.5% lower average latency respectively.

1.6 Thesis Outline

The rest of the thesis is organized as follows.

- Chapter 2 contains literature survey on the studies of NoC, which includes topology and routing algorithm.
- Chapter 3 covers the methodology for the work done in this thesis. This also includes the general approach taken for the research done in this work, as well as tools and platform used.
- Chapter 4 presents the evaluation results of mesh topology. We also have simulated the topologies with appropriate routing algorithms under different ratios of traffic pattern.
- Chapter 5 describes the proposed topology that was designed based on hierarchical mesh topology for large-scale NoC called RaMesh. In addition, this chapter also presents a proposed routing algorithm for the proposed topology.
- Chapter 6 presents the results and analysis of the experimentations to compare average latency under different ratios of traffic and different traffic models, and hardware cost.
- Chapter 7 summarizes the thesis, re-stating contributions, and suggest directions for future research.

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