MODELING AND ANALYSIS OF CYLINDRICAL GATE-ALL AROUND SILICON NANOWIRE FET INCLUDING BOHM QUANTUM POTENTIAL MODEL

MUHAMMAD A'TIF BIN ABD RAZAK

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Specially dedicated to *Mak* and *Abah*

I really miss both of you.

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ABSTRACT

According to Moores's Law, the number of transistors per square inch on integrated circuits are doubled every year. Now, the transistors size has been scaled down to 15nm. The smaller the transistors size gives more space for transistors to be added in system on chip (SoC) thus will provide a lot of functionality. This can be fundamentally viewed as mechanism leads to deviation of the functional behavior from its ideal case. However, the reduction of channel length into nanometer regime would cause short channel effects (SCEs). New transistor device architecture such as gate-all-around silicon nanowire (GAASiNW) field-effect-transistor (FET) is believed to be a promising future device to solve the scaling problem especially SCEs. GAASiNW is proved to be more immune to SCEs compared to conventional FET. Due to continuous device scaling, quantum effects cannot be neglected especially with today's technology has reaching 10nm technology node. It has been pointed out by previous researchers that quantum effect such as tunneling effect has become one of the fundamental limitation to accurately describe the charge distribution in GAA SiNW. In this research project, an analytic carrier models in conducting channel for improving electrical characteristic of GAASiNW is investigated. One major focus of this study is to enhance fundamental understanding of quantum effect in an optimized GAASiNW FET device by investigating in details how these quantum effects influence device's electrical characteristics. The study of quantum effect and comparison between quantum models on GAASiNW FET are compared. The study are conducted by using 3-D TCAD tools. The analytic drift-diffusion including Bohm quantum potential (BQP) model are carried out as its device carrier transport. It is proved that the proposed GAASiNW device with BQP model as the carrier transport able to reduce the DIBL by 83% when applying a low doped at S/D region. In fact, the proposed GAASiNW FET model with BQP model shows a good electrical characteristic when the channel length is scaled to 20 and 16nm.

ABSTRAK

Menurut Undang-undang Moores, bilangan transistor per inci persegi pada litar bersepadu meningkat dua kali ganda setiap tahun. Sekarang, saiz transistor telah dikurangkan kepada 15nm. Lebih kecil saiz transistor memberikan lebih banyak ruang bagi transistor untuk ditambah dalam sistem cip (SoC) dengan itu akan menyediakan banyak fungsinya. Ini secara asasnya dilihat sebagai mekanisma yang membawa kepada salah tingkah laku fungsi transistor dari kes idealnya. Walau bagaimanapun, pengurangan panjang saluran ke rejim nanometer akan menyebabkan kesan saluran pendek (SCEs). Senibina peranti transistor baru seperti gate di sekeliling wayar nano silikon (GAASiNW) transistor kesan medan (FET) dipercayai menjadi peranti masa depan yang mampu untuk menyelesaikan masalah skala besar terutama SCEs. GAASiNW terbukti lebih kebal terhadap SCE berbanding dengan FET konvensional. Oleh kerana skala peranti berterusan, kesan kuantum tidak boleh diabaikan terutamanya dengan teknologi hari ini mencapai teknologi 10nm. Para penyelidik terdahulu telah menunjukkan bahawa kesan kuantum seperti kesan terowong telah menjadi salah satu batasan asas untuk menerangkan dengan tepat penggantian caj di GAA SiNW. Dalam projek penyelidikan ini, model pembawa analitik akan diselidiki dalam menjalankan saluran untuk meningkatkan ciri-ciri elektrik GAASiNW. Satu tumpuan utama kajian ini adalah untuk meningkatkan pemahaman asas mengenai kesan kuantum dalam peranti GAASiNW FET yang dioptimumkan dengan menyiasat secara terperinci bagaimana kesan kuantum ini mempengaruhi ciri-ciri elektrik peranti. Kajian mengenai kesan kuantum dan perbandingan antara model kuantum pada FAS GAASiNW telah dilakukan. Kajian ini dilakukan menggunakan alat TCAD 3-D. Penyebaran aliran analitik termasuk potensi kuantum Bohm (BQP) dilakukan sebagai pengangkutan pembawa peranti. Adalah terbukti bahawa peranti GAASiNW yang dicadangkan dengan model BQP sebagai pengangkutan pembawa mampu mengurangkan DIBL sebanyak 83% apabila menggunakan doping rendah di bahagian

S / D. Malah, model GAASiNW FET yang dicadangkan dengan model BQP menunjukkan ciri-ciri elektrik yang baik walaupun panjang saluran dikecilkan menjadi 20 dan 16nm.

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LIST OF ABBREVIATION

BQP	-	Bohm Quantum Model
DIBL	-	Drain Induced Barrier Lowering
FET	-	Field-Effect Transistor
SCE	-	Short Channel Effect
GAASiNW	-	Gate-All Around Silicon nanowire
SoC	-	System on Chip
SS	-	Subthreshold Swing

LIST OF SYMBOLS

V_{th}	-	Threshold Voltage
V_g	-	Voltage Gate
V_d	-	Voltage Drain
I_D	-	Drain Current
I_{on}	-	On-Current
I_{off}	-	Off-Current
L_{eff}	-	Channel Length
t_{ox}	-	Oxide Thickness
$\mathcal{E}_y$	-	Electric Field Drain

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CHAPTER 1

INTRODUCTION

1.1 Project Background

Previously conventional MOSFET was used in nonelectrical technologies. The conventional MOSFET structure is called planar structure. The planar structure of conventional MOSFET has been successfully implemented using single gate where the structure are having source, drain, and bulk device. The single gate structure was successfully control the on and off of the MOSFET current and being widely used in all silicon companies. However, due to scaling down the channel length of MOSFET into nanowire regime, the SCEs becomes a big challenges to conventional MOSFET.

The researches come out with an idea of moving the planar structure to a novel structure to overcome short channel effect. The novel structure will be having multiple gates used in MOSFET structure. One of the novel structure of MOSFET which successfully implemented in silicon companies is Fin-Field Effect Transistor (FinFET) transistor [1]. Intel also already implemented this kind of technology however it is being called CMOS tri-gate transistor [2]. Another novel structure transistor which shows promising capabilities in term of transistor performance is Gate-all around Silicon Nanowire FET GAASiNW.

The GAASiNW is actually silicon on insulator (SOI) devices which having gate all around the silicon and connected to source and drain [3]. The GAA SiNW FET is the latest nanowire technology which not implement yet in any silicon companies and still in the research based. From previous researches, the GAASiNW outperform FinFET performance and more immune to SCEs [4].

1.2 Problem Statement

Due to continuous scaling down channel length of the transistor, short channel effects will become a major thread to the transistor. As for GAASiNW device structure, due to scaling down the structure into nanowire, the quantum effects cannot be neglected especially with today's technology has reaching 10nm technology node. It has been pointed out by previous researchers that quantum effect such as tunnelling has become one of the fundamental limitation to accurately describe the charge distribution in GAASiNW [5]. This can be fundamentally viewed as mechanism leads to deviation of the functional behaviour from its ideal case.

1.3 Research Objectives

The objectives of this project:

1. To design GAASiNW device structure and analyze its electrical characteristics by using 3D TCAD Tools.
2. To define the best quantum analytical model to be included in the GAASiNW device structure.
3. To analyze the performance improvement of GAASiNW including quantum effect model which is BQP model and validate with others work

1.4 Scope of Project

In this project, a model of GAASiNW will be designed by using 3D TCAD Tools. The analytic model of device structure including the carrier mobility will be incorporated as a tunnelling model in the device design. The model then will be simulated by using the TCAD tools to generate the I-V curves of GAASiNW and its electrical characteristics will be extracted such as threshold voltage (Vth), on-current (I_{on}), off-current (I_{off}), Drain Induced Barrier Lowering (DIBL) and Subthreshold Swing (SS). The device performance will be optimized by including the quantum

analytic model, to be specific, in this device structure, BQP model as the tunnelling model. Then, the electrical characteristics will be compared and validated precisely with others' work.

1.5 Report Organization

The scope of the project includes the analytic models literature reviews and simulation process of GAA SiNW FET. The thesis which represent the full report of the project which will explain in detail all of the work conducted. The thesis is divided into five chapters.

Chapter 1 provides the general overview and project background, the project objectives, the scope of work, problem statement, expected results and methodology flow.

Chapter 2 explains the literature review of the project and its comparison from other researches project. The several types of GAA SiNW FET structure will be introduced. The chapter also provides reason for the carrier mobility analytic model selections to be implemented in this project.

Chapter 3 presents the methodology related to the project. It includes quantum analytic models to be used in simulating the GAA SiNW FET, steps to implement the analytic models in the design using TCAD tools. The 3D designed of GAA SiNW FET and its explanation are also provided in this chapter.

All the simulation results obtained from developed model will be further discussed in Chapter 4 of the thesis. The analysis and discussion of the obtained results are also presented in this chapter.

Chapter 5, the last chapter of the thesis, presents the conclusions of the project and the recommendations for future work.

1.6 Research Methodology

In order to realize this project, it is important to organize the methodology parts. These are the general methodology to ensure the proper flow of this project:

I. Literature review on structure, quantum effect and carrier mobility analytic model of GAA SiNW FET
II. Develop GAA SiNW FET structure using TCAD Tools
III. 3D Device Simulation using TCAD Tools
IV. Record the electrical characteristic of GAA SiNW FET model designed
V. Optimize the result by including quantum analytic model in the design
VI. Validate the result by comparing what have been done in literature review paper
VII. Thesis write up

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