ELECTROCHEMICALLY DEPOSITED GERMANIUM ON SILICON AND ITS CRYSTALLIZATION BY RAPID MELTING GROWTH

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ABSTRACT

It is well known that continuous miniaturization of transistors tends to create several problems such as current leakage, short channel effect, etc. Therefore, introduction of new channel material with higher carrier mobilities such as Germanium (Ge) is suggested to overcome this physical limitation and also to improve the performance of conventional transistors in chips. Basically, there are several techniques to grow Ge such as Chemical Vapour Deposition (CVD) and Molecular Beam Epitaxy (MBE) system. However, these processes require high vacuum environment, highly depend on such hard-to-control variables as well as costly. Therefore, an alternative method that practically cheaper to grow Ge utilizing electrochemical and rapid melting technique is investigated here. In this thesis, a systematic study of electrochemical deposition of Ge on Silicon (Si) substrate is outlined. Results show the unwanted Germanium Dioxide (GeO_2) tends to form in the air-exposed process and germanium tetrachloride:dipropylene glycol ($GeCl_4$:$C_6H_{14}O_3$) electrolyte. Therefore, a Nitrogen (N_2) controlled ambient is preferable. The uniform amorphous Ge film on Si (100) substrate was successfully obtained at the optimum current density of 20 $mAcm^{-2}$ in germanium tetrachloride:propylene glycol ($GeCl_4$:$C_3H_8O_2$) electrolyte. Crystallization of electrodeposited Ge on Si (100) was demonstrated by rapid melting process. Effect of different annealing temperatures from 1000 to 1100 ^oC has also been studied. Raman spectra and Electron Backscattering Diffraction (EBSD) result confirmed that the grown Ge was highly oriented with the crystal orientation identical to that of Si (100) substrate at all annealing temperature tested. Based on depth profile from Auger Electron Spectroscopy (AES) measurement and Raman spectra, it was found that Si-Ge mixing occurred upon rapid melting process, particularly at near the Si-Ge interface caused by atoms diffusion. Calculated Si fraction diffused into Ge region in the Si-Ge mixing was high at higher annealing temperature that shows good agreement with solidus curve of Ge-Si equilibrium phase diagram. Correspondingly, the amount of Ge diffused into Si region also increased as annealing temperature increased. The result also shows that the tensile strain turns from high to low with the increase of annealing temperature. In addition, it drastically becomes more compressive as the depth is approaching the interface of Ge and Si. The difference in thermal expansion coefficient is a possible cause to generate such strain behaviour. For applications, the presence of strain in channel will improve the transistor performance by enhancing the carrier mobility. In conclusion, this study proves that electrochemical deposition and rapid melting growth technique are promising methods for synthesizing crystalline Ge and significantly contribute to the improvement of carrier mobility. It is expected that high performance Complementary Metal Oxide Semiconductor (CMOS) transistor scaling and Moore's Law will continue in the future through new materials introduction in the transistor structure and by incorporating significantly appropriate levels of strain and composition of Ge/Si in the channel.

ABSTRAK

Adalah diketahui umum bahawa pengecilan berterusan transistor cenderung untuk mewujudkan beberapa masalah seperti arus bocor, kesan saluran pendek dan lain-lain. Maka, pengenalan bahan saluran baru dengan mobiliti pembawa yang lebih tinggi seperti Germanium (Ge) dicadangkan untuk mengatasi had fizikal ini dan juga untuk meningkatkan prestasi transistor konvensional dalam cip. Pada asasnya, terdapat beberapa teknik untuk pertumbuhan Ge seperti sistem Pemendapan Wap Kimia (CVD) dan Pancaran Molekul Epitaksi (MBE). Tetapi, proses ini memerlukan persekitaran vakum yang tinggi, sangat bergantung kepada pembolehubah sukar dikawal serta kos yang tinggi. Oleh itu, satu kaedah alternatif praktikal berkos rendah untuk pertumbuhan Ge menggunakan teknik elektrokimia dan lebur pesat dikaji disini. Dalam tesis ini, kajian sistematik berkaitan pemendapan elektrokimia Ge pada Silikon (Si) substrat dilaporkan. Keputusan menunjukkan Germanium Dioksida (GeO_2) yang tidak diingini cenderung untuk terbentuk dalam proses terdedah kepada udara dan penggunaan elektrolit germanium tetraklorida:dipropylene glikol ($GeCl_4$:$C_6H_{14}O_3$). Oleh itu, ambien terkawal Nitrogen (N_2) adalah lebih baik. Filem Ge amorfus yang seragam pada substrat Si (100) telah berjaya diperolehi pada ketumpatan arus optimum 20 $mAcm^{-2}$ di dalam elektrolit germanium tetraklorida:propylene glycol ($GeCl_4$:$C_3H_8O_2$). Penghabluran Ge yang dielektropendap pada Si (100) telah ditunjukkan oleh proses lebur pesat. Kesan suhu pemanasan yang berbeza dari 1000 ke 1100 ^oC juga telah dikaji. Raman spektra dan Pembelauan Balik Serakan Elektron (EBSD) mengesahkan bahawa Ge yang ditumbuhkan adalah berorientasi tinggi dengan orientasi kristal sama dengan Si (100) substrat. Berdasarkan profil kedalaman daripada pengukuran Auger Elektron Spektroskopi (AES) dan Raman spektra, didapati bahawa percampuran Si-Ge berlaku apabila pertumbuhan lebur pesat, terutamanya berhampiran antara muka lapisan Si-Ge yang disebabkan oleh resapan atom-atom. Kiraan pecahan Si yang disebarkan ke rantau Ge dalam pencampuran Si-Ge didapati tinggi pada suhu pemanasan yang lebih tinggi, menepati dengan gambarajah fasa keseimbangan lengkung pepejalan Ge-Si. Sejajar dengan itu, jumlah Ge diresapkan ke rantau Si juga meningkat dengan peningkatan suhu lebur. Hasil kajian juga menunjukkan terikan tegangan bertukar dari tinggi ke rendah dengan peningkatan suhu peleburan. Di samping itu, ia secara drastik menjadi lebih mampat apabila kedalaman menghampiri rantau antara muka Ge dan Si. Perbezaan pekali pengembangan terma antara kedua-dua bahan adalah mungkin penyebab berlakunya ketegangan tersebut. Bagi aplikasi, kewujudan ketegangan dalam saluran akan meningkatkan prestasi transistor dengan meningkatkan mobiliti pembawa. Kesimpulannya, kajian ini membuktikan bahawa pemendapan elektrokimia dan teknik pertumbuhan lebur pesat merupakan kaedah yang baik untuk mensintesis kristal Ge dan memberi sumbangan dalam peningkatan mobiliti pembawa. Dijangka bahawa pengecilan Pelengkap Oksida Logam Semikonduktor (CMOS) transistor prestasi tinggi dan Undang-undang Moore akan berterusan melalui pengenalan bahan-bahan baru dalam struktur transistor dan dengan menggabungkan Ge/Si ke dalam saluran dengan ketegangan dan komposisi yang sesuai.

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LIST OF ABBREVIATIONS

2D	-	two-dimensional
3D	-	three-dimensional
AES	-	Auger electron spectroscopy
AFM	-	atomic force microscopy
a-Ge	-	amorphous germanium
Ar	-	argon
C	-	carbon
CCD	-	charge coupled device
$C_3H_8O_2$	-	propylene glycol
$C_6H_{14}O_3$	-	dipropylene glycol
CH_3COOH	-	acetic acid
CMOS	-	complementary metal oxide semiconductor
Cu	-	copper
CVD	-	chemical vapor deposition
DC	-	direct current
DI	-	deionized
EBSD	-	electron backscattering diffraction
EDS	-	energy dispersive x-ray spectroscopy
FESEM	-	field emission scanning electron microscopy
FET	-	field effect transistor
FWHM	-	full width at half maximum
Ge	-	germanium
$GeBr_4$	-	germanium bromide
$GeCl_4$	-	germanium tetrachloride
GeH_4	-	germane
GeI_4	-	germanium (IV) iodide

GeO_2	-	germanium dioxide
GOI	-	germanium-on-insulator
H_2O	-	water
H_2O_2	-	hydrogen peroxide
H_2SO_4	-	sulphuric acid
HeCd	-	helium cadmium
HF	-	hydrofluoric acid
HNO_3	-	nitric acid
IR	-	infra red
ITRS	-	International Technology Roadmap for Semiconductors
LCD	-	liquid crystal display
LED	-	light-emitting diode
MBE	-	molecular beam epitaxy
MOSFET	-	metal oxide semiconductor field effect transistor
N_2	-	nitrogen
NH_3	-	ammonia
Ni	-	nickel
NMOS	-	n-channel MOSFET
O	-	oxygen
PET	-	polyethylene terephthalate
PMOS	-	p-channel MOSFET
Pt	-	platinum
RCA	-	Radio Corporation of America
RF	-	radio frequency
RHEED	-	reflection high-energy electron diffraction
RMG	-	rapid melting growth
RMS	-	root-mean-square
rpm	-	rotation per minute
RTA	-	rapid thermal annealing
SC	-	standard cleaning
sccm	-	standard cubic centimeters per minute
Si	-	silicon
Si_xGe_{1-x}	-	silicon germanium
SiN_x	-	silicon nitride

SiO_2	-	silicon dioxide
SEM	-	scanning electron microscopy
SPM	-	sulphuric peroxide mixtures
TEM	-	transmission electron microscopy
ULSI	-	ultra-large-scale-integrated circuits
UV	-	ultra violet
XRD	-	x-ray diffraction

LIST OF SYMBOLS

Å	-	angstrom (1 Å = 1.0 x 10^{-10} meters)
$n(\omega)$	-	Bose-Einstein occupation number
cm	-	centimeter
J	-	current density
^oC	-	degree Celcius
ϕ	-	diameter
$\omega_i(q)I$	-	dispersion of ith phonon branch
v_d	-	drift velocity
E		electric field
eV	-	electron volt
ω	-	frequency
$\Delta\omega$	-	frequency shift
d	-	grain size (in nm)
Γ	-	line width
μm	-	micrometer
μ	-	mobility
r_o	-	nanocrystal radius
nm	-	nanometer
I	-	peak intensity from the spectra
x	-	Si composition (x: $0 \leq x \leq 1$)
ε	-	strain
m^*_t	-	transverse electron mass
λ	-	wavelength
q	-	wave vector

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CHAPTER 1

INTRODUCTION

1.1 Overview of present ultra-large-scale-integrated circuits (ULSIs) technology

Silicon (Si) based electronics is one of the most successful technologies in history. Introduction of several innovations such as strained Si [1], high-*k* materials [2-4] and tri-gate [4-6] structure also have enhanced the performance of Si ultra-large-scale-integrated circuits (ULSIs). Conforming to Moore's Law, about more than 10^{19} transistors are made each year and these gains have been possible because the physical size of transistors has been scaling to smaller dimensions progressively, that called as miniaturization process [4, 7-10]. Principally, this miniaturization of transistors is known to be very helpful in increasing the performance of the Si-ULSIs [4, 8-12].

Nevertheless, continuous miniaturization of transistors down to nano-scale regime tends to create several problems such as short channel effect [11, 12], gate leakage current [11, 13] and others. Owing to these physical limitations, the miniaturization of transistors becomes increasingly difficult and the conventional scaling rule will not be enough to enhance the performance of the ULSIs.

According to the International Technology Roadmap for Semiconductors (ITRS) 2009 edition [14], new channel materials with higher carrier mobilities than Si are promising to enhance the switching speed of complementary metal oxide

semiconductor (CMOS) transistors [7, 8, 15-21]. Over the past decade, much attention has been paid to germanium (Ge) and III-V semiconductor channels [7, 8, 15-32] as the candidates to fulfil such purposes. A co-integration of these materials on Si platform should enable the realization of the so-called More than Moore technology [15]. Interestingly, these materials are not only can be used to fabricate high speed conventional CMOS, but also to fabricate new transistors with different operating principles, such as tunnel field effect transistor (FET) [2] and plasma wave device [33, 34] etc, as well as to fabricate various kinds of functional devices such as sensors [35-37], optical devices [38], detectors [34, 39-42], and solar batteries [43], display panels [44, 45] and ultra high frequency electronic devices [34, 40, 46, 47].

In addition, co-integration of these materials on the Si platform is beneficial since Si is a cheap material and available in large wafer size. Si technology is mature and Si based devices are still needed for certain purposes. Therefore, the growth method of these materials, particularly Ge films in this present study, should be tailored so that the well developed Si technology still could be utilized with minimum modification and cost.

Nowadays, there are many researches on the growth of Ge on Si [48-52] which seems to accelerate the realization of such technology. As a result, a co-integration of Ge on Si platform, i.e. Ge/Si heterostructure, seems to offer the present ULSIs with superb multi-functionalities [23]. The evolution idea of Si based nanoelectronics devices is illustrated in **Figure 1.1**.

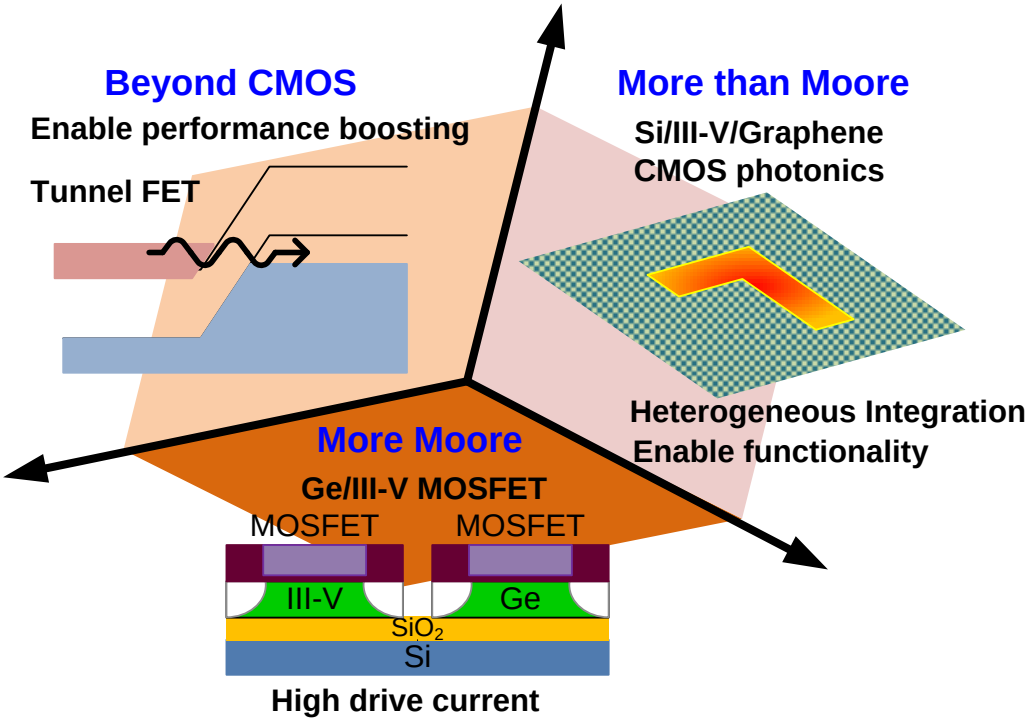

Figure 1.1 Evolution of Si based nanoelectronics (adopted from ref [53, 54])

1.2 Future heterogeneous integration on silicon platform

As the next-generation technology, advanced heterogeneous integration on Si platform has been considered as the promising and practical direction [54]. In this concept, new semiconductor materials with higher carrier mobility than Si are becoming the ideal channel materials to enhance the performance of the conventional transistors in the chips. Ge exhibits electron mobility two times greater and hole mobility four times greater than that of Si [48]. Therefore, Ge channel devices are expected to provide significant performance enhancement.

The growth of high quality materials on Si, particularly Ge films in this present study, is highly required in order to realize such concept of heterogeneous integration. As reported by Takagi *et al.* [23], co-integration of these functional materials on Si platform seems to offer the present ULSIs with superb multi-

REFERENCES

1. Hoyt, J. L., Nayfeh, H. M., Eguchi, S., Aberg, I., Xia, G., Drake, T., Fitzgerald, E. A. and Antoniadis, D. A. Strained Silicon MOSFET Technology. *International Electron Devices Meeting (IEDM).* December 8-11. San Francisco, California. 2002.
2. Boucart, K. and Ionescu, A. M. Double-Gate Tunnel FET with High-k Gate Dielectric. *IEEE Trans. Electron Devices,* 2007. 54(7): 1725-1733.
3. Gnani, E., Reggiani, S., Rudan, M., and Baccarani, G. Effects of High-k (HfO_2) Gate Dielectrics in Double-Gate and Cylindrical-Nanowire FETs Scaled to the Ultimate Technology Nodes. *IEEE Trans. Nanotechnol.,* 2007. 6(1): 90-96.
4. Chau, R., Doczy, M., Doyle, B., Datta, S., Dewey, G., Kavalieros, J., Jin, B., Metz, M., Majumdar, A and Radosavljevic, M. Advanced CMOS Transistors in the Nanotechnology Era for High-Performance, Low-Power Logic Applications. *Proceedings of 7th International Conference in Solid-State and Integrated Circuits Technology*. October 18-21. Beijing, China. 2004.
5. Ferain, I., Colinge, C. A., and Colinge, J. P. Multigate Transistors as the Future of classical Metal–Oxide–Semiconductor Field-Effect Transistors. *Nature*, 2011. 479(7373): 310-316.
6. Takagi, S. High Mobility Channel CMOS Technologies for Realizing High Performance LSI's. *IEEE Custom Integrated Circuits Conference (CICC '09).* September 13-16. San Jose, California. 2009
7. Wistey, M., Singisetti, U., Burek, G., Kim, E., Thibeault, B. J., Nelson, A., Cagnon, J., Lee, Y-J., Bank, Seth R., Stemmer, S., McIntyre, P. C., Gossard, A. C. and Rodwell, M. J., III-V/Ge Channel Engineering for Future CMOS. *ECS Trans.,* 2009. 19(5): 361-372.

8. Thompson, S. E., and Parthasarathy, S. Moore's Law: The Future of Si Microelectronics. *Mater. Today*, 2006. 20 - 25.

9. Murphy, B. T., Haggan, D. E. and Troutman, W. W. From Circuit Miniaturization to the Scalable IC. *Proc. IEEE,* 2000. 88(5): 691-703.

10. Theis, T. N. Beyond the Silicon Transistor: Personal Observations. *Comput. Sci. Eng*., 2003. 5(1): 25-29.

11. Timp, G., Bourdelle, K. K., Bower, J. E., Baumann, F. H., Boone, T., Cirelli, R., Evans-Lutterodt, K., Garno, J., Ghetti, A., Gossmann, H., Green, M., Jacobson, D., Kim, Y., Kleiman, R., Klemens, F., Kornlit, A., Lochstampfor, C., Mansfield, W., Moccio, S., Muller, D. A., Ocola, I. E., O'Malley, M. I., Rosamilia, J., Sapjeta, J., Silverman, P., Sorsch, T., Tennant, D. M., Timp, W. and Weir, B. E. Progress Toward 10 nm CMOS Devices. *Technical Digest of International Electron Devices Meeting (IEDM)*. December 6-9. San Francisco, California. 1998.

12. Ng, K. K., Eshraghi, S. A., and Stanik, T. D. An Improved Generalized Guide for MOSFET Scaling. *IEEE Trans. Electron Devices*, 1993. 40(10): 1895-1897.

13. Gehring, A., and Selberherr, S. Gate Leakage Models for Device Simulation. *Proceedings of 7th International Conference on Solid-State and Integrated Circuits Technology*. October 18-21. Beijing, China. 2004.

14. International Technology Roadmap for Semiconductors. Retrieved 31 August 2012, from http://public.itrs.net/links/2009ITRS/Home2009.htm

15. Takagi, S., Sugiyama, M., Yasuda, T., and Takenaka, M. Ge/III-V Channel Engineering for Future CMOS. *ECS Trans*., 2009. 19(5): 9-20.

16. Nayfeh, A., Chi On, C., Yonehara, T., and Saraswat, K. C. Fabrication of High-Quality p-MOSFET in Ge Grown Heteroepitaxially on Si. *IEEE Electron Device Lett.*, 2005. 26(5): 311-313.

17. Zhiyuan, C., Park, J. S., Bai, J., Jizhong, L., Hydrick, J., Fiorenza, J. and Lochtefeld, A. Aspect Ratio Trapping Heteroepitaxy for Integration of Germanium and Compound Semiconductors on Silicon. *9th International Conference on Solid-State and Integrated-Circuit Technology (ICSICT 2008)*. October 20-23. Beijing, China. 2008.

18. Ahmed, A. H. Z., and Tait, R. N. Characterization of an Amorphous $Ge_xSi_{1-x}O_y$ Microbolometer for Thermal Imaging Applications. *IEEE Trans. Electron Devices,* 2005. 52(8): 1900-1906.

19. Jawad, M. J., Hashim, M. R. and Ali, N. K. Hydrogen Sensor Based on Schottky Barriers of Pd/Geo_2 Using a Low Cost Electrochemically Deposited Thin GeO_2 Film. *2010 International Conference on Enabling Science and Nanotechnology (ESciNano)*. December 1-3. Kuala Lumpur, Malaysia. 2010.

20. Khan, M. A., Farhan, M., and Hogan, T. P. Low Temperature Synthesis of Germanium Oxide Nanowires by Thermal Evaporation of Germanium in an Oxidizing Environment. *IEEE Nanotechnology Materials and Devices Conference (NMDC '09)*. June 2-5. Traverse City, Michigan, USA. 2009.

21. Wang, K. L., Dongho, C., Jianlin, L., and Chen, C. Ge/Si Self-Assembled Quantum Dots and Their Optoelectronic Device Applications. *Proc. IEEE*, 2007. 95(9): 1866-1883.

22. Bescond, M., Cavassilas, N., Kalna, K., Nehari, K., Raymond, L., Autran, J. L., Lannoo, M. and Asenov, A. Ballistic Transport in Si, Ge and GaAs Nanowire MOSFETs, *IEDM Technical Digest (IEEE)*. 2005. 526.

23. Takagi, S., Sugiyama, M., Yasuda, T. and Takenaka, M., Ge/III-V Channel Engineering for Future CMOS, *Graphene and Emerging Materials for Post-CMOS Applications*. Pennington: Electrochemical Society Inc. 2009. 1: 19-20.

24. Rusli, N. I., Tanikawa, M., Mahmood, M. R., Yasui, K. and Hashim, A. M. Growth of High-Density Zinc Oxide Nanorods on Porous Silicon by Thermal Evaporation. *Materials*, 2012. 5(12): 2817-2832.

25. Astuti, B., Tanikawa, M., Rahman, S. F. A., Yasui, K., and Hashim, A. M. Graphene as a Buffer Layer for Silicon Carbide-on-Insulator Structures. *Materials*, 2012. 5(11): 2270-2279.

26. Anisuzzaman, M., Muta, S., Takahashi, M., Hashim, A. M., and Sadoh, T. Orientation-Control of Ge-Stripes-on-Insulator by Narrowing in Rapid-Melting Growth from Si (111) Seed. *ECS Solid State Letters*. 2013. 2(9): P76-P78.

27. Hashim, A. M., Anisuzzaman, M., Muta, S., Sadoh, T. and Miyao, M. Epitaxial-Template Structure Utilizing Ge-on-Insulator Stripe Arrays with

Nano-Spacing for Advanced Heterogeneous Integration on Si Platform. *Jpn. J. Appl. Phys*., 2012. 51: 06FF04.

28. Gao, Q., Kang, J. H., Tan, H. H., Jackson, H. E., Smith, L. M., Yarrison-Rice, J. M., Zou, J. and Jagadish, C. Growth and Characterization of Compound Semiconductor Nanowires on Si. *11th IEEE Conference on Nanotechnology (IEEE-NANO)*. August 15-18. Portland, Oregon. 2011.
29. Cantoro, M., Merckling, C., Jiang, S., Guo, W., Waldron, N., Bender, H., Moussa, A., Douhard, B., Vandervorst, W., Heyns, M. M., Dekoster, J., Loo, R. and Caymax, M. Towards the Monolithic Integration of III-V Compound Semiconductors on Si: Selective Area Growth in High Aspect Ratio Structures vs. Strain Relaxed Buffer-Mediated Epitaxy. *IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*. October 14-17. La Jolla, California. 2012.
30. Datta, S. and Chau, R. Silicon and III-V Nanoelectronics. *IEEE 17th International Conference on Indium Phosphide and Related Materials (IPRM)*. May 8-12. Glasgow, United Kingdom. 2005.
31. Hill, R. J. W., Baraskar, A., Park, C., Barnett, J., Majhi, P., and Jammy, R. Compound Semiconductors on Silicon for Future Generation VLSI. *IEEE International SOI Conference (SOI).* October 11-14. San Diego, California. 2010.
32. Caymax, M., Merckling, C., Gang, W., Orzali, T., Weiming, G., Vandervorst, W., Dekoster, J. Waldron, N., and Thean, A. Epitaxy of III-V based Channels on Si and Transistor Integration for 12-10 nm Node CMOS. *2012 International Conference on in Indium Phosphide and Related Materials (IPRM)*. August 27-30. Santa Barbara, California. 2012.
33. Veksler, D. B., Muraviev, A. V., Elkhatib, T. A., Salama, K. N., and Shur, M. S. Plasma Wave FET for Sub-Wavelength THz Imaging. *International Semiconductor Device Research Symposium (ISDRS)*. December 12-14. Maryland, USA. 2007.
34. Hashim, A. M., Kasai, S., and Hasegawa, H. Observation of First and Third Harmonic Responses in Two-Dimensional AlGaAs/GaAs HEMT Devices due to Plasma Wave Interaction. *Superlattices Microstruct.*, 2008. 44(6): 754-760.

35. Liu, Y., Gopalafishan, K., Griffin, P. B., Ma, K., Deal, M. D., and Plummer, J. D. MOSFETs and High-Speed Photodetectors on Ge-on-Insulator Substrates Fabricated Using Rapid Melt Growth. *IEDM Technical Digest of IEEE International Electron Devices Meeting*. December 13-15. San Francisco, California. 2004.

36. Abidin, M. S. Z., Hashim, A. M., Sharifabad, M. E., Rahman, S. F. A., and Sadoh, T. Open-Gated pH Sensor Fabricated on an Undoped-AlGaN/GaN HEMT Structure. *Sensors*, 2011. 11(3): 3067-3077.

37. Mohamad, M., Mustafa, F., Hashim, A. M., Rahman, S. F. A., Aziz, A. A., and Hashim, M. R. Fabrication of Pt-Circular Schottky Diode on Undoped AlGaN/GaN HEMT. *J. Appl. Sci.,* 2010. 10(19): 2338-2342.

38. Itabashi, S., Nishi, H., Tsuchizawa, T., Watanabe, T., Shinojima, H., Park, S., Yamada, K., Ishikawa, Y. and Wada, K. Integration of Optical Devices Based on Si, Ge and SiO_x. *7th IEEE International Conference on Group IV Photonics (GFP).* September 1-3. Beijing, China. 2010.

39. Wang, J. and Lee, S. Ge-Photodetectors for Si-Based Optoelectronic Integration. *Sensors*, 2011. 11(1): 696-718.

40. Hashim, A. M., Mustafa, F., Rahman, S. F. A., and Rahman, A. R. A. Dual-Functional On-Chip AlGaAs/GaAs Schottky Diode for RF Power Detection and Low-Power Rectenna Applications. *Sensors,* 2011. 11(8): 8127-8142.

41. Herman, M. A. Silicon-Germanium Heterostructures: Properties, Technology, and Application in Infrared Detectors. *Opto-Electron. Rev.,* 1997. 5(3): 191-204.

42. Michel, J., J. Liu, and Kimerling, L. C. High-performance Ge-on-Si Photodetectors. *Nat. Photonics*, 2010. 4: 527-534.

43. Claeys, C. and Simoen, E. *Germanium-Based Technologies: From Materials to Devices*. 2007, Amsterdam: Elsevier Science. 480.

44. Miyao, M., Toko, K., Tanaka, T., and Sadoh, T. High-Quality Single-Crystal Ge Stripes on Quartz Substrate by Rapid-Melting-Growth. *Appl. Phys. Lett*., 2009. 95(2): 022115-3.

45. Toko, K., Nakao, I., Sadoh, T., Noguchi, T., and Miyao, M. Electrical Properties of Poly-Ge on Glass Substrate Grown by Two-Step Solid-Phase Crystallization. *Solid-State Electron.,* 2009. 53(11): 1159-1164.

46. Eastman, L.F. Summary Abstract: Compound Semiconductor Structures for High Speed, High Frequency Devices. *J. Vac. Sci. Technol., B,* 1983. 1(2): 455-455.

47. Trew, R. J., Shin, M. W., and Gatto, V. Wide Bandgap Semiconductor Electronic Devices for High Frequency Applications. *Technical Digest of 18th Annual Gallium Arsenide Integrated Circuit (GaAs IC) Symposium*. November 3-6. Orlando, Florida. 1996.

48. Huang, Q., Bedell, S. W., Saenger, K. L., Copel, M., Deligianni, H., and Romankiwa, L. T. Single-Crystalline Germanium Thin Films by Electrodeposition and Solid-Phase Epitaxy. *Electrochem. Solid-State Lett*., 2007. 10(11): D124-D126.

49. Huang, S., Xia, Z., Xiao, H., Zheng, J., Xie, Y., and Xie, G. Structure and Property Of Ge/Si Nanomultilayers Prepared by Magnetron Sputtering. *Surf. Coat. Technol*., 2009. 204(5): 558-562.

50. McComber, K. A., Duan, X., Liu, J., Michel, J., and Kimerling, L. C. Single-Crystal Germanium Growth on Amorphous Silicon. *Adv. Funct. Mater*., 2012. 22(5): 1049-1057.

51. McComber, K. A., Jifeng, L., Michel, J., and Kimerling, L. C. Low-Temperature Germanium Ultra-High Vacuum Chemical Vapor Deposition for Back-End Photonic Integration. *6th IEEE International Conference on Group IV Photonics (GFP '09)*. September 9-11. San Francisco, California. 2009.

52. Chen, C., Li, C., Huang, S., Zheng, Y., Lai, H., and Chen, S. Epitaxial Growth of Germanium on Silicon for Light Emitters. *Int. J. Photoenergy,* 2012. 2012: 768605 1-8.

53. Takagi, S. and Takenaka, M. Advanced CMOS Technologies Using III-V/Ge Channels. *International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA).* June 15-17. Hsinchu, Taiwan. 2011.

54. Takagi, S. and Takenaka, M. III-V/Ge CMOS Technologies on Si Platform. *International Symposium on VLSI Technology (VLSIT)*. June 15-17. Honolulu, Hawaii. 2010.

55. Jordan, J.P., The ABC's of germanium. *Electr. Eng*., 1952. 71(7): 619-625.

56. Oyanagi, H., Sakamoto, K., Shioda and Sakamoto, T. Ge Epitaxial Overlayers on Si (001) Studied by Surface-Sensitive X-Ray Absorption Fine

Structure: Evidence for Strain-Induced Surface Rearrangement. *Jpn. J. Appl. Phys.*, 1994. 33(Part 1, No. 6A): 3545 - 3552.

57. Fujinaga, K., Low-Temperature Heteroepitaxy of Ge on Si by GeH_4 in Gas Low Pressure Chemical Vapor Deposition. *J. Vac. Sci. Technol., B,* 1991. 9(3): 1511-1516.
58. Oyanagi, H., Sakamoto, K., Shioda, R., Kuwahara, Y., and Haga, K. Ge Overlayers on Si (001) Studied by Surface-Extended X-Ray-Absorption Fine Structure. *Phys. Rev. B,* 1995. 52(8): 5824-5829.
59. Yeom, H. W., Sasaki, M., Suzuki, S., Sato, S., Hosoi, S., Iwabuchi, M., Higashiyama, K., Fukutani, H., Nakamura, M., Abukawa, T. and Kono, S. Existence of a Stable Intermixing Phase for Monolayer Ge on Si (001*). Surf. Sci.*, 1997. 381(1): L533-L539.
60. De Seta, M., Capellini, G., Evangelisti, F., and Spinella, C. Intermixing-Promoted Scaling of Ge/Si (100) Island Sizes. *J. Appl. Phys.*, 2002. 92(1): 614-619.
61. Jie, X., Wei, L., Yongjie, H., Yue, W., Hao, Y., and Lieber, C. M. Ge/Si Nanowire Heterostructures as High-Performance Field-Effect Transistors. *Nature*, 2006. 441(7092): 489-493.
62. Hu, W., Cheng, B., Xue, C., Su, S., Xue, H., Zuo, Y., and Wang, Q. Ge-on-Si for Si-based Integrated Materials and Photonic Devices. *Frontiers of Optoelectronics.* 2012. 5(1): 41-50.
63. Liu, J., Camacho-Aguilera, R., Bessette, J. T., Sun, X., Wang, X., Cai, Y., Kimerling, L. C. and Michel, J. Ge-on-Si Optoelectronics. *Thin Solid Films*, 2012. 520(8): 3354-3360.
64. Zhu, X. Y. and Lee, Y. H. Defect-Induced Si/Ge intermixing on the Ge/Si (100) Surface. *Phys. Rev. B,* 1999. 59(15): 9764-9767.
65. Liao, M. H., Lee, C. H., Hung, T. A., and Liu, C. W. The Intermixing and Strain Effects on Electroluminescence of SiGe Dots. *J. Appl. Phys.*, 2007. 102(5): 053520-5.
66. Miyao, M., Tanaka, T., Toko, K., and Tanaka, M. Giant Ge-on-Insulator Formation by Si–Ge Mixing-Triggered Liquid-Phase Epitaxy. *Appl. Phys Express*, 2009. 2: 045503.
67. Jawad, M. J., Hashim, M. R., Ali, N. K., C´orcoles, E. P., and Sharifabad, M. E. An Alternative Method to Grow Ge Thin Films on Si by Electrochemical

Deposition for Photonic Applications. *J. Electrochem. Soc.,* 2012. 159(2): D124-128.

68. Butterman, W.C. and Jorgenson, J.D. *Mineral Commodity Profiles: Germanium*, in Open-File Report 2004-1218. 2004, USGS: Virginia. p. 4.
69. Virginia Semiconductor. 2002. The General Properties of Si, Ge, SiGe, SiO_2 and Si_3N_4. Retrieved from http://www. virginiasemi.com/pdf/general propertiessi62002.pdf
70. Barski, A., Derivaz, M., Rouviere, J. L., and Buttard, D. Epitaxial Growth of Germanium Dots on Si (001) Surface Covered by a Very Thin Silicon Oxide Layer. *Appl. Phys. Lett*., 2000. 77(22): 3541-3543.
71. Sorianello, V., Colace, L., Assanto, G., Notargiacomo, A., Armani, N., Rossi, F. and Ferrari, C. Thermal Evaporation of Ge on Si for Near Infrared Detectors: Material and Device Characterization. *Microelectron. Eng*., 2011. 88(4): 526-529.
72. Ishikawa, Y. and Wada, K. Germanium for Silicon Photonics. *Thin Solid Films*, 2010. 518(6, Supplement 1): S83-S87.
73. Larrson, M., Eflving, A., Hussain, M. I., Holtz, P. O., and Ni, W.-X. Luminescence Properties of Ge Quantum Dots Produced by MBE at Different Temperatures. *First IEEE International Conference on Group IV Photonics.* September 29 – October 1. Hong Kong, China. 2004.
74. Miura, A., Irisawa, T., Koh, S., Nakagawa, K., and Shiraki, Y. Fabrication of High-Ge Fraction Relaxed SiGe-on-Insulator Virtual Substrate by MBE Growth and Thermal Annealing. *2002 International Conference on Molecular Beam Epitaxy*. September 15-20. San Francisco, California. 2002.
75. Yang, R., Li, K., Li, G., Peng, C., and Li, Y. The Properties of Epitaxial Pure Germanium Films on Silicon Substrate. *Proceedings of 6th International Conference on Solid-State and Integrated-Circuit Technology*. October 22-25. Shanghai, China. 2001.
76. Jun, S.-I., Rack, P. D., McKnight, T. E., Melechko, A. V., and Simpson, M. L. Low-Temperature Solid-Phase Crystallization of Amorphous Silicon Thin Films Deposited by RF Magnetron Sputtering with Substrate Bias. *Appl. Phys. Lett.,* 2006. 89(2): 022104-3.
77. Lokhande, C. D. and Pawar, S. H. Electrodeposition of Thin Film Semiconductors. *Phys. Status Solidi A*, 1989. 111(1): 17-40.

78. Jayakrishnan, S., Pushpavanam, M., and Shenoi, B. A. Electrodeposition from Organic Solutions of Metals That are Difficult to Deposit from Aqueous Solutions. *Surface Technology*, 1981. 13: 225 - 240.

79. Endres, F., and Abedin, S. Z. E. Nanoscale Electrodeposition of Germanium on Au (111) from an Ionic Liquid: An In Situ STM Study of Phase Formation. *Phys. Chem. Chem. Phys.*, 2002. 4: 1640–1657.

80. Endres, F., Ionic Liquids: Promising Solvents for Electrochemistry. *Z. Phys. Chem.,* 2004. 218: 255–283.

81. Mukhopadhyay, I. and Freyland, W. Thickness Induced Metal–Nonmetal Transition in Ultrathin Electrodeposited Ge Films. *Chem. Phys. Lett.,* 2003. 377: 223–228.

82. Szekely, G. Electrodeposition of Germanium. *J. Electrochem. Soc.,* 1951. 98(8): 318 - 324.

83. Szekely, G. *Electroplating of Germanium*, in U.S. Patent 2, 690, 422. 1951.

84. Saitou, M., Sakae, K., and Oshikawa, W. Evaluation of crystalline germanium thin films electrodeposited on copper substrates from propylene glycol electrolyte. *Surf. Coat. Technol.*, 2002. 162: 101 - 105.

85. Huang, Q., Deligianni, H., and Romankiwa, L. T. Anisotropic Growth of Nanostructures in Germanium Electroplating. *Electrochem. Solid-State Lett.,* 2007. 10(11): D121-D123.

86. Freyland, W., Zell, C. A., Abedin, S. Z. E. and Endres, F. Nanoscale Electrodeposition of Metals and Semiconductors from Ionic Liquids. *Electrochim. Acta*, 2003. 48, 3053-3061.

87. Abidin, M. S. Z. A, Matsumura, R., Anisuzzaman, M., Park, J.-H., Muta, S., Mahmood, M. R., Sadoh, T. and Hashim, A. M. Crystallization of Electrodeposited Germanium Thin Film on Silicon (100). *Materials,* 2013. 6(11): 5047-5057.

88. Sakaike, K., Higashi, S., Murakami, H., and Miyazaki, S. Crystallization of Amorphous Ge Films Induced by Semiconductor Diode Laser Annealing. *Thin Solid Films*, 2008. 516(11): 3595-3600.

89. Sameshima, T., Watakabe, H., Kanno, H., Sadoh, T., and Miyao, M. Pulsed Laser Crystallization of Silicon–Germanium Films. *Thin Solid Films,* 2005. 487(1–2): 67-71.

90. Suzuki, A. and Isomura, M. Crystalline Growth of Germanium Thin Films on Single Crystal Silicon Substrates by Solid Phase Crystallization. *J. Non-Cryst. Solids,* 2012. 358(17): 2166-2170.

91. Going, R., Tsu-Jae King, L., and Wu, M. C. Rapid Melt Grown Germanium Gate PhotoMOSFET on a Silicon Waveguide. *IEEE Photonics Conference (IPC)*. September 8-12. Washington, USA. 2013.

92. Liu, Y., Deal, M. D. and Plummer, J. D. Rapid Melt Growth of Germanium Crystals with Self-Aligned Microcrucibles on Si Substrates. *J. Electrochem. Soc.,* 2005. 152(8): G688-G693.

93. Toko, K., Ohta, Y., Sakane, T., Sadoh, T., Mizushima, I., and Miyao, M. Single-Crystalline (100) Ge Networks on Insulators By Rapid-Melting Growth Along Hexagonal Mesh-Pattern. *Appl. Phys. Lett.,* 2011. 98(4): 042101-3.

94. Toko, K., Tanaka, T., Ohta, Y., Sadoh, T., and Miyao, M. Defect-free Ge-on-Insulator with (100), (110), and (111) Orientations by Growth-Direction-Selected Rapid-Melting Growth. *Appl. Phys. Lett.,* 2010. 97(15): 152101-3.

95. Sadoh, T., Toko, K., Kurosawa, M., Tanaka, T., Sakane, T., Ohta, Y., Kawabata, N., Yokoyama, H. and Miyao, M. SiGe-Mixing-Triggered Rapid-Melting-Growth of High-Mobility Ge-on-Insulator. *Key Eng. Mater.,* 2011. 470: 8-13.

96. Sasaki, M., Abukawa, T., Yeom, H. W., Yamada, M., Suzuki, S., Sato, S. and Kono, S. Auger Electron Diffraction Study of The Initial Stage of Ge Heteroepitaxy on Si (001). *Appl. Surf. Sci.,* 1994. 82–83(0): 387-393.

97. Brinkman, W. F., Haggan, D. E., and Troutman, W. W. A History of the Invention of the Transistor and Where It Will Lead Us. *IEEE J. Solid-State Circuits,* 1997. 32(12): 1858-1865.

98. Morton, J. A. Present Status of Transistor Development. *Proc. IRE,* 1952. 40(11): 1314-1326.

99. Gosling, W. The Pre-History of the Transistor. *Radio and Electronic Engineer*. 1973. 43(1.2): 10.

100. Datta, S., Brask, J., Dewey, G., Doczy, M., Doyle, B., Ben, J., Kavalieros, J., Metz, M., Majumdar, A., Radosavljevic, M. and Chau, R. Advanced Si and SiGe Strained Channel NMOS and PMOS Transistors with High-K/Metal-

Gate Stack. *Proceedings of the 2004 Meeting Bipolar/BiCMOS Circuits and Technology*. September 12-14. Montreal, Canada. 2004.

101. Miyao, M., Murakami, E., Etoh, H., Nakagawa, K., and Nishida, A. High Hole Mobility in Strained Ge Channel of Modulation-Doped p-$Si_{0.5}Ge_{0.5}$/Ge/$Si_{1-x}Ge_x$ Heterostructure. *J. Cryst. Growth*, 1991. 111(1–4): 912-915.
102. Shang, H., Frank, M. M., Gusev, E. P., Chu, J. O., Bedell, S. W., Guarini, K. W., and Ieong, M. Germanium Channel MOSFETs: Opportunities and Challenges. *IBM J. Res. Dev.*, 2006. 50(4.5): 377-386.
103. Atuchin, V. V., Gavrilova, T. A., Gromilov, S. A., Kostrovsky, V. G., Pokrovsky, L. D., Troitskaia, I. B., Vemuri, R. S., Carbajal-Franco, G. and Ramana, C.V. Low-Temperature Chemical Synthesis and Microstructure Analysis of GeO2 Crystals with a-Quartz Structure. *Cryst. Growth Des.*, 2009. 9(4): 1829–1832.
104. Yan, W. X., Lian, D., Fang, D. G., Peng, W., Wei, W., Duo, W. L., and Yong, Q. Synthesis and Characterization of Nano/Microstructured Crystalline Germanium Dioxide with Novel Morphology. *Chin. Sci. Bull.*, 2009. 54: 2810 - 2813.
105. Jawad, M. J., Hashim, M. R., and Ali, N. K. Synthesis, Structural, and Optical Properties of Electrochemically Deposited GeO_2 on Porous Silicon. *Electrochem. Solid-State Lett.*, 2011. 14(2): D17-D19.
106. Terakado, N. and Tanaka, K. Photo-Induced Phenomena in GeO_2 Glass, Hokkaido University. p. 1 - 20.
107. Terakado, N. and Tanaka, K. Photo-Induced Phenomena in Sputtered GeO_2 Films. *J. Non-Cryst. Solids*, 2005. 351: 54 - 60.
108. Zhou, M., Shao, L., and Miao, L. Matrix Isolation Infrared Spectroscopic and Density Functional Theoretical Calculations of the GeO_2- and GeO_4- Anions. *J. Phys. Chem. A*, 2002. 106: 6483-6486.
109. Terakado, N. and Tanaka, K. Photo-Induced Phenomena in GeO_2 Glass. *J. Non-Cryst. Solids*, 2006. 352(36–37): 3815-3822.
110. Robert D. Brown, J. *Germanium*. U.S. Geological Survey. 2000.
111. Andersen, R.A. *Algal Culturing Techniques*. 2005: Academic Press.

112. Micoulaut, M., Cormier, L., and Henderson, G. S. The Structure of Amorphous, Crystalline and Liquid GeO_2. *J. Phys. Condens. Matter,* 2006. 18: R753–R784.

113. Scott, J. F. Raman Spectra of GeO_2. *Phys. Rev. B: Condens. Matter,* 1970. 1(8): 3488 - 3493.

114. Bai, Z. G., Yu, D. P., Zhang, H. Z., Ding, Y., Wang, Y. P., Gai, X. Z., Hang, Q.L., Xiong, G.C. and Feng, S.Q. Nano-scale GeO_2 Wires Synthesized by Physical Evaporation. *Chem. Phys. Lett.,* 1999. 303: 311–314.

115. Wu, X. C., Song, W. H., Zhao, B., Sun, Y. P., and Du, J. J. Preparation and Photoluminescence Properties of Crystalline GeO_2 Nanowires. *Chem. Phys. Lett.,* 2001. 349: 210 -214.

116. Hu, J. Q., Li, Q., Meng, X. M., Lee, C. S., and Lee, S. T. Synthesis and Nanostructuring of Patterned Wires of a-GeO_2 by Thermal Oxidation. *Adv. Mater.,* 2002. 14(19): 1396 - 1399.

117. Kim, H. W., Lee, J. W., Kebede, M. A., Kim, H. S., and Lee, C. Catalyst-Free Synthesis of GeO_2 Nanowires Using the Thermal Heating of Ge Powders. *Curr. Appl Phys.,* 2009. 9: 1300–1303.

118. Liu, Y., Deal, M. D., and Plummer, J. D. High-Quality Single-Crystal Ge on Insulator by Liquid-Phase Epitaxy on Si Substrates. *Appl. Phys. Lett.,* 2004. 84(14): 2563-2565.

119. Tweet, D. J., Lee, J. J., Maa, J.-S., and Hsu, S. T. Characterization and Reduction of Twist in Ge on insulator Produced by Localized Liquid Phase Epitaxy. *Appl. Phys. Lett.,* 2005. 87(14): 141908-3.

120. Gao, F., Lee, S. J., Balakumar, S., Du, A., Foo, Y.-L., and Kwong, D. L. (2006). Ge Diffusion and Solid Phase Epitaxy Growth to Form $Si_{1-x}/Ge_x/Si$ and Ge on Insulator Structure. *Thin Solid Films,* 2006. 504(1–2): 69-72.

121. Balakumar, S., Roy, M. M., Ramamurthy, B., Tung, C. H., Fei, G., Tripathy, S., Dongzhi, C., Kumar, R., Balasubramanian, N. and Kwong, D. L. Fabrication Aspects of Germanium on Insulator from Sputtered Ge on Si-Substrates. *Electrochem. Solid-State Lett.,* 2006. 9(5): G158-G160.

122. Toko, K., Sakane, T., Tanaka, T., Sadoh, T., and Miyao, M. Defect-Free Single-Crystal Ge Island Arrays on Insulator by Rapid-Melting-Growth Combined with Seed-Positioning Technique. *Appl. Phys. Lett.,* 2009. 95(11): 112107-3.

123. Koh, H. Y. S., *Rapid Melt Growth of Silicon Germanium for Heterogenous Integration on Silicon*. Department of Electrical Engineering. 2011, Stanford University: United States. 215.

124. Schroder, D. K., *Semiconductor Material and Device Characterization*. 3rd ed. Hoboken, New Jersey: John Wiley & Sons, Inc. 800., 2006

125. Alfaro-Calderon, P., Cruz-Irisson, M., and Wang-Chen, C. Theory of Raman Scattering by Phonons in Germanium Nanostructures. *Nanoscale Res. Lett.,* 2008. 3: 55 - 59.

126. Alonso, M. I., and Winer, K. Raman Spectra of c-$Si_{1-x}Ge_x$ Alloys. *Phys. Rev. B: Condens. Matter,* 1989. 39(14): 10056-10062.

127. Colomban, P. and Slodczyk, A. Raman Intensity: An Important Tool in the Study of Nanomaterials and Nanostructures. *Acta Phys. Pol. A,* 2009. 116(1): 7 - 12.

128. De Wolf, I., Maes, H. E., and Jones, S. K. Stress Measurements in Silicon Devices through Raman Spectroscopy: Bridging The Gap Between Theory and Experiment. *J. Appl. Phys.,* 1996. 79(9): 7148-7156.

129. Dharma-wardana, M. W. C., Aers, G. C., Lockwood, D. J., and Baribeau, J. M. Interpretation of Raman Spectra of Ge/Si Ultrathin Superlattices. *Phys. Rev. B: Condens. Matter,* 1990. 41(8): 5319-5331.

130. Fujii, M., Hayashi, S., and Yamamoto, K. Growth of Ge Microcrystals in SiO_2 Thin Film Matrices: A Raman and Electron Microscopic Study. *Jpn. J. Appl. Phys.,* 1991. 30: 687 - 694.

131. Ichimura, M., Usami, A., Wakahara, A., and Sasaki, A. Raman Study of Strain Relaxation in Ge on Si. *J. Appl. Phys.,* 1995. 77(10): 5144-5148.

132. Kolobov, A. V. Raman Scattering from Ge Nanostructures Grown on Si Substrates: Power and Limitations. *J. Appl. Phys.,* 2000. 87(6): 2926-2930.

133. Kolobov, A. V., Maeda, Y., and Tanaka, K. Raman Spectra of Ge nanocrystals Embedded into SiO_2. *J. Appl. Phys.,* 2000. 88(6): 3285-3289.

134. Parker, J. H., Jr., Feldman, D. W., and Ashkin, M. Raman Scattering by Silicon and Germanium. *Phys. Rev.,* 1967. 155(3): 712-714.

135. Pezzoli, F., Bonera, E., Grilli, E., Guzzi, M., Sanguinetti, S., Chrastina, D., Isella, G., von Känel, H., Wintersberger, E., Stangl, J. and Bauer, G. Raman Spectroscopy Determination of Composition and Strain in $Si_{1-x}Ge_x$/Si Heterostructures. *Mater. Sci. Semicond. Process.,* 2008. 11(5–6): 279-284.

136. Application notes (RA39) : *Strain Measurements of a Si Cap Layer Deposited on a SiGe Substrate Determination of Ge Content.* HORIBA Jobin Yvon.

137. Strain Measurements of a Si Cap Layer Deposited on a SiGe Substrate Determination of Ge Content. Retrieved 9 June 2012, 2012, from http://www.intercovamex.com/biblioteca_de_aplicaciones/SEMICONDUCTORES/Mediciones%20de%20tension%20de%20de%20una%20capa%20de%20Si%20depositada%20en%20un%20sustrato%20de%20SiGe.%20Determinacion%20del%20contenido%20de%20Ge.pdf

138. Perova, T. S., Wasyluk, J., Lyutovich, K., Kasper, E., Oehme, M., Rode, K., and Waldron, A. Composition and Strain in Thin $Si_{1-x}Ge_x$ Virtual Substrates Measured by Micro-Raman Spectroscopy and X-Ray Diffraction. *J. Appl. Phys.,* 2011. 109(3): 033502-033511.

139. Mooney, P. M., Dacol, F. H., Tsang, J. C., and Chu, J. O. Raman Scattering Analysis of Relaxed Ge_xSi_{1-x} Alloy Layers. *Appl. Phys. Lett.,* 1993. 62(17): 2069-2071.

140. Kartopu, G., Bayliss, S. C., Karavanskii, V. A., Curry, R. J., Turan, R., and Sapelkin, A. V. On the Origin of the 2.2–2.3 eV Photoluminescence from Chemically Etched Germanium. *J. Lumin.,* 2003. 101(4): 275-283.

141. Paillard, V., Puech, P., Laguna, M. A., Carles, R., Kohn, B., and Huisken, F. Improved One-Phonon Confinement Model for an Accurate Size Determination of Silicon Nanocrystals. *J. Appl. Phys.,* 1999. 86(4): 1921-1924.

142. Volodin, V., Gorokhov, E., Efremov, M., Marin, D., and Orekhov, D. Photoluminescence of GeO_2 Films Containing Germanium Nanocrystals. *JETP Lett.,* 2003. 77(8): 411-414.

143. Zacharias, M. and Fauchet, P. M. Light Emission from Ge and GeO Nanocrystals. *J. Non-Cryst. Solids,* 1998. 227 - 230: 1058–1062.

144. Gao, T., Tong, S., Zheng, X., Wu, X., Wang, L., and Bao, X. Strong Visible Photoluminescence from Ge/Porous Si Structure. *Appl. Phys. Lett.,* 1998. 72(25): 3312-3313.

145. Ko, T. S., Shieh, J., Yang, M. C., Lu, T. C., Kuo, H. C., and Wang, S. C. Phase Transformation and Optical Characteristics of Porous Germanium Thin Film. *Thin Solid Films,* 2008. 516(10): 2934-2938.

146. Memming, R., *Electron Transfer Processes between Excited Molecules and Semiconductor Electrodes,* Semiconductor Electrochemistry. 2007, Wiley-VCH Verlag GmbH. 300-331.

147. Mestanza, S. N. M., Swart, J. W., Doi, I., and Frateschi, N. C. Synthesis of Ge Nanocrystals Grown by Ion Implantation and Subsequent Annealing. *Proceedings of the 6th International Caribbean Conference on Devices, Circuits and Systems*. April 26-28. Playa del Carmen, Mexico. 2006.

148. Khan, A. F., Mehmood, M., Rana, A. M., and Muhammad, T. Effect of Annealing on Structural, Optical and Electrical Properties of Nanostructured Ge Thin Films. *Appl. Surf. Sci.*, 2010. 256(7): 2031-2037.

149. Abd Rahim, A. F., Hashim, M. R., Rusop, M., Ali, N. K., and Yusuf, R. Room Temperature Ge and ZnO Embedded Inside Porous Silicon Using Conventional Methods for Photonic Application. *Superlattices Microstruct.*, 2012. 52(5): 941-948.

150. Liu, F. Q., Wang, Z. G., Li, G. H., and Wang, G. H. Photoluminescence from Ge Clusters Embedded in Porous Silicon. *J. Appl. Phys.*, 1998. 83(6): 3435-3437.

151. Martineau, F., Namur, K., Mallet, J., Delavoie, F., Endres, F., Troyon, M., and Molinari, M. Electrodeposition at Room Temperature of Amorphous Silicon and Germanium Nanowires in Ionic Liquid. *Symposium K, E-MRS 2009 Spring Meeting. 2009: IOP Conference Series: Materials Science and Engineering*. June 8-12. Strasbourg, France. 2009.

152. Olesinski, R. W. and Abbaschian, G. J. The Ge–Si (Germanium-Silicon) System. *Bulletin of Alloy Phase Diagrams*. 1984. 5(2): 180-183.

153. Wan, J., Luo, Y. H., Jiang, Z. M., Jin, G., Liu, J. L., Wang, K. L., Liao, X. Z., and Zou, J. Effects of Interdiffusion on the Band Alignment of GeSi Dots. *Appl. Phys. Lett.*, 2001. 79(13): 1980-1982.

154. Baranov, A. V., Fedorov, A. V., Perova, T. S., Moore, R. A., Yam, V., Bouchier, D., Le Thanh, V., and Berwick, K. Analysis of Strain and Intermixing in Single-Layer Ge/Si Quantum Dots Using Polarized Raman Spectroscopy. *Phys. Rev. B: Condens. Matter,* 2006. 73(7): 075322.

155. Tojo, Y., Matsumura, R., Yokoyama, H., Kurosawa, M., Toko, K., Sadoh, T., and Miyao, M. High-Quality Formation of Multiply Stacked SiGe-on-

Insulator Structures by Temperature-Modulated Successive Rapid-Melting-Growth. *Appl. Phys. Lett.*, 2013. 102(9): 092102-092104.

156. Pezzoli, F., Bonera, E., Grilli, E., Guzzi, M., Sanguinetti, S., Chrastina, D., Isella, G., von Kanel, H., Wintersberger, E., Stangl, J. and Bauer, G. Phonon Strain Shift Coefficients in $Si_{1-x}Ge_x$ Alloys. *J. Appl. Phys.*, 2008. 103(9): 093521-093524.
157. Ishikawa, Y., Wada, K., Liu, J., Cannon, D. D., Luan, H.-C., Michel, J., and Kimerling, L.C. Strain-Induced Enhancement of Near-Infrared Absorption in Ge Epitaxial Layers Grown on Si Substrate. *J. Appl. Phys.*, 2005. 98(1): 013501(1)-013501(9).
158. Abidin, M. S. Z., Morshed, T., Chikita, H., Kinoshita, Y., Muta, S., Anisuzzaman, M., Park, J. H., Matsumura, R., Mahmood, M. R., Sadoh, T. and Hashim, A. M. The Effects of Annealing Temperatures on Composition and Strain in Si_xGe_{1-x} Obtained by Melting Growth of Electrodeposited Ge on Si (100). *Materials*. 2014. 7, 1409-1421