iii

# RTL IMPLEMENTATION OF ONE-SIDED JACOBI ALGORITHM FOR SINGULAR VALUE DECOMPOSITION

WAN AHMAD ZAINIE BIN WAN MOHAMAD

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Universiti Teknologi Malaysia

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Specially dedicated to my parents,

my other half and

my children.

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# ABSTRACT

Multi-dimensional digital signal processing such as image processing and image reconstruction involve manipulating of matrix data. Better quality images involve large amount of data, which result in unacceptably slow computation. A parallel processing scheme is a possible solution to solve this problem. This project presented an analysis and comparison to various algorithms for widely used matrix decomposition techniques and various computer architectures. As the result, a parallel implementation of one-sided Jacobi algorithm for computing singular value decomposition (SVD) of a 2x2 matrix on field programmable gate arrays (FPGA) is developed. The proposed SVD design is based on pipelined-datapath architecture The design process is started by evaluating the algorithm using Matlab, design datapath unit and control unit, coding in SystemVerilog HDL, verification and synthesis using Quartus II and simulated on ModelSim-Altera. The original matrix size of 4x4 and 8x8 is used to with the SVD processing element (PE). The result are compared with the Matlab version of the algorithm to evaluate the PE. The computation of SVD can be speed-up of more than 2 by increasing the number of PE at the cost of increased in circuit area.

# ABSTRAK

Pemprosesan multi dimensi isyarat digital seperti pemposesan imej dan perstrukturan semula imej melibatkan manipulasi data matrik. Imej yang berkualiti melibatkan pemprosesan data dalam jumlah yang besar, seterusnya mengakibatkan pengiraan yang amat perlahan dan tidak dapat diterima. Salah satu cara untuk menyelesaikan masalah ini adalah dengan menggunakan skim pemprosesan selari. Projek ini membentangkan analisa dan perbandingan terhadap pelbagai algoritma yang digunakan secara meluas dalam teknik menguraikan matrik dan pelbagai senibina computer. Hasilnya, pelaksanaan selari algoritma One-sided Jacobi bagi mengira Singular Value Decomposition untuk matrix 2x2 direka untuk FPGA. Rekabentuk SVD yang dicadangkan adalah berdasarkan senibina pipelined-datapath. Proses rekabentuk bermula dengan menulis kembali algoritma untuk Matlab, merekabentuk laluan data dan system kawalan, seterusnya mengekod menggunakan SystemVerilog HDL, pengesahan dan simulasi menggunakan perisian Quartus II dan ModelSim-Altera. Saiz matrix 4x4 dan 8x8 digunakan dengan elemen pemprosesan SVD. Keputusan pengiraan dibandingkan dengan keputusan pengiraan Matlab untuk menilai pelaksaan. Pengiraan SVD meningkat melebihi 2 kali ganda dengan meningkat bilangan elemen pemprosesan, dengan kos peningkatan kawasan litar yang digunakan.

# TABLE OF CONTENTS

# LIST OF TABLES

# LIST OF FIGURES

# LIST OF ABBREVIATION

| | | |
|---|---|---|
| iobd | - | I/O block diagram |
| RTL | - | Register Transfer Level |
| SVD | - | Singular Value Decomposition |

# LIST OF APPENDICES

# CHAPTER 1

# INTRODUCTION

## 1.1    Background

Multi-dimensional digital signal processing such as image processing and image reconstruction involve manipulating of matrix data. Better quality images involve large amount of data, which result in unacceptably slow computation. A parallel processing scheme is a possible solution to solve this problem.

## 1.2    Problem Statement

The time to compute the matrix decomposition increases significantly with the increase of the size of the matrix. Using parallel algorithm to reduce the time to compute huge matrices as seen in image processing is not sufficient, thus it is necessary to implement the parallel algorithm in parallel processors too.

Therefore, it is justify to design a data path unit which implement a parallel algorithm, and a control unit capable to run multiple of such data path unit in parallel.

**1.3    Objectives of the Project**

Followings are the objectives for this project:-

(1)    To study matrix decomposition techniques and parallel processing hardware implementation on FPGA.

(2)    To design, simulate and verify the RTL implementation of the matrix decomposition algorithm using SystemVerilog HDL.

(3)    To evaluate the speedup improvement by comparing parallel processing against single processing.

**1.4    Scope of the Project**

The scope of this project focuses on the study of matrix decomposition techniques to translate single processing task to two or more processing tasks. Implement and verify a matrix decomposition algorithm using MATLAB. The algorithm is mapped into RTL implementation using System Verilog HDL, targeted for Altera FPGA board. The design is captured, simulated, verified and synthesized using ModelSim-Altera and Altera Quartus II and. A speedup improvement analysis is done by comparing single processing versus parallel processing.

**1.5    Significance of the Study**

This project proposes a parallel RTL implementation of matrix decomposition algorithm to speed up the computation for large matrices, suitable for image processing.

**1.6    Thesis Organization**

The rest of the thesis is organized based on the following structure.

Chapter 2 covers literature review of this project, which are related theoretical background and related works. Discussion on literature review mainly focus on hardware implementation of various matrix decomposition techniques, especially the singular value decomposition.

Chapter 3 describes the methodology to achieve the project objectives. This includes explanation on the architecture components, implementation flow, development environment and verification techniques.

Chapter 4 presents details on the results of simulation of the proposed RTL design and implementation. This chapter also includes evaluation of the implemented algorithmic processor for verification and benchmarking.

Chapter 5 summarizes this thesis, stating limitations of this project and provides suggestions for future works.

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