

HIGH SPEED – ENERGY EFFICIENT SUCCESSIVE APPROXIMATION
ANALOG TO DIGITAL CONVERTER USING TRI-LEVEL SWITCHING

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To my beloved husband and family

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ABSTRACT

This thesis reports issues and design methods used to achieve high-speed and high-resolution Successive Approximation Register analog to digital converters (SAR ADCs). A major drawback of this technique relates to the mismatch in the binary ratios of capacitors which causes nonlinearity. Another issue is the use of large capacitors due to nonlinear effect of parasitic capacitance. Nonlinear effect of capacitor mismatch is investigated in this thesis. Based on the analysis, a new Tri-level switching algorithm is proposed to reduce the matching requirement for capacitors in SAR ADCs. The integral non-linearity (INL) and the differential non-linearity (DNL) of the proposed scheme are reduced by factor of two over conventional SAR ADC, which is the lowest compared to the previously reported schemes. In addition, the switching energy of the proposed scheme is reduced by 98.02% compared with the conventional SAR architecture. A new correction method to solve metastability error of comparator based on a novel design approach is proposed which reduces the required settling time about 1.1τ for each conversion cycle. Based on the above proposed methods two SAR ADCs: an 8-bit SAR ADC with 50MS/sec sampling rate, and a 10-bit SAR split ADC with 70 MS/sec sampling rate have been designed in 0.18 μ m Silterra complementary metal oxide semiconductor (CMOS) technology process which works at 1.2V supply voltage and input voltage of 2.4Vp-p. The 8-bit ADC digitizes 25MHz input signal with 48.16dB signal to noise and distortion ratio (SNDR) and 52.41dB spurious free dynamic range (SFDR) while consuming about 589 μ W. The figure of merit (FOM) of this ADC is 56.65 fJ/conv-step. The post layout of the 10-bit ADC with 1MHz input frequency produces SNDR, SFDR and effective number of bits (ENOB) of 57.1dB, 64.05dB and 9.17Bit, respectively, while its DNL and INL are -0.9/+2.8 least significant bit (LSB) and -2.5/+2.7 LSB, respectively. The total power consumption, including digital, analog and reference power, is 1.6mW. The FOM is 71.75fJ/conv. step.

ABSTRAK

Tesis ini melaporkan isu dan teknik reka bentuk yang diguna untuk menghasilkan penukar analog kepada digital Daftar Penghampiran Berturutan (SAR ADCs) yang berkelajuan dan resolusi tinggi. Satu kelemahan utama teknik ini berkaitan dengan ketakpadanan dalam nisbah perduaan kapasitor yang menyebabkan ketaklinaran. Satu lagi isu ialah penggunaan kapasitor besar disebabkan oleh kesan ketaklinaran kapasitor parasitik. Kesan ketaklinaran kapasitor parasitik ini dikaji dalam tesis ini. Hasil daripada kajian ini, satu cara pensuisan Tri-tahap algoritma dicadangkan untuk mengurangkan keperluan sepadan kapasitor dalam SAR ADC. Ketidaklelurusan kamilan (INL) dan ketidaklelurusan perbezaan (DNL) pensuisan yang dicadangkan berjaya dikurangkan sebanyak dua kali ganda dan ini adalah yang paling rendah berbanding kaedah konvensional. Kuasa pensuisan juga dikurangkan sebanyak 98.02%. Satu cara pembetulan untuk menyelesaikan ralat metastabiliti juga dicadangkan dan berjaya mengurangkan masa menetap kepada 1.1τ bagi setiap kitar penukaran. Berdasarkan kepada teknik yang dicadangkan, dua SAR ADC telah direka bentuk: satu 8-bit SAR ADC dengan kadar pensampelan 50MS/saat dan satu 10-bit SAR ADC-Pecahan dengan kadar pensampelan 70MS/saat. Keduanya menggunakan proses CMOS 0.18 μm daripada Silterra dengan bekalan kuasa 1.2V dan voltan masukan 2.4Vp-p. Bagi masukan 25MHz, ADC 8-bit mendigitalkan 48.16dB isyarat kepada hingar dan kadar herotan (SNDR) dan 52.41dB julat dinamik bebas palsu (SFDR) dengan menggunakan kuasa 589 μW . Angka kebaikan (FOM) untuk ADC ini adalah 56.65 fJ/penukaran langkah. Pasca bentangan bagi ADC 10-bit dengan ulangan masukan 1MHz menghasilkan SNDR, SFDR and nombor bit berkesan (ENOB) of 57.1dB, 64.05dB dan 9.17Bit, setiap satu, manakala DNL and INL adalah -0.9/+2.8 bit paling kurang nilai (LSB) dan -2.5/+2.7 LSB. Jumlah semua kuasa yang diguna termasuk litar digital, analog dan kuasa rujukan adalah 1.6mW. FOM pula adalah 71.75fJ/penukaran langkah.

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LIST OF ABBREVIATION

A/D	-	Analog-to-Digital
ADC	-	Analog-to-Digital Converter
BW	-	bandwidth product
CM	-	Common Mode
CMOS	-	Complementary Metal Oxide Semiconductor
D/A	-	Digital-to-Analog
DAC	-	Digital-to-Analog Converter
dB	-	Decibel
DC	-	Direct Current
DNL	-	Differential Non-Linearity
DR	-	Dynamic Range
ENOB	-	Effective Number Of Bits
FOM	-	Figure-of-merit
IC	-	Integrated Circuit
INL	-	Integral Non-Linearity
IOT	-	Internet of Things
LSB	-	Least Significant Bit
MOSFET	-	Metal Oxide Semiconductor Field Effect Transistor
MSB	-	Most Significant Bit
NMOS	-	n-channel Metal Oxide Semiconductor
OTA	-	Operational Transconductance Amplifier
PMOS	-	p-channel Metal Oxide Semiconductor
S/H	-	Sample-and-Hold
SAR	-	Successive Approximation Register
SC	-	Switched Capacitor
SFDR	-	Spurious Free Dynamic Range
SNDR	-	Signal-to-Noise-and-Distortion Ratio

SNR	-	Signal-to-Noise Ratio
SoC	-	System on a Chip
SOI	-	Silicon On Insulator
T/H	-	Track-and-Hold
THD	-	Total Harmonic Distortion
VCO	-	Voltage Controlled Oscillator
V _{pp}	-	Volts peak-to-peak

LIST OF SYMBOLS

C	-	Capacitor
C_G	-	Gate capacitance
C_L	-	Load capacitance
C_{ox}	-	Gate oxide capacitance
dB	-	Decibel
f	-	Frequency
f_s	-	Sampling frequency
g_m	-	Transconductance
g_{ds}	-	Channel conductance
$h(t)$	-	Sampling function
I_D	-	Drain current
kHz	-	Kilohertz
K	-	Boltzmann's constant
L	-	Channel length
L_{min}	-	Minimum channel length
MHz	-	Megahertz
N	-	Number of bits
nF	-	Nanofarad
pF	-	Picofarad
R	-	Resistor
R_{ON}	-	Switch on-resistance
T	-	Absolute temperature, sampling period
t	-	Time
t_{ox}	-	Oxide thickness
τ	-	Time constant
V_-	-	Inverting Input

V_+	-	Non-inverting Input
V_{dd}	-	Positive supply voltage
V_{dsat}	-	Drain-source saturation voltage
V_{FS}	-	Full-scale voltage
V_{GS}	-	Gate-source voltage
V_{pp}	-	Voltage Peak-to-Peak
V_{ref}	-	Voltage Reference
V_{Supply}	-	Voltage Supply
V_{th}	-	Threshold voltage
W	-	Channel width
μF	-	Microfarad
μ	-	Carrier mobility
σ^2	-	Variance

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CHAPTER 1

INTRODUCTION

1.1 Introduction

Due to the advancement in fabrication technology in recent decades, transistors have become faster making possible to achieve high-rate energy-efficient digital circuits. For analog circuits the evolution of technology is not as beneficial. Besides of high speed performance and energy efficiency, there are several advantages of processing in digital domain such as storage capability, unlimited signal to noise ratio, programmability and performing complex algorithms. Thus, there is an increasing trend to perform more and more signal processing functions in digital.

Since the nature of signals needed to be processed in real world is analog, there is an increasing demand for analog to digital converters (ADCs). ADCs act as the entrance gates in digital signal processing systems. They have crucial roles in modern signal processing and communication systems because their speed and accuracy can effect on overall system performance.

Recently, the applications of ADCs have been expanded widely as many electronic systems that used to be entirely analog have been implemented using digital electronics [1]. This research is focused on high speed ADCs with sampling frequencies greater than 5 MS/sec and resolutions 10-14 bits used in many types of instrumentation (including digital oscilloscopes, spectrum analyzers, and medical imaging), video, radar, communications applications (including IF sampling,

software radio, base stations, and set-top boxes) and consumer electronics equipment (such as digital cameras, display electronics, DVDs, enhanced definition TVs).

On the other hand, during the last decade much effort has been put into the reduction of the supply voltage and the supply power of mixed signal CMOS systems. Three main reasons can be given for the necessity of low-voltage circuits. The first one comes from the continued down-scaling of device feature size. As the channel length is scaled down into submicron and the gate-oxide thickness becomes only several nanometres thick, the supply voltage has to be reduced due to reliability issues. The second reason is referred to the increasing components on chip. A silicon chip can only dissipate a limited amount of power per unit area. The last reason is dictated by portable, battery-powered equipment. One of the most effective ways to reduce active power consumption is by lowering the supply voltage [2].

However lowering supply voltage creates a number of challenges in high speed, high resolution circuit design. Unlike digital circuits and systems that have enjoyed benefits of scaling, there are some serious issues which analog circuits deal with them such as ever-shrinking signal range, lower device gain, poor matching, and increased substrate noise [3]. Since there is only comparator circuit as analog component in SAR-ADCs and there isn't any gain stage to amplify residue in SAR ADCs, this architecture is more popular among various ADC architectures for low voltage applications.

This work concentrates on low voltage SAR ADC by searching for and developing techniques and circuit structures suitable for low voltage designs. In parallel, this work also aims to achieve high-accuracy high-speed low-power design.

1.2 Problem statement

SAR ADCs are conventionally used for medium-speed medium-resolution applications as categorized as the first group of applications mentioned above. Recently, many intelligent design techniques and advances in CMOS technologies

have enhanced the conversion rate and resolution achieved by SAR architecture. However there are some issues to design high speed low-voltage SAR ADC with high resolution as explained below.

1.2.1.1 Architectural issues of SAR ADC to achieve high sampling rate

As mentioned above the most component of SAR ADC are digital circuits and digital circuits benefit from scaling technology process. Therefore it is expected that SAR ADCs, also benefit from small technology process. Figure 1.1 shows the sampling rate of SAR ADCs versus their technologies consisting of all SAR ADCs published from 1999 to 2014 from [4] and other outstanding designs from different journals such as [5-7]. As explained it is clear that SAR ADC is a compatible architecture with technology advancement.

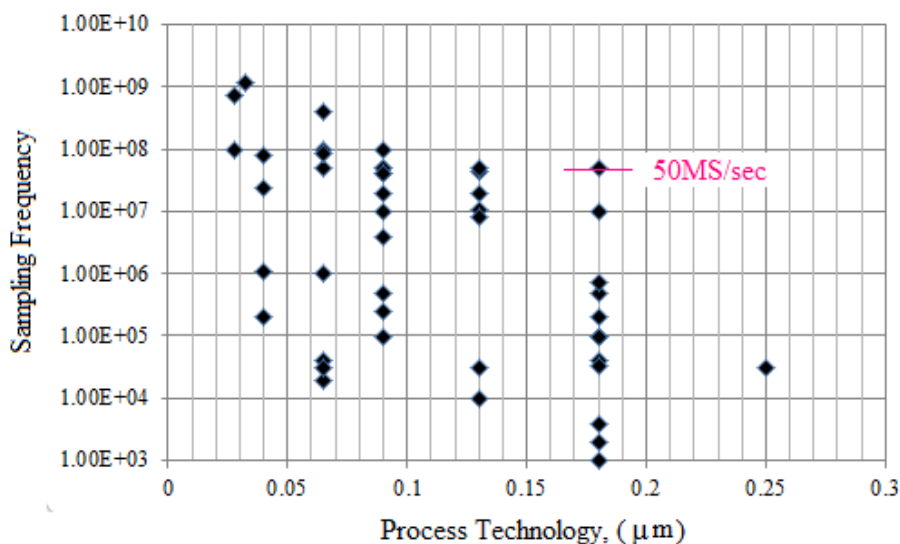


Figure 1.1 Conversion rate of SAR ADCs in different CMOS technology process [7].

Although SAR ADC benefits from technology scaling, the main limitation of this ADC to achieve high conversion rate is not related to the technology. The main obstacle to speed up the SAR ADCs is due to large capacitor- arrays consisting of a number of unit capacitors. To achieve high resolution, large size and large number of unit capacitors are needed which takes longer time to settle the comparison voltage levels in every conversion cycles [8].

Decreasing the total capacitance of the capacitor arrays is an effective solution to obtain high speed SAR ADC which can be implemented with two methods. The first method is reduction of the unit capacitor size. Since the

comparison voltage in each conversion cycle is obtained by charge redistribution in capacitor array, the ratios between capacitors determine the comparison voltage level. Therefore any mismatch between capacitor leads to errors in conversion steps and deviation from ideal I/O transfer function which is known as non-linearity effects. Therefore some extra circuits should be added for calibration or error correction. The second method to decrease the total capacitance array is by decreasing the number of unit capacitors which requires a new search algorithm or new switching methods.

1.2.1.2 Effect of lowering supply voltage on SAR ADC sampling rate

As mentioned above most SAR ADC components are digital circuits. Although down scaling supply voltage leads to decrease energy per operation in digital circuits, it causes increase in delay [9-12]. In fact power consumption is reduced at the cost of lower performance. Since changes in supply voltage affects all gates in the same way, delay of any gate remains roughly proportional to the delay of an inverter which is investigated with detail in [13]. As conclusion, as power supply voltage approximates to the threshold voltage, delay of digital cells is increased and maximum operation speed is limited.

Further SAR ADC operation is based on consecutive switching of capacitive DAC, there is another effective factor of switch conductance to determine the required DAC settling time. In real implementation, NMOS and PMOS devices are used as switches which operate on linear region like a resistor. There is a direct relation between current from drain to source, I_{ds} , of MOSFETs in ON-state and applied voltage to the gate-source connection, V_{gs} .

Since the maximum applied V_{gs} is limited to the supply voltage, supply voltage reduction results to decrease the conductance of MOSFETs. As V_{gs} is decreased, the conductance of switch is reduced which means more time is required for DAC settling. Figure 1.2 shows the conductance of switch, g_{ds} , versus V_{ds} for different V_{gs} values for an NMOS transistor of Silterra's 0.18 μ m CMOS technology. As explained above, as supply voltage reduces and $(V_{dd} - V_{th})$ decreases, digital circuit delay

increases. Hence the SAR logic unit consisting of digital circuits needs more time which means less conversion speed.

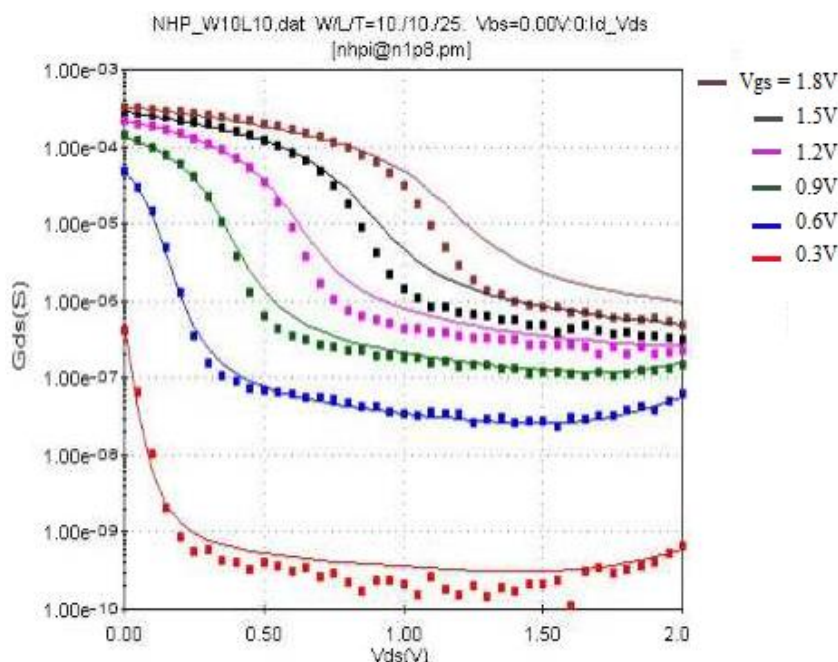


Figure 1.2 g_{ds} - V_{ds} curve at different V_{gs} for an NMOS transistor with size of $w/l=10 \mu/10 \mu$ in Silterra 0.18um CMOS technology.

Based on the above explanation, as supply voltage approximates to the threshold voltage it is expected to limit the conversion rate of SAR. Figure 1.3 shows sampling rate of SAR ADCs versus $(V_{dd} - V_{th})$ of all SAR ADCs published from 1999 to 2014 from [4] and other outstanding designs from different journals. This graph confirms that sampling rate of SAR ADCs decreases as $(V_{dd} - V_{th})$ reduces.

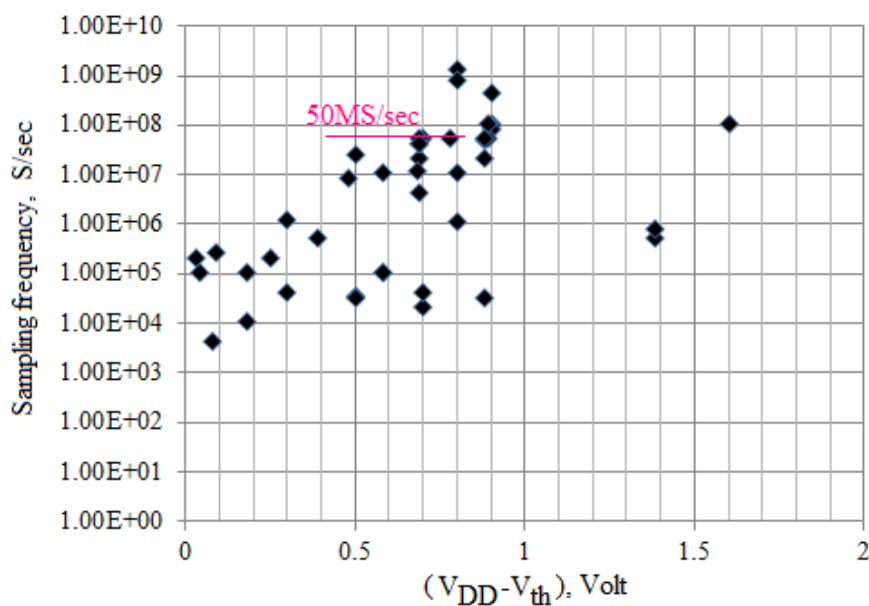


Figure 1.3 Conversion rate of SAR ADCs in different CMOS technology process versus $(V_{dd} - V_{th})$ (from 1997 to 2014) [7].

1.2.1.3 Sampling switch issues

The low supply voltage inherently limits the maximum input signal swing of an ADC, and thus may lead to a poor peak signal-to-noise ratio (SNR). To achieve higher accuracy and higher signal to noise and distortion ratio (SNDR), it is better to have larger input range which is limited to the power rails. However rail-to-rail input leads to the difficulty of circuit design (especially analog parts) in rail-to-rail condition.

The sampling switches as the input gate of SAR ADC has an important role in determining the overall performance. MOSFET transistor is a natural switch which is extensively used in S/H. However there are several issues (such as charge injection [14] , clock feed through, MOS transconductance variation [15-17] , body effect [18-23]) which are exacerbated for low voltage rail-to-rail condition. By considering the limitation of maximum tolerable voltage for gate-source connection of MOSFETs, tracking rail-to-rail input voltage is not possible with a simple MOSFET switch. Furthermore, in comparison to input signal range, threshold voltage variation is not negligible and causes nonlinearity effect on “ON” state switch resistance [14, 24, 25]. To achieve high-speed high-resolution ADCs, high-resolution high speed switches are needed.

Although there are some techniques to boost the V_{gs} and make it signal independent, final achieved V_{gs} value is a function of V_{dd} , too. Thus lowering supply voltage means restricting the band width of switches performances, too. The techniques mentioned above are discussed and analyzed more deeply in the following chapters.

The above mentioned issues to enhance the conversion rate of SAR ADCs and additional difficulties resulting from lowering supply voltage call for research work to design proper circuits, concentrated on rail-to-rail low voltage designs, and finding new methods for enhancing SAR-ADC characteristics at this condition.

1.2.1.4 Metastability error of comparator

One of the comparator error which is known as metastability error is a degrading factor in SAR ADC performance. Metastability is a problem that occurs in

all latching comparators as the output does not saturate to valid regions of logical one or zero during comparison time. Since the conversion process of SAR ADC is a serial operation, any error in output of comparator in each cycle penetrates to the remind process without any chance to get back and doing correction. Although there are some techniques to solve this issue, but most of them are not suitable solutions for low voltage applications due to the required analog components. Further investigation of metastable error besides of incomplete DAC settling shows more research work is required to develop current solutions or find new approach.

1.3 Objectives

This PhD thesis focuses on design of a rail-to-rail low voltage SAR ADC in 0.18 μ m process CMOS technology. By taking into account the aforementioned problem statements, the following objectives are the main concern of this research.

1. To investigate non-linear effect of capacitor mismatch and effective methods to control it.
2. To implement the design using a small power supply voltage of 1.2V.
3. To enhance SAR-ADC conversion speed higher than 50MS/sec.

1.4 Scope of work

The scope of this research is as explained below:

- Investigation capacitor mismatch:

Capacitor mismatch is an inevitable issue of capacitive DAC arrays and all SAR ADCs suffer from this issue beyond their used technologies and applied supply voltages. Thus investigation of capacitor mismatch and finding a model consisting of all effective factors to control the resulted nonlinearities in converter performance is within the scope of this research.

- Proposing a new switching algorithm

Since the mismatch requirement and switching algorithm determine the size and number of unit capacitors in SAR ADC, a switching algorithm is developed to decrease the number of unit capacitors without damaging the linearity of performance.

- The choice of process technology and supply voltage

When we look at the new application areas where we see the future wave of sub stream innovation happening such as medical and wearable's, IoT, ... we see that it is not necessarily needed to use the most advanced technologies such as 28nm [26]. The chosen technology for this work is 0.18um CMOS technology process which is the most popular and commercial technologies in the last decade [26-28]. Now the main challenge in this mature technology is enhancement of energy efficiency which is studied through circuit architecture development and decreasing the supply voltage [6, 7, 29-32]. According to the shown supply voltage margin reduction in [33], 1.2 volt is considered as the supply voltage.

- Development of conversion rate

CMOS technology and supply voltage in this work are 0.18 μ m and 1.2V, respectively. As shown in Figure 1.1, the maximum achieved conversion rate in 0.18um technology is 50MS/sec in [6, 7]. Further $(V_{dd} - V_{th})$ is a value between 0.6V and 0.7V which the maximum achieved conversion rate is 50MS/sec as shown in Figure 1.3. The highest speed converters in this range are 9-bit with 40MS/sec and two 10-bit ADCs with 50MS/sec in 90nm, 65nm and 0.18um technologies, respectively [6, 34, 35]. The goal of this work is to achieve conversion rate higher than 50 MS/sec.

- Development in sampling switch design

The sampling switches as the fundamental block are investigated at low supply voltage. Some solutions are proposed to enhance their performance.

- Development in metastability solution

A new development in correction method for metastability error is proposed which is useful for incomplete settling of DAC output voltage, also.

1.5 Contributions

In this thesis, two SAR ADCs are presented with 5 contributions which are listed below. The main contributions lead to improve the conversion rate and linearity performance of SAR ADCs at low supply voltage, energy efficient condition.

1. Nonlinear effect of capacitor mismatch on SAR ADC performance is investigated which leads to the development of a new model of capacitor mismatch on capacitive-DACs. Based on the new model, effective factors to control the non-linear effect of capacitor mismatch are determined.
2. From the achieved results from the above mentioned investigation, a new Tri-level switching algorithm is proposed to reduce the matching requirement for capacitors in SAR ADCs. The integral non-linearity (INL) and the differential non-linearity (DNL) of the proposed scheme are reduced by factor of two over the conventional SAR ADC which is the lowest compared to the previous schemes. In addition, the switching energy of the proposed scheme is reduced by 98.02% as compared with the conventional architecture which is the most energy-efficient algorithms in comparison with the previous algorithms, too.
3. Nonlinear effect of parasitic capacitors on split SAR ADC performance is investigated and a new error correction method is proposed to improve its performance. In the proposed method, the maximum possible error is measured before the ADC starts the conversion process. Since this error is negative, it is injected to the DAC array by pre-charging the LSB array during MSB conversion phase. After complete the conversion process, an error correction is applied through MATLAB software. Differential nonlinearity (DNL) of ADC before compensation is within -1LSB and $+4.3\text{LSB}$ which is restricted to

-0.9LSB and +2.8LSB after applying compensation. Also, integral nonlinearity (INL) of ADC before compensation is within -4.4LSB and +5.3LSB which is restricted to -2.5LSB and +2.7LSB after applying compensation.

4. One of the comparator error which is known as metastability error is a degrading factor in SAR ADC performance. A new development in correction method for metastability error is proposed which is useful for incomplete settling of DAC output voltage, also.
5. A new optimized CMOS switch is proposed consisting of a bootstrapped NMOS switch and a boosted PMOS switch as a transmission gate. By utilizing this technique, the nonlinearity resulting from the threshold voltage variation (body effect) of NMOS switch is mitigated, considerably, compared to standard CMOS switch or a bootstrapped NMOS switch.

1.6 Thesis Organization

The rest of the thesis is organized as follows.

Chapter 2 reviews the successive approximation structure and its positive and negative characteristics. This chapter is followed by introducing the previous solutions and designs in terms of search algorithms and switching schemes in the published high-performance SAR ADCs. After review of conversion process and algorithms, the metastable state of comparator and conventional solution is introduced. At the last part of this chapter a review on sampling switches, which is subjected to develop in this thesis, is presented.

Chapter 3 presents research methodology of this research. At first, analysis of nonlinear effect resulted from capacitor mismatch is discussed. Then the proposed switching algorithm is presented with its performance details in aspect of linearity and energy consumption. Next the first ADC design which is based on the presented algorithm is explained. For the second ADC design split architecture is combined

with the new algorithm. This section is followed by investigation of nonlinear error from parasitic capacitors. The presented investigation is a way to reach the proposed correction method.

Chapter 4 presents the circuit design details and layout preparation. This chapter starts with the proposed sampling CMOS switch which acts as entrance gate of ADC. The circuits of comparator, clock generation and output buffers are presented at the following of this chapter. At the second part of this chapter layout of the second ADC is exposed and discussed.

Chapter 5 exposes the achieved results from simulation of each circuit. The simulation condition applied to the designed ADCs is discussed which is followed by simulation results of both designed ADCs. Finally, the performances of designed ADCs are compared with previous published works.

Chapter 6 concludes the research findings. Recommendations for future works are also addressed to assist other researchers in pursuing the works for further development and improvement.

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