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Quantitative Power Loss Analysis and Optimisation in Nth-order Low Voltage Multilevel Converters

Alexander Petersen [1*], David A. Stone [1], Martin P. Foster [1], Jonathan N. Davidson[1]

[1] Electrical and Electronic Engineering, University of Sheffield, 3 Solly Street, Sheffield, S1 4DE, UK
[*]apetersen1@sheffield.ac.uk

Abstract: Focusing on cascaded H-bridge converters for grid-tie battery energy storage, a practical, analytical method is derived to evaluate the switching-associated power loss in multilevel converters, evaluated from a number of sources of loss. This new method is then used to find performance trends in the use of converters of increasing order over a range of switching frequencies. This includes an experimental analysis into predicting the performance of MOSFET body diodes. Our analysis with this model shows that a multilevel converter can have lower losses than the equivalent single bridge, three-level converter, particularly at higher switching frequencies, due to the availability of suitable switching devices. It also has interesting implications for enabling the use of cutting-edge non-silicon power switching devices to further improve potential efficiencies.

1. Introduction

Multilevel converters today are used almost exclusively in applications where devices simply do not exist with suitable ratings, such as high/medium voltage converters. Existing literature has discussed the benefits of multilevel converters for a range of other, lower voltage applications. This paper seeks to answer the question of how many levels is too many – a topic notable by its absence from the literature. Of particular interest to the authors are the potential benefits found through the use of multilevel converters in bidirectional grid-tie battery energy storage systems – an emerging application which promises to grow dramatically as public policy favours low carbon intelligent energy systems [1].

The use of, specifically, cascaded H-bridge multilevel converters in grid energy storage applications can not only permit the converter to do much of the work that would normally be performed by a separate battery management system (BMS) [2-4] such as cell or string balancing, but can enable the use of heavily degraded or second life battery packs by dynamically favouring degraded strings [5, 6]. Battery storage is also particularly suited to the use of multilevel converters due to the easy creation of split DC voltage sources through separating battery packs into smaller strings, thereby avoiding the need for large capacitors to split a main DC supply or multiple DC supplies.

That is not to say that multilevel converters are only suitable for battery energy storage applications – far from it. Their use in motor drives, for example, is also the subject of a significant body of research [7-10]. The benefits in this application are significant reductions in total harmonic distortion [7, 8, 10] as well as reduction in overall noise [9].

The number of levels used in the converters that feature in the cited literature, which covers both physical prototypes and simulation, vary significantly: from as low as 5 levels [8] to as many as 19 levels [6]. In all of these publications and throughout the field, the research focusses on the specific benefit that a multilevel converter can have in the given application without justifying the number of levels used. A pragmatic design engineer must ask themselves, "how many levels should the converter have?" but current research provides little guidance on how to make that decision.

This research aims to bridge the gap between academic observation and commercial justification, by answering this important question. While it is a complex and application-specific question, this paper tackles the issue from the perspective of power loss associated with the switching devices. Unlike other cutting-edge power converter optimisation methods [11], there is a focus on the creation of a practical method, while still minimising loss in model precision.

This paper differs from other multilevel optimisation research as in mainstream multilevel converter applications the number of levels is dictated solely by the ratings of the best devices and the voltage being switched across. As such, optimisation in these fields focusses in other areas, such as modulation strategy [12] or size of DC link [13]. Unfortunately, this existing body cannot be used in this paper due to the significantly lower voltage range.

Existing power loss analysis research is also found lacking as it either fails to use practical methods for finding parameters [14,15], doesn't define the loss model at all [16], or does detailed analysis of a highly idealised model [17].

2. Method

A large dataset of power switching devices (specifically silicon MOSFETs) was assembled to evaluate the trends in converter performance under a range of conditions. These devices were selected to represent a cross-section of devices with sufficient current rating – from low to high voltage rating and from the contemporary to the somewhat dated. Over a range of switching frequencies and number of cascaded bridges in the converter, the total power loss for every device with a sufficient drain-source voltage and drain current rating is evaluated. The device with the lowest total loss is the best device choice for that converter.

As a benchmark reference for development, and to provide a focus to the research, we use a typical converter specification. The specification is for a single-phase bidirectional grid-battery interface for use in a domestic setting. The multilevel converter technology in use will be

the cascaded H-bridge topology, an Nth-order example being shown in figure 1, which enables string balancing for grid-attached energy storage applications. The method shown in this paper can be easily applied to other specifications or multilevel converter topologies as required. The design specifications of the reference converter are:

- 230V 50Hz grid connection (UK and EU standard),
- 500V nominal DC link voltage (while unusually high, overhead is required for bad string avoidance [5, 6]),
- 6kW power capacity (akin to a high power domestic electric vehicle charger with vehicle-to-grid connection).

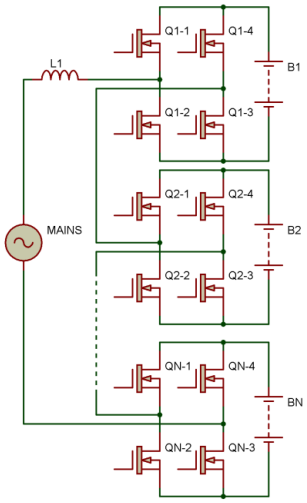

Fig. 1. A circuit diagram of an Nth-order cascaded H-bridge multilevel converter for grid-tie battery energy storage applications.

To derive a good comparative metric for loss in these converters, each source of power loss is considered in turn and evaluated. The sources of loss considered are:

- on-state resistance (section 2.1),
- transient loss in the gate (section 2.3),
- transient drain-source or 'output' loss (section 2.4),
- transient and quiescent gate driver losses (section 2.5-7)
- power loss in the diodes (section 2.8).

The derivation of these is considered in turn.

2.1. On-state resistance

All power field effect transistors (FETs) have a finite on-state resistance between drain and source, $R_{DS,ON}$. This is the dominant source of loss in many applications, particularly at low switching frequencies. This figure is readily available on datasheets for any device, but varies with temperature. To better approximate the true resistance found in operation, the on-state resistance at TJ=80°C was extracted from the datasheet.

The total on-state resistance is related to N, where N is defined as the 'order' of the converter; that is, the number of cascaded bridges. It is distinct from the number of voltage levels available from the converter, n. These quantities are related, however, as n = 2N+1. If one neglects the dead time and switching time (a reasonable approximation for calculation of resistive on-state loss), then the current, I_{RMS}, flows through two power FETs in each bridge, and therefore $R_{TOTAL} = 2NR_{DS,ON}$. So the expression for total power loss due to on-state resistance is:

$$P_{R_{DS,ON}} = 2N{I_{RMS}}^2 R_{DS,ON} \quad (1)$$

2.2. Capacitance Variation Estimation

Many of the subsequent methods depend upon precise knowledge of the capacitance between the various terminals of the devices; for example, in the integrals in (2), (3) and (5). However, these capacitances vary significantly with the drain-source voltage experienced by the device. This relationship is highly non-linear, and bears little pattern from device to device. Figure 2 shows the capacitance curves for three different devices, showing the input capacitance, C_{iss}, the output capacitance, C_{oss}, and the feedback capacitance, C_{rss}.

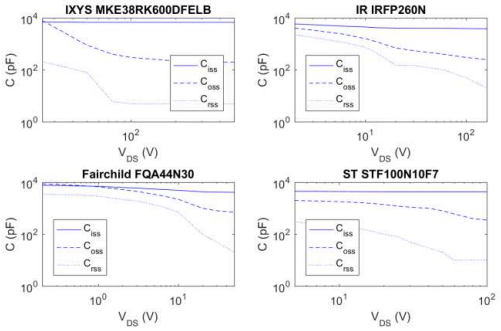

Fig. 2. Comparison of a number of MOSFET capacitance curves, showing how they vary with respect to the drain-source voltage, V_{DS}.

Due to the emphasis on producing a practical analysis and design methodology, the data entry required to copy these curves is prohibitive. Optical character recognition methods were investigated to allow automated datasheet information extraction, but the lack of consistency in data provided and the very poor quality of the plots on some datasheets made this almost impossible. As a result, a simplifying linearised approximation was made.

Both C_{oss} (output capacitance) and C_{rss} (feedback capacitance) are approximated by an initial linear region, becoming flat after a chosen voltage threshold, the approximation is therefore fully defined by three values: the maximum capacitance, the minimum capacitance and the voltage at which the minimum capacitance is to be evaluated. Meanwhile, C_{iss} (input capacitance) approximated as a constant value. Figure 3 shows a pair of graphs comparing the actual capacitance curves of two devices with their corresponding linearised approximation. Based on figure 3, the linearising approximation appears adequate, but the important thing is how the integral with respect to voltage compares between the real data and the estimation.

To validate this approximation the precise datasheet information was compared to the linearised approximation

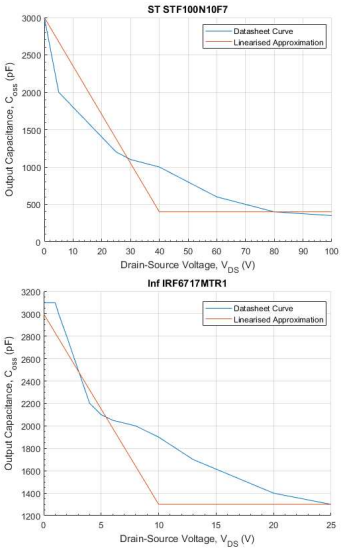

Fig. 3. The linearised approximation plotted alongside the precisely extracted datasheet curves displayed on linear axes for two devices.

as well as an experimental series for a small subset of the devices listed in Appendix A. The linearising assumption induces error in estimation of the Miller charge with a standard deviation of 26% relative to the precise datasheet curves. However, the precise curve estimation has a standard deviation in error from experimental results of 40%, so the error between the precise datasheet information and the linearised approximation is small when compared to the error between the precise datasheet information and the experimental results. We are therefore content to rely on the linearising assumption.

2.3. Transient Loss in the Gate

This is a measure of the power dissipated in the gate of switching devices in the power converter and is found by estimating the charge-voltage curve during turn-on, which is related to the energy lost at the gate during a single cycle by:

$$E_{GATE} = \int_0^{\Sigma Q_G} V_{GS}(Q_G) dQ_G \quad (2)$$

The gradients of the curve in figure 4 from 0 to Q_1 and from Q_1+Q_{MILLER} to ΣQ are easily derived from the device datasheet, as they can be determined from the input capacitance, C_{iss}. C_{iss} varies with respect to the drain-source voltage, V_{DS}, but a linearised approximation of this relationship (and other capacitance-voltage curves) is taken from the datasheet for every device. In the case of C_{iss} specifically, it is treated as a constant value with respect to the drain-source voltage, which is a good approximation according to device datasheets.

The flat region in the centre of the plot in figure 4 is known as the Miller shelf. Here, the gate-source voltage remains constant while the transistor turns on, during which time the gate-drain capacitance charges through the gate. The Miller charge is calculated from the integral of the drain-source capacitance, also known as the feedback capacitance or C_{rss}, with respect to the drain-source voltage. As such, the Miller Charge is (non-linearly) correlated to the maximum drain-source voltage across which the device is switching. The relationship between C_{rss} and V_{DS} is again approximated by the linearised relationship described in section 2.2.

The calculations are further complicated as the maximum drain-source voltage, $V_{DS,MAX}$, varies sinusoidally with time as a result of the AC grid connection. This must be accounted for, as shown in (3).

$$Q_{MILLER,AV}(V_{DS}) = \frac{\int_0^{\pi/2\omega} Q(V_{DS,MAX}\sin(\omega t))dt}{\pi/2\omega}, \omega = 2\pi f_{mains} \quad (3)$$

The voltage at which the Miller shelf occurs, labelled in figure 4 as the plateau voltage, $V_{PLATEAU}$, is approximated from information available on datasheets. Only a small number of datasheets provide a figure $V_{PLATEAU}$. In other cases, $V_{PLATEAU}$ is estimated as 150% of the threshold voltage, a figure available for all devices. The accuracy of this estimation was tested for a set of one in ten devices (eight devices in total) selected over a range of voltage ratings from the full set found in Appendix A. The standard deviation of error was 8%, with the outliers at no more than 20% - so this estimation was deemed reasonable.

With the charge-voltage curve calculated, and, by extension, the energy dissipated in the gate in a single switching cycle (2), it is trivial to extend the energy dissipation calculation to the total power dissipated into the gates of the FETs throughout the converter. Since only one bridge switches at any one time and each of the four FETs in the H-bridge goes through a turn on once per cycle, the total power dissipated in the gates is:

$$P_{GATE} = 4E_{GATE} \times f_{switching} \quad (4)$$

2.4. Transient Output Loss

Output loss is the power that is expended in charging the capacitance between the drain and the source, Coss, during turn on and turn off. The energy dissipated during a single event is given in (5).

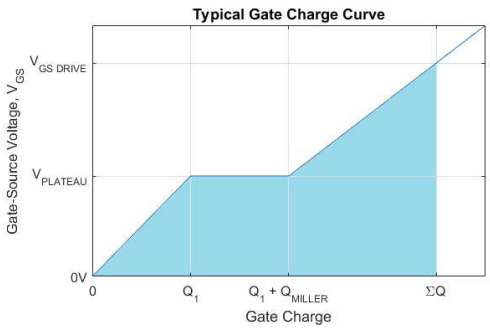

Fig. 4. A typical MOSFET gate charge-voltage curve, with some key values annotated.

$$E_{OUT} = \iint_0^{V_{DS,MAX}} C_{oss}(V_{DS}) d^2 V_{DS} = \int_0^{V_{DS,MAX}} Q_{oss}(V_{DS}) dV_{DS} \quad (5)$$

However, as VDS is sinusoidally time varying, (5) needs to be adjusted accordingly in a similar fashion to (3):

$$E_{OUT,AV} = \frac{\int_0^{\pi/2\omega} E_{OUT}(V_{DS,MAX} \sin(\omega t)) dt}{\pi/2\omega}, \omega = 2\pi f_{mains} \quad (6)$$

This capacitance-voltage relationship is, again, non-linear and inconsistent from device to device, but can be approximated using a linearised relationship outlined in Section 2.2. The total power can be calculated from the single switching event loss according to (7), noting that loss occurs during turn-off as well as turn-on:

$$P_{OUT} = 8E_{OUT_{AV}} \times f_{switching} \quad (7)$$

2.5. Gate Drive Dissipation

A generic gate drive was modelled to derive an expression for loss in the gate drive. Figure 5 shows the model used, with M1 being the power FET. The labels 'SYSTEM A' and 'SYSTEM B' shown in figure 5 denote where the main power FET connects to the rest of the converter. For simplicity, an optocoupled solution with an isolated DC-DC converter was used instead of a transformer isolated gate drive. The losses in a transformer isolated gate drive would be different, but the overall effect on converter loss is unlikely to be large. This simplification does not affect the validity of the comparative results of this research, but it serves as an example of a way in which the exact figures produced vary according to design decision.

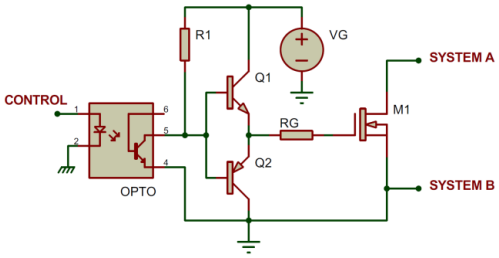

Fig. 5. A Circuit diagram of the gate drive model

Losses in the gate drive are separated into two parts: transient loss and quiescent loss.

2.5.1. Transient Gate Drive Dissipation

Transient gate drive loss is calculated with reference to figure 4. The highlighted area under the curve is the energy dissipated in the gate, E_{GATE}, while the product of the drive voltage and the total charge is the total energy being put in by the gate drive. Therefore, the transient energy lost in the gate drive, i.e. the area above the curve bounded by the gate drive voltage, is the difference between the two:

$$E_{DRIVE,T} = \left(C_{iss} V_{GS,DRIVE} + Q_{MILLER,AV}\right) \times V_{GS,DRIVE} - E_{GATE} \quad (8)$$

To calculate power loss, energy is then multiplied by four, for each switching device operating during a switching cycle, and multiplied by the switching frequency. Equation 9 also incorporates η, which is a measure of efficiency of the isolated DC supply for the gate drive, VG in figure 5, which, while load dependent, a typical value of 75% was found in datasheets.

$$P_{DRIVE,T} = 4E_{DRIVE,T} f_{switching}/\eta \quad (9)$$

2.5.2. Quiescent Gate Drive Dissipation

To calculate the quiescent power dissipation in the gate drive circuit, the peak current requirement of the driver must be evaluated. To find peak current requirement, the maximum time to perform a single switching operation must be found because faster switching requires higher peak driver current.

The turn-on behaviour of a MOSFET is show in figure 6a. The device has turned on by time t_2. The time

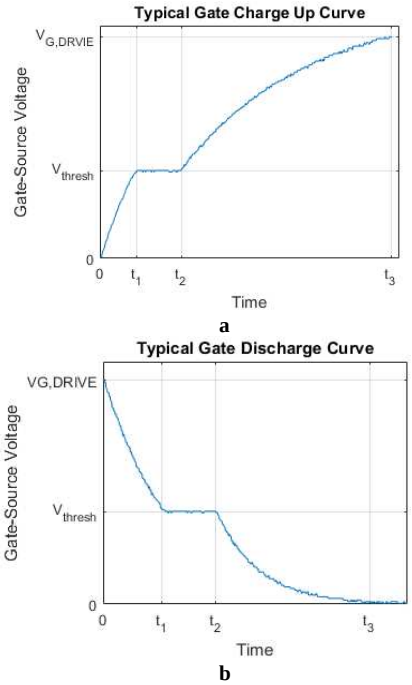

Fig. 6. A plot of the turn-on **(a)** and turn-off **(b)** behaviour of a typical MOSFET with respect to time, labelled with key values. This is real world data for the Fairchild FCH47N60.

before t_1 is an exponential relationship dictated by between the input capacitance C_{iss} and the gate resistance R_g. Between t_1 and t_2 is the Miller Shelf. As part of the gate dissipation calculations, the Miller Charge has already been calculated, and with a given plateau voltage and gate resistance the time can too be found.

During the period 0 to t_1 there is a classic resistor-capacitor exponential charge between C_{iss} and R_G, and in the period t_1 to t_2 the voltage is fixed. The expressions in these two periods being:

$$t_{ON} = t_1 + t_2,$$
$$t_1 = -\ln\left(1 - \frac{V_{PLATEAU}}{V_{GS,DRIVE}}\right).C_{iss}.R_g,$$
$$t_2 = \frac{Q_{MILLER}.R_g}{V_{PLATEAU}} \quad (10)$$

Maximum switching time is calculated from the resolution of the PWM occurring and the fundamental switching frequency of the converter. For instance, if the converter is running at 100kHz switching frequency with 8-bit PWM, the minimum time base is $T/2^8 \approx 40$ns, where T is the minimum time increment possible for an 8-bit PWM clock. An estimation of how hard the devices must be driven to attain this speed is then easily derived from information readily available about the device and the application. However, this method proved too restrictive, as many devices that should have been capable were deemed to be too slow – therefore the switching period constraint was relaxed. This results in a more reasonable design constraint but at the cost of slightly higher harmonic distortion.

The relationship between slower turn on/off and the increased harmonic distortion was investigated in literature both from the perspective of grid-tie inverter technology [18-20], but also from the perspective of switching time and dead time related harmonic distortion in class D amplifier design [21,22]. This yielded no feasible method for predicting the harmonic distortion in a generalised case.

Increasing the switching period constraint by a factor of three was found to yield credible results with respect to devices being capable of high switching frequencies or not, so a threefold factor was applied to the previously outlined method. This is a worthwhile compromise for the generation of this generalised, comparative metric.

Equation (10) shows how to calculate the turn-on time. The turn-off time is computed similarly, though as can be seen in the discharge curve in figure 6, t_1 will be different due to a larger voltage swing occurring. The edge condition for this being:

$$(t_{ON} + t_{OFF}) \times (1.2 \times t_{dead}) = \frac{3}{f_{switching} \times 2^{N_{PWM\ res}}} \quad (11)$$

The sum of turn-on and turn-off time, t_{ON} and t_{OFF}, with the addition of the dead time, t_{dead} (inflated by 20% as a safety margin), permits the calculation of the require gate resistor, R_g (see figure 5). The peak current requirement of the gate drive is then calculated from the gate resistor R_g and the peak drive voltage $V_{GS,DRIVE}$, i.e. $I_{MAX}=V_{GS,DRIVE}/R_g$.

To calculate the quiescent loss of the gate driver from the peak current requirement requires inspection of the circuit diagram in figure 5. A key source of quiescent loss is R_1, its value being related to the gate resistor by the gain of the main drive transistors Q_1 and Q_2. For example, if Q1 and Q2 were to have a nominal current gain of 100, R_1 would be 100 times the size of Rg. The quiescent power loss in that resistor would then be the $P_{R1}=V_{GS,DRIVE}^2/R_1$.

There is also quiescent loss in the isolated DC-DC converter. While every device is a little different the loss tends to be approximately 15% of rated output - this is included in the loss estimation also. Furthermore, losses in the opto-isolator are due to the infrared LED inside, with drive current as high as 30mA [23]. Knowing that the LEDs in each gate drive are on half of the time, and the drive voltage (taken as 5V here), this source of quiescent gate drive loss can be quantified.

While quiescent loss in the gate drive is reasonably small and is understandably often neglected in the design of a converter, for multilevel converters of high order these small sources of loss add up. For example, with four gate drives in each bridge, and with up to 25 cascaded bridges considered in this method, that is quiescent loss in as much as 100 gate drives.

2.6. Diode Loss

To Loss in diode conduction is to be evaluated, considering both forward- and reverse-conduction using both the body diode and external high performance diodes. High performance switching diodes have little or no reverse recovery, but are permanently in the conduction path, thereby adding loss. Use of the body diode avoids this additional burden in the conduction path but will have inferior recovery performance. Information on the performance of body diodes is limited, however.

The goal was therefore to find a method that permitted estimation of the relevant characteristics for the body diode based on data that is available for the device. A literature review yielded nothing relevant, with existing research focusing on 'in-depth' experimental analysis of specific devices and die-level modelling rather than deriving trends from available information.

An experimental investigation was conducted where the body diodes of a number of MOSFETs (see Appendix B) were characterised, and the parameter trends with respect to maximum drain-source voltage rating and maximum continuous drain current (T_J=80°C) rating were evaluated.

To decide upon the quantities to be measured during this characterization, the model for loss must be considered. The model consists of two parts:

- power loss due to free-wheel conduction while all four switching devices in a bridge are off,
- power loss as the diode experiences reverse recovery.

To facilitate these calculations, the I-V curves were traced and the reverse recovery charge, Q_{rr}, was measured.

I-V curves were traced using a Keithley 2612A sourcemeter up to a sufficiently high current to enter the ohmic region. As a result, the diode was modelled as forward voltage drop with a series resistance. This is a reasonable approximation as the behaviour of the diode near its conductance threshold is unimportant to the loss model, as it will not operate there.

Reverse recovery charge was measured using a custom testing platform which rapidly transitions a diode from forward biased to reverse biased and measures current flow over time during the reverse recovery period. These

tests were performed on a set of 60 devices with a range of current rating and voltage ratings (see Appendix B), after which the data was analysed to find the trends in the data. The best fit between performance and voltage and current rating was found and is documented in equations (12)-(14). While these predictions have some error, with a standard deviation as high as 0.8 of the mean, they offer a method for calculating a first order approximation of body diode performance.

$$\log_{10}(Q_{rr}(nC)) = 0.863\log_{10}(V_{DS,MAX}(Volts)) + 0.585\log_{10}(I_{D,MAX}(Amps)) - 2.139 \quad (12)$$

$$V_{D,FWD}(Volts) = -0.0659\log_{10}\left(I_{D,MAX}(Amps)\right) + 0.754 \quad (13)$$

$$R_{D,ON}(Ohms) = 0.0303\log_{10}\left(V_{DS,MAX}(Volts)\right) + 0.0746 \quad (14)$$

Calculating energy dissipated in the body diodes during dead time is trivial, as RMS system current and dead time already having been defined, also accounting for two diodes conducting in the bridge every cycle.

$$P_{D,dead} = 2I_{RMS}V_{D,fwd} \times t_{dead} \times f_{switching} \quad (15)$$

Energy dissipation during reverse recovery is more complicated to evaluate. It occurs as a result of a pulse of current that passes through the bridge across the DC link, the diodes permitting back conduction and effectively shorting the bridge until the reverse recovery charge is depleted.

While there is a more exhaustive method that permits calculating the power dissipation in each element of the system (diode, FET or DC link) which does depend on numerous parameters such as battery resistance and inductance, only total power dissipation during diode reverse recovery is relevant in this study. The total diode reverse recovery energy is the product of the reverse recovery charge and the voltage across the link (16).

$$P_{D,RR} = 2Q_{RR} \times \frac{V_{DC}}{N} \times f_{switching} \quad (16)$$

A separate pair of high performance Schottky (or at least rapid recovery) diodes – one in series with the MOSFET and one in parallel for free-wheel – is commonly used as an alternative to the body diode. These external diodes assure negligible power loss due to reverse recovery, at the expensive of placing two diodes in the conduction path for each bridge. This means that, in a high order converter, the benefit of using the separate diodes in terms of reverse recovery performance may be outweighed the cost in terms of power loss of the numerous series diodes in the conduction path otherwise.

Calculations for the use of high-performance external diodes are easier due to the lack of reverse recovery, but it must include the power dissipation due to additional diodes placed in the conduction path. The diode considered for these calculations was the Vishay ETH3006 hyperfast-recovery 30A power diode.

3. Results

3.1. Silicon Devices

As outlined at the beginning of section 2, all the loss estimations will be combined to give a figure for total loss, and then the device with the lowest total loss is found for a given set of conditions. Initially, only silicon power MOSFETs are considered. Figure 7 shows the resulting optimal devices for a range of converter order values at a switching frequency of 10kHz, representative of a low but credible switching frequency (many modern, higher power rated converters may run as low as 4kHz). The total bar height shows the total power loss for the optimal device selected, the far left of these points being for a converter consisting of a single H-bridge, with multilevel converters of increasing order towards the right of the figure. The contribution of the specific sources of loss are represented by the colour-coded bar breakdown.

Perhaps surprisingly, our analysis shows multilevel converters can have lower total loss than a conventional single full bridge despite having many more devices. At the relatively low switching frequency of 10kHz, on-state resistance dominates the loss in the converter due to fewer switching operations occurring per unit time, and lower rated voltage devices that may be used in higher order have sufficiently lower on-state resistance that total resistance in the conduction path is lower despite there being many more devices in series. In figure 7, for example, the lowest loss is achieved with ten cascaded bridges making it optimal in that regard.

Figures 7-9 also have a cost value (online unit cost for medium volume of some 500-2000 units in pounds sterling in November 2016) representative of only the total cost of the MOSFETs in use in the converter; construction, passive component and gate drive costs are neglected. It shows not only that power dissipation can be lower, but device cost need not be much higher and, indeed, is sometimes lower. Cost is not a parameter in the optimisation due to the difficulty in evaluating the total system cost from arbitrary parameters.

Figures 8 and 9 show the same type of relationship as figure 7, but at switching frequencies of 80kHz in figure 8 and 600kHz in figure 9. The maximum power dissipation in the converter for under any optimal condition at 10kHz is approximately 80W, whereas the at 80kHz it is above 120W and at 600kHz it is almost 450W. This is not unexpected, as, with more switching operations per second, there is more energy to be dissipated per unit time from almost all sources (except on-state resistance and quiescent losses).

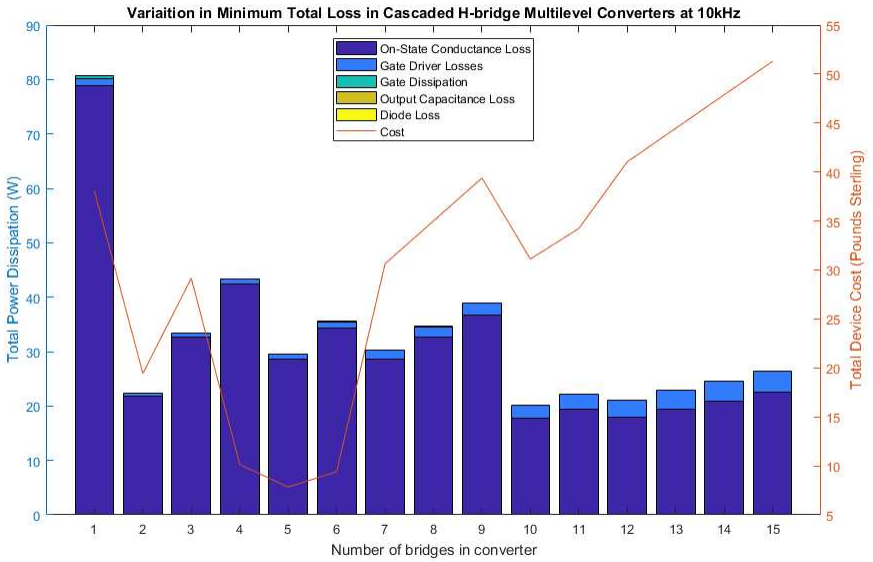

Fig. 7. Minimum losses displayed as both a total value and its component parts, with respect to increasing number of cascaded H-bridges at fs=10kHz.

The results at 80kHz (in figure 8) have similar implications to those at 10kHz (in figure 7), namely that a single H-bridge is not the lowest loss solution. All result sets have the same distinctive discontinuities because lower voltage rated devices become viable with higher order multilevel converters. In the 80kHz case, like the 10kHz case, the on-state resistance still dominates, and while not to as great an extent, most of the optimal devices remain the same form 10kHz to 80kHz. Transient output loss and gate dissipation in all cases is very low - the only devices that have significant loss in these areas are some older, higher voltage rated devices that are quickly optimised out, particularly at higher switching frequencies.

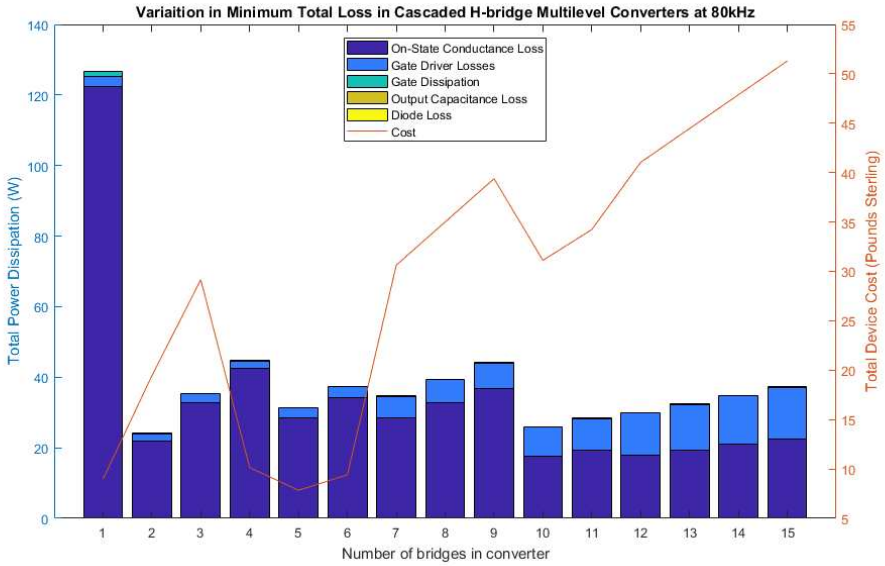

Fig. 8. Minimum losses displayed as both a total value and its component parts, with respect to increasing number of cascaded H-bridges at fs=10kHz.

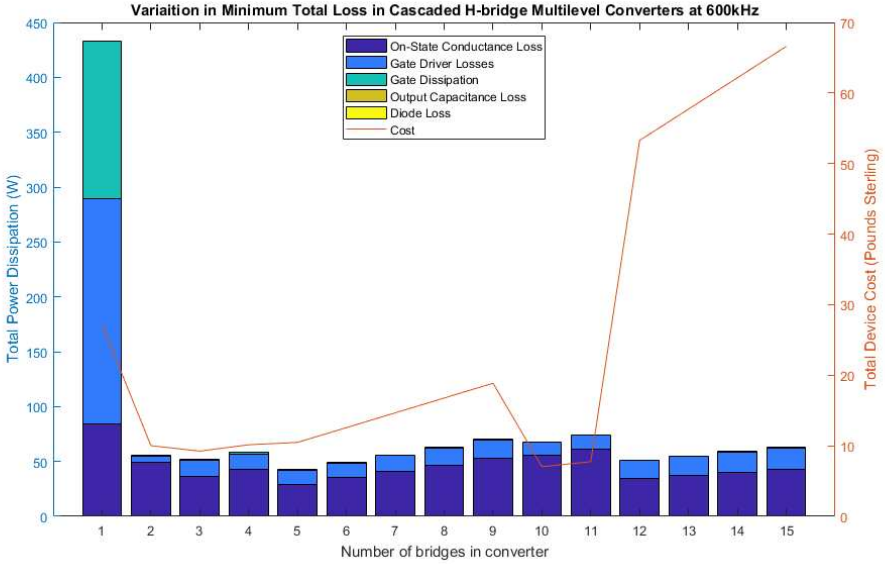

Fig. 9. Minimum losses displayed as both a total value and its component parts, with respect to increasing number of cascaded H-bridges at fs=600kHz.

Figure 9 shows a more extreme case in terms of high switching frequency and has a notable outlier at the single H-bridge mark, with vastly greater power dissipation than any other case. The device in question, the STMicroelectronics STW62N65M5, would require a very high performance heatsink to avoid thermal destruction. This demonstrates that multilevel converters can be much more practical at higher switching frequencies. While operating at higher switching frequency does have a detrimental impact on converter efficiency, with higher loss across the board at 600kHz than 10kHz, it could enable the construction of much smaller converters with much reduced filtering requirements for noise injected in to the power network.

Interestingly, under all conditions shown, the optimal solution was the use of the body diode rather than external high-performance diodes. This is thanks to the significant power loss in the multiple diodes (two per bridge) in the conduction path at any one time in the use of external, high-speed diodes. The power loss due to diode reverse conduction during recovery and worsened free-wheel performance in the use of body diodes is smaller, even at lower converter order.

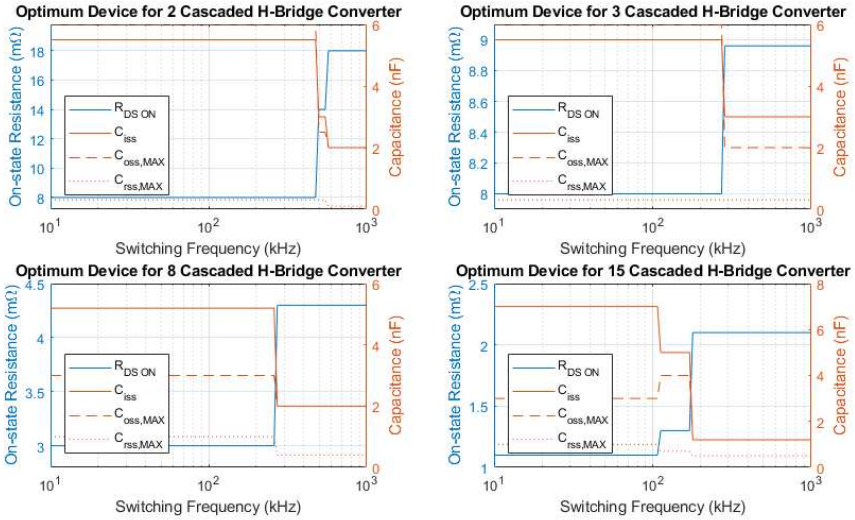

Fig. 10. A series of figures each showing the on-state resistance (blue) and capacitance (orange) figures for the optimum device at a specific number of cascaded bridges with increasing switching frequency.

Figure 10 shows that for a given number of cascaded bridges, with increasing switching frequency, devices with lower capacitance values tend to be selected at the expense of higher on-state resistance. This is as one might expect.

Overall, the results show that more levels in a converter can lower the overall losses and that multilevel converters can make higher switching frequencies much more accessible, with the silicon devices available.

3.2. SPICE Validation

While the individual assumptions used in this paper have been validated, the overall results are also validated using SPICE. A small, random selection of devices were modelled at various conditions using LTSpice with manufacturer device models. This validation uses a selection of device ratings and product ranges. Infineon manufacturer SPICE models claim to have been validated while other models do not come with such claims; however, they are presumably reasonably accurate.

Figure 11 shows the SPICE model used in the validation of the one of the devices under a certain set of conditions. V2 represents maximum voltage across the device with R2 used to limit current to emulate the real system. The value for the gate resistor R1 is derived using the method outlined in this paper.

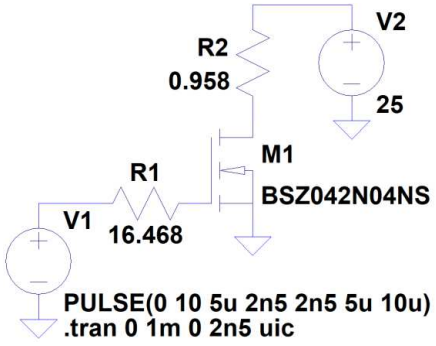

Fig. 11. SPICE model used in validation of Infineon BSZ042N04NS

Some variation is to be expected, particularly at higher frequencies, as the SPICE models include device gate resistance within the device, whereas this paper considers all gate resistance as being external to the device, in addition to other small differences. A comparison of the results from both the method outlined in this paper and SPICE are shown in table 1.

Table 1 shows that the SPICE simulation results are broadly similar to the results of the proposed method. This affirms the validity of the new method, despite its access only to the relatively coarse information available on any device datasheet.

3.3. Advanced Power Switching Devices

The analyses so far have only considered silicon MOSFETs, but there are other options. The seemingly obvious use of IGBTs, very common in industrial applications, can be eliminated as an uncompetitive option for this specification. Firstly, they are only relevant as a comparison at a single bridge, not only due to lack of low voltage rated devices, but also because their conduction path loss is from collector-emitter saturation that is fairly constant rather than an on-state resistance which reduces with lower voltage rating, resulting in prohibitively high loss with numerous series devices.

Even under the most favourable conditions they are also not competitive with modern MOSFET devices at this power level. Our preliminary analysis showed that in the range of 100A load current and above, loss in power MOSFETs and IGBTs is approximately on parity, with IGBTs even winning out at lower switching frequencies. However, in the 6kW power range specified for this converter, using a slightly modified form of the loss assessment method described in section II, MOSFETs are always optimal.

Another obvious class of switching device to be analysed are silicon carbide (SiC) power FETs. A number of these devices were added to the database. It was found, however, that they never featured as optimal devices, but instead consistently performed similarly to the poorly performing 600V and 500V silicon MOSFETs. It appears that at the 500V and 600V mark – the lowest range of SiC device ratings and the top end of Si device ratings in this analysis – SiC power FETs in this power range are no better than their silicon counterparts, apart from higher temperature tolerance. At higher voltages, 1200V and beyond, conventional silicon devices are largely surpassed by SiC devices.

The dataset was extended to include a small selection of GaN power switching devices. GaN power devices rated to voltage and current levels appropriate to this application are just reaching the market. The data for a series of devices manufactured by Efficient Power Conversion (EPC), specifically their 5th and 6th generation eGaN series devices, was added to the dataset for comparison (see Appendix A). It was shown that these devices can enable very significant reductions in power dissipation, as seen in figure12.

Device Name	Switching Frequency (kHz)	No of Cascaded Bridges	New Method Prediction (W)	SPICE Prediction (W)	Difference (%)
Infineon BSC076N06NS3	250	6	71	69	2.7
Infineon BSC320N20NS3	400	3	168	146	13
Infineon BSZ042N04NS3	100	10	63	64	1.6
Infineon BSZ0904NS1	20	14	81	91	12
Infineon IPD053N06N	500	5	48	37	22
Infineon IPP200N15N3	40	2	61	61	0.3
Infineon IPP320N20N3	800	4	229	184	20
Infineon IRFZ44N	250	8	268	234	13

Table 1. A comparison of results from the proposed method alongside SPICE simulation results.

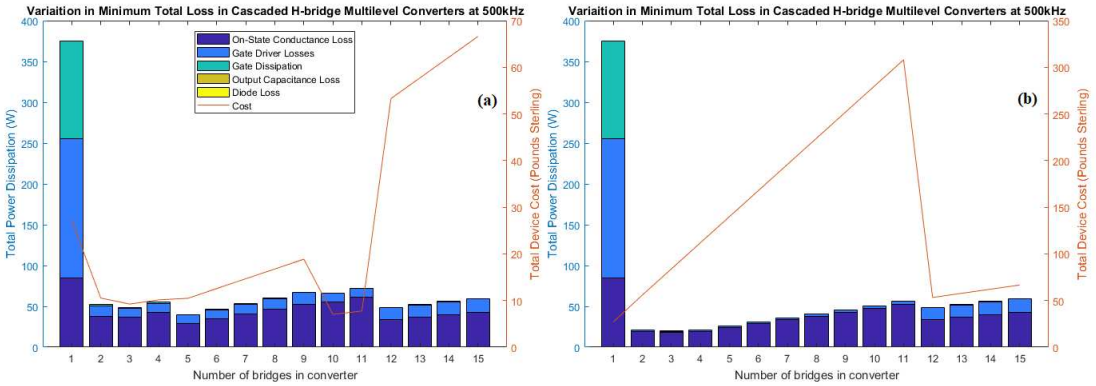

Fig. 12. (a) System switching loss plot for 500V DC link at 500kHz considering only conventional silicon devices. **(b)** Includes EPC's eGaN power devices.

This analysis was performed over a range of number of switching frequencies and it was found that these GaN devices could have up to 84% less loss than conventional silicon – observe the difference in loss for two to eleven cascaded bridges figures 12(a) and 12(b). However, this is at the expense of significant additional cost. The higher order converter loss results are unaffected due to the lack of very low voltage rated devices in EPC's eGaN series, just as the one bridge result is unchanged due to the lack of higher voltage rated eGaN devices. A full method and more extensive results can be found in [24].

4. Discussion

At low switching frequency, the conventional wisdom that a single bridge solution is best. This is not true where losses are critical. The wide availability of lower voltage rated devices might be worth the increased number of devices placed in the conduction path thanks in a large part to their much lower on-state resistance. So, critically, it is not just that the lowest loss solution is a multilevel converter for some conditions, but for all conditions within the scope of this study. Furthermore, the ability to operate at much higher switching frequencies without prohibitive power loss bodes well for a potential increase in popularity of multilevel solutions. This is particularly true when accounting for the ability to use newer switching device technologies such as GaN. While these technologies are expensive and confined to niche usage for now, the price of these devices is likely to reduce. In coming years GaN devices also further enable access to higher switching frequencies, comfortably in excess of 1MHz, which can help further reduce the cost and bulk associated with passive components.

These potential benefits sit alongside the key advantage of the use of cascaded H-bridge converters in grid-tie battery energy storage: they reduce requirement for external cell balancing. Cell balancing is a significant burden for large battery strings, and as outlined in the introductions this converter topology can deal with much of this in the converter itself [3-6].

So, why are not battery energy storage systems not already multilevel? It is an unproven technology in industry and would likely require significant investment before systems reach market in quantity. There also other potential disadvantages that are beyond the scope of this analysis - including cost. A transistor to be used across twenty cascaded bridges is significantly more than one twentieth of the cost. Furthermore, there is an increased quantity of support circuitry (e.g. gate drives) needed and a more complex controller.

5. Conclusion

This analysis has produced a quantitative method for comparing the power loss in low voltage cascaded H-bridge multilevel converters over a range of switching frequencies and also over a range of number of cascaded bridges in the converter. While only considered for a medium power grid-tie bidirectional battery energy storage system, the method could easily be adapted for any cascaded H-bridge multilevel converter and, with some additional work, other converter topologies too. The tools developed for the prediction of silicon MOSFET body diode performance are likely to be useful over a wide range of applications also. The results of these analyses help to strengthen the case for multilevel converters as not only a way of achieving some specific novel benefit, but also having lower power loss and, by extension, increase converter efficiency.

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7. Appendices

7.1. Appendix A

List of all silicon MOSFET devices used in main analysis:

Inf BSB165N15NZ3	Inf BSZ040N06LS5	Inf IPB65R045C7
Inf IPP65R045C7	ST STW62N65M5	Toshiba TK49N65W
ST STW56N65M2	ST STI57N65M5	Inf BSC320N20NS3
Fairchild FDP2710	IR IRFP4229	Vishay SUM45N25
Inf AUIRFP4409	Toshiba 2SK3176	ST STB40NF20
IXYS IXFT50N30Q3	Inf IPA075N15N3	IR IRFI4228
Inf BSC190N15NS3	Fairchild FDMS86255	Fairchild FDMS86200
Toshiba TK40A10N1	Vishay IRFP064PBF	Inf IRFI4410ZPBF
Toshiba TK46A08N1	Fairchild FDMC86340	Toshiba TK35A08N1
Inf BSC076N06NS3G	Inf IPD053N06N	Fairchild FDD86540
Toshiba TPCA8048-H	Inf IRFI1010N	Inf IPD30N06S2
Vishay SQD50N05-11	Inf AUIRFZ44N	Toshiba TK50P04M1
Toshiba TPCA8015-H	Vishay SQD50N04-4	Inf IPD50N04S4L-08
Toshiba TPCA8026	Fairchild FDMC8010	Inf IRFH5301TR2PBF
Vishay SIR862DP-T1	Fairchild FDMS3602S	Inf BSZ036NE2LS
Inf IPW65R045C7	IXYS MKE38RK600	Inf AUIRFZ46NL
ST STW56N60DM2	Fairchild FCH47N60N	Toshiba TPCA8045-H

Inf IPP320N20N3	IR IRFP260N	ONSemi NVTFS5811
Toshiba 2SK2995	Toshiba 2SK2967	Inf BSZ0904NSI
Inf IRFB4137	Fairchild FQA44N30	Inf BSZ042N06NS
Inf BSB165N15NZ3G	Inf IPP200N15N3	Inf IRFZ44NPBF
Inf BSC360N15NS3G	ST STF100N10F7	Inf BSZ042N04NS
Toshiba TK34A10N1	Fairchild FDMS86103	TI CSD17573Q5B
Renesas RJK0852DPB	Inf IPD30N08S2	Inf IRF6717MTR1
ST TF100N6F7		

List of all EPC eGan devices used in supplementary analysis:

EPC EPC2034	EPC EPC2023	EPC EPC2015C
EPC EPC2029	EPC EPC2032	EPC EPC2033

URL to download .xslx of database compiled:

www.sheffield.ac.uk/eee/research/emd/fetdb

7.2. Appendix B

List of all silicon MOSFET devices used in diode characterisation:

AUIRF1010	IPP200N15	IXFL210N30
AUIRFP4409	IPP320N20	MDP1921
BSC076N06	IPW60R041	MKE38RK600
BSP318S	IRF3315	NVTFS5811
BSZ036NE2	IRF530N	PSMN1R2
BSZ042N04	IRF640	RFD14N05
FCH47N60	IRF740	SI4840
FDBL86210	IRF7493	SPP20N60
FDL100N50	IRL8113	SQD50N05
FDMS86255	IRF840	SQJA86EP
FDN359AN	IRFB4227	STP16NF06
FDN8601	IRFML8244	STP55NF06
FDU3N40	IRFP064	STY145N65
FQA44N30	IRFP4229	TK40A10
IPA65R280	IRFP4668	TK49N65
IPB034N03	IRFS7734	TK72A12
IPB65R045	IRFU224	TPCA8026
IPB65R660	IRL2703	TPCA8048