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A Non-Isolated Bipolar Gate Driver with Self-Driven Negative Bias Generator in High-Side-Only Application

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***Abstract*—With the development of power electronic converters, size reducing and reliability extending are desired. For modern converter that utilises inductors or transformers, the dimensions of magnetic components are commonly inversely proportional to its switching frequency. With the increase of switching frequency, higher dv/dt may cause miss-triggering faults and unstable turn-off. Those issues can be relieved by applying a negative bias to conduct the turn-off. However, a separate DC-DC converter is normally required to generate this negative voltage. In this paper, a novel self-driven negative bias generator for high-side switch is introduced. The novel gate driver can provide bipolar gate driving capability without the need for a separate negative voltage supply. A prototype converter has been built and verified that the proposed bipolar gate driver could effectively generates the required negative voltage for power semiconductor driving without using a charge pump or switching converter.**

Keywords: Power converter, Gate driver, negative bias

I. INTRODUCTION

Along with the development of semiconductor technology, the widely-used DC to DC converter is trending towards increasing its switching frequency to mega-hertz level [1 and 2]. Using higher switching frequency reduces the size of passive components and therefore increases the power density [1]. However, several issues can be found in applications fitted with high-frequency switching technology. Those issues include, but are not limited to high switching losses, dV/dt causes miss-triggering, and inefficient overdrive [3, 4 and 5].

For a MOSFET based converter, the operation of a MOSFET is essentially controlled by charging and discharging its gate parasitic capacitor [3]. In a conventional converter, as per the schematic shown in Fig.1, the total driving loss can be calculated using the following equation.

$$P_{Gate} = f_s \times V_{Drv} \times \int_0^{\frac{1}{f_s}} I_{Drv}\, dt = f_s \times V_{Drv} \times Q_{Gate}$$

Where f_s is the switching frequency, V_{Drv} is the driving voltage, I_{Drv} is the instantaneous driving current, Q_{Gate} is the total gate charge.

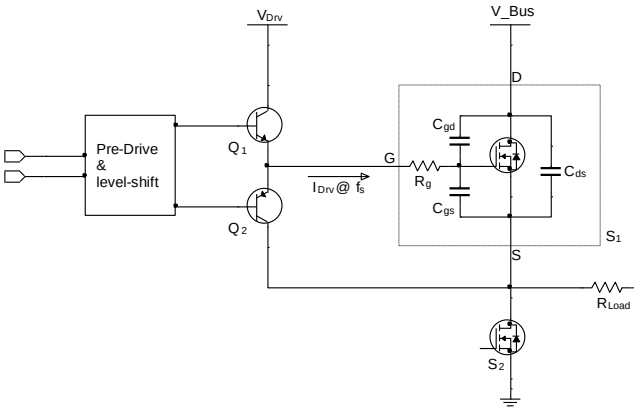

Fig. 1: Conventional gate drive circuit with parasitic components of MOSFET.

In order to reduce the driving loss or recover energies from the gate parasitic capacitor, several resonant gate drivers have been introduced [6 to 12]. In brief, the resonant gate driving approach uses an LC resonant circuit to charge and discharge the gate parasitic capacitor, while "C" is the equivalent gate capacitance [5]. Some researches [13, 8] use the leakage inductance of a driving transformer, but most of those circuits use a discrete component for the inductor [6, 7, 14 and 15]. This could avoids potential manufacture variations, however, causes additional complicities. Moreover, to avoid any simultaneous turned-on of both high-side and low-side switches, the timing control for those resonant gate drivers can be challenging due to component tolerances.

With the trend of increasing the switching frequency, the rising time and falling time when driving a MOSFET is also decreased, which has the effect of increasing the voltage slew rate (dv/dt) on the switch node [5]. As shown in Fig.2, using the full-bridge converter (only half bridge is shown) as an example, at the instant when S1 is turned-on, the voltage at the switching node S will be increasing with a very high slew rate. With such a big voltage change over the limited time, the high dV/dt and corresponding current change will inject a pulsed voltage (V_{pulse}) into the gate parasitic capacitor of

S2 [5]. In the worst case, V_{pulse} becomes high enough to exceed the gate threshold (V_{gs}) of S2, and S2 will be turned on. In the last decade, this problem became significantly important with the introduction of the HEX MOSFET and the Logic MOSFET that can be turned-on by a logic level voltage. Moreover, in some of the modern resonant gate driver designs [8, 9, 13 and 15], the gate terminal is left open after been turned-off, which significantly increases the risk of being falsely turned-on. Other designs like [14] provide a current path by using a separate MOSFET but this requires precise timing control.

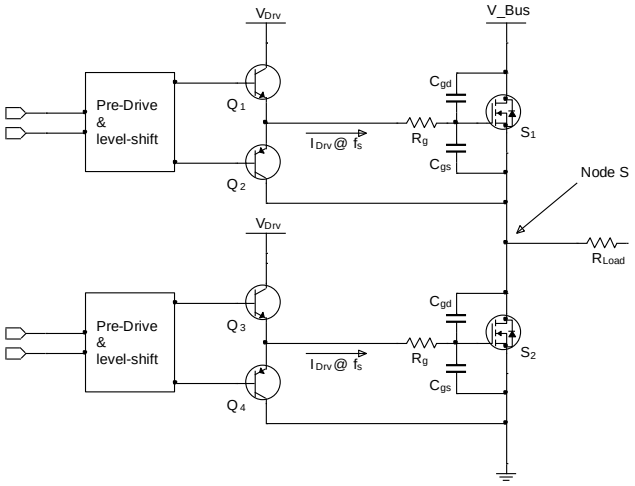

Fig. 2: Half-bridge of a full-bridge converter showing its switching node S.

To prevents false triggers, in practice, a circuit may use a high driving voltage (V_{Drv}) and utilise MOSFETs with higher V_{gs}. However, although a higher V_{Drv} may reduce the on-state resistance (R_{ds}), the gate driving efficiency will be compromised according to [5].

In comparison, using a MOSFET with a low V_{gs}, then if V_{Drv} is minimised to ensure a definite turn-on, high enough to be free from component tolerance and any potential parasitic elements, then the turn-on power loss will be minimised [5]. To prevent the MOSFET from the false triggering, a small negative voltage should be applied to maintain the off status of the semiconductor. However, to generate the required negative voltage may be challenging, particularly in a high-frequency converter where the negative biasing current may reach several hundreds of milliamps, numerically.

To supply the required negative voltage, an additional DC-DC power supply (or isolated DC-DC power supply for an isolated driver) is customary, as shown in Fig. 3. These additional power supplies are undesirable in terms of footprint and additional cost, and suffer from limited lifetime due to utilising electrolytic capacitors.

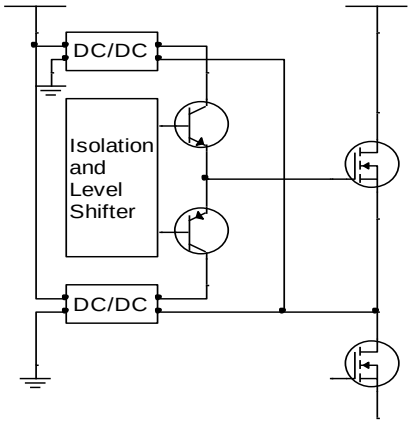

Fig. 3: The conventional approach to achieve bipolar driving.

For a widely-used non-isolated bridge drive, a boost driver is widely used to generate the high voltage required for high-side MOSFET driving, which normally consists of a boost diode and boost capacitor. The boost circuit replaces the DC-DC supply that provides the positive bias. However, it is still required to have a separate power supply to provide a negative bias.

II. BIPOLAR GATE DRIVING USING CONVENTIONAL GATE DRIVER

To avoid the requirement of a separate DC-DC supply, the schematic of the proposed novel gate driver is shown in Fig. 4. Compared with the conventional boosted driver, only seven components: C2, D2, D4, R1, R2, R3, Q3 are added.

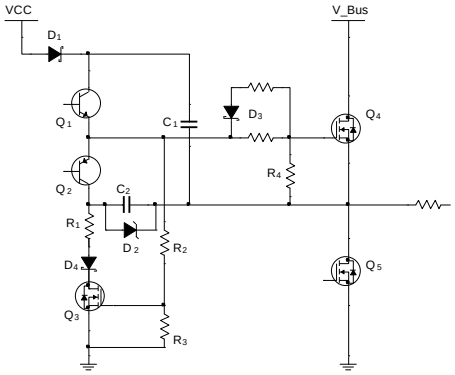

Fig. 4. Schematic of the proposed bipolar gate driver.

Based on the schematic shown in Fig. 4, the operating sequences are now described, where 'Sx' denotes the sequence number.

S0, before Q_4 is turned-on and whilst Q_5 is turned-on: C_1 is charged by VCC through D_1 so that the energy used to turn on Q_4 is stored in C_1. The voltage on C_1 can be approximated as VCC – V_{FD} where V_{FD} is the forward voltage drop of D_1 when the switching period of the full-bridge is lower than T_p given as:

$$T_p = 5(R_{DS} + \Delta R_{DS} \times T) \times C_1$$

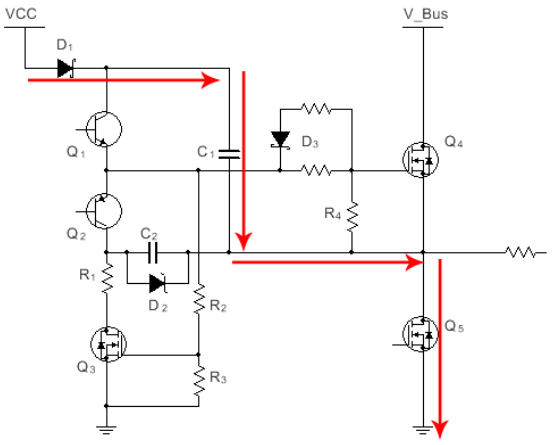

Fig. 5. Simplified schematic of the proposed bipolar gate driver, stage 0.

S1, when Q_1 is turned-on and Q_5 is turned-off: C_1 will be discharged through Q_1, and the energy stored in C_1 will be applied to the Gate terminal of Q_4. Since C_1 is referenced to the sink terminal of Q_4, a voltage equal to VCC will be applied across the gate and sink terminal of Q_4, Q_4 is turned-on and similarly, Q_3 is turned-on. Since the voltage used to drive Q_4 (approximately V_Bus+VCC) is normally higher than the maximum V_{GS} voltage, a voltage divider consisting of R_2 and R_3 is used to provide a drive voltage for Q_3. The resistance of R_2 and R_3 can be calculated by using the following equation, where V_{th} is the voltage desired for drive Q_3.

$$R_2 = \frac{(VCC + V_{bus} - V_{th}) \times R_3}{V_{th}}$$

Meanwhile, when Q_4 and Q_3 are turned-on, V_Bus will be applied to the series connected C_2 and R_1; C_2 will therefore be charged. Whilst C_2 is being charged, R_1 limits the current flow through Q_3 and C_2 to avoid a surge current and protect the Zener diode. The voltage rating of Q_3 should be higher than V_Bus-V_{D2}. The voltage across C_2 is set by the Zener diode D_2; the voltage across C_2 will rise to the reverse breakdown threshold voltage of D_2, the Zener diode will be broken down and C_2 will stop charging with a voltage across it of $-V_{D2}$.

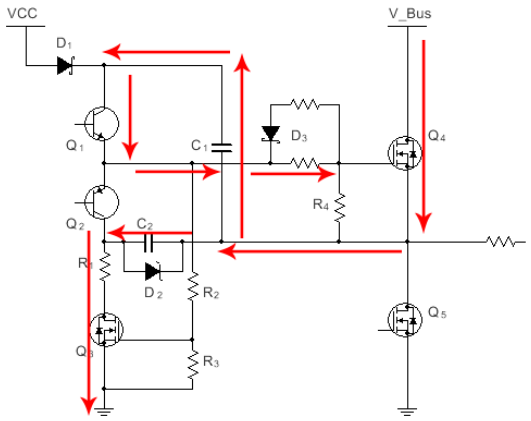

Fig. 6. Simplified schematic of the proposed bipolar gate driver, stage 1.

S2, dead-time, while Q_2 is turned-on: C_2 will be discharged through Q_2. Since the positive side of C_2 is connected to the sink terminal of Q_4, a negative voltage will be applied to the Gate terminal of Q_4. The gate charge on Q_4 is therefore depleted through the gate resistors and D_3. As the capacitance of C_2 is much higher than the gate capacitance of Q_4, the negative voltage is maintained on the gate of Q_4 to ensure a solid turn-off.

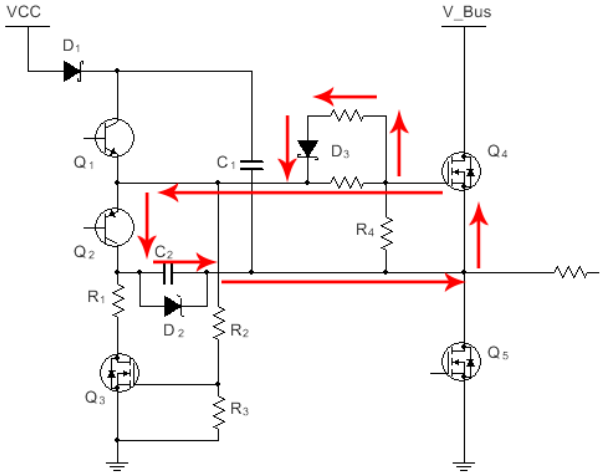

Fig. 7. Simplified schematic of the proposed bipolar gate driver, stage 2.

S3, when Q_4 remains off and Q_5 is turned-on: C_2 will maintain a negative voltage onto the gate of Q_4, and C_1 will be charged through D_1.

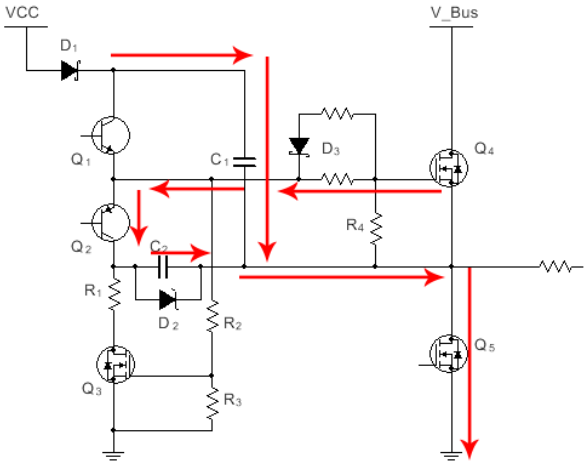

Fig. 8. Simplified schematic of the proposed bipolar gate driver, stage 3.

S4, dead-time, Q_4 remains off and Q_5 turned-off: C_2 maintains a negative voltage onto the gate of Q_4 but C_1 is now fully charged and ready to turn Q_4 on.

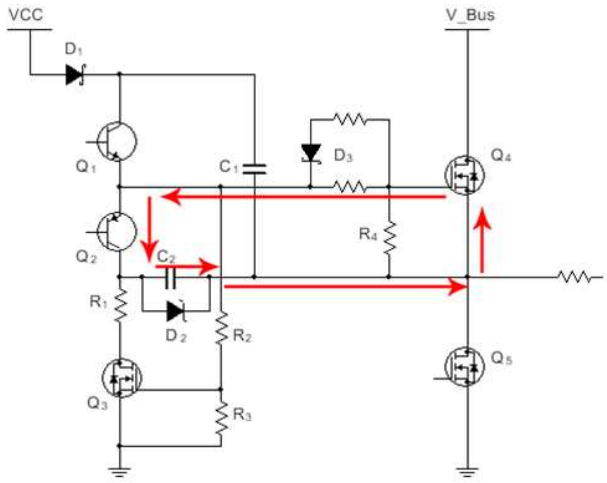

Fig. 9. Simplified schematic of the proposed bipolar gate driver, stage 4.

As can be seen from the sequence of operation, C_1 acts as the positive power source and C_2 acts as the negative power source. When C_1 discharges to turn Q_4 on, C_2 will be charged. Whereas during C_2 discharges to turn Q_4 off, C_1 will be charged. Since the power source that charges C_2 is V_Bus, the additional negative bias generator will not consume power from VCC, hence the output capability of the power supply, providing VCC, is unaffected and the power drawn from V_Bus is negligible.

III. SIMULATION

Based on the circuit topology introduced in the previous section, a SPICE module has been built to verify the design. The simulation schematic is shown in Fig. 10. In the simulation circuit, two voltage-controlled switches are used to simulate a conventional gate driver and provides 50% duty cycle drive signal. The detailed schematic is showing in the following figure.

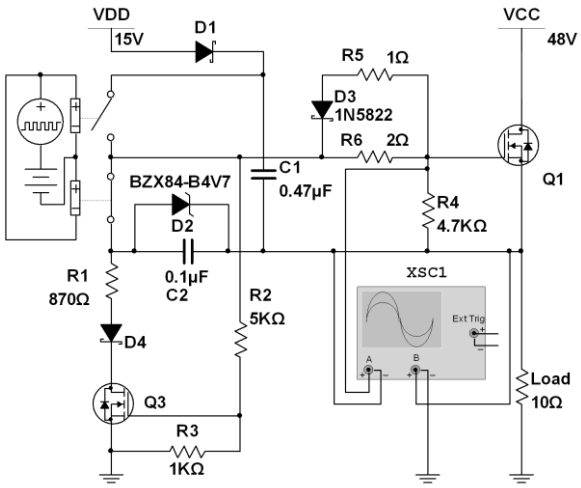

Fig.10. Simulink schematic of the proposed gate drive circuit.

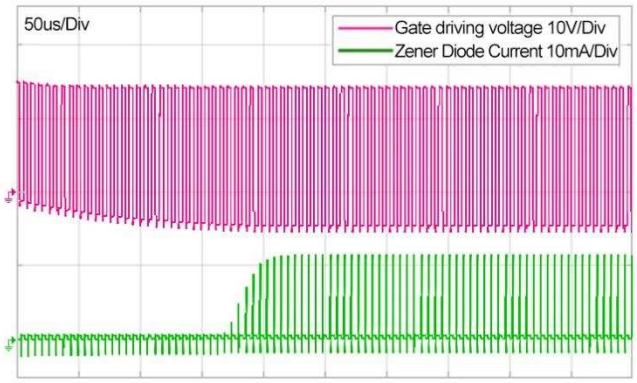

Fig. 11. Simulated waveforms represents the converter

During simulation, Fig. 11 clearly shows the establishment progress of the desired negative bias. As can be seen from the figure, just after the first cycle, some negative bias can already be observed from the gate drive signal. Meanwhile, by progressively charging C_2, the current flow through the Zener diode is increasing until a steady state peak current, as can be seen from Fig. 11 as the green waveform.

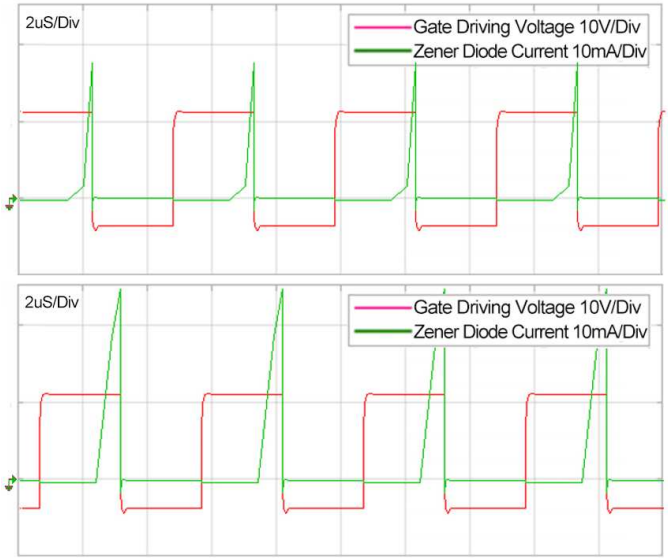

Fig. 12. Simulated waveforms showing different Zener diode current at R1=800Ohms (Upper) and 700Ohms (Lower).

As shown in Fig. 12, corresponded to a smaller current limiting resistor R_1 more current will be carried by the Zener diode at the end of each cycle after C_2 been charged to the desired voltage. This will not only affect the gate driving efficiency but also causes over heating of the Zener diode.

IV. PROTOTYPE DESIGN

A prototype converter has been built to evaluate the proposed gate driving topology as simulated in the previous section. The prototype is designed to deliver up to 450W of power to the load. The prototype converter is shown in Fig. 13. The converter is specified to be powered by 24-48V DC power. Its on-board 8052 microcontroller drives a proposed gate driver consisting of IR2103 conventional gate driver chip and the

additional circuitries shown in Fig. 10. The gate drive signals then drives MOSFET to provided AC output with frequencies at 100 kHz.

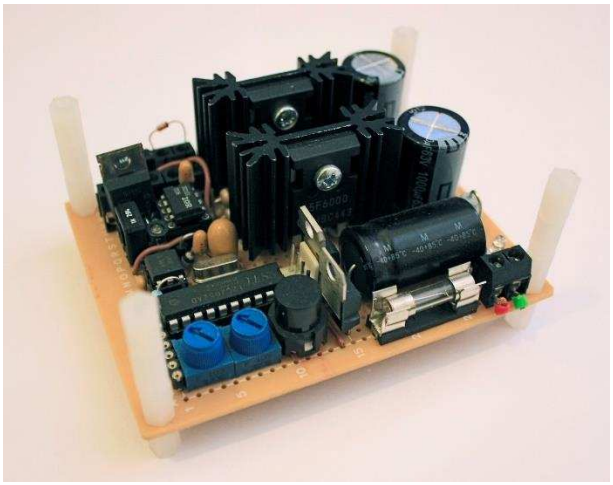

Fig. 13. Prototype WPT transmitter employing wireless PLL.

The schematic of the drive section is detailed in Fig. 14. Using the signals provided by the IR2103, proposed circuit can be easily integrated.

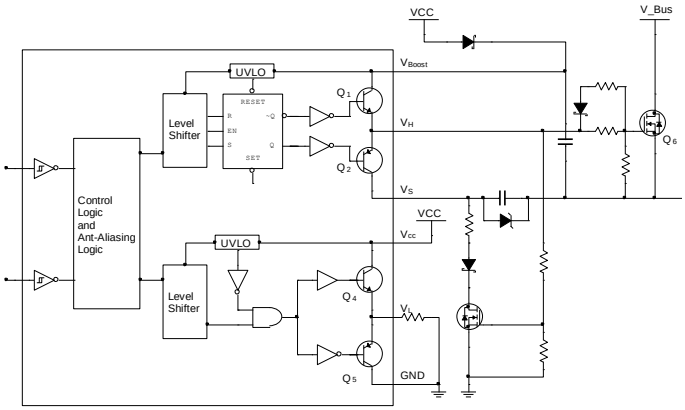

Fig. 14. Prototype WPT transmitter employing wireless PLL.

V. TEST AND EVALUATION

The prototype converter shown in Fig. 13 has been evaluated with a 24V power source. Using the schematic shown in Fig. 10, Fig. 15 shows the voltage across C_2 during start-up. As can be seen from the figure, the desired negative voltage can be achieved rapidly dependant on the duty cycle of Q_1 and corresponded C_2 and R_1. Using this voltage, Fig. 16 shows the gate driving voltage across Gate-Source terminal of Q_1. Fig. 16 clearly demonstrates that even after several cycles from start-up, some negative voltage has appeared on the gate driving output.

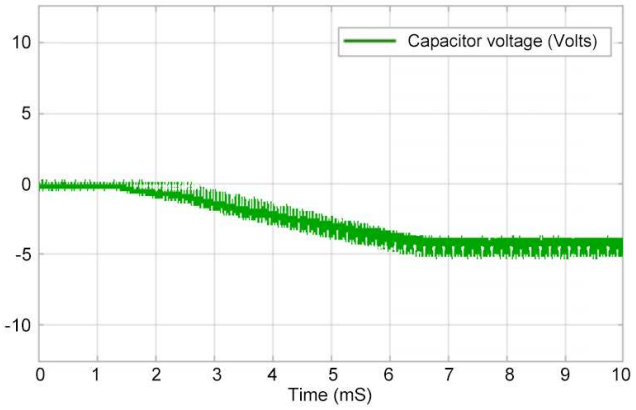

Fig. 15. The voltage measured across C_2 demonstrating its charging progress.

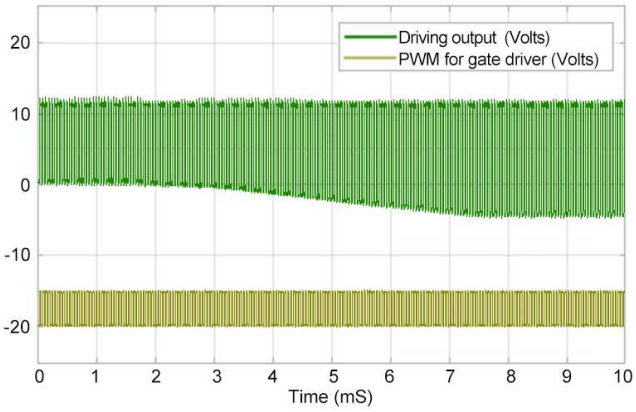

Fig. 16. Gate driving output (Green) and logical gate drive signal (Yellow), showing the establishment of bipolar driving voltage.

The minimum negative bias applied to the MOSFET will depend on the duty cycle of high-side MOSFET, which also represents the duty cycle of C_2. The Zener diode D_2 can only limit the minimum biasing level when designed duty cycle is achieved so that sufficient energy is stored into C_2. If the duty cycle of the charging C2 is lower than the designed value, negative voltage with lower amplitude will be applied. The following Fig. 17 shows the different negative biasing levels at different duty cycles.

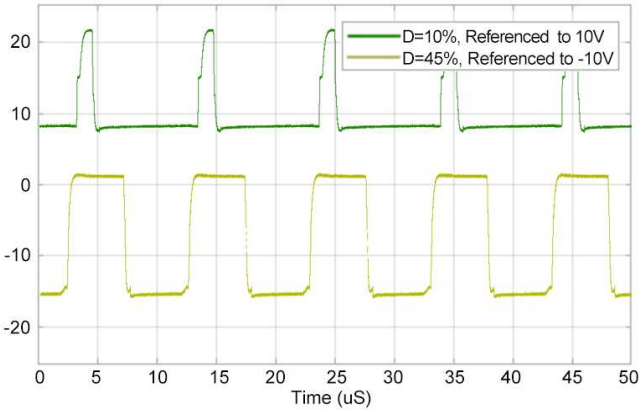

Fig. 17. Gate driving output showing the biasing level verse duty cycle.

VI. CONCLUSION

This paper described the design and operation of a technique for generating a negative bias for MOSFET bipolar driving in non-isolated MOSFET driving and demonstrated how the desired negative voltage can be obtained. The evaluation has shown that by using the negative bias generator, negative voltage for MOSFET gate driving can be achieved without using a charge pump and switching regulator. Using a power converter as an example, while the desired negative bias generator guaranteed a solid turn-off, using MOSFETs with lower Vgs and driving them using an optimised turn-on voltage could significantly reduce the driving loses. Several key components can be calculated using equations provided in this paper. Finally, the methodology introduced in this paper can also be used in other gate driving topologies and isolations to remove the need for a power source that provides negative voltage.

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