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Modelling Framework for Parallel SiC Power MOSFETs Chips in Modules developed by Planar Technology

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***Abstract*—This paper presents a modelling framework to simulate transients and steady state performance for SiC power MOSFETs modules. The electro-thermal modelling is implemented using Simscape/MATLAB program based on the single chip characteristics provided in the datasheet. The method can easily incorporate multiple chips and module parasitic components providing a tool for module characterization and to support module design optimization. The simulated model is then experimentally validated at different voltage buses and junction temperatures for a novel SiC MOSFET Module design consists of two parallel chips per switch developed using wire-bond free planar technology.**

Keywords—SiC Power MOSFET, Modelling, Parallel Chips per Switch, Planar Technology.

I. INTRODUCTION

Silicon carbide (SiC) Power MOSFET, as one of the major applications of the wide bandgap power devices, has a advantages over the conventional silicon power MOSFET due to its lower on state resistance, higher power density and higher blocking voltage. SiC power MOSFETs represent excellent replacements for the insulated gate bipolar transistors (IGBTs) and gate turn-off thyristors (GTOs) at higher blocking voltages applications since SiC power MOSFETs can operate at higher switching frequencies with lower switching losses. This is highly significant as it can significantly reduce the size of passive components in the power converters. Thanks to these superior characteristics, SiC power MOSFET has become one of the leading candidate for the power converter applications in the aircraft systems, where size and weight are governing factors especially for the More Electric Aircraft (MEA) development [1-2].

Power electronics modules employing a number of parallel chips per switch are commonly used for increasing the output current capability and lowering conduction losses. Therefore, the developed power converter can operate at the required output power without reaching the maximum allowable junction temperature of the power devices. A number of power modules manufacturing technologies have emerged in recent years. Wire-bonding techniques to interconnect semiconductor chips to external terminal contact is a mature technology widely used in power electronics manufacturing. Reliability is a stringent requirement in transportation application including in particular aircraft power systems. Reliability concerns might limit the applicability of existing technologies and will require improvements on standard packaging technologies to meet industry requirements. One such improvement in the power electronics industry is related to the development of wire-bond free interconnect technologies for the manufacture of the SiC Power MOSFET module to replace the traditional wire bonding process which is often considered as the main failure mechanism in power electronics devices reducing the remaining useful lifetime (RUL) of the whole power converters [3].

Accurate modelling of the electrical and electro-thermal behaviour of power electronics module is of essential importance to support the design and development stage of novel power modules concepts. Accurate modelling of power electronics modules require the use of accurate models of the semiconductor devices in static and transient switching conditions, detailed modelling of the parasitic elements resulting from interconnections between chips and terminals as well as accurate modelling of the thermal effects on device characteristics and coupling with thermal dynamics of the module and environmental constraints.

A number of models suitable for electrical and coupled electro-thermal simulation of SiC power MOSFETs have been proposed in literature [4-10]. Most of these use analytical models based on differential-algebraic equations suitable for SPICE-type circuit simulators [4-5]. Input-output characteristics are typically based on analytical formulations with parameters typically extracted from datasheets and/or experimental characterization. A full representation of device's characteristics based on analytical fitting of characteristics in all operating conditions [6] is not straightforward. Saber's ModelArchitect provides a tool for power MOSFETs modelling based on tabulated look-up tables of device characteristics which can be obtained from datasheets and/or measurements, potentially guaranteeing an excellent fidelity. The model, however, is not available in the public do-main and cannot be used in other simulation environments. On the another hand, modelling parallel chips modules developed by planar technology are not investigated previously in the aforementioned papers.

This paper provides an electrical modelling environment to demonstrate the SiC Power MOSEFTs performance in paralleling chip MOSFET modules developed by planar technology. The modelling framework is based on the single chip characteristics provided in its datasheet. The simulated model is experimentally validated at different junction temperatures for a prototype SiC MOSFET Module consisting of two parallel chips per switch manufactured by Siemens AG.

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II. SIMULATION ENVIRONMENT

Simscape modelling language has been chosen as the proposed modelling environment thanks to the ability to easily model and simulate complex systems of differential-algebraic equations. This allows components, subsystems and system models represented in different physical domains and forms to be integrated and simulated in a unified environment to fully account multi-physics interactions.

A. The Electrical Model

The MOSFET model is based on the sub-circuit illustrated in Fig. 1.

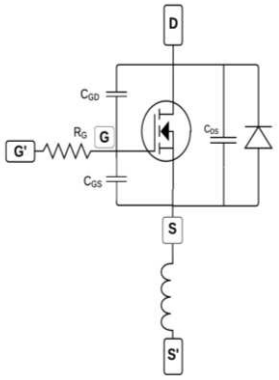

Figure 1: Subcircuit model of power MOSFETs

The transfer characteristic of the MOSFET is given by the nonlinear relationship:

$$I_{DS} = I_{DS}\,(V_{DS},\ V_{GS},\ T) \tag{1}$$

where the drain-source current I_{DS} is a function of the drain-source voltage V_{DS}, the gate-source voltage V_{GS}, and Temperature T. Voltage dependent parasitic capacitances can be measured at the device terminals and are typically given in the datasheets as the input C_{iss}, output C_{oss}, and reverse transfer C_{rss} capacitances:

$$C_{iss}\,(V_{DS}) = C_{GS} + C_{GD} \tag{2}$$

$$C_{oss}\,(V_{DS}) = C_{DS} + C_{GD} \tag{3}$$

$$C_{rss}\,(V_{DS}) = C_{GD} \tag{4}$$

Voltage-dependent capacitances are also represented by look-up tables in the model, where the general formula relating the voltage and the current in the capacitor is implemented as follows:

$$\begin{aligned}
&\frac{d(CV)}{dt} = i \\
&C\frac{dV}{dt} + V\frac{dC}{dt} = i \\
&C\frac{dV}{dt} + V\frac{dC}{dV}\frac{dV}{dt} = i \\
&[C + V\frac{dC}{dV}]\cdot\frac{dV}{dt} = i \\
&C_{New}\cdot\frac{dV}{dt} = i \\
&where\ C_{New} = [C + V\frac{dC}{dV}]
\end{aligned} \tag{5}$$

The reverse recovery process of the body diode is also analytically modelled using the method proposed in [11].

$$i_{PN} = \frac{q_E - q_M}{T_M} \tag{6}$$

$$0 = \frac{dq_M}{dt} + \frac{q_M}{\tau} - \frac{q_E - q_M}{T_M} \tag{7}$$

$$q_E = I_s\ \tau\left[\exp\left(\frac{v_{PN}}{n\,V_T}\right) - 1\right] \tag{8}$$

where;

i_{PN} : the diode current

V_{PN} : the diode Voltage

q_E : the reverse recovery charge

q_M : the forward bias injected charge

τ :the diffusion time constant 1

T_M : the diffusion time constant 2

I_s : the reverse saturation current

V_T :the thermal voltage

n : constant equals to 2 for high voltage p-n junction diode

The model results in a system of seven coupled differential-algebraic equations. Simscape language is selected for the proposed modelling as it is ideally suitable for description of physical systems described by implicit differential algebraic equations. A flow chart demonstrating the structure of the program used to simulate the characteristics of the SiC MOSFET is illustrated in Fig. 2.

B. Simulation of One Chip per Switch

A Simscape circuit for the SiC MOSFET Model is presented in Fig.3.

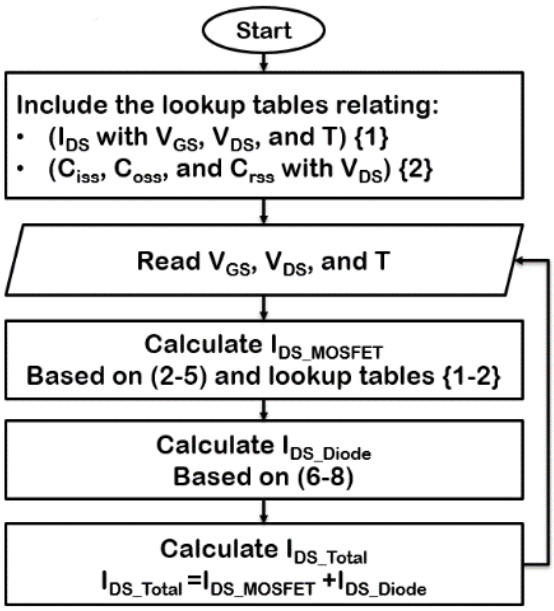

Figure 2: Flow chart of the simulating program

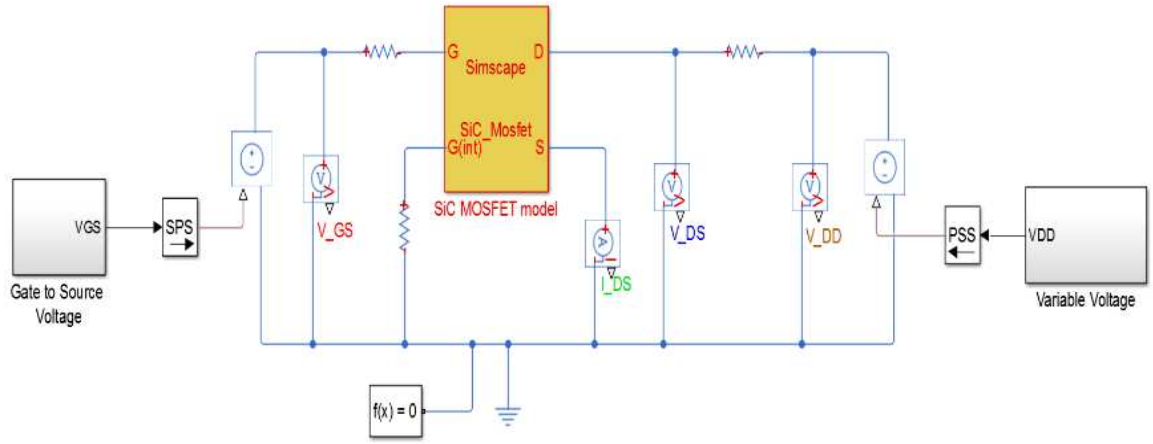

Figure 3: Simscape Circuit for SiC MOSFET Model

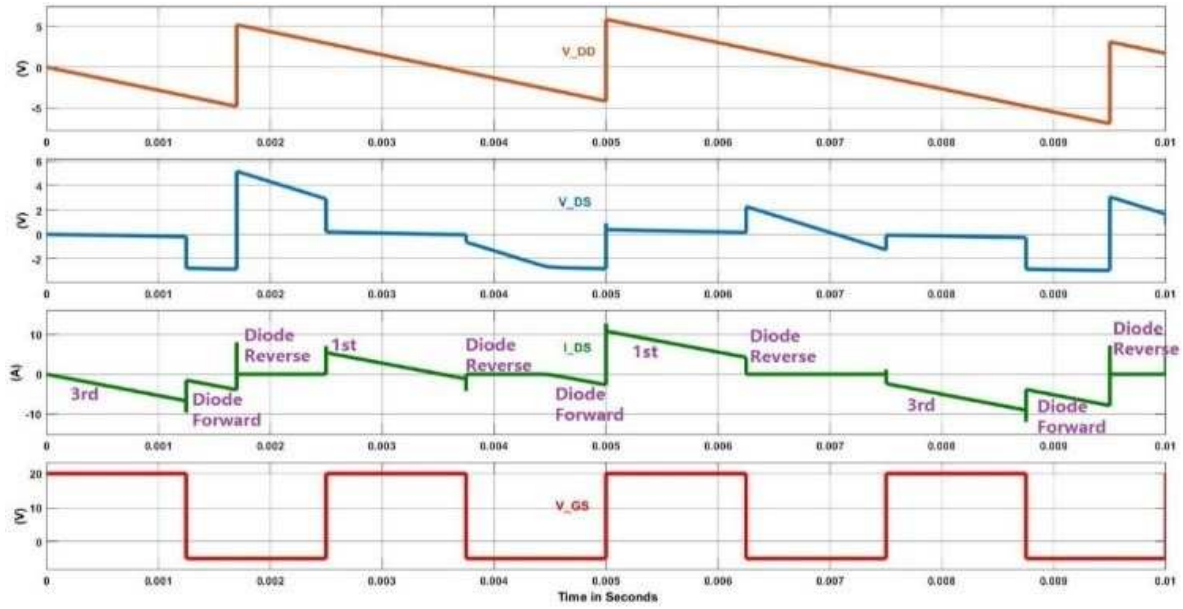

Figure 4: SiC MOSFET voltage and current waveforms at variable V_{DD}

Fig. 4 shows some exemplary waveforms illustrating the behaviour in different operating conditions including forward and reverse conduction. The MOSFET operating states are dependent on the gate-source voltage V_{GS}. When V_{GS} is high at 20V, the MOSFET is in conducting state and the current can flow in both directions while V_{DS} is close to zero. When V_{GS} is negative, the MOSFET behaviour is dictated by its body diode and the device current is dependent on whether it is forward or reverse-biased.

Figures 5, 6, and 7 provide comparisons between the output characteristics of the SiC MOSFET given in the datasheet for the CREE C2M0025120D SiC Power MOSFET [12] and those predicted by the Simscape SiC MOSFET Model.

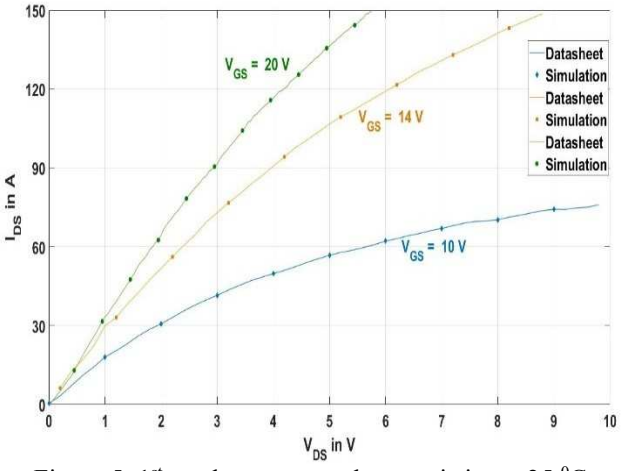

Figure 5: 1st quadrant output characteristics at 25 ^{0}C

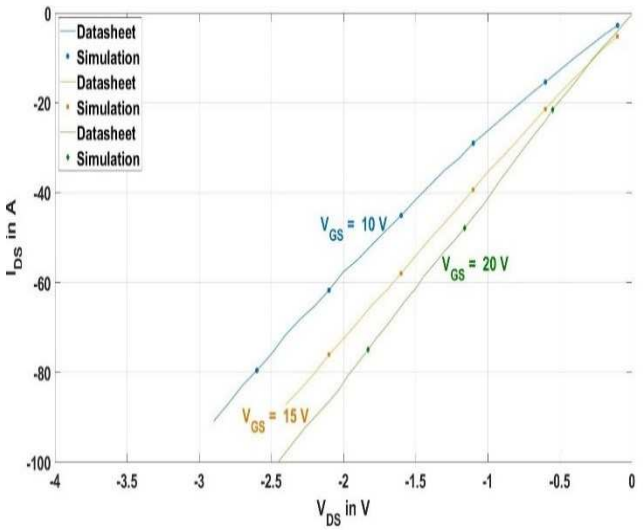

Figure 6: 3rd quadrant output characteristics at 25 ^{0}C

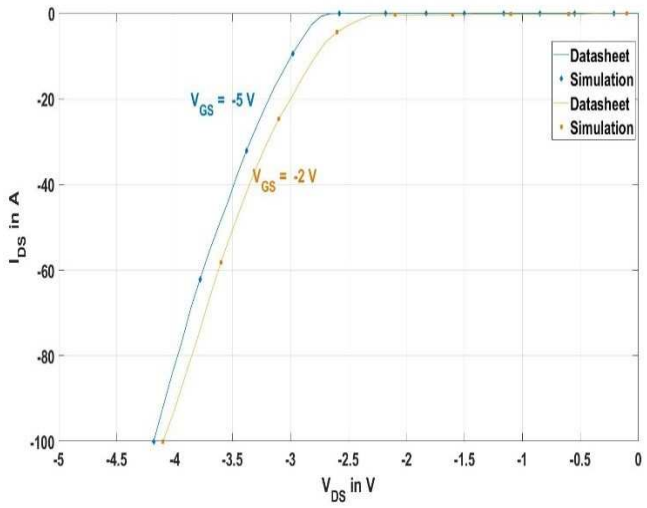

Figure 7: Body diode output characteristics at 25 ^{0}C

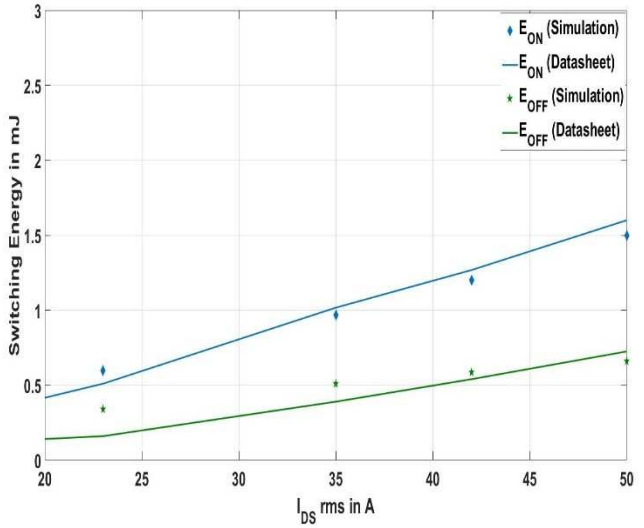

Figure 8: Switching Energy vs. Drain Current at V_{DD} = 800V and 25 ^{0}C

Finally, Figure 8 shows comparisons between the estimated switching energy during the on and off periods (Eon and Eoff respectively) in the simulated mode and those provided in the datasheet. There are some divergence between the estimated Eon and Eoff by the simulated model and those provided in the datasheet, especially at lower current level. This is mainly due to the procedures, which were taken to measure these energies in the datasheet, are not given as well as the parasitic inductance in the circuit, which both have great influence on the measured energy values especially at lower magnitudes.

III. Two Parallel Chip per Switch

A prototype SiC power MOSFET designed by Siemens AG, having two parallel chips per switch, is utilized in this paper in order to validate the proposed simulated model. The chips used in the prototype module are CREE C2M0025120D SiC Power MOSFET. The schematic of the prototype module is illustrated in Fig. 9.

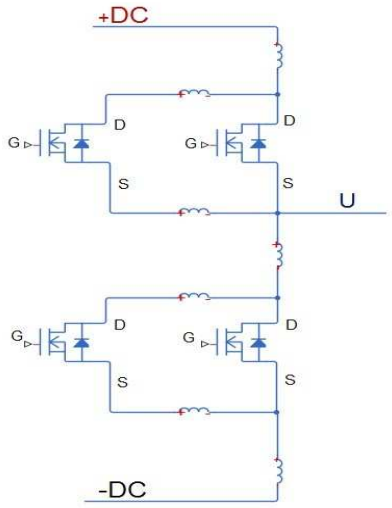

Figure 9: Prototype SiC MOSFET Module (two parallel chips per Switch)

A. The Experimental Validation

The experimental setup implemented in this paper in demonstrated in Figure 10. The hot plate is used for varying and controlling the junction temperature (T_J) of the MOSFET module. The probes, which are utilized to capture the voltage/current waveforms under study are; CWTUM Rogowski current waveform transducer for measuring I_{DS} along with LeCory ADP305 high voltage differential probe for measuring V_{DS} and V_{GS}.

The Simscape circuit for modelling the experimental environment is illustrated in Fig. 11. Comparisons between the measured V_{GS}, V_{DS}, and I_{DS} waveforms in the experimental setup and those developed by the simulated model are illustrated in Fig.12 at (300V DC Bus and 25 ^{0}C T_J) and Fig.13 at (500V DC Bus and 125 ^{0}C T_J). A good agreement is shown between the measurement and simulation for the V_{GS}, V_{DS}, and I_{DS} waveforms at different voltage and temperature values. On the another hand, the measured V_{GS} is relatively noisy compared to the simulated one and this is mainly the due to connecting cables between the gate drive board and the MOSFET module which cause such oscillatory behaviour, which doesn't relate to the model of the MOSFET module itself.

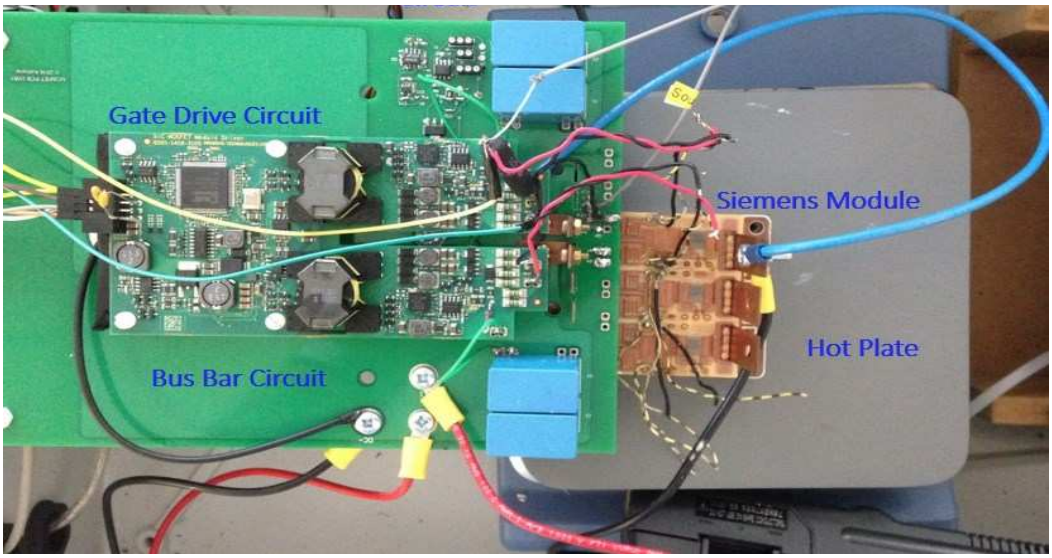

Figure 10. Experimental Setup

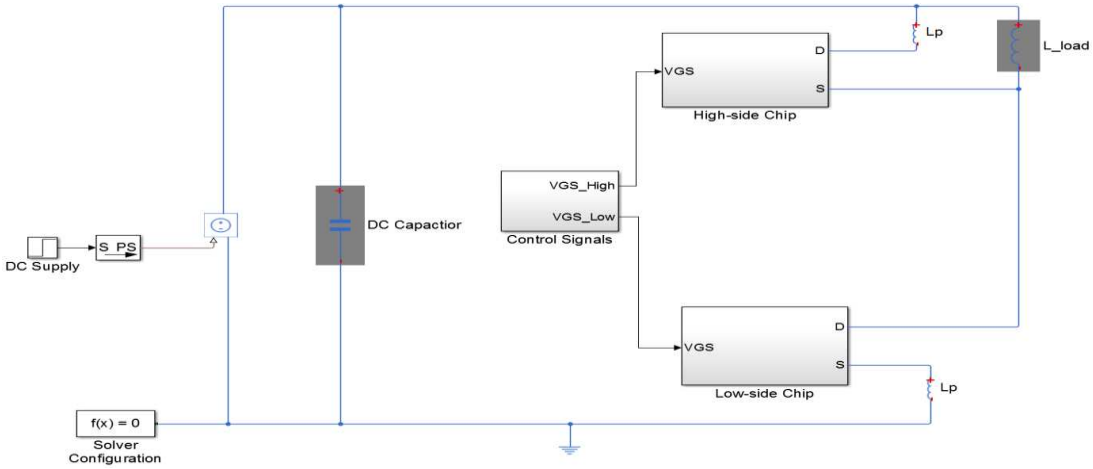

Figure 11. Simscape circuit for modelling the experimental setup

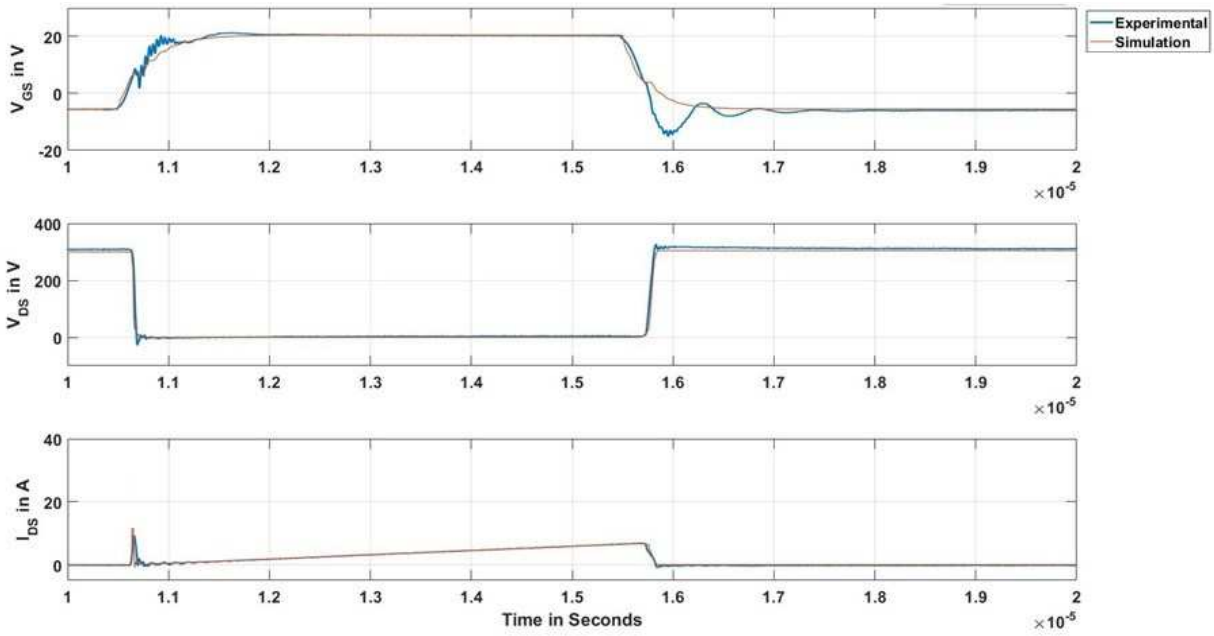

Figure 12: V_{GS}, V_{DS}, and I_{DS} waveforms at 300V DC Bus and 25^0C

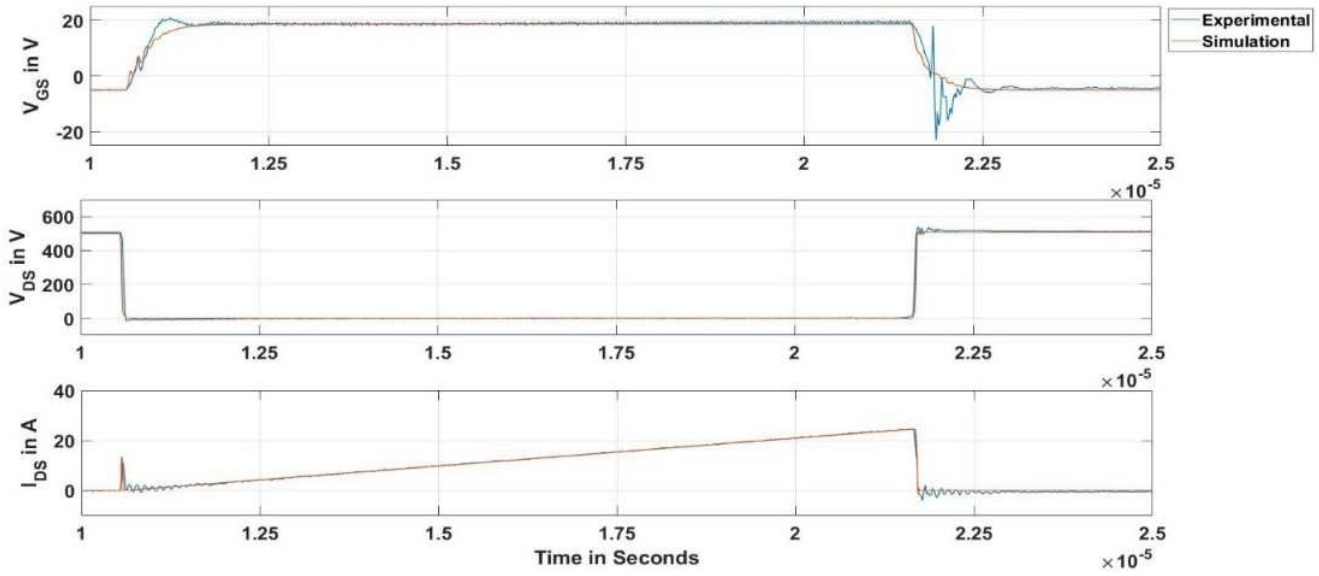

Figure 13: V_{GS}, V_{DS}, and I_{DS} waveforms at 500V DC Bus and 120^{0}C

B. *The Effects of Intra-Chips Parasitics*

The proposed Simscape Model in this paper also provides the flexibility of modelling the parasitics of the module; either between the parallel chips or between the lower and upper chips. The parasitics inductance can be included in the Simscape circuit directly at arbitrary locations with different values without changing the core Simscape program, so that the parasitics of the real MOSFET Module can been correctly modelled. Fig. 14 illustrates several locations, where the parasitics inductance (L_P) can be included between chips. Additionally, Figures 15 and 16 shows the V_{GS}, V_{DS}, and I_{DS} waveforms at different values of $L_{P(i)}$ at switching on and off respectively.

IV. Conculsion and Future Work

A new electro-thermal modelling framework is presented in this paper for SiC power MOSEFT chips. The modelling method can be used to model electrical and electro-thermal behaviour of novel SiC-based modules. The modelling method is based on simple static characteristics available in devices' datasheets. The methodology allows a simple modelling of the interaction and transient dynamics resulting from parasitics in complex modules topologies. The model is validated in an experimental environment on prototype modules having two parallel chips per switch at different DC bus voltage and T_J. The model presents a flexible tool to evaluate switching and steady-state behaviour of SiC-based power converters and for evaluating the effects of parasitics to support the design process of novel power modules layout. The research work is still ongoing to model larger SiC power modules consists of six chips per switch.

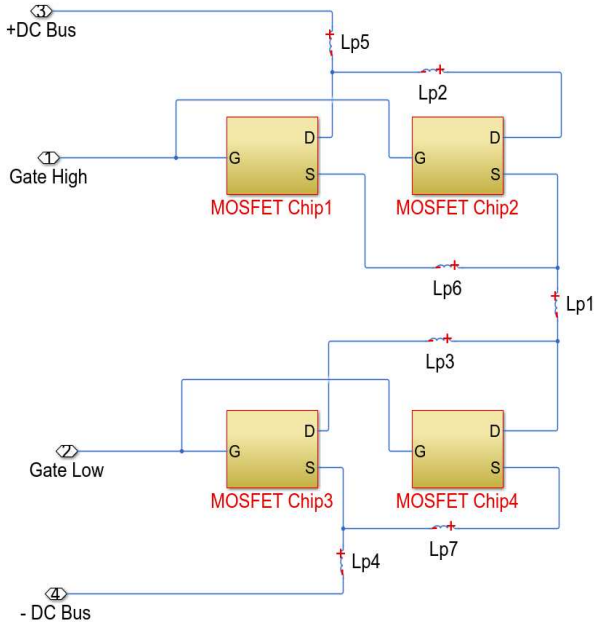

Figure 14 the parasitics inductances $L_{P(i)}$ in the intra-chips

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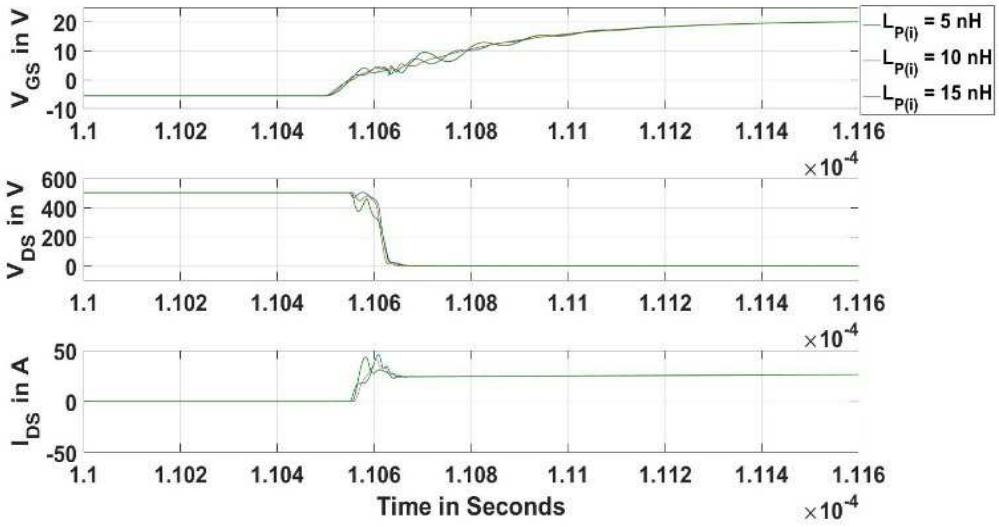

Figure 15: V_{GS}, V_{DS}, and I_{DS} at different $L_{P(i)}$ at switching on

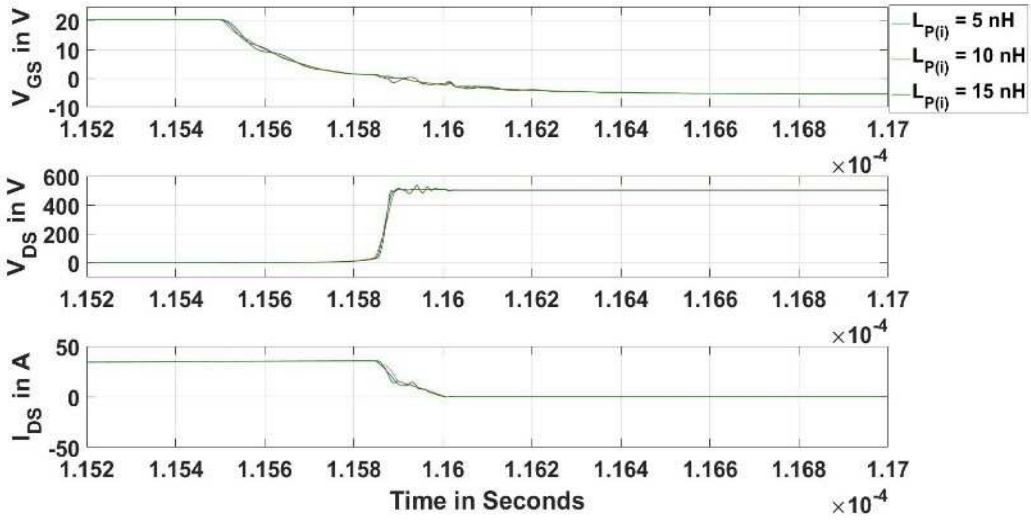

Figure 16: V_{GS}, V_{DS}, and I_{DS} at different $L_{P(i)}$ at switching off

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