



*Citation for published version:*

University of Hong Kong , Li, S, Tan, SC & Hui, SYR 2019, 'A single-phase three-level flying-capacitor PFC rectifier without electrolytic capacitors', IEEE Transactions on Power Electronics, vol. 34, no. 7, pp. 6411-6424. <https://doi.org/10.1109/TPEL.2018.2871552>

*DOI:*

[10.1109/TPEL.2018.2871552](https://doi.org/10.1109/TPEL.2018.2871552)

*Publication date:*

2019

*Document Version*

Peer reviewed version

[Link to publication](#)

© 2018 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other users, including reprinting/ republishing this material for advertising or promotional purposes, creating new collective works for resale or redistribution to servers or lists, or reuse of any copyrighted components of this work in other works.

## University of Bath

### General rights

Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

### Take down policy

If you believe that this document breaches copyright please contact us providing details, and we will remove access to the work immediately and investigate your claim.

# A Single-Phase Three-Level Flying-Capacitor PFC Rectifier without Electrolytic Capacitors

Wenlong Qi, *Student Member, IEEE*, Sinan Li, *Member, IEEE*, Siew-Chong Tan, *Senior Member, IEEE* and S. Y. (Ron) Hui, *Fellow, IEEE*

*Abstract*— A component-minimized and low-voltage-stress single-phase PFC rectifier without electrolytic capacitor is proposed in this paper. Component minimization is achieved by embedding an active pulsating-power-buffering (PPB) function within each switching period, such that typical add-on power electronic circuits for PPB is no longer needed. Additionally, with a three-level flying-capacitor configuration, the voltage stresses of switching devices can be reduced more than 50% as compared to existing solutions that are based on embedded PPB. The relationship between the inductance requirement and the patterns of the modulation carriers, and how it can be utilized to minimize the magnetics of the rectifier, is also discussed. A 110 W hardware prototype is designed and tested to demonstrate the feasibilities of the proposed rectifier. An input power factor of over 0.97, peak efficiency of 95.1%, and output voltage ripple of less than 4.3%, across a wide load range have been experimentally obtained.

*Index Terms*—PFC rectifier, active power decoupling, three-level flying capacitor, automatic power decoupling.

## I. INTRODUCTION

There is a growing demand for high power density, high conversion efficiency, and high reliability ( $H^3$ ) single-phase PFC rectifiers in support of emerging technologies and applications. For example, the service lifetime of an LED driver is expected to match that of the state-of-the-art LED technologies (i.e., > 10 years) [1], [2], while the driver itself should fit inside a light bulb, which requires a high power density design of the driver [3]–[6]. A second example is that according to *Quick Charge 4+* specifications, the envisaged power rating of a next-generation mobile phone charger is 4 times higher than that of conventional chargers. A substantial increase in the power density of the chargers is expected if the chargers' sizing is unchanged [7], [8].

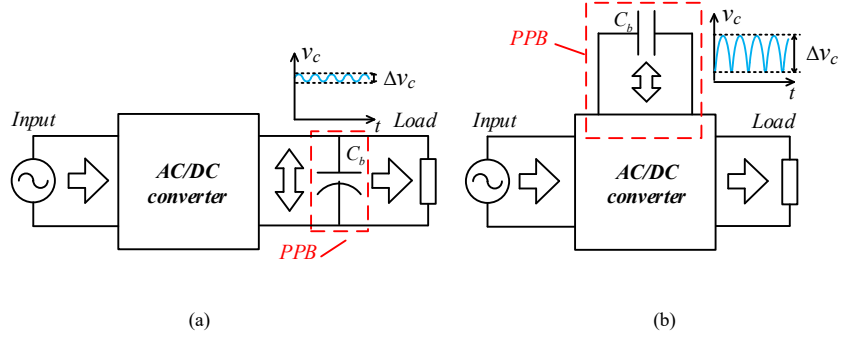


Fig. 1. (a) Power conversion architecture of conventional single-phase power converter with passive PPB and (b) three-port architecture with active PPB.

Single-phase PFC rectifiers inherently require a substantial energy storage capacity to buffer the double-line frequency power imbalance between the ac line and the dc load [9]–[13]. One effective approach to increase the power density of a PFC rectifier is to minimize the size of the system’s energy storage requirement. Fig. 1(a) and (b), respectively, depict the power conversion architecture of a conventional single-phase PFC rectifier with passive pulsating-power-buffering (PPB) and a recently proposed three-port architecture with active PPB. As opposed to the conventional configuration where an energy storage capacitance  $C_b$  is directly attached to the dc-link, the capacitance  $C_b$  of the configuration in Fig. 1(b) is decoupled from the dc-link and its voltage has the freedom to fluctuate with a larger amplitude whilst retaining a constant dc-link voltage. Here  $E_{PPB} = C_b \bar{V}_c \Delta v_c$ , where  $E_{PPB}$  is the PPB energy and is a constant irrespective of the size of  $C_b$ ,  $\Delta v_c$  is the peak-to-peak amplitude of the voltage ripple of  $C_b$ , and  $\bar{V}_c$  is the average voltage of  $C_b$ . Therefore,  $C_b$  can be drastically reduced by enlarging  $\Delta v_c$ . The power density of the rectifier is increased with a smaller  $C_b$ . It also enables non-electrolytic capacitors with prolonged lifetime and low ESR, e.g. film capacitors or laminated ceramic capacitors, to be used for PPB. This leads to high-reliability and high-efficiency system design of the rectifier.

Various types of single-phase PFC rectifiers with active PPB have been recently proposed. One possible

type is based on the direct cascade of a dc active filter to the output of a front-end PFC rectifier to perform active PPB [14], [15]. Despite the reduction of energy storage size, the need for extra power electronics to form the dc active filter contradicts the aim of system volume reduction. To simplify the circuit structure, a concept of switch integration has been proposed. In [16]–[19], the interesting idea of sharing the use of one phase leg of the front-end full-bridge PFC rectifier with that of a half-bridge dc active filter, leading to an integrated solution without additional active switches, is explored. To further reduce the number of active and passive components used, a new concept of PPB embedded switching is recently proposed [20]–[22]. In a typical two-level converter (e.g. buck converter), there are only two switching states within one switching cycle. With the PPB embedded switching, extra switching states are introduced within one switching cycle and are utilized to achieve active PPB function. This discards the need for dc active filter. In [20], [21], new single-phase topologies with PPB embedded switching have been proposed, featuring only two active switches and one inductor. A bridgeless version of this rectifier with improved power conversion efficiency is proposed in [23]. To date, among all the reported active PPB rectifiers, the single-phase rectifiers employing PPB embedded switching achieves the minimum number of active and passive components used. However, despite their merits, these rectifiers suffer badly from high voltage stress. Active switches and diodes in most of the configurations reported must withstand a voltage up to  $V_{ac}+V_{dc}$ , where  $V_{ac}$  is the peak line voltage and  $V_{dc}$  is the output voltage. This leads to higher switching losses and the mandatory use of expensive high-voltage components.

In this paper, a low-voltage-stress single-phase PFC rectifier with a three-level flying-capacitor configuration and PPB embedded switching is proposed. The number of active switches and inductors remains minimum at two and one respectively, while the flying capacitor serves two purposes of clamping the voltage stresses of all power devices and operating as a PPB capacitor. The solution effectively overcomes the drawbacks of previous solutions. The operating principles, control method, as well as design considerations of the rectifier, are detailed in Section II to IV. Section IV also provides a discussion on the relationship

between the inductance requirements versus different modulation methods, and an explanation on how this relationship can be utilized to minimize the magnetics of the rectifier. Section V presents the experimental results under various steady-state and dynamic operating conditions. Section VI give a conclusion to this paper.

## II. SINGLE-PHASE THREE-LEVEL FLYING-CAPACITOR PFC RECTIFIER WITH PPB EMBEDDED SWITCHING

### A. Circuit Configuration

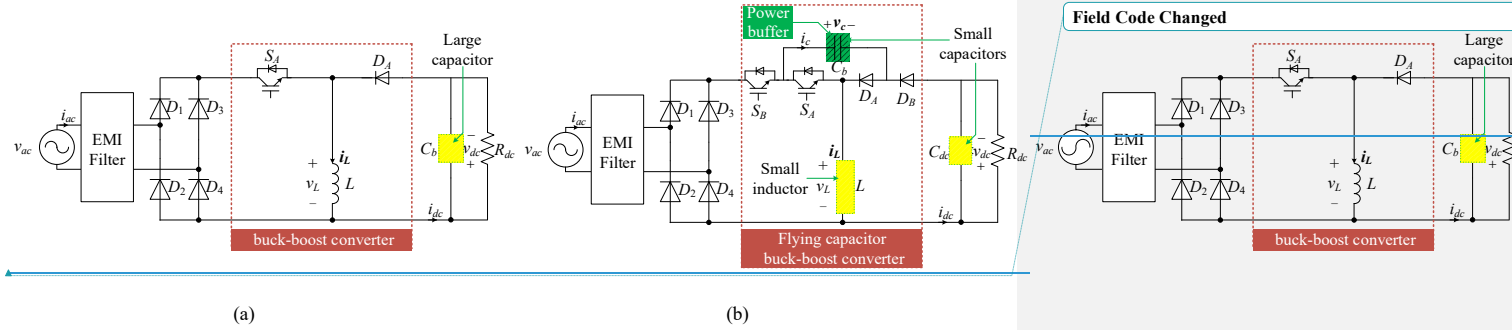


Fig. 2. Circuit diagrams of (a) conventional buck-boost PFC rectifier and (b) the proposed three-level flying-capacitor PFC rectifier based on PPB embedded switching.

Fig. 2(a) and (b) show respectively the circuit configurations of a conventional buck-boost PFC rectifier and the proposed three-level PFC rectifier with PPB embedded switching. Compared to the former, the proposed converter is augmented with one additional set of active switch  $S_B$ , diode  $D_B$  and capacitor  $C_b$ . The converter can be regarded as a buck-boost version of the conventional three-level flying-capacitor converter based on a buck converter's configuration [24]. An extra charging and discharging state of the flying capacitor  $C_b$  is created by the extra components, as will be detailed in Section II-B. Consequently, active PPB function can be embedded within each switching cycle, leading to substantially reduced requirement for  $C_b$  as compared to that of the rectifier configuration given in Fig. 1(a). Importantly, the proposed rectifier enjoys low voltage stresses for its switching devices due to the voltage clamping characteristic of the three-level configuration. Moreover, inductor  $L$  can be significantly reduced via appropriate modulation methods, as will be explained in Section IV.

### B. Operating Principles

Assuming the continuous-conduction-mode (CCM) of operation, the rectifier has four switching states as depicted in Fig. 3. Here, the electromagnetic interference (EMI) filter is neglected and the ac line voltage  $v_{ac}$  and the front-end diode bridge is [is-are](#) presented as a rectified voltage source  $|v_{ac}|$ .

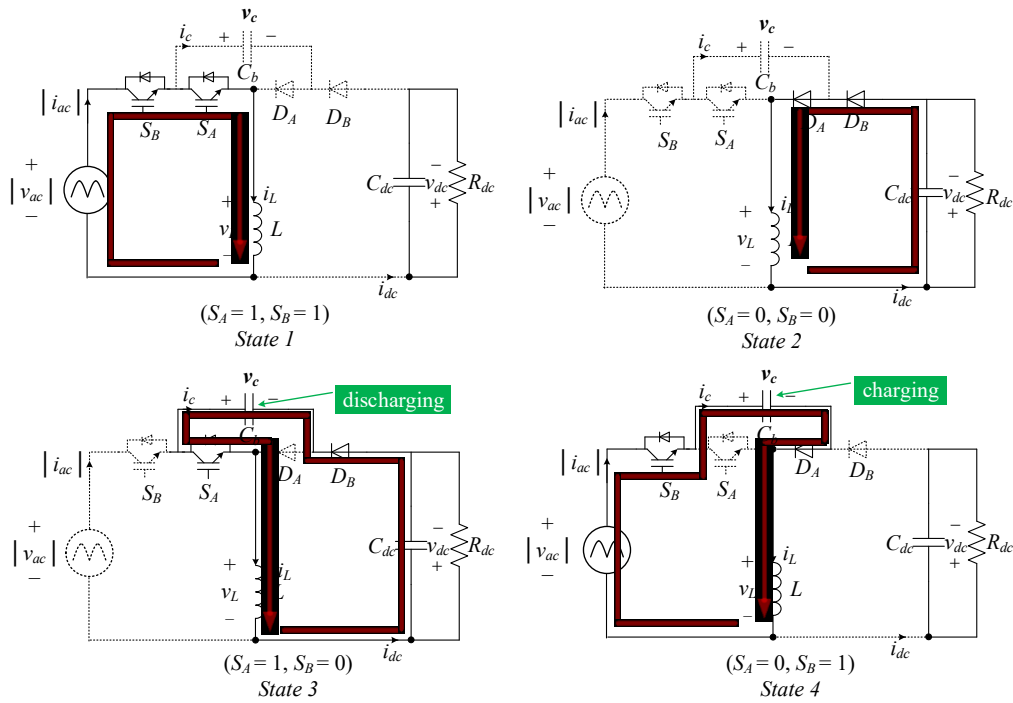


Fig. 3. Equivalent circuits of the proposed rectifier during *State 1–State 4*.

In *State 1* and *State 2*, both the active switches  $S_A$  and  $S_B$  are concurrently turned on and off, respectively, and inductor  $L$  is charged by the input voltage  $|v_{ac}|$  and discharged to the load ( $C_{dc}$  and  $R_{dc}$ ), respectively. These two switching states are identical to that of a conventional buck-boost converter. Here, the capacitor  $C_b$  is in the idle mode. In *State 3* and *State 4*,  $C_b$  is part of the power flow path. Specifically,  $C_b$  is discharged with an inductor current  $i_L$  in *State 3* and charged by  $i_L$  in *State 4*. By controlling the duration of *State 3* and *State 4*,

active PPB utilizing  $C_b$  can be achieved. The switching patterns of the four switching states, the corresponding charging/discharging states of  $C_b$ , and the inductor voltage  $v_L$  are summarized in Table I.

Table I. Summary of Switching States.

| Operating State | $S_A$ | $S_B$ | $C_b$     | $v_L$            |
|-----------------|-------|-------|-----------|------------------|
| State 1         | 1     | 1     | Idle      | $ v_{ac} $       |
| State 2         | 0     | 0     | Idle      | $-v_{dc}$        |
| State 3         | 1     | 0     | Discharge | $v_c - v_{dc}$   |
| State 4         | 0     | 1     | Charge    | $ v_{ac}  - v_c$ |

### C. Steady-State Circuit Analysis

Assuming a unity power factor and pure sinusoidal waveforms for the ac line voltage  $v_{ac}$  and current  $i_{ac}$ , i.e.,

$$\begin{cases} v_{ac} = V_{ac} \sin \omega t \\ i_{ac} = I_{ac} \sin \omega t \end{cases}, \quad (1)$$

where  $V_{ac}$  and  $I_{ac}$  are the amplitudes of  $v_{ac}$  and  $i_{ac}$ , and  $\omega$  is the line frequency, the instantaneous input power at the ac line  $p_{ac}$  can be expressed as

$$p_{ac} = v_{ac} i_{ac} = \frac{V_{ac} I_{ac}}{P_{dc}} - \frac{V_{ac} I_{ac}}{P_r} \cos(2\omega t). \quad (2)$$

Equation (2) indicates that  $p_{ac}$  consists of a constant dc power  $P_{dc}$  and a double-line-frequency pulsating power  $p_r$ . To output a stable dc power,  $p_r$  must be fully buffered by  $C_b$ . Assuming that the power in  $L$  is purely reactive and all power losses are neglected, the voltage and current of  $C_b$  can thus be calculated as [16], [25]

$$v_c = \sqrt{\bar{V}_c^2 - \frac{P_{dc}}{\omega C_b} \sin(2\omega t)}, \quad (3)$$

$$i_c = -\frac{P_{dc} \cos(2\omega t)}{\sqrt{\bar{V}_c^2 - \frac{P_{dc}}{\omega C_b} \sin(2\omega t)}}, \quad (4)$$

where  $\bar{V}_c$  is the average voltage of  $v_c$  and is a design variable.

By denoting the durations of *State 1–State 4* respectively as  $d_1T_s$ ,  $d_2T_s$ ,  $d_3T_s$  and  $d_4T_s$ , where  $T_s$  is the switching period, then  $d_1–d_4$  must comply with the equation

$$d_1 + d_2 + d_3 + d_4 = 1. \quad (5)$$

Based on Table I, the duty cycles of the switches  $S_A$  and  $S_B$  are related to  $d_1–d_4$  as

$$d_A = d_1 + d_3, \quad (6)$$

$$d_B = d_1 + d_4. \quad (7)$$

Meanwhile, with reference to Fig. 3, input current  $i_{ac}$ , output current  $i_{dc}$  and capacitor current  $i_c$  over  $T_s$  can be calculated as

$$\langle i_{ac} \rangle_{T_s} = (d_1 + d_4) \langle i_L \rangle_{T_s} = d_B \langle i_L \rangle_{T_s}, \quad (8)$$

$$\langle i_{dc} \rangle_{T_s} = (d_2 + d_3) \langle i_L \rangle_{T_s} = (1 - d_B) \langle i_L \rangle_{T_s}, \quad (9)$$

$$\langle i_c \rangle_{T_s} = (d_4 - d_3) \langle i_L \rangle_{T_s} = (d_B - d_A) \langle i_L \rangle_{T_s}, \quad (10)$$

where  $i_L$  is the averaged inductor current over  $T_s$ . It is evident from (10) that when  $d_3 > d_4$  (or  $d_A > d_B$ ),  $i_c$  is negative and  $C_b$  is discharged, and vice versa. This is consistent with the description given in Fig. 3.

Summation of (8) and (9) leads to the steady-state expression of  $i_L$  as

$$\langle i_L \rangle_{T_s} = \langle i_{ac} \rangle_{T_s} + \langle i_{dc} \rangle_{T_s}. \quad (11)$$



Hence,  $i_L$  is varying at the double-line frequency with a dc offset. Solution of (8)–(11) yields the steady-state equations of  $d_A$  and  $d_B$  as

$$\begin{cases} d_A = \frac{\langle |i_{ac}| \rangle_{T_s} - \langle i_c \rangle_{T_s}}{\langle i_L \rangle_{T_s}} = \frac{\langle |i_{ac}| \rangle_{T_s} - \langle i_c \rangle_{T_s}}{\langle |i_{ac}| \rangle_{T_s} + \langle i_{dc} \rangle_{T_s}} \\ d_B = \frac{\langle |i_{ac}| \rangle_{T_s}}{\langle i_L \rangle_{T_s}} = \frac{\langle |i_{ac}| \rangle_{T_s}}{\langle |i_{ac}| \rangle_{T_s} + \langle i_{dc} \rangle_{T_s}} \end{cases} \quad (12)$$

To ensure the circuit operation,  $d_A$  and  $d_B$  in (12) must be within the range of 0–100%. Therefore, the first operating constraint of the rectifier is

$$\langle -i_{dc} \rangle_{T_s} \leq \langle i_c \rangle_{T_s} \leq \langle |i_{ac}| \rangle_{T_s}. \quad (13)$$

According to Fig. 3, a second operating constraint of the rectifier is

$$|v_{ac}| + V_{dc} \geq v_c. \quad (14)$$

Equation (14) ensures that  $D_B$  is reverse biased and turned OFF in *State 1* and *State 4*.

Solution of (13) indicates that the output voltage  $V_{dc}$  has a lower boundary of

$$V_{dc} \geq \frac{V_{ac}}{2}, \quad (15)$$

which can be explained using (34) in Section IV.

The voltage conversion characteristics of the rectifier can be obtained as follows. By averaging (2) over a line period  $T_{line}$  and utilizing (8) and (9), one yields

$$\langle v_{dc} \rangle = \frac{\langle d_B |v_{ac}| \langle i_L \rangle_{T_s} \rangle_{T_{line}}}{\langle (1-d_B) \langle i_L \rangle_{T_s} \rangle_{T_{line}}}. \quad (16)$$

Equation (16) shows the steady-state voltage conversion characteristics of the proposed rectifier. It resembles that of the conventional buck-boost converter, except that there are extra averaging operator and inductor current term in the denominator and numerator, respectively. Based on (15) and (16), the rectifier can theoretically give any positive output voltage higher than  $V_{ac}/2$  provided that the operating constraints of (13) and (14) are satisfied.

#### D. Gate signal generation

The gate signal generation method is not unique. According to (8)–(10), duty ratios  $d_1$ ,  $d_2$  and  $d_4$  can be expressed in terms of  $d_3$  as

$$\begin{cases} d_1 = \frac{\langle i_{ac} \rangle_{T_s} - \langle i_c \rangle_{T_s}}{\langle i_L \rangle_{T_s}} - d_3 = \frac{\langle i_{ac} \rangle_{T_s} - \langle i_c \rangle_{T_s}}{\langle i_{ac} \rangle_{T_s} + \langle i_{dc} \rangle_{T_s}} - d_3 \\ d_2 = \frac{\langle i_{dc} \rangle_{T_s}}{\langle i_L \rangle_{T_s}} - d_3 = \frac{\langle i_{dc} \rangle_{T_s}}{\langle i_{ac} \rangle_{T_s} + \langle i_{dc} \rangle_{T_s}} - d_3 \\ d_4 = \frac{\langle i_c \rangle_{T_s}}{\langle i_L \rangle_{T_s}} + d_3 = \frac{\langle i_c \rangle_{T_s}}{\langle i_{ac} \rangle_{T_s} + \langle i_{dc} \rangle_{T_s}} + d_3 \end{cases} \quad (17)$$

Equation (17) suggests that there is freedom in choosing  $d_3$ , which leads to different  $d_1$ ,  $d_2$ ,  $d_4$  and thus different inductor current ripples. The patterns of the signal carriers for modulating  $d_A$  and  $d_B$  have a direct impact on  $d_3$ . Fig. 4 shows one possible modulation strategy where  $d_A$  and  $d_B$  are modulated using two 180° phase-shifted triangular carriers, *Carrier\_a* and *Carrier\_b*, respectively. Phase-shifted modulation is commonly adopted for controlling multilevel converters to boost the effective switching frequency, resulting in a minimized volume of the magnetics [13], [24], [26].

As shown in Fig. 4, the active switching states are *State 1*, *State 3* and *State 4* when  $d_A + d_B \geq 1$ , while they change to *State 2*, *State 3* and *State 4* when  $d_A + d_B < 1$ . In both scenarios, the voltage across the inductor is switched between three voltage levels. Mathematically, this means

$$\begin{cases} d_1 + d_3 + d_4 = 1 & (d_A + d_B \geq 1) \\ d_2 + d_3 + d_4 = 1 & (d_A + d_B < 1) \end{cases} \quad (18)$$

Solution of (17) and (18) leads to the steady-state duty ratios of  $d_1$ – $d_4$  as shown in (19) and (20).

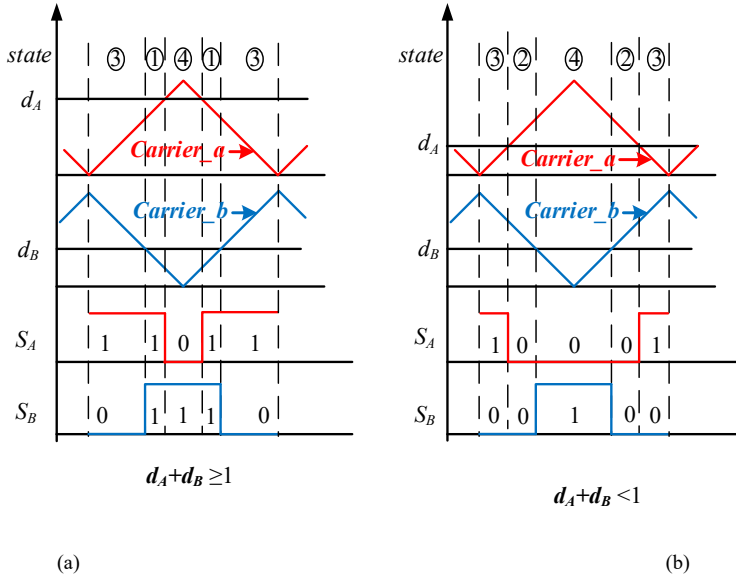


Fig. 4. Gate signal patterns for  $S_A$  and  $S_B$  generated by two  $180^\circ$ -shifted triangular carriers when (a)  $d_A + d_B \geq 1$  and (b)  $d_A + d_B < 1$ .

$$\begin{cases} d_1 = d_A + d_B - 1 = \frac{\langle i_{ac} \rangle_{T_s} - \langle i_c \rangle_{T_s} - \langle i_{dc} \rangle_{T_s}}{\langle i_{ac} \rangle_{T_s} + \langle i_{dc} \rangle_{T_s}} \\ d_2 = 0 \\ d_3 = d_A - d_1 = \frac{\langle i_{dc} \rangle_{T_s}}{\langle i_{ac} \rangle_{T_s} + \langle i_{dc} \rangle_{T_s}} \\ d_4 = d_B - d_1 = \frac{\langle i_c \rangle_{T_s} + \langle i_{dc} \rangle_{T_s}}{\langle i_{ac} \rangle_{T_s} + \langle i_{dc} \rangle_{T_s}} \end{cases} \quad (d_A + d_B \geq 1), \quad (19)$$

$$\begin{cases}
 d_1 = 0 \\
 d_2 = 1 - d_A - d_B = \frac{\langle i_{dc} \rangle_{T_s} - \langle |i_{ac}| \rangle_{T_s} + \langle i_c \rangle_{T_s}}{\langle |i_{ac}| \rangle_{T_s} + \langle i_{dc} \rangle_{T_s}} \\
 d_3 = d_A = \frac{\langle |i_{ac}| \rangle_{T_s} - \langle i_c \rangle_{T_s}}{\langle |i_{ac}| \rangle_{T_s} + \langle i_{dc} \rangle_{T_s}} \\
 d_4 = d_B = \frac{\langle |i_{ac}| \rangle_{T_s}}{\langle |i_{ac}| \rangle_{T_s} + \langle i_{dc} \rangle_{T_s}}
 \end{cases} \quad (d_A + d_B < 1). \quad (20)$$

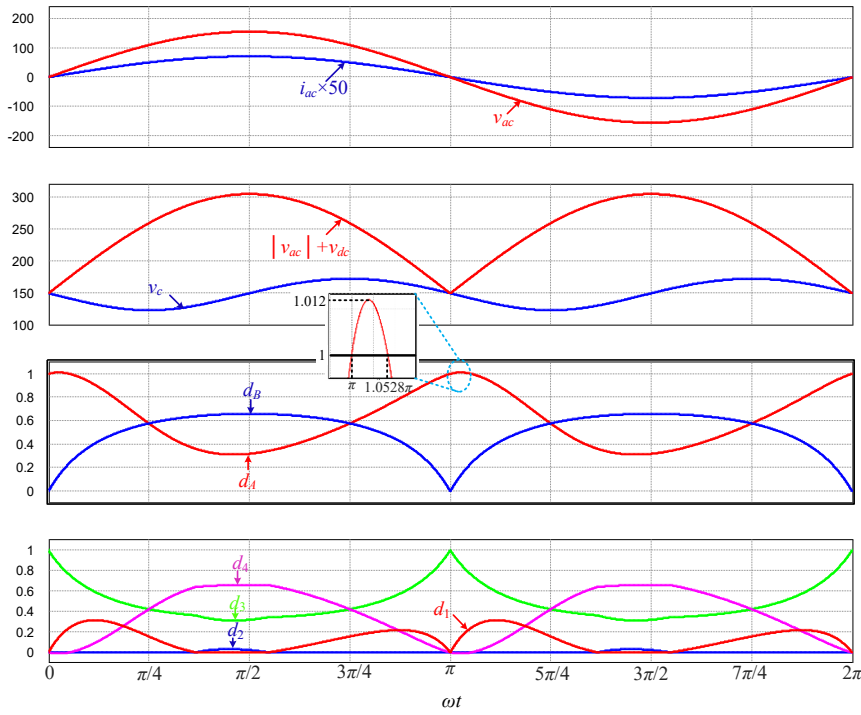


Fig. 5. Calculated  $d_1$ – $d_4$ ,  $d_A$ ,  $d_B$  and the key system operating waveforms.

Fig. 5 depicts the calculated waveforms of  $|v_{ac}| + v_{dc}$ ,  $v_c$ ,  $d_1$ – $d_4$ ,  $d_A$  and  $d_B$  based on (1), (3), (12), (19) and (20) during a line period for a 110 W rectification system, where the average voltage of  $v_c$  over a line period

is chosen as  $\bar{v}_c = V_{dc}$  (110 V<sub>rms</sub> ac input, and 150 V dc output). The detailed specifications used in the calculation can be found in Section IV and V. It is shown that operating constraint (14) is always satisfied and  $d_B$  falls within the range of 0–100%. However, the calculated  $d_A$  marginally exceeds the limit of 100% at around the zero-crossing instant of the line voltage for a very short interval, and will be bounded at 100% in a practical design. According to (12),  $d_A$  exceeding 100% indicates that  $-i_{dc} > i_c$  during this short interval and thus the constraints in (13) are violated. In practice, however, this is generally not a problem because (i)  $i_{ac}$  and  $i_{dc}$  can still be precisely regulated according to (8) and (9) through the control of  $d_B$ , and (ii) the period of  $d_A$  exceeding 100% can be designed very short by properly selecting  $C_b$ , as will be demonstrated in Section IV.

### III. ENHANCED AUTOMATIC POWER DECOUPLING CONTROL

Theoretically, an open-loop control based on (12) can be employed to achieve the desired circuit operation. However, a practical converter inevitably possesses power losses, component tolerances and nonlinearities, which must be properly compensated through a closed-loop control. As discussed in [27], a three-port PFC rectifier in Fig. 1(b) is essentially a highly coupled and highly nonlinear system. In this paper, the nonlinear control method known as Enhanced Automatic Power Decoupling (E-APD) control that has been proposed in [27], is adopted. The controller can numerically transform the original system into two fully decoupled and linear subsystems to achieve enhanced robustness and stability via a simple control structure.

According to Fig. 3, the state-space-averaged equations of the rectifier can be obtained as

$$\begin{cases} L \frac{di_L}{dt} = d_B |v_{ac}| - (1 - d_B)v_{dc} - (d_A - d_B)v_c \\ C_{dc} \frac{dv_{dc}}{dt} = -\frac{v_{dc}}{R_{dc}} + d_A i_L \\ C_b \frac{dv_c}{dt} = (d_B - d_A)i_L \end{cases} \quad (21)$$

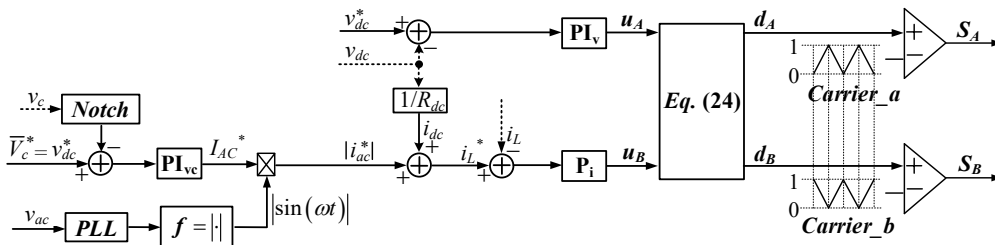
The three differential equations in (21) describe the dynamics at the ac port (i.e.,  $i_L$ ), dc port (i.e.,  $v_{dc}$ ) and the ripple port (i.e.,  $v_c$ ), respectively. Equation (21) also indicates that the system is coupled (between the system dynamics and the two control inputs (i.e.,  $d_A$  and  $d_B$ )) and nonlinear (due to the multiplying operation of the control inputs and system states). The E-APD control strategy requires the ac and dc port dynamics to be the control outputs. Therefore, two new control inputs,  $u_A$  and  $u_B$ , are introduced such that

$$\begin{cases} L \frac{di_L}{dt} = u_B \\ C_{dc} \frac{dv_{dc}}{dt} = -\frac{v_{dc}}{R_{dc}} + u_A \end{cases}, \quad (22)$$

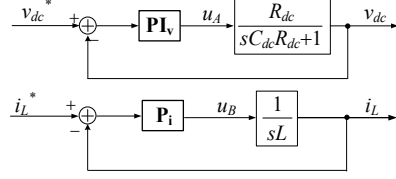
where  $u_A$  and  $u_B$  are, respectively,

$$\begin{cases} u_A = d_A i_L \\ u_B = d_B |v_{ac}| - (1 - d_B) v_{dc} - (d_A - d_B) v_c \end{cases}. \quad (23)$$

Equation (22) describes two decoupled and first-order linear subsystems, where  $i_L$  and  $v_{dc}$  can be individually controlled by  $u_A$  and  $u_B$ . Conventional linear controllers can then be easily designed to achieve the desired steady-state and dynamic performance. With the E-APD control, the dynamics at the ripple-port, i.e.,  $v_c$ , is indirectly controlled and no dedicated PPB control is needed. This is because any power imbalance between the ac-port and dc-port power (which are determined by  $i_L$  and  $v_{dc}$ ) shall be automatically transferred to the ripple port according to the energy conservation principle.



(a)



(b)

Fig. 6. (a) Overall control diagrams of the employed enhanced automatic-power-decoupling control and (b) its equivalent closed-loop diagram.

Fig. 6 (a) shows the complete control block diagram of the proposed PFC rectifier. Here  $u_A$  and  $u_B$  are firstly obtained from a proportional-Integral (PI) and a proportional (P) compensator, i.e.,  $PI_v$  and  $PI_i$ , respectively, which are converted into  $d_A$  and  $d_B$  and then modulated for generating the gate driving signals. The feedback-linearization-decoupling law for converting the new control inputs (i.e.,  $u_A$  and  $u_B$ ) back to the original control inputs (i.e.,  $d_A$  and  $d_B$ ) can be derived by solving (23) as

$$\begin{cases} d_A = \frac{u_A}{i_L} \\ d_B = \frac{u_B + v_{dc} - d_A v_c}{|v_{ac}| + v_{dc} - v_c} \end{cases} \quad (24)$$

The equivalent closed-loop diagram of Fig. 6(a) is depicted in Fig. 6(b) based on (22), from which  $PI_v$  and  $PI_i$  can be designed following the same procedures as discussed in [27]. In Fig. 6(a), the reference signal  $i_L^*$  is obtained by summing the rectified line current reference  $|i_{ac}^*|$  and the output current  $i_{dc}$  according to (11), where  $|i_{ac}^*|$  is obtained from an outer voltage loop regulating  $\bar{V}_c$  at  $\bar{V}_c^*$  and  $i_{dc}$  is estimated from  $v_{dc}$  for simplicity. Here,  $\bar{V}_c^* = v_{dc}^*$  is selected to meet the operating constraint of (14) whilst maximizing the voltage fluctuation range of  $v_c$ . A notch filter with a stopping band at the double-line frequency is employed to extract  $\bar{V}_c$ .

#### IV. DESIGN CONSIDERATIONS

##### A. Active Switches and Diodes Design

The voltages across the power devices of the proposed PFC rectifier during *State 1–State 4* are shown in Table II, based on which their minimum voltage ratings are also calculated. Due to the flying capacitor configuration, the minimum voltage ratings of  $S_A$  and  $D_A$  (i.e.,  $V_A$ ) are equal to  $V_{cmax}$  (i.e., the maximum voltage of  $v_c$ ),

$$V_A = V_{cmax} = \sqrt{V_{dc}^2 + \frac{P_{dc}}{\omega C_b}}, \quad (25)$$

while the minimum voltage ratings for  $S_B$  and  $D_B$  (i.e.,  $V_B$ ) are equal to the maximum voltage of  $v_{dc} + |v_{ac}| - v_c$ ,

$$V_B = \max_{0 \leq t \leq T_{line}} \{v_{dc} + |v_{ac}| - v_c\} = \max_{0 \leq t \leq T_{line}} \left\{ V_{dc} + |V_{ac} \sin \omega t| - \sqrt{V_{dc}^2 - \frac{P_{dc}}{\omega C_b} \sin(2\omega t)} \right\}. \quad (26)$$

Table II. Voltage stresses and minimum voltage ratings for  $D_1–D_4$ ,  $D_A$ ,  $D_B$ ,  $S_A$  and  $S_B$ .

| Operating State        | $S_A$      | $D_A$      | $S_B$                             | $D_B$                             | $D_1–D_4$ |
|------------------------|------------|------------|-----------------------------------|-----------------------------------|-----------|
| State 1                | 0          | $v_c$      | 0                                 | $v_{dc} +  v_{ac}  - v_c$         |           |
| State 2                | $v_c$      | 0          | $v_{dc} +  v_{ac}  - v_c$         | 0                                 |           |
| State 3                | 0          | $v_c$      | $v_{dc} +  v_{ac}  - v_c$         | 0                                 |           |
| State 4                | $v_c$      | 0          | 0                                 | $v_{dc} +  v_{ac}  - v_c$         |           |
| Minimum voltage rating | $V_{cmax}$ | $V_{cmax}$ | $\max\{v_{dc} +  v_{ac}  - v_c\}$ | $\max\{v_{dc} +  v_{ac}  - v_c\}$ | $V_{ac}$  |

In Fig. 7,  $V_A$  and  $V_B$  are compared against  $V_{ac}+V_{dc}$  with respect to different (i) output voltage, (ii) output power, and (iii) PPB capacitance. Based on Fig. 7, the following observations can be made:

- (1) In Fig. 7(a),  $V_A$  scales almost linearly with  $V_{dc}$  while  $V_B$  remains approximately constant at  $V_{ac}$ . The linearity of  $V_A$  versus  $V_{dc}$  is evident from (25), as  $V_A \approx V_{dc}$  if  $V_{dc}^2 \gg \frac{P_{dc}}{\omega C_b}$ , while the quasi-constant



characteristic of  $V_B$  is mainly due to (26) that  $V_B = \max_{0 \leq t \leq T_{ine}} \{ |v_{ac}| + \Delta v_c \} \approx \max_{0 \leq t \leq T_{ine}} \{ |v_{ac}| \} = V_{ac}$  provided that the

voltage ripple  $\Delta v_c$  is sufficiently small as compared to  $V_{ac}$ . The above observations indicate that operating

the rectifier at a low  $V_{dc}$  helps to reduce the voltage stress of  $V_A$  and the switching loss of  $S_A$ . However, a low

$V_{dc}$  leads to high conduction losses especially in the output diodes  $D_A$  and  $D_B$ . If  $V_{dc}$  can be chosen, An optimal  $V_{dc}$  might

be selected close to  $V_{ac}$  (i.e., here  $V_{ac} = 155$  V), in this situation, when  $V_A \approx V_B \approx V_{dc} \approx V_{ac}$ . This not only ensures

a low profile of the conduction loss but also enables power devices with similar voltage ratings to be selected;

(2) In Fig. 7(b),  $V_{dc}$  is fixed at 150 V. Both  $V_A$  and  $V_B$  increase almost linearly with  $P_{dc}$  but at a very slow rate. This is because  $V_A \approx V_B \approx V_{dc} \approx V_{ac}$  which are almost constant as mentioned above for Fig. 7(a). The slight deviation of  $V_A$  and  $V_B$  from  $V_{dc}$  at different  $P_{dc}$  is mainly due to the increased voltage ripple  $\Delta v_c$  as  $P_{dc}$  increases. Overall,  $V_A$  and  $V_B$  exhibit almost similar maximum voltage stresses within a wide load range when  $V_{dc} \approx V_{ac}$  is selected;

(3) In Fig. 7(c), both  $V_A$  and  $V_B$  are found decreasing with the increase of  $C_b$  for a constant  $V_{dc}$  and  $P_{dc}$ . Again, this is simply because a larger  $C_b$  leads to a smaller  $\Delta v_c$ ;

(4) The voltage stresses of  $V_A$  and  $V_B$  are approximately half of  $V_{ac} + V_{dc}$  for a wide range of  $P_{dc}$  and  $C_b$  combinations when  $V_{dc} \approx V_{ac}$ , as  $V_A \approx V_B \approx V_{dc} \approx V_{ac}$ .

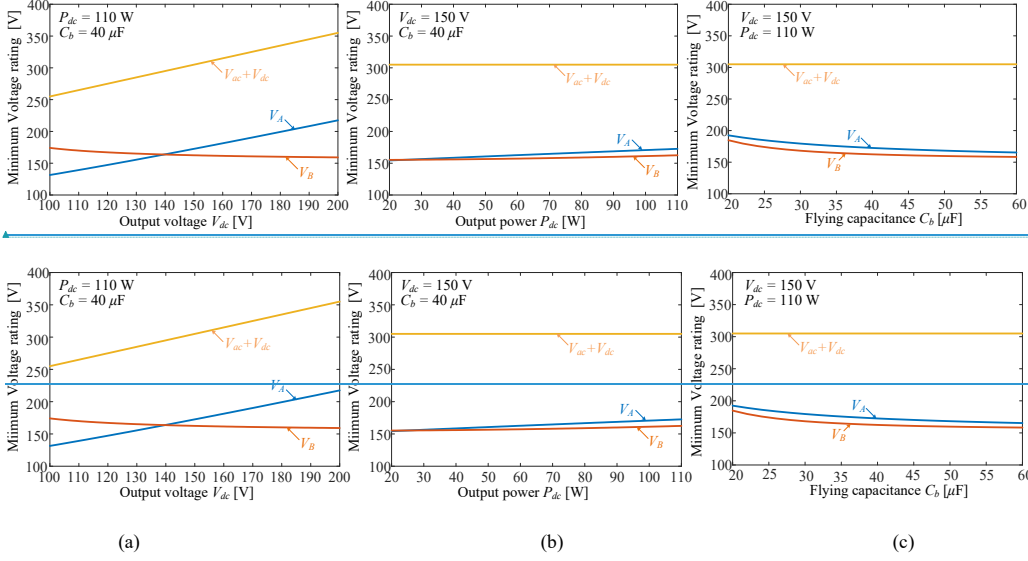


Fig. 7. The minimum voltage stresses versus (a) output voltage, (b) output power and (c) flying capacitance.

### B. Flying Capacitor Design

With the objective of power density improvement,  $C_b$  should be minimized under the constraints of (13) and (14) whilst ensuring that the voltage ratings of all power devices are not exceeded.

Firstly, according to (3) and (4) and noticing  $\bar{V}_c = V_{dc}$ ,  $v_c$  and  $i_c$  can be expressed as

$$v_c = \sqrt{V_{dc}^2 - \frac{P_{dc}}{\omega C_b}} \sin(2\omega t), \quad (27)$$

$$i_c = -\frac{P_{dc} \cos(2\omega t)}{\sqrt{V_{dc}^2 - \frac{P_{dc}}{\omega C_b}}}. \quad (28)$$

In the meantime, it is assumed that the variation range of  $d_A$  and  $d_B$  are

$$\begin{cases} 0 \leq d_A \leq 1 + \varepsilon \\ 0 \leq d_B \leq 1 \end{cases}, \quad (29)$$

where  $\varepsilon > 0$  is the incremental duty cycle exceeding 100%, as explained in Section II, and is a design choice. A smaller  $\varepsilon$  implies a shorter duration of the period when  $d_A$  is clamped at 100%. By combining (12), (14), and (29), one obtains the precise operating constraints of the rectifier as

$$\begin{cases} -(1+\varepsilon)i_{dc} - \varepsilon|i_{ac}| \leq i_c \leq |i_{ac}| \\ v_c \leq |v_{ac}| + v_{dc} \end{cases}. \quad (30)$$

Solution of (30) using (27) and (28) leads to the first design constraint of  $C_b$  as:

$$C_b \geq \max \{C_{b1}, C_{b2}, C_{b3}\}, \quad (31)$$

where

$$C_{b1} = \max_t \left( \frac{P_{dc} \sin(2\omega t)}{-\omega V_{ac} (2V_{dc} |\sin \omega t| + V_{ac} |\sin^2 \omega t|)} \right), \quad \omega t \in (0, 2\pi], \quad (32)$$

$$C_{b2} = \max_t \left( \frac{P_{dc} \sin(2\omega t)}{\omega \left[ V_{dc}^2 - \left( \frac{V_{dc} \cos(2\omega t)}{(1+\varepsilon) + \frac{2\varepsilon V_{dc} |\sin \omega t|}{V_{ac}}} \right)^2 \right]} \right), \quad \omega t \in \left( 0, \frac{\pi}{4} \right) \cup \left( \frac{3\pi}{4}, \frac{5\pi}{4} \right) \cup \left( \frac{7\pi}{4}, 2\pi \right), \quad (33)$$

$$C_{b3} = \frac{P_{dc}}{\omega \left( V_{dc}^2 - \left( \frac{V_{ac}}{2} \right)^2 \right)}. \quad (34)$$

For  $\varepsilon = 2\%$ ,  $P_{dc} = 110$  W,  $V_{dc} = 150$  V, and  $V_{ac} = 155$  V, it can be numerically determined that  $C_{b1} = 12.55$   $\mu\text{F}$ ,  $C_{b2} = 12.97$   $\mu\text{F}$ , and  $C_{b3} = 17.69$   $\mu\text{F}$ . Then according to (31),  $C_b \geq 17.69$   $\mu\text{F}$

Secondly, the design constraints of  $C_b$  regarding the voltage ratings of all power devices can be resolved based on (25), (26) and Fig. 7(c), given  $V_A \leq V_{A_d}$  and  $V_B \leq V_{B_d}$ . Fig. 7(c) shows that both  $V_A$  and  $V_B$  increase monotonically with the reduction of  $C_b$ . Therefore, the minimum  $C_b$  complying with the voltage stresses requirement can be easily determined. For example, given  $V_{A_d} = V_{B_d} = 175$  V, Fig. 7(c) indicates that

$$C_b \geq C_{b4}, \quad (35)$$

where  $C_{b4} = 36 \mu\text{F}$  can be identified. The final selection of  $C_b$  must satisfy both (31) and (35). Therefore,  $C_b = 40 \mu\text{F}$  is selected in this design.

### C. Inductor Design

The inductor  $L$  should be designed such that (i) the rectifier operates in the CCM and (ii) the high-frequency inductor current ripple  $\Delta i_L$  is less than a pre-specified value  $\Delta i_{L\_rated}$ .

The CCM operation requires that

$$\Delta i_L < 2i_L. \quad (36)$$

According to (11), the minimum value of  $i_L$  during  $T_{line}$  is  $I_{dc}$  when  $i_{ac} = 0$ . As the maximum value of  $\Delta i_L$  is  $\Delta i_{L\_rated}$ , a sufficient condition for ensuring CCM operation is

$$\Delta i_{L\_rated} < 2I_{dc\_min}. \quad (37)$$

where  $I_{dc\_min}$  is the minimum load current.

To satisfy design criteria (ii), the peak-to-peak inductor current ripple  $\Delta i_L$  needs to be resolved. The patterns of the carriers for modulating  $d_A$  and  $d_B$  have a major impact on  $\Delta i_L$  and thereby leading to different inductance requirement. In this study, four typical carrier patterns are studied (depicted in Fig. 8), namely, a pair of triangular carriers which are in phase and  $180^\circ$  phase-shifted (carrier pair  $w$  and  $x$ , respectively), and a pair of sawtooth carriers which are in phase and out of phase (carrier pair  $y$  and  $z$ , respectively). Here, carriers pair  $x$  is employed as an illustrative example for calculating  $\Delta i_L$ .

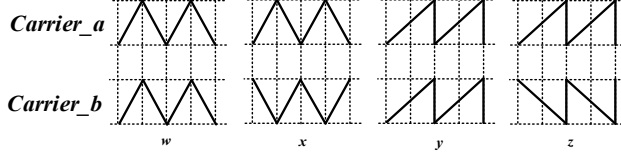


Fig. 8. Four patterns of tested carriers.

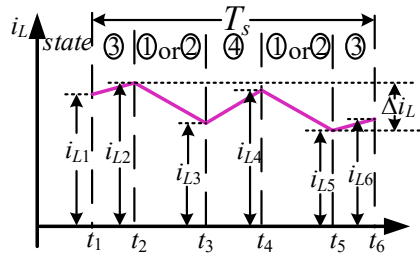


Fig. 9. Schematic diagram of the inductor current with carriers pair  $x$  during one switching period.

The inductor current waveform within one switching cycle is depicted in Fig. 9. At instances  $t_1-t_6$ ,  $i_L$  reaches its peaks or valleys of  $i_{L_n}$ , respectively, where  $n \in \{1,2,3,4,5,6\}$ , and

$$i_{L(m+1)} = i_{L_m} + \Delta i_{L_m}, \quad m \in \{1,2,3,4,5\}, \quad (38)$$

with  $\Delta i_{L_m}$  being the incremental inductor current during the interval from  $t_m$  to  $t_{m+1}$ . According to the annotated switching states as shown in Fig. 9,  $\Delta i_{L_m}$  can be derived as

$$\left\{ \begin{array}{l} \Delta i_{L1} = \frac{\gamma_1}{L} = \frac{d_3 T_s (v_c - v_{dc})}{2L} \\ \Delta i_{L2} = \frac{\gamma_2}{L} = \begin{cases} \frac{d_1 T_s |v_{ac}|}{2L} & (d_A + d_B \geq 1) \\ -\frac{d_2 T_s v_{dc}}{2L} & (d_A + d_B < 1) \end{cases} \\ \Delta i_{L3} = \frac{\gamma_3}{L} = \frac{d_4 T_s}{L} (|v_{ac}| - v_c) \\ \Delta i_{L4} = \frac{\gamma_4}{L} = \begin{cases} \frac{d_1 T_s |v_{ac}|}{2L} & (d_A + d_B \geq 1) \\ -\frac{d_2 T_s v_{dc}}{2L} & (d_A + d_B < 1) \end{cases} \\ \Delta i_{L5} = \frac{\gamma_5}{L} = \frac{d_3 T_s (v_c - v_{dc})}{2L} \end{array} \right. \quad (39)$$

The peak-to-peak inductor current ripple  $\Delta i_L$  during the  $k$ th switching period is therefore

$$\Delta i_L [k] = \max \{i_{L1}[k], L i_{L6}[k]\} - \min \{i_{L1}[k], L i_{L6}[k]\}, \quad (40)$$

which is a function of  $L$ . The minimum inductance  $L_{\min}$  can be obtained by equating the maximum  $\Delta i_L$  over  $T_{line}$  to  $\Delta i_{L\_rated}$  with the aid of (1), (19), (20) and (27) and is resolved as

$$L_{\min} = \frac{1}{\Delta i_{L\_rated}} \max_k \left( \max \left\{ 0, \sum_1^{i=1} \gamma_i [k], L \sum_1^{i=5} \gamma_i [k] \right\} - \min \left\{ 0, \sum_1^{i=1} \gamma_i [k], L \sum_1^{i=5} \gamma_i [k] \right\} \right), \quad k \in [1, T_{line}/T_s], \quad (41)$$

Following a similar calculation procedure,  $\Delta i_L$  for other carrier pairs in Fig. 8 can be obtained and their corresponding  $L_{\min}$  can be determined. The minimum inductance requirement for the conventional buck-boost PFC rectifier in Fig. 2(a) is also calculated as

$$L'_{\min} = \max \left\{ \frac{v_{dc} |v_{ac}| T_s}{(v_{dc} + |v_{ac}|) \Delta i_{L\_rated}} \right\}, \quad (42)$$

given the same ripple requirement and CCM operation.

In Fig. 10(b) and (c), the **normalized** minimum inductance requirement ( $L_{\min} / L'_{\min}$ ) for the proposed rectifier with four types of carrier pair are compared at different  $P_{dc}$  and  $V_{dc}$ , respectively. Here,  $\Delta i_{L\_rated} = 0.6$  A,  $C_b = 40 \mu\text{F}$ ,  $f_s = 25 \text{ kHz}$  are selected in order to perform the calculation. With reference to these curves, the following observation can be made:

(1) In both Fig. 10(a) and (b), firstly,  $L_{\min}$  for carrier pair  $x$  is found identical to that of  $z$  (both are out-of-phase carrier pair), while that for  $w$  is identical to that for  $y$  (both are in-phase carrier pair). Secondly,  $L_{\min}$  for  $x$  and  $z$  is much smaller than that for  $w$  and  $y$  throughout the whole  $P_{dc}$  and  $V_{dc}$  range (e.g., at  $V_{dc} = 128$  V, an inductance reduction of more than 60% can be obtained.) The results suggest that out-of-phase carriers are highly effective in minimizing the magnetics of the proposed rectifier. Thirdly,  $L_{\min}$  for all types of carrier pair is smaller than  $L'_{\min}$ . This is expected as the proposed rectifier employs a three-level structure while the conventional buck-boost PFC rectifier is a two-level switching converter;

(2) In Fig. 10(a),  $L_{\min}$  for  $w$  and  $y$  is almost constant while that for  $x$  and  $z$  scales linearly with  $P_{dc}$ . Therefore,  $L_{\min}$  should be designed at full load power;

(3) In Fig. 10(b),  $L_{\min}$  for  $w$  and  $y$  increases with the output voltage, while that for  $x$  and  $z$  firstly decreases and then increases with  $V_{dc}$ . The curve suggests that for wide-output-voltage-range applications,  $L_{\min}$  should be selected based on the maximum  $V_{dc}$  when  $w$  or  $y$  is selected, while  $L_{\min}$  should be designed based on the minimum and the maximum  $V_{dc}$  with  $x$  or  $z$ .

Per above discussions,  $L = 2.5$  mH can be selected for a 100 V–200 V output, 110 W system modulated with carriers pair  $x$  or  $z$ .

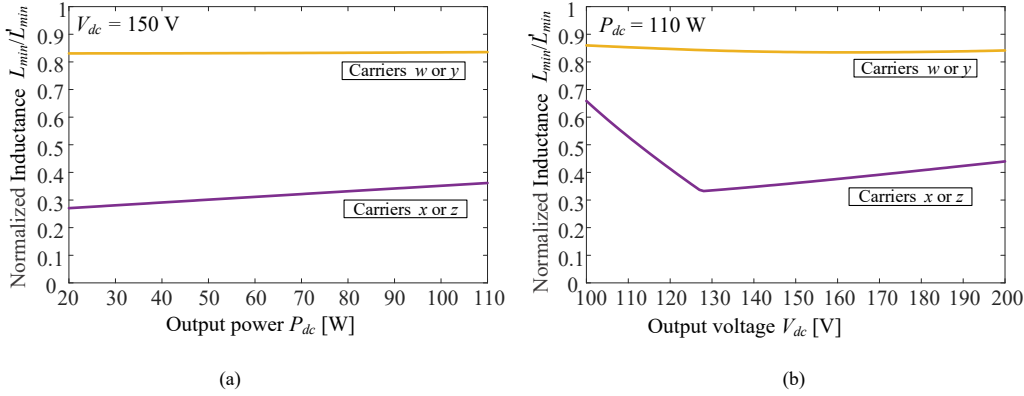


Fig. 10. The normalized minimum inductance requirement for the proposed PFC rectifier with four types of carrier pair versus (a) output power and (b) output voltage.

#### D. Comparison with Prior-Art Buck-Boost-Derived PFC Rectifiers

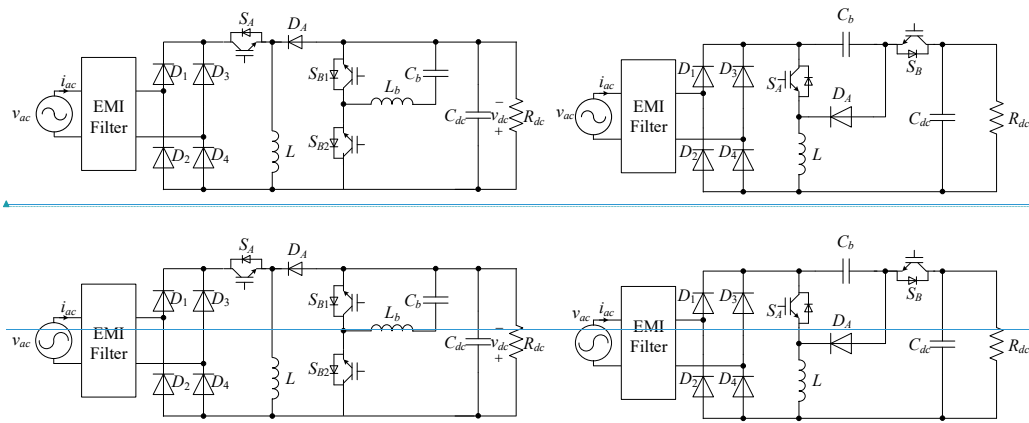
Compared with boost-type PFC rectifier, the key merit of the buck-boost type PFC rectifier is its wider output voltage range (including voltage-buck capability). Therefore, it is more suitable buck-boost PFC rectifier in the application requiring wider dc voltage range, such as speed controlled dc motor drivers and dimming LED drivers. Also, the buck-boost PFC rectifier can be used as a front-end PFC rectifier with lower output dc voltage than its boost-type counterpart for e.g. PC, laptop adapters or LED drivers. As a result, a lower voltage rating switches with lower switching and conduction loss can be selected for the second stage downstream dc/dc converter.

Four circuit topologies based on the buck-boost PFC rectifiers are examined and compared. They are listed as follows:

1. Circuit-A: conventional buck-boost rectifier shown in Fig. 2(a);
2. Circuit-B: a buck-boost rectifier cascaded by a buck-type dc active filter shown in Fig. 11(a);
3. Circuit-C: a previously proposed PPB embedded switching PFC rectifier shown in Fig 11. (b) [21];
4. Circuit-D: the proposed three-level flying-capacitor PFC rectifier shown in Fig 2(b).



The comparison is conducted with respect to ten key figure-of-merits (See Table III), including the number of active switches and inductors used, size of buffering capacitance, level of voltage stresses of the semiconductor switches, and size of the inductance required, etc. All the topologies are evaluated under the same conditions:  $f_{sw} = 25$  kHz,  $P_{dc} = 110$  W,  $V_{dc} = 150$  V,  $V_{ac} = 155$  V, and  $\Delta i_{L\_rated} = 0.6$  A for the inductor. The buffering capacitance of the conventional buck-boost PFC rectifier is designed for a 5% peak-to-peak dc voltage ripple, while that for the other three topologies are designed assuming  $\Delta v_c = 33\%$  of  $V_{dc}$ .



Field Code Changed

Fig. 11. (a) Buck-boost rectifier cascaded by a buck-type dc active filter, and (b) PPB embedded switching buck-boost PFC rectifier in [21].

Table III. Comparison of the Proposed Circuit with Prior-Art Buck-Boost PFC Rectifiers.

|   | Buck-Boost Rectifier (Fig. 2(a)) | Buck-Boost Rectifier Cascaded by a dc Filter (Fig. 11(a)) | PPB Embedded Switching Rectifier (Fig. 11(b)) | Proposed Rectifier (Fig. 2(b)) |
|---|----------------------------------|---|---|--------------------------------|
| Power Buffering Method                  | Passive                          | Active  | Active  | Active                         |
| Buffering Capacitance $C_b$ ( $\mu F$ ) | 259.5                            | 46.7  | 20.1  | 40.0                           |

|  |            |  |                          |                          |
|--|------------|--|--------------------------|--------------------------|
| Peak Voltage of Buffering Capacitor (V)                | 150        | 150  | 360                      | 175                      |
| Maximum Storage Energy of Buffering Capacitor (J)      | 5.8        | 1.1  | 2.6                      | 1.2                      |
| Number of Active Switches                              | 1          | 3  | 2                        | 2                        |
| Number of Inductors                                    | 1          | 2  | 1                        | 1                        |
| Voltage Stress of Active Switches (V)                  | $S_A: 305$ | $S_A: 305$<br>$S_{B1}: 150$<br>$S_{B2}: 150$ | $S_A: 360$<br>$S_B: 187$ | $S_A: 175$<br>$S_B: 175$ |
| Voltage Stress of Diodes (except for diode bridge) (V) | $D_A: 305$ | $D_A: 305$                                   | $D_A: 360$               | $D_A: 150$<br>$D_B: 175$ |
| Main Inductance $L$ (mH)                               | 5.1        | 5.1  | 5.1                      | 1.8                      |
| PPB Inductance $L_b$ (mH)                              | 0          | 1.4  | 0                        | 0                        |
| Efficiency   | 95.5%      | 94.4%  |                          |                          |

Formatted: Font color: Red

From Table III, the following observations can be made:

(i) Solutions based on active PPB can significantly reduce the energy storage (> 55% reduction) as compared to the passive solution. As the stored energy needed is directly proportional to the volume of the capacitor (assuming a constant dielectric), the results indicate a volume reduction of more than 55% in the PPB capacitor. Table III also indicates that almost minimum energy storage is achieved via using Circuit B and Circuit D;

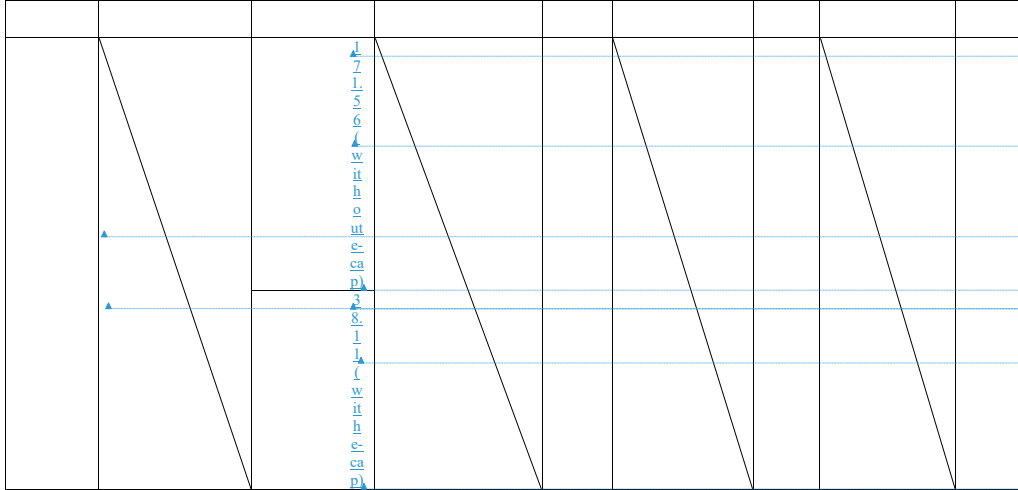
(ii) Among all the active PPB solutions, rectifier based on PPB embedded switching concept (Circuit C and Circuit D) achieves the minimum number of active switches and inductors used;

(iii) The voltage stress of the buck-boost switch  $S_A$  in Circuit A and Circuit B are independent of the PPB capacitance and ~~is~~ are fixed at  $V_{ac}+V_{dc} = 305$  V, while those for Circuit C and Circuit D are PPB capacitance dependent. With an enlarged ripple  $\Delta v_c$  due to a smaller  $C_b$ , the voltage stress of  $S_A$  in Circuit C is increased by 19.6%. In contrast, Circuit D has the lowest voltage stress among all the four topologies (i.e., 42.6% reduction compared to Circuit A and Circuit B, and 51.3% compared to Circuit C). In addition, the voltage stress of the diodes (except for the diode bridge) in Circuit D are also the lowest among the solutions;

(iv) The main inductances  $L$  for Circuit A to C are identical, given the same inductor current ripple requirement. In contrast, Circuit D achieves 64.7% reduction in the main inductance by employing an out-of-phase carrier pair for modulation.

(v) Among all the active PPB solutions, circuit-D achieve highest efficiency. The efficiency of circuit-D (95.1%) is a little lower but closed to circuit-A (95.5%), because although the circuit-D uses more active switches and diodes than circuit-A, the voltage rating of circuit-D is lower than that of circuit-A, which enable switches with lower conduction and switching loss (Lower  $R_{DSon}$  and forward voltage) can be selected; also the inductance of the circuit-D is smaller than circuit-A which enable less conduction loss of the inductor for circuit-D.





Formatted: Font: 8 pt, Not Italic, Font color: Red

Formatted: Font: 8 pt, Font color: Red

Formatted: Font: 8 pt, Font color: Red

Formatted: Centered, Indent: Left 3.75 ch

Formatted: Font: Not Italic, Font color: Red

Formatted: Font color: Red

Formatted: Font: 8 pt, Not Italic, Font color: Red

Formatted: Centered, Indent: Left 3.75 ch

Formatted: Font: 8 pt, Font color: Red

Formatted: Font: 8 pt, Not Italic, Font color: Red

#### IV. EXPERIMENTAL VERIFICATION

Table IV. Key Experiment Parameters.

| Parameters                                   | Values                    | Parameters             | Values             |
|--|---------------------------|------------------------|--------------------|
| Input ac RMS voltage                         | 110 V                     | Line frequency         | 60 Hz              |
| Output dc voltage $V_{dc}$                   | 100–200 V                 | Switching frequency    | 25 kHz             |
| Output capacitor $C_{dc}$                    | 10 $\mu$ F                | Flying capacitor $C_b$ | 40 $\mu$ F         |
| Inductor $L$                                 | 2.5 mH                    | Load resistor $R_{dc}$ | 350 $\Omega$       |
| $D_A$ – $D_A$ , Diode bridge $D_A$ and $D_B$ | UF5404-E3/54              | $S_A$ and $S_B$        | SHHP25N40AOT20S60L |
| Input $D_A$ and $D_B$ EMI filter             | 1 mH, 1 $\mu$ F SCS206AGC |                        |                    |

Formatted: Font: Not Italic

Formatted: Font: Not Italic

Formatted: Font color: Red

Formatted: Font: Not Italic, Font color: Red

Formatted: Font color: Red

Formatted: Font: Not Italic, Font color: Red

Formatted: Font color: Red

Formatted: Font color: Red

Formatted: Font color: Red

Formatted: Font: 10.5 pt, Font color: Red, (Asian) Chinese (PRC), Do not check spelling or grammar

Formatted: Font color: Red

Formatted: Font color: Red

A proof-of-concept 110 W prototype with the component specifications given in Table IV is constructed and tested. The photo of the experimental setup is shown in Fig. 12. An off-the-shelf 40  $\mu$ F/250 V film capacitor is chosen for  $C_b$  by trading off between minimizing the PPB capacitance and voltage stresses of the power components. An inductor of 2.5 mH is selected for  $L$  to ensure a maximum inductor current ripple of 0.6 A and CCM operation according to Fig. 10. An input EMI filter with cut-off frequency of 5 kHz is adopted to filter harmonic current in switching-frequency, since the input current of the buck-boost converter is uncontinuous. The E-APD controller is implemented using a low-cost DSP (TMS320F28069). Although, this

type of DSP isn't suitable for low cost equipment such as LED light bulb, quick charger, it should be noted that the DSP is only chosen off the shelf and hasn't been optimized according to the computational complexity.

The steady-state waveforms of the proposed PFC rectifier are shown in Fig. 13 (a)–(c), with an output voltage of 100 V, 150 V, and 200 V respectively. In all three scenarios, unity power factor is achieved and the output voltage is well regulated at the respective references with negligible low-frequency voltage ripples 7.5 V, 8.2 V and 8.7 V respectively. This low-frequency voltage ripple might be further reduced by enlarging output capacitance  $C_{dc}$ , using more elegant sensors and MCUs with less delay time and higher precision, or adopting an advanced controller with infinite gain at specific frequency such as proportional-resonant (PR) or repetitive controller. Meanwhile, the voltage across the PPB capacitor  $C_b$  is pulsating significantly at a double-line frequency, indicating that  $C_b$  is buffering the imbalanced power between the input and output. The peak to peak voltage amplitude of  $v_c$  are 23 V, 36 V and 45 V which are closed to the design specification based on equation (27). These waveforms also confirm that the proposed rectifier has both voltage step down and step up capabilities and that a wide output voltage range is attainable.

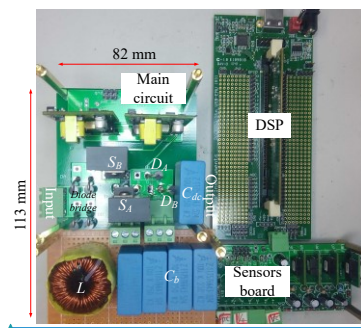


Fig. 12. Photograph of the experimental setup.

Formatted: Centered

Field Code Changed

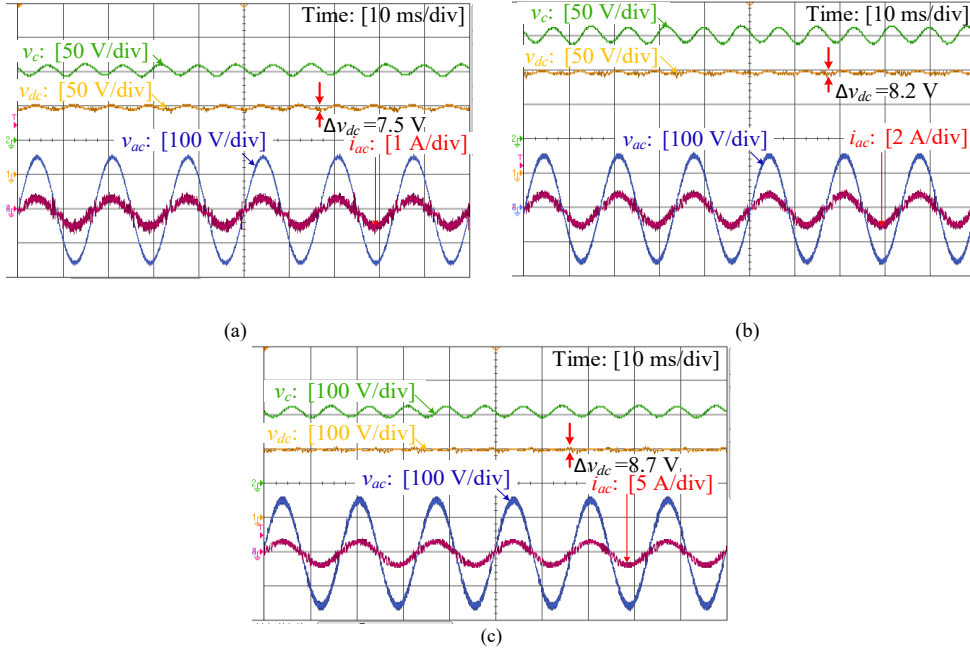
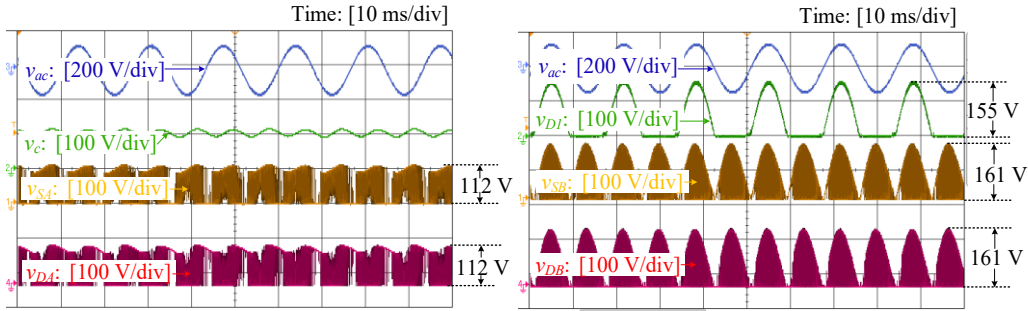
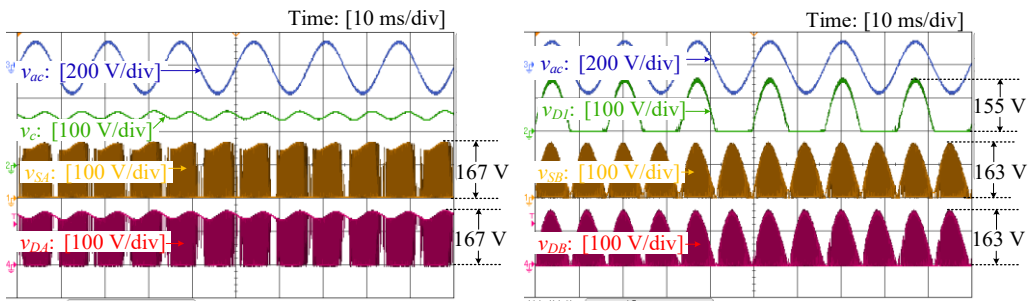


Fig. 13. Measured steady-state waveforms of the PFC rectifier at (a)  $v_{dc}^* = 100 \text{ V}$ , (b)  $v_{dc}^* = 150 \text{ V}$  and (c)  $v_{dc}^* = 200 \text{ V}$ .

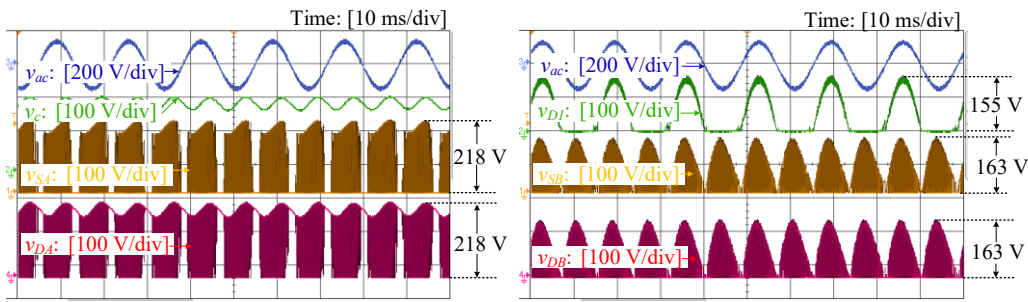
The voltage waveforms of all switching devices are captured and compared to  $v_{ac}$  and  $v_c$  at different output voltage levels, as illustrated in Fig. 14. It can be seen that voltage stresses for  $S_A$  and  $D_A$  are clamped by  $v_c$  which scales proportionally with  $V_{dc}$ . Therefore,  $V_A$  is minimum (i.e., 112 V) among the three tested scenarios when  $V_{dc}$  is minimum (i.e., 100 V), and vice versa. On the other hand, the voltage stress  $V_B$  is almost constant in all three scenarios. The results confirm the previous analysis that  $V_B \approx V_{ac}$  for a wide load and power range. The voltage stresses at the optimal output voltage are annotated in Fig. 14(b), from which it is evident that all power devices, including the diodes in the bridge rectifier, exhibit almost identical voltage stresses closed to  $V_{ac}$ . In contrast, the voltage stresses for the active switches and diodes (excluding those in the bridge rectifier) in the conventional buck-boost converter and existing three-port PFC rectifier with PPB embedded switching must be at least doubled. The waveforms illustrated in Fig. 14 confirm the reduced voltage stresses of the proposed PFC rectifier.



(a)



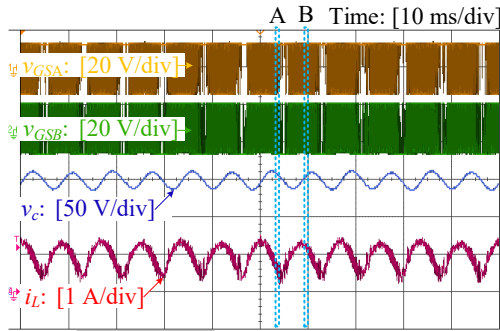
(b)



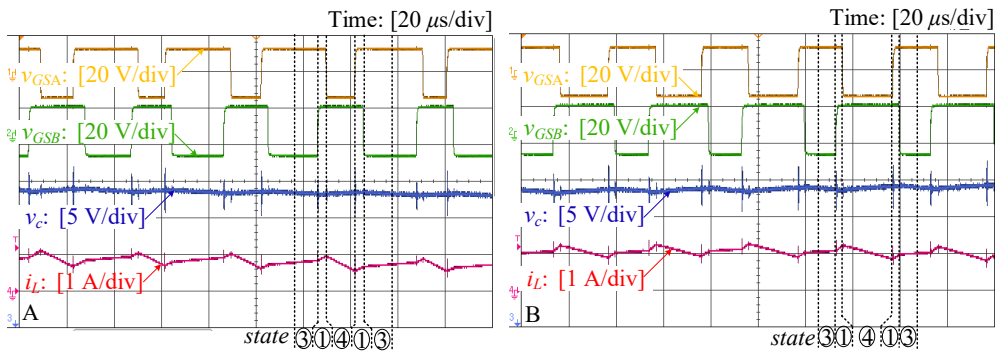
(c)

Fig. 14. Measured voltage waveforms of all switching devices at (a)  $v_{dc}^* = 100$  V, (b)  $v_{dc}^* = 150$  V and (c)  $v_{dc}^* = 200$  V.





(a)



(b)

(c)

Fig. 15. (a) An overview of the switching waveforms of the inductor current and capacitor voltage against the gate signals, (b) zoom-in view at viewpoint A during the capacitor discharging phase and (c) at viewpoint B during the capacitor charging phase (viewpoint B).

Fig. 15 (a) shows an overview of the waveforms of the gate signals for  $S_A$  and  $S_B$ , the inductor current  $i_L$  and  $v_c$ . The zoom-in waveforms at viewpoint A (i.e., capacitor discharging phase) and B (i.e., capacitor charging phase) are shown in Fig. 15 (b) and (c), respectively. It can be observed that  $d_A > d_B$  (or  $d_3 > d_4$ ) at viewpoint A, meaning that  $C_b$  is discharged for a longer duration than being charged, leading to a decreased  $v_c$  over  $T_s$ . Conversely,  $d_A < d_B$  (or  $d_3 < d_4$ ) at viewpoint B, meaning that  $C_b$  is charged longer and  $v_c$  is

increasing. It can be observed, the current ripple of inductor current  $\Delta i_L$  is always lower than 0.6 A, which is in agree with the design specification. These results are consistent with the steady-state circuit analysis given in Section II.

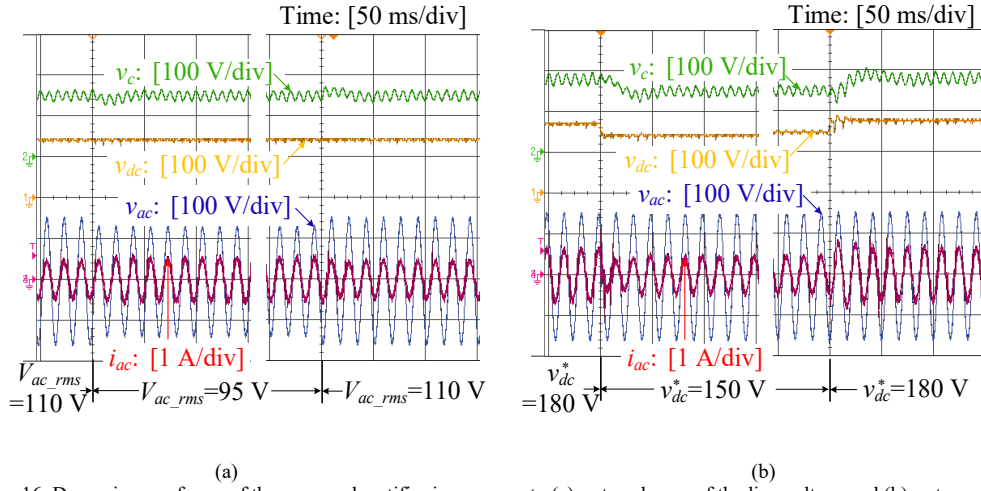


Fig. 16. Dynamic waveforms of the proposed rectifier in response to (a) a step change of the line voltage and (b) a step change of  $v_{dc}^*$ .

The input voltage disturbance rejection capability and the reference tracking performance are also evaluated by stepping up/down the line voltage and the output voltage's reference, as illustrated in Fig. 16 (a) and (b) respectively. In Fig. 16 (a), despite large line voltage excursions,  $v_{dc}$  is almost immune to the line voltage disturbances and the rectifier retains tight dc voltage regulation. The step change of the line voltage will produce a sudden change of the input power, leading to imbalanced power between the ac input and the dc output. Due to the robustness of the E-APD control strategy, the imbalanced power is automatically transferred to  $C_b$ , resulting in instant voltage variations in  $v_c$  subsequent to the transient interval. **In Fig. 16 (b),  $v_{dc}$  tracks its reference quickly and achieves almost zero steady-state error in both voltage step down and up tests.** Based on E-APD control, the dynamic mode of two controlled variables ( $i_L$  and  $v_{dc}$ ) with respect to their references are first-order transfer function. Therefore  $v_{dc}$  reaches its steady state within 2 ms with its reference step up as designed. Meanwhile, the averaged  $v_c$  also changes accordingly to ensure proper circuit

operation. The waveforms demonstrate fast reference tracking performance of the rectifier with E-APD control.

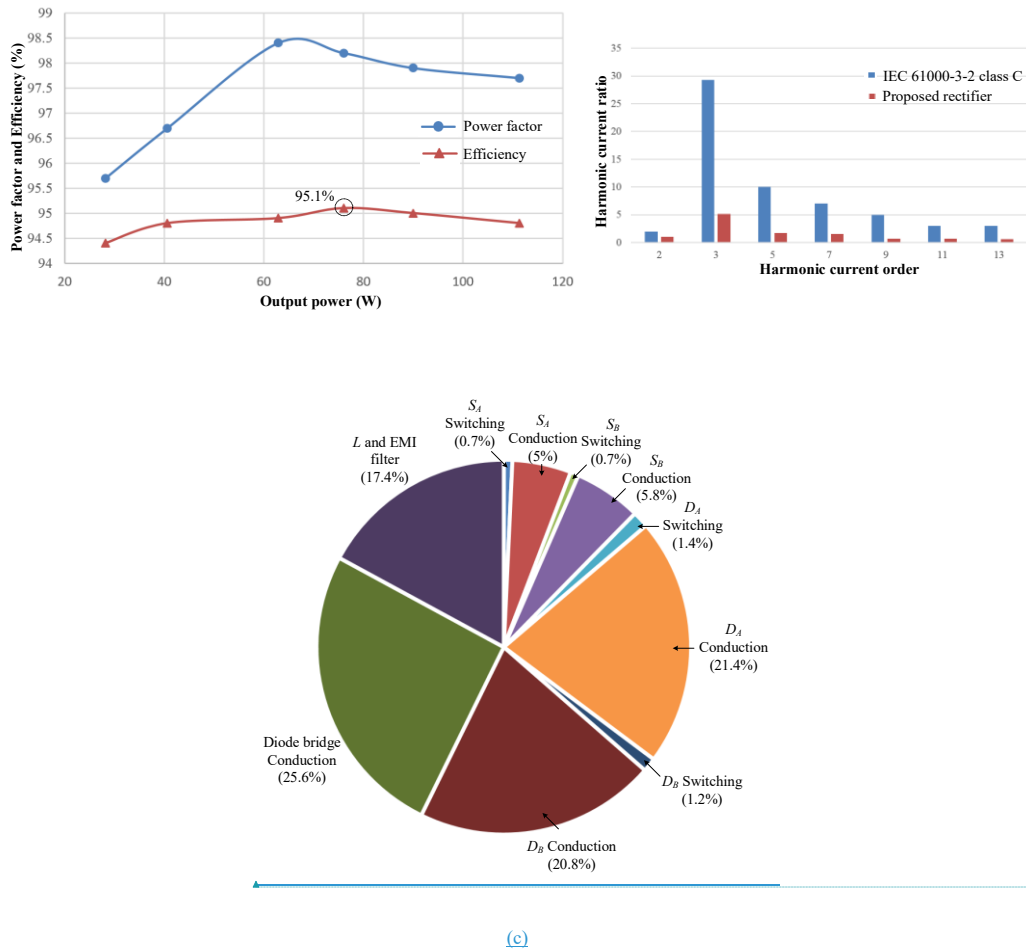


Fig. 17. (a) Measured power factor and efficiency of the proposed PFC rectifier versus the output power, and (b) measured input current harmonics in comparison with IEC 61000-3-2 class C and (c) estimated loss breakdown.

Fig. 17(a) illustrates the rectifier's power conversion efficiency over a load range from 30 W to 110 W at  $V_{dc} = 150$  V. The rectifier reaches a peak efficiency of 95.1% and the efficiency curve is shown to be fairly flat

Field Code Changed

for a wide load range. The current spectrum of the line current is also recorded in Fig. 17(b) at full load (i.e., 110 W). The results show that the rectifier meets IEC 61000-3-2 Class C limit whilst achieving a power factor of 0.977 and a total harmonics distortion of 5.8%. [A detailed estimated power loss breakdown is illustrated in Fig. 16\(c\) at full load \(i.e., 110 W\). It can be seen that the conduction loss of the diodes \(the diode bridge,  \$D\_A\$  and  \$D\_B\$ \) take more than two third \(67.8%\) of the loss.](#)

### CONCLUSIONS

In this paper, a single-phase three-level flying-capacitor PFC rectifier without electrolytic capacitor is proposed. By taking advantage of its inherent PPB embedded switching capabilities, the rectifier features only two active switches, one inductor, and two small capacitors. Additionally, with a three-level configuration, the voltage stresses for power devices are effectively reduced. Moreover, through quantitative analysis, it is shown that the minimum inductance requirement of the rectifier is closely related to the patterns of the modulation carriers. Out-of-phase carries are employed, enabling more than 60% inductance reduction as compared to the case when in-phase carriers are used. Experiments on a 110-W hardware prototype demonstrated the feasibilities of the proposed rectifier.

### REFERENCES

- [1] M. Rico-secades, A. J. Calleja, J. Ribas, E. L. Corominas, J. M. Alonso, J. Cardesin, and J. Garcia-garcia, "Evaluation of a low-cost permanent emergency lighting system based on high-efficiency LEDs," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1386–1390, Sep. 2005.
- [2] P. S. Almeida, D. Camponogara, M. A. D. Costa, H. Braga, and J. M. Alonso, "Matching LED and driver life spans: a review of different techniques," *IEEE Ind. Electron. Mag.*, vol. 9, no. 2, pp. 36–47, Jun. 2015.
- [3] Y. Wang, J. M. Alonso, and X. Ruan, "A review of LED drivers and related technologies," *IEEE Trans. Ind. Electron.*, vol. 64, no. 7, pp. 5754–5765, Jul. 2017.
- [4] Y. C. Li and C. L. Chen, "A novel single-stage high-power-factor AC-to-DC LED driving circuit with leakage inductance energy recycling," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 793–802, Feb. 2012.
- [5] J. M. Alonso, J. Viña, D. G. Vaquero, G. Martínez, and R. Osorio, "Analysis and design of the integrated double Buck – Boost converter as a high-power-factor driver for power-LED lamps," *IEEE Trans. Ind. Electron.*, vol. 59, no. 4, pp. 1689–1697, Apr. 2012.
- [6] S. Li, S. C. Tan, C. K. Lee, E. Waffenschmidt, S. Y. R. Hui, and C. K. Tse, "A survey, classification, and critical review of light-emitting diode drivers," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1503–1516, Feb. 2016.
- [7] "How the ZTE Nubia Z17 phone draws power from the BatPower PD6 power bank through USB power delivery," 2017. [Online]. Available: <https://gtrusted.com/review/how-the-zte-nubia-z17-phone-draws-power-from-the-batpower-pd6-power-bank-through-usb-power-delivery>.
- [8] "Snapdragon 845 mobile platform|qualcomm"," 2018. [Online]. Available: <https://www.qualcomm.com/products/snapdragon-845-mobile-platform>.
- [9] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1292–1306, Sep. 2005.

- [10] H. Hu, S. Harb, N. Kutkut, I. Batarseh, and Z. J. Shen, "A review of power decoupling techniques for microinverters with three different decoupling capacitor locations in PV systems," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2711–2726, Jun. 2013.
- [11] M. A. Vitorino, L. F. S. Alves, R. Wang, and M. B. De Rossiter Correa, "Low-frequency power decoupling in single-phase applications: a comprehensive overview," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2892–2912, Apr. 2017.
- [12] Q. Li and P. Wolfs, "A review of the single phase photovoltaic module integrated converter topologies with three different DC link configurations," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1320–1333, May 2008.
- [13] H. Watanabe, T. Sakuraba, K. Furukawa, K. Kusaka, and J. Itoh, "Development of DC to single-phase AC voltage source inverter with active power decoupling based on flying-capacitor DC/DC converter," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 4992–5004, Jun. 2018.
- [14] R. Wang, F. Wang, D. Boroyevich, R. Burgos, R. Lai, P. Ning, and K. Rajashekara, "A high power density single-phase PWM rectifier with active ripple energy storage," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1430–1443, May 2011.
- [15] S. Wang, X. Ruan, K. Yao, S. C. Tan, Y. Yang, and Z. Ye, "A flicker-free electrolytic capacitor-less AC-DC LED driver," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4540–4548, Nov. 2012.
- [16] W. Qi, H. Wang, X. Tan, G. Wang, and K. D. T. Ngo, "A novel active power decoupling single-phase PWM rectifier topology," in *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, 2014, pp. 89–95.
- [17] S. Li, W. Qi, S. C. Tan, and S. Y. R. Hui, "Integration of an active filter and a single-phase AC/DC converter with reduced capacitance requirement and component count," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4121–4137, Jun. 2016.
- [18] Y. Tang and F. Blaabjerg, "A component-minimized single-phase active power decoupling circuit with reduced current stress to semiconductor switches," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 2905–2910, Jun. 2015.
- [19] Q. C. Zhong, W. L. Ming, W. Sheng, and Y. Zhao, "Beijing converters : bridge converters with a capacitor added to reduce leakage currents ," *IEEE Trans. Ind. Electron.*, vol. 64, no. 1, pp. 325–335, Jan. 2017.
- [20] Y. Ohnuma and J. I. Itoh, "A novel single-phase buck PFC AC-DC converter with power decoupling capability using an active buffer," *IEEE Trans. Ind. Appl.*, vol. 50, no. 3, pp. 1905–1914, May 2014.
- [21] S. Li, W. Qi, S. C. Tan, and S. Y. Ron Hui, "A Single-Stage Two-Switch PFC Rectifier with Wide Output Voltage Range and Automatic AC Ripple Power Decoupling," *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 6971–6982, Sep. 2017.
- [22] Y. Liu, Y. Sun, M. Su, and F. Liu, "Control method for the Sheppard – Taylor PFC rectifier to reduce capacitance requirements," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2714–2722, Mar. 2018.
- [23] Y. Liu, Y. Sun, and M. Su, "A control method for bridgeless Cuk/Sepic PFC rectifier to achieve power decoupling," *IEEE Trans. Ind. Electron.*, vol. 64, no. 9, pp. 7272–7276, Sep. 2017.
- [24] Y. Lei, C. Barth, S. Qin, W.-C. Liu, I. Moon, A. Stillwell, D. Chou, T. Foulkes, Z. Ye, Z. Liao, and R. C. N. Pilawa-Podgurski, "A 2-kW single-phase seven-level flying capacitor multilevel inverter with an active energy buffer," *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8570–8581, Nov. 2017.
- [25] P. T. Krein, R. S. Balog, and M. Mirjafari, "Minimum energy and capacitance requirements for single-phase inverters and rectifiers using a ripple port," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4690–4698, Nov. 2012.
- [26] T. A. Meynard, M. Fadel, and N. Aouda, "Modeling of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 44, no. 3, pp. 356–364, Jun. 1997.
- [27] S. Li, W. Qi, S. C. Tan, and S. Y. Hui, "Enhanced automatic-power-decoupling control method for single-phase AC-to-DC converters," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1816–1828, Feb. 2018.