Design Considerations for Voltage Sensorless Control of a PFC Single-Phase Rectifier Without Electrolytic Capacitors

***Abstract*—A voltage sensorless controller is developed for a two-switch single-phase rectifier that involves power factor correction and active pulsating power buffering without electrolytic capacitors. While a two-switch rectifier normally requires four sensed signals for control, only one current sensor is required in this proposal, thereby offering advantages such as low cost, high compactness, isolation between control and power circuits, and improved reliability. While the basic operating principle follows that of a conventional voltage sensorless controller for single-switch converters, several critical design considerations are the key to the success of the implementation which is explained in detail. The feasibilities of the controller are experimentally testified with a 100-W rectifier prototype regarding both steady-state and dynamic performance.**

***Index Terms*— Voltage sensorless control, single-phase ac-to-dc converters, power decoupling, two-switch rectifier.**

I. Introduction

Single-phase power converters require substantial energy storage to buffer their inherent double-line frequency pulsating power [1]. It is widely known that conventional single-phase converters employing electrolytic capacitors (E-caps) on the dc-link as a passive pulsating power buffer (PPB) are bulky and unreliable [2]–[4]. Recently, there is a growing demand for high power density, high efficiency, and high reliability (H^3) single-phase PFC rectifiers in the market [5]–[12]. Subsequently, new single-phase solutions with active PPB without E-caps have been proposed [13]–[15]. As opposed to the conventional PFC rectifiers, the PPB capacitor (see C_b in Fig. 1) is detached from the dc-link and connected to a third ripple port. Therefore, C_b can be greatly reduced by increasing its voltage fluctuation, and non-E-caps with high energy density and reliability, such as film or ceramic capacitors, can be used in lieu of E-caps to achieve high compactness and long lifetime [16] –[18].

In general, the control of an active PPB-based single-phase PFC rectifier require at least four sensors (see Fig. 1):

(i) an ac voltage sensor for detecting the phase angle of the source voltage which is then used to generate the ac current reference i_{ac}^* for power factor control;

(ii) a dc-link voltage sensor for regulating dc-link voltage and overvoltage protection;

(iii) a ripple port voltage sensor for active pulsating-power-buffering control;

(iv) inductor current sensor(s) for achieving closed-loop power factor control, dc voltage regulation, active pulsating power buffering control, and overcurrent protection.

The use of four or more sensors (together with their associated isolated power supplies) increases the complexity of control circuitry. For applications with very stringent cost and space requirements (such as retrofit LED lighting application), the use of many sensors is unviable [19]. Additionally, the quality of a sensed signal is usually subjected to the amount of electrical noise coupled from the switching power converters. Distortion to any of the sensed signals could easily lead to system instability and deteriorate the overall reliability. Based on the above two considerations, a reduction in the required number of sensors is highly desired. In [20], a current sensorless control method is proposed to eliminate one inductor current sensor in the active PPB circuit. However, four sensors (an ac voltage sensor, a dc-link voltage sensor, a ripple port voltage sensor, and an inductor current sensor in the ac/dc converter) are still needed for the overall system control. To the best of our knowledge, no method for achieving a minimum number of sensors for a switched mode rectifier with PFC and PPB has been reported.

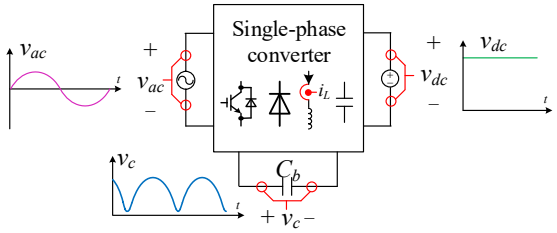


Fig. 1. A generic three-port model of a single-phase power converter with an active PBB together with its operating waveforms.

In this paper, a voltage sensorless controller is implemented for a type of active PPB-based single-phase rectifier featuring only one inductor [21]. Only one inductor current sensor is needed. The sensed inductor current is used for two functions, namely, (i) as a feedback and feedforward signal to generate the control signals for PFC, dc-link voltage regulation and active PPB; (ii) to estimate the ac voltage, the dc-link voltage, and the ripple port voltage of the rectifier. Voltage sensorless control based on sensing the inductor current has been previously reported in [22]–[24] for a family of single-switch dc/dc and ac/dc converters. However, existing methods *cannot* be directly applied to an active-PPB-based rectifier having typically two or more active switches, as they involve more switching states, and more state variables need to be determined to accomplish the control [22]–[24]. This paper focuses on the design aspect and demonstrates a single-current-sensor solution (specifically for active-PPB-based rectifiers) that can accurately distinguish all the switching states while simultaneously estimating all the three voltage signals. The basic principles of the voltage sensorless control are explained in Section II. Guidelines for designing the amplitude-modulation demodulators (AMD) and the differentiator for a practical implementation of the controller are included in Section III with the challenges highlighted. The limitations of the control method are also discussed. In Section IV, the feasibility and the performance of the voltage sensorless controller are examined experimentally

with a 100-W prototype. Finally, Section V concludes the paper.

II. Principles of Voltage Sensorless Control

The circuit topology of the studied active-PPB-based rectifier is shown in Fig. 2(a) [21]. The selection of this 2-switch PFC rectifier for demonstrating the voltage sensorless control is due to its topological simplicity. Among all active PPB-based single-phase solutions reported thus far, this rectifier utilizes the minimum number of active switches and inductors. Therefore, the number of switching states involved and the current measurement needed is minimal. Fig. 2(a) also shows an overview of the controller structure, with the detailed implementation showed in Fig. 2(b).

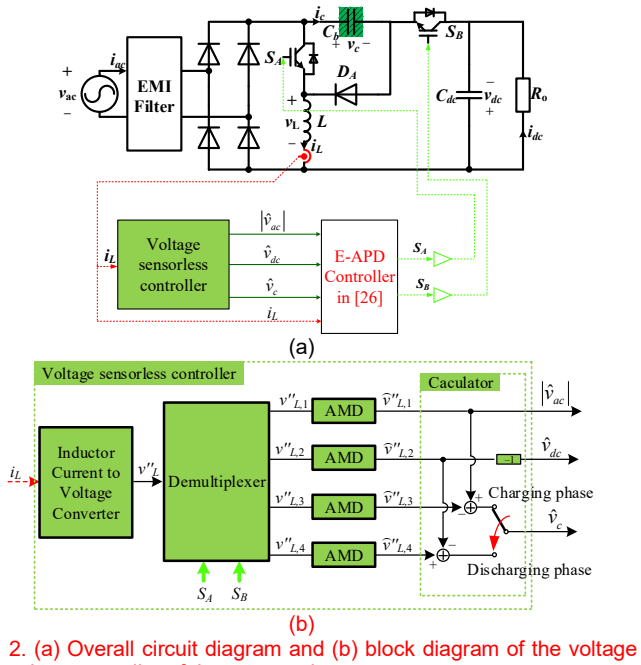


Fig. 2. (a) Overall circuit diagram and (b) block diagram of the voltage sensorless controller of the proposed converter system.

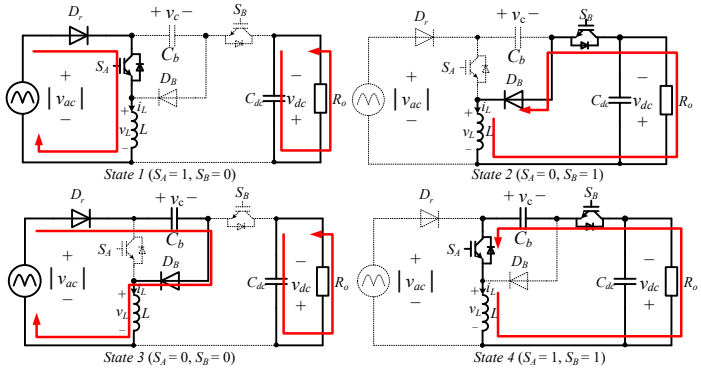


Fig. 3. The equivalent circuit of the rectifier in each of the four operation states: State 1–State 4.

With two active switches and assuming a continuous conduction mode (CCM) of operation, the rectifier has four switching states, i.e., $\{S_A, S_B\} = \{1, 0\}$, $\{0, 1\}$, $\{0, 0\}$, and $\{1, 1\}$. The equivalent circuit of the corresponding switching states is shown in Fig. 3. Here, the front-end electromagnetic interference (EMI) filter is excluded for the ease of analysis. D_r is an equivalent representation of the diode bridge rectifier.

In state 1, the inductor L is charged by $|v_{ac}|(t)$. The inductor voltage $v_{L,1}$ is

$$v_{L,1} = |v_{ac}| = L\, di_L/dt|_{\text{state 1}} > 0. \quad (1)$$

In state 2, the inductor L is discharged by the load R_o, i.e.,

$$v_{L,2} = -v_{dc} = L\, di_L/dt|_{\text{state 2}} < 0. \quad (2)$$

In state 3, the PPB capacitor C_b is switched into the circuit and is charged by inductor current i_L. Consequently (noting that $v_c > |v_{ac}| + v_{dc}$)

$$v_{L,3} = |v_{ac}| - v_c = L\, di_L/dt|_{\text{state 3}} < 0. \quad (3)$$

Finally, in state 4, C_b is discharged with current i_L, and the inductor voltage $v_{L,4}$ is

$$v_{L,4} = v_c - v_{dc} = L\, di_L/dt|_{\text{state 4}} > 0. \quad (4)$$

By adjusting the duty ratio of state 3 and state 4, the instantaneous power flowing into and out of the PPB capacitor C_b can be precisely controlled, thereby achieving active PPB. Assuming a unity power factor, zero power loss, and a fixed output power, the instantaneous power at the ac and dc side of the rectifier (i.e., $p_{ac}(t)$ and $p_{dc}(t)$, respectively) and the typical inductor voltage waveforms for the positive half line period are shown in Fig. 4(a). The waveforms in the negative half line period are identical and are not repeated.

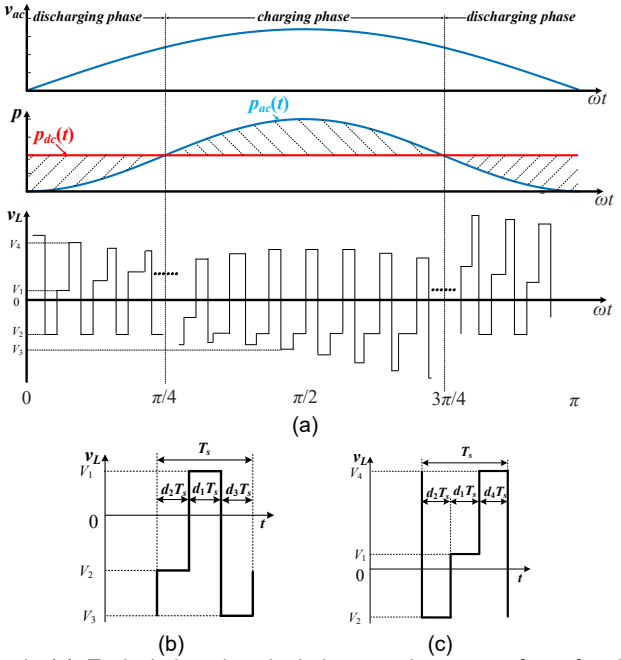


Fig. 4. (a) Typical time-domain inductor voltage waveform for the positive half line period, and characteristics of the inductor voltage during PPB capacitor (b) charging phase, (c) discharging phase.

As shown, when $p_{ac}(t) > p_{dc}(t)$, the PPB capacitor operates in the charging phase ($\omega t \in (\pi/4, 3\pi/4)$), where ω is the angular line frequency. The active switching states are state 1, 2 and 3. Thus, v_L has three voltage levels, $V_1 = v_{L,1}$, $V_2 = v_{L,2}$, and $V_3 = v_{L,3}$ (see Fig. 4(b)). According to equation (1)–(3), the variables $|v_{ac}|(t)$, $v_{dc}(t)$, and $v_c(t)$ can be estimated from the envelopes of v_L:

$$|v_{ac}|(t) \cong \overset{\frown}{v}_{L,1}(t), \quad (5)$$

$$v_{dc}(t) \cong -\overset{\frown}{v}_{L,2}(t), \quad (6)$$

$$v_c(t) \cong \overset{\frown}{v}_{L,1}(t) - \overset{\frown}{v}_{L,3}(t), \quad (7)$$

where operator $\overset{\frown}{g}$ represents the envelope of the signal. The approximations adopted in (5)–(7) are justified as the switching

frequency is generally much faster as compared to the rate of change of $|v_{ac}|(t)$, $v_{dc}(t)$, and $v_c(t)$.

Similarly, when $p_{ac}(t) \le p_{dc}(t)$, the PPB capacitor is operating in the discharging phase ($\omega t \in (0,\pi/4) \cup (3\pi/4, \pi)$). The active switching states are state 1, 2, and 4 (see Fig. 4(c)). v_L also has three voltage levels, $V_1 = v_{L,1}$, $V_2 = v_{L,2}$, and $V_4 = v_{L,4}$. $|v_{ac}|(t)$ and $v_{dc}(t)$ can still be estimated using (5) and (6), but v_c must be estimated using (according to (1), (2) and (4))

$$v_c(t) \cong \hat{v}_{L,4}(t) - \hat{v}_{L,2}(t). \tag{8}$$

The need for a different state-estimation algorithm poses the first design challenge to the sensorless controller implementation compared to that in a conventional single-switch converter. The duty ratios d_1–d_4 with respect to each switching states during the charging and discharging phases of the PPB are listed in Table I according to [21].

Table I. Theoretical Duty Cycles d_1–d_4 during different operating phases.

	d_1	d_2	d_3	d_4
Charging phase	$\frac{\lvert i_{ac}\rvert - i_c}{\lvert i_{ac}\rvert + i_{dc}}$	$\frac{i_{dc}}{\lvert i_{ac}\rvert + i_{dc}}$	$\frac{i_c}{\lvert i_{ac}\rvert + i_{dc}}$	0
Discharging phase	$\frac{\lvert i_{ac}\rvert}{\lvert i_{ac}\rvert + i_{dc}}$	$\frac{i_{dc} + i_c}{\lvert i_{ac}\rvert + i_{dc}}$	0	$\frac{i_c}{\lvert i_{ac}\rvert + i_{dc}}$

Based on the above discussions, a schematic diagram of the voltage sensorless controller that can estimate $|v_{ac}|(t)$, $v_{dc}(t)$, and $v_c(t)$ using only the measurement of the inductor current i_L is shown in Fig. 2(b). Here the inductor current to voltage converter (ICVC) block is used to obtain a scale down and filtered inductor voltage v_L signal (i.e., v''_L) from i_L; the demultiplexer is used to decode the switching inputs (S_A, S_B) to differentiate the switching states and to route the associated v''_L (i.e., $v''_{L,i}$) to one of the four amplitude modulation demodulator (AMD) channels; the AMD is used for envelop reconstruction; finally, the calculation block is used to process the envelop signals and yield all the voltage signals needed based on (5)–(8). Detailed design of the ICVC, the AMD, and other design considerations are discussed as follows.

III. Detailed Design Considerations

A. *Compensation for the Voltage Drops of the System Parasitic Elements*

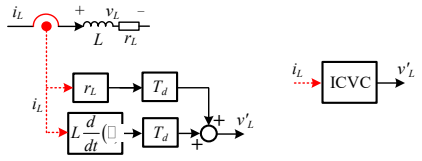


Fig. 5. Inductor model with consideration of the winding resistance.

The discussions in Section II are based on an ideal inductor model without considering the power loss. A more accurate inductor model should incorporate the winding resistance r_L, as shown in Fig. 5. With this model, the inductor voltage v_L is related to its current i_L by

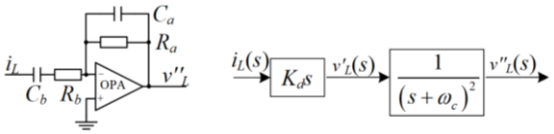
$$v_L = L\frac{di_L}{dt} + r_L i_L. \tag{9}$$

The ICVC can be constructed by summing the outputs of a differentiator and a proportional gain amplifier as shown at the bottom of Fig. 5 with

$$v'_L = T_d\left(L\frac{di_L}{dt} + r_L i_L\right) = T_d v_L, \tag{10}$$

where T_d is the time constant of the differentiator. For the 100 W prototype adopted in this work, the peak inductor current of the rectifier is i_{L_peak} = 2.29 A and the voltage drop in r_L (i.e., 0.2 Ω) is 0.458 V, which is 0.3% of $v_{L,1}$, 0.4% of $v_{L,2}$, 0.3% of $v_{L,3}$, and 0.2% of $v_{L,4}$, and are almost negligible. Therefore, the proportional compensation term is neglected in the final design. For applications where the voltage drop in r_L constitutes a more significant portion of v_L, the proportional term must be included to improve the estimation accuracy.

B. *Design of the Differentiator*



(a) (b)

Fig. 6. (a) Time differentiator circuit used in the prototype and (b) its *s*-domain block diagram.

Fig. 6(a) illustrates the time differentiator circuit employed in the design. Given $C_aR_a = C_bR_b$, the transfer function of the differentiator circuit can be derived as

$$G_{diff}(s) = \frac{v''_L(s)}{i_L(s)} = \frac{K_d s}{(s+\omega_c)^2}, \tag{11}$$

where $K_d = -(C_aR_b)^{-1}$, $\omega_c = (C_aR_a)^{-1} = (C_bR_b)^{-1}$. (11) indicates that the differentiator circuit also incorporates a critically-damped second-order low-pass term with a cut-off frequency at ω_c. The equivalent *s*-domain block diagram is shown in Fig. 6(b). Note that the output of the differentiator circuit v''_L differs from the scaled inductor voltage signal v'_L given in (10) due to the extra low-pass filter term. On designing the cut-off frequency of the differentiator circuit, the following considerations should be taken:

(i) v'_L should be extracted as accurately as possible;

(ii) high-frequency noise (e.g. due to the ringing of i_L and/or the EMI coupled to the printed circuit board of the differentiator circuit) should be attenuated as much as possible.

Following the above guidelines, the design of ω_c can be quantified by studying the power spectrum of v''_L relative to that of v'_L. Firstly, as v'_L is a scaled version of v_L, the instantaneous v'_L can be expressed in a compact form as

$$v'_L(t) = \sum_{k=0}^{M} v'_{L,k}(t) \text{ and } v'_{L,k}(t) = v'_{L,k}(t + T_{l/2})$$
$$= \begin{cases} V'_{1,k} & kT_s \le t \le kT_s + t_{1,k} \\ V'_{2,k} & kT_s + t_{1,k} \le t \le kT_s + t_{2,k} \\ V'_{3,k} & kT_s + t_{2,k} \le t \le kT_s + t_{3,k} \\ V'_{4,k} & kT_s + t_{3,k} \le t \le kT_s + t_{4,k} = (k+1)T_s \end{cases}, \tag{12}$$

where $T_{l/2}$ is the half line period, M is the number of switching cycles per $T_{l/2}$ ($M \approx T_{l/2} * f_s$, f_s is the switching frequency), $v'_{L,k}(t)$ is the $v'_L(t)$ signal during the kth switching cycle, $V'_{i,k} = T_d V_{i,k}$ is the voltage levels of $v'_{L,k}(t)$ for switching state i, and $t_{i,k} = d_{i,k} T_s$ is the time interval of switching state i with $d_{i,k}$ being the corresponding duty ratios. As $v'_L(t)$ is symmetrical about $\omega t = \pi$, only the spectrum in the positive half line period is calculated. The total energy of $v'_L(t)$ in the kth switching cycle is

$$E'_{L,k} = \int_{kT_s}^{(k+1)T} |v'_{L,k}(t)|^2 dt = \sum_{i=1}^{4}\left[\left(V'_{i,k}\right)^2 d_{i,k} T_s\right], \tag{13}$$

and the average power spectrum of $v'_L(t)$ over $T_{l/2}$ is

$$P'_L = \frac{1}{T_{l/2}} \sum_{k=0}^{M} E'_{L,k}. \tag{14}$$

On the other hand, the power spectrum of v''_L can be calculated in the frequency domain according to Parseval theorem. If the cutoff frequency of the differentiator circuit is selected as $\omega_c = m\omega_s = 2m\pi f_s$, where m is an integer to be designed, then the total energy of $v''_L(t)$ in the kth switching cycle is

$$E''_{L,k} = \sum_{i=1}^{4}\sum_{q=-mM}^{mM}\left|X_{L,i,k}(q)\right|^2 = \sum_{i=1}^{4}\left(X_{L,i,k}{}^2(0) + 2\sum_{q=1}^{mM}\left|X_{L,i,k}(q)\right|^2\right), \quad (15)$$

where $X_{L,i,k}(q)$ is the coefficient of the q^{th} harmonics of the Fourier series of $v'_{L,i,k}(t)$ where,

$$v'_{L,i,k}(t) = \begin{cases} V'_{i,k} & 0 \le t < t_{i,k} \\ 0 & t_{i,k} \le t < T_{l/2} \end{cases}, i = 1, 2, 3, 4, \quad (16)$$

and

$$X_{L,i,k}(q) = \frac{V'_{i,k}}{T_{l/2}} d_{i,k} T_s \sin c \frac{q\pi d_{i,k} T_s}{T_{l/2}} e^{-j\frac{2q\pi}{T_{l/2}}(kT_s + d_{i,k}T_s/2)}. \quad (17)$$

The averaged power spectrum of v''_L over $T_{l/2}$ is then

$$P''_L = \frac{1}{T_{l/2}}\sum_{k=0}^{M} E''_{L,k}. \quad (18)$$

The ratio $\rho = P''_L / P'_L$ can then be used as a relative measure of the signal extraction capability of the differentiator.

Fig. 7 illustrates the calculated ρ versus m based on $V_{i,k}$ and $d_{i,k}$ values in Table I. Evidently, a larger m (i.e., a higher ω_c) gives a higher ρ and thus a better signal extraction which is desirable.

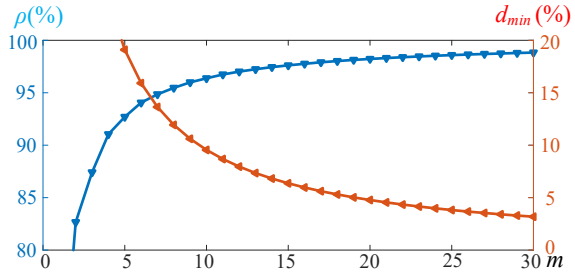


Fig. 7. Theoretical ρ and d_{min} versus m.

On the other hand, ω_c also determines a minimum duty ratio d_{min} that can be distinguished for switching state i. When $d_i < d_{min}$, $V'_{i,k}$ cannot be detected accurately. d_{min} is an important design variable that poses the second design challenge in the controller implementation as d_i may become zero. This can be explained by studying the step response v_{LP} of a critically-damped second-order low-pass filter:

$$v_{LP}(t) = 1 - (1 + \omega_c t)e^{-\omega_c t}. \quad (19)$$

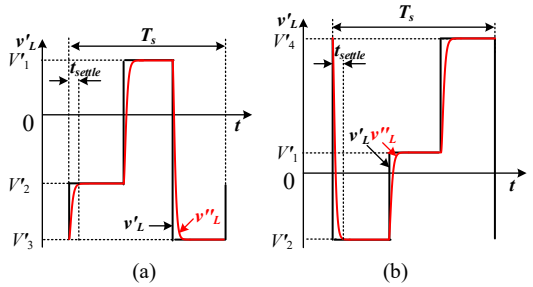


Fig. 8. The dynamic waveforms of v''_L given $v'_L(t)$ in (a) the PPB charging phase and (b) the PPB discharging phase.

(19) indicates that the settling time of the low-pass filter is approximately $t_{settle} \approx 6/\omega_c$ for the output to settle within ± 2% of the steady-state error band. Fig. 8(a) and (b) show the waveforms of v''_L given v'_L during PPB charging and discharging phase, respectively. Clearly, d_{min} can be resolved as

$$d_{\min} = t_{settle}/T_s \approx 3/\pi m. \quad (20)$$

Based on (20), the relationship between m and d_{min} is calculated and shown in Fig. 7. As m increases, d_{min} decreases. A smaller d_{min} is highly desirable as it ensures a wider applicable range of the voltage sensorless controller. Considering both ρ and d_{min}, m can be selected in the range of 15 and 25. In our prototype design, m=20 is chosen, leading to ρ= 98.22% and d_{min} = 4.78%.

C. Design of the AMD Circuits

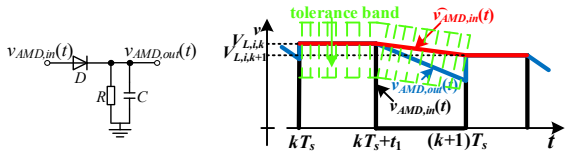


Fig. 9. (a) The AMD circuit in the prototype, and (b) typical input and output waveforms of AMD circuit in the kth switching cycle.

The design of the AMD circuit mainly involves the determination of the time constant of the RC network, i.e., τ=RC. As there are four switching states, four AMD circuits are required. Fig. 9 illustrates the typical input and output waveforms of an AMD circuit during the kth switching cycle. The output signal $v_{AMD\_out,k}$ is required to follow the envelope of the input signal $v_{AMD\_in,k}$ (i.e., $\hat{v}_{AMD\_in,k}$) within a tolerance band. The diode D is an equivalent representation of the internal switch of the demultiplexer. The AMD design is more challenging than that in traditional wireless communication applications (where the carrier is pure sinusoidal waveform) as the signal carrier is a pulsed signal with a time-varying pulse width. From Fig. 9, it follows that

$$v_{AMD\_out,k}(t) = \begin{cases} v_{AMD\_in,k}(t) & kT_s < t \le kT_s + t_1 \\ v_{AMD\_in,k}(kT_s + t_1)e^{-\frac{t-(kT_s+t_1)}{\tau}} & kT_s + t_1 < t \le (k+1)T_s \end{cases}, \quad (21)$$

and

$$\hat{v}_{AMD\_in,k}(t) = \begin{cases} v_{AMD\_in,k}(t) & kT_s \le t \le kT_s + t_1 \\ c(t - kT_s - t_1) + v_{AMD\_in,k}(kT_s + t_1) & kT_s + t_1 < t \le (k+1)T_s \end{cases}, \quad (22)$$

where $c = \dfrac{v_{AMD\_in,k}\left[(k+1)T_s\right] - v_{AMD\_in,k}(kT_s + t_1)}{T_s - t_1}$. To meet the design requirement, $v_{AMD\_out,k}$ and $\hat{v}_{AMD\_in,k}$ must satisfy

$$e_{AMD,k} = \left|\frac{v_{AMD\_out,k}\left[(k+1)T_s\right] - \hat{v}_{AMD\_in,k}\left[(k+1)T_s\right]}{\hat{v}_{AMD\_in,k}\left[(k+1)T_s\right]}\right| \le \varepsilon, \quad (23)$$

where ε is the desired tolerance band ($\varepsilon \in [0,1]$), $e_{AMD,k}$ is the maximum relative error between $v_{AMD\_out,k}$ and $\hat{v}_{AMD\_in,k}$ within the kth switching cycle. To simplify the analysis, it is also assumed that $v_{AMD\_in,k}(kT_s) \approx v_{AMD\_in,k}(kT_s + t_1) = V'_k$, where, $V'_k = V'_{i,k}$ for switching state i. Solution of (21)–(23) gives the design criteria of τ as

$$\tau_\alpha^{-1} \le \tau^{-1} \le \tau_\beta^{-1} \quad (24)$$

where $\tau_\alpha = \max\left[0, (t_1 - T_s)/\ln\left[(1+\varepsilon)V'_{k+1}/V'_k\right]\right]$, and $\tau_\beta = (t_1 - T_s)/\ln\left[(1-\varepsilon)V'_{k+1}/V'_k\right]$.

A smaller ε gives a higher envelope predicting precision. However, (24) suggests that the upper/lower boundaries τ_α/τ_β of τ decreases/increases with a decrease of ε. That is, the selection range of τ shrinks as ε decreases. If ε is too small, there will be no solution for τ covering the whole operating range (where $d_i > d_{min}$). Fig. 10 depicts the $1/\tau_\alpha$ and the $1/\tau_\beta$ curves for the critical (and minimum) value of ε_{min} during the positive half line period when there exists only one solution for τ. ε_{min} can be numerically calculated by solving

$$\min_{\omega t\in[\omega t_1,\omega t_2]} \tau_\beta^{-1}(\omega t) = \max_{\omega t\in[\omega t_1,\omega t_2]} \left[\tau^{-1}{}_\alpha(\omega t), 0\right], \tag{25}$$

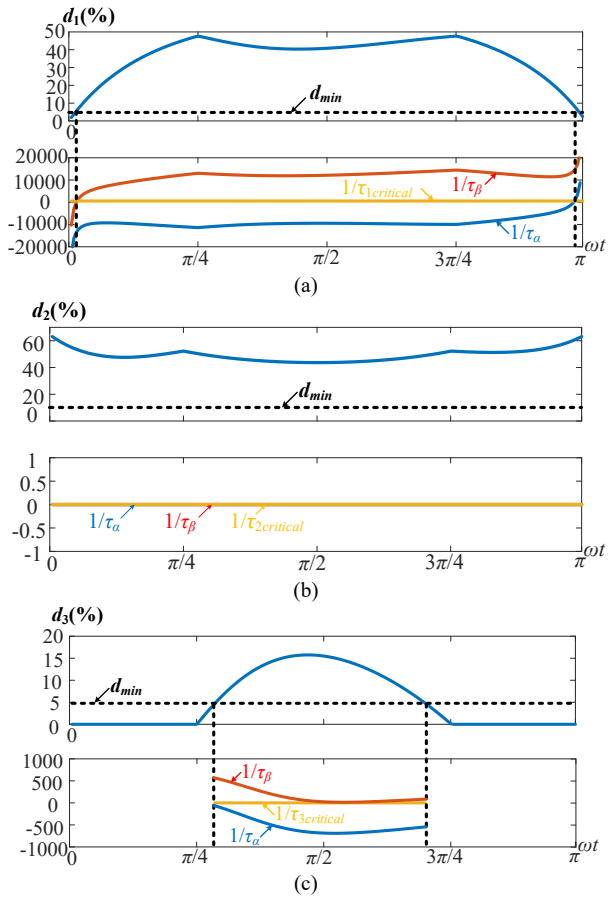
for envelope prediction in switching states 1 and 3, and

$$\min_{\omega t\in[0,\pi]} \tau_\beta^{-1}(\omega t) = \max_{\omega t\in[0,\pi]} \left[\tau_\alpha^{-1}(\omega t), 0\right], \tag{26}$$

for switching state 2, and

$$\min_{\omega t\in[0,\omega t_1]\cup[\omega t_2,\pi]} \tau_\beta^{-1}(\omega t) = \max_{\omega t\in[0,\omega t_1]\cup[\omega t_2,\pi]} \left[\tau_\alpha^{-1}(\omega t), 0\right], \tag{27}$$

for switching state 4, where ωt_1 and ωt_2 are the critical angular frequencies satisfying $d_i(\omega t_1) = d_i(\omega t_2) = d_{min}$ as designed in (20). Once ε_{min} is determined, the corresponding τ can be calculated by substituting ε_{min} back to (25)–(27). The theoretical ε_{min} and the corresponding $1/\tau_{critical}$ are tabulated in Table II (assuming that d_{min}=4.78%). For $1/\tau_{critical}$ =0 (i.e., $\tau_{critical} \to \infty$) in switching state 2 and 3, design is not possible. A larger ε value than ε_{min} leads to a more practical τ value that can be implemented. With off-the-shelf components, a possible set of ε and τ values is also given in Table II.



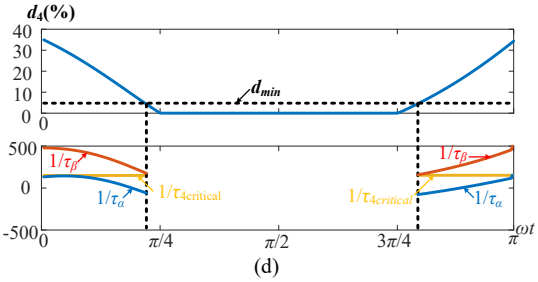


Fig. 10. The upper and lower boundaries (i.e., $1/\tau_\alpha$,$1/\tau_\beta$) and the $1/\tau_{critical}$ curves for the critical value of ε_{min} during the positive half line period for (a) switching state 1, (b) switching state 2, (c) switching state 3, and (d) switching state 4.

Table II. Critical, Designed, and Measured Values *of* ε and $1/\tau$.

	Switching State 1	Switching State 2	Switching State 3	Switching State 4
$\varepsilon_{\min}$	0.2	0	0.01	0.0045
$1/\tau_{critical}$ (Hz)	600	0	0	150
ε_{design}	0.21	0.001	0.02	0.009
$1/\tau_{design}$ (Hz)	577	45	300	300
ε_{real} (experimental)	0.22	0.012	0.05	0.05

D. *Further Considerations*

As mentioned, there is a d_{min} for recovering $V'_{i,k}$. Due to the exponential decaying term in (19), $v''_{L,i}(t)$ quickly approaches zero when $d_i < d_{min}$. According to Fig. 2(b), the output signal of the i_{th} AMD circuit, i.e., $\hat{v}''_{L,i}(t)$, can then be simplified as

$$\hat{v}''_{L,i}(t) = \begin{cases} 0 & 0 \le d_i < d_{\min} \\ \hat{v}_{L,i}(t) & d_{\min} \le d_i \end{cases}, \tag{28}$$

assuming that (i) the AMD circuit is perfect with zero envelope tracking error, (ii) $\omega_c \to \infty$ (no low-pass filter), and (iii) $K_d = 1$ (no voltage scaling). Clearly, when $0 < d_i < d_{min}$, the error between $\hat{v}''_{L,i}(t)$ and $\hat{v}_{L,i}(t)$ is significant if $\hat{v}_{L,i}(t)$ is not close to zero. A large estimation error will disturb the normal operation of the system, which must be avoided. This poses the third design challenge. To further explain this issue, Fig. 11 shows the expected and the estimated inductor voltage envelope (i.e., $\hat{v}_{L,i}(t)$ and $\hat{v}''_{L,i}(t)$) versus d_i according to (28).

It is shown that in switching state 1,

$$\hat{v}''_{L,1}(t) = \begin{cases} 0 & \omega t \in [0,\omega t_1]\cup[\omega t_2,\pi] \\ \hat{v}_{L,1}(t) & \omega t \in [\omega t_1,\omega t_2] \end{cases} \cong \hat{v}_{L,1}(t). \tag{29}$$

Equation (29) is justified for the reason that $\hat{v}_{L,1}(t) = |\hat{v}_{ac}|(t) \cong 0 = \hat{v}''_{L,1}(t)$ for $\omega t \in (0, \omega t_1]\cup[\omega t_2, \pi]$ as d_{min} is small and $\omega t_1 \approx 0$ and $\omega t_2 \approx \pi$. In switching state 2, as d_2 is always larger than d_{min}, $\hat{v}_{L,2}(t)$ can always be accurately predicted using $\hat{v}''_{L,2}(t)$ throughout the operating range. In switching state 3, $\omega t_1 \approx \pi/4$, and $\omega t_2 \approx 3\pi/4$. As $\hat{v}_{L,3}(t) = |\hat{v}_{ac}| - \hat{v}_c < -\hat{v}_{dc} = 0$, $\hat{v}_{L,3}(t)$ cannot be predicted by $\hat{v}''_{L,3}(t)$ during $\omega t \in [\pi/4, \omega t_1]\cup[\omega t_2, 3\pi/4]$ even if d_{min} is small. Similarly, $\hat{v}_{L,4}(t)$ cannot be predicted by $\hat{v}''_{L,4}(t)$ during $\omega t \in [\omega t_1, \pi/4,]\cup[3\pi/4, \omega t_2]$.

Based on $\hat{v}''_{L,i}(t)$, the expected values of $|v_{ac}|(t)$, $v_{dc}(t)$, and $v_c(t)$ and their estimations (i.e., $|\hat{v}_{ac}|(t)$, $\hat{v}_{dc}(t)$, and $\hat{v}_c(t)$) can be found and are shown in Fig. 12. Due to the d_{min} constraint imposed by the differentiator design, a significant voltage dip

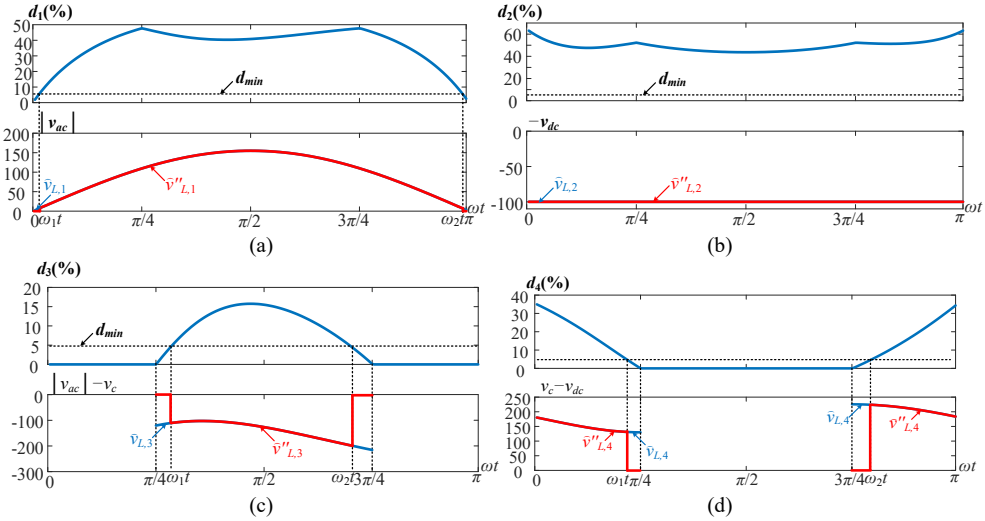


Fig. 11. Waveforms of the expected and estimated inductor voltage in switching (a) state 1, (b) state 2, (c) state 3, and (d) state 4, assuming (i) zero envelope tracking error, (ii) $\omega_c \to \infty$, and (iii) $K_d = 1$.

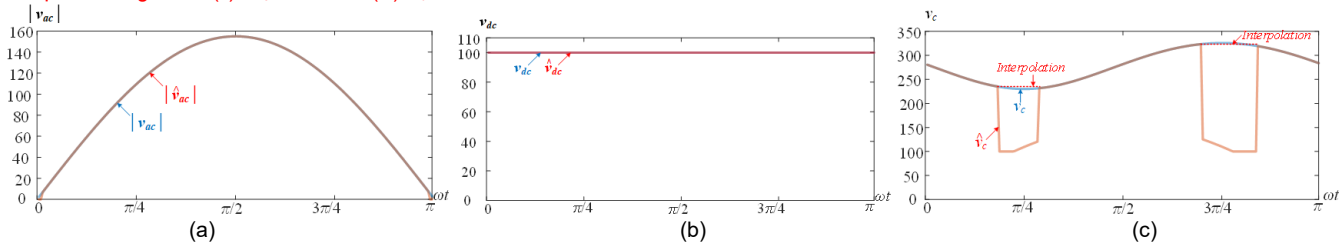


Fig. 12. Waveforms of the expected and estimated voltages of $|v_{ac}|$, v_{dc}, and v_c.

can be observed in $\hat{v}_c(t)$ at around $\omega t \approx \pi/4$ and $3\pi/4$. On the other hand, $|\hat{v}_{ac}|(t)$ and $\hat{v}_{dc}(t)$ are highly accurate as compared to their expected signals. To solve the voltage dipping issue, $\hat{v}_c(t)$ is deliberately held constant during the voltage dipping intervals, as illustrated in Fig. 12 (as red dotted lines). This is plausible since (i) the rate of change of $v_c(t)$ near $\omega t = \pi/4$ and $3\pi/4$ is approximately zero and thus $v_c(t)$ is almost constant and (ii) v_c is symmetrical around $\omega t = \pi/4$ and $3\pi/4$. The signal holdup can be easily achieved using either an analog or a digital controller. In this work, the digital approach is employed. Other advanced signal interpolation techniques can be further applied to reduce the estimation errors as and when required.

A second consideration is the effect of the inductor tolerance to the estimation accuracy. According to the principles of the proposed voltage sensorless control, the estimated voltages are directly proportional to the inductance L. If the actual inductance is L while the predicted inductance is $\hat{L}$, the true voltage v and the estimated voltage $\hat{v}$ shall satisfy:

$$\frac{v}{\hat{v}} = \frac{L}{\hat{L}}. \tag{30}$$

Therefore, the voltage estimation error relative to the true voltage signal is $e_{relative} = \left|\hat{L}/L - 1\right|$. For example, when L has a 10% tolerance, $e_{relative} = 10\%$. The voltage estimation errors will lead to voltage offsets during system operation but will not lead to input current distortion. With this voltage sensorless control method, it is crucial to estimate the inductance accurately, which may not be viable for mass production. An alternative method which may improve the voltage prediction accuracy is to use a coupled winding to obtain the voltage information across the inductor [25]. Following the principle of a simple transformer, this approach requires no knowledge of L. The secondary-side voltage is simply scaled by the transformer's turns ratio which can be determined precisely and conveniently. On top of that, this approach eliminates the need for a differentiator circuit which is not only susceptible to noises but also causing the voltage dipping issue.

IV. Experimental Verification

Experiments are performed with a 100-W two-switch buck-boost PFC rectifier prototype to demonstrate the effectiveness of the voltage sensorless control design. The detailed specifications of the rectifier, the ICVC circuit, and the AMD circuits are given in Table III. The design of the rectifier is based on the procedures described in [21]. Additionally, following (11), the ICVC circuit is designed to have a dc gain of 1/50 such that the outputs of the voltage sensorless controller fall within the Analog-to-Digital-Converter (ADC) compatible voltage range used in the prototype for digital control. The overall circuit diagram of the voltage sensorless controller is shown in Fig. 13, of which the diodes D_1– D_4 are used to generate a blanking period to prevent the potential current spikes of i_L from propagating to the AMD circuits at the switching instances, and the diodes D_5 and D_6 are used to switch between switching state 3 and 4 for estimating v_c. An enhanced automatic-power-decoupling controller (E-APD) based on feedback linearizations theory is further employed to control the overall system in a closed-loop. The detailed controller design follows that reported in [26], [27] and is not repeated here. A photograph of the laboratory prototype is shown in Fig. 14. The power density of this 100-W prototype (without the controller) is measured at 25.4 W/in^3 by component. It should be noted that both the two-switch PFC rectifier and the controller are for proof-of-concept only and are not optimized

for the final product. The size of the proposed controller can be greatly reduced by turning it into a control IC through a mixed signal analog/digital process. This is, however, out of the scope of this paper.

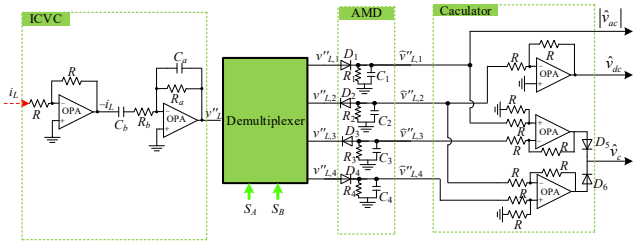


Fig. 13. Detailed circuit diagram of the proposed voltage sensorless controller.

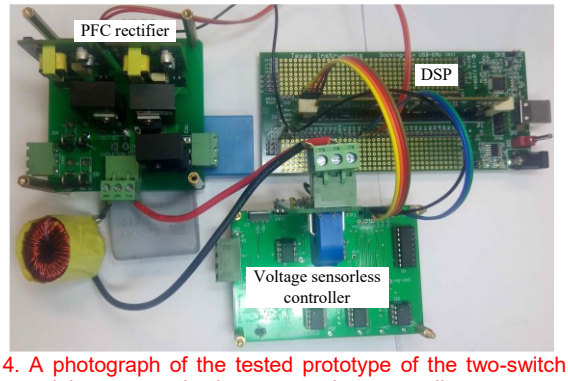


Fig. 14. A photograph of the tested prototype of the two-switch PFC rectifier and the proposed voltage sensorless controller.

A. *Performance of the Voltage Estimator*

Fig. 15(a) shows the steady-state output waveform of ICVC (i.e., v''_L) operating at full load, with the zoom-in waveforms shown in Fig. 15 (b)−(c) respectively at point *A* (PPB capacitor charging phase) and *B* (PPB capacitor discharging phase). Three voltage levels can be observed in the waveforms. These observations agree well with the theoretical analysis given in Section II. The settling time regarding the rising and falling edges of v''_L is around 2 μs, indicating that the minimum duty ratio d_{min} that can be identified is 5%. This matches closely with the theoretical value of 4.78% given in Section III.

Fig. 16 shows the respective actual and estimated (without signal interpolation) waveforms of $|v_{ac}|$, v_{dc}, and v_c in steady state. Both sets of waveforms are captured simultaneously using two oscilloscopes. Generally, the estimated voltage signals follow similar wave shapes as the actual voltage signals with a scaling factor of around 1/50. The sudden voltage dips around the peaks and the valleys of $\hat{v}_c$ can also be seen, and the reason for their existence is explained in Section III-D. Interpolation is then performed by the digital controller during voltage dipping period to reduce the estimation error, as marked out using the red dotted line. The maximum ε (after signal interpolation) are given in Table II. The measured ε are closed to the designed values stated in Table II.

The dynamic performances of the designed voltage sensorless controller are also examined.

Fig. 17 (a) and (b) illustrate the transient waveforms of the actual and the estimated (without signal interpolation) $|v_{ac}|$, v_{dc}, and v_c for a step change of v_{ac} from 90 Vrms to 110 Vrms, and Fig. 18 (a) and (b) illustrate the transient waveforms when there is a step change in the reference of v_{dc} from 95 V to 105 V. As the voltage (envelop) estimations are updated in a cycle-by-cycle manner, the responses of the voltage sensorless controller are sufficiently fast for closed-loop control. Moreover, as the switching states are exactly differentiated by the demultiplexer, there are no cross-interference issues among the estimated voltages. The voltage sensorless controller is thus reliable.

B. *Performance of Two-Switch Buck-Boost Rectifier with Voltage Sensorless Control*

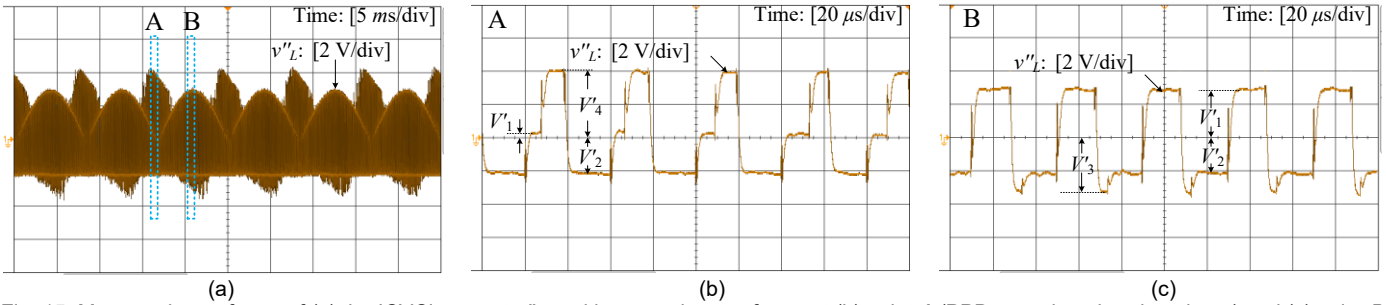
Table III. Key Specifications of the Prototype.

PFC rectifier			
Rated power P_o	100 W	AC line frequency	60 Hz
Peak AC voltage V_{ac}	155 V	Power-buffering capacitor C	10 μF
DC output voltage V_{dc}	100 V	Switching frequency f_s	25 kHz
Output capacitor C_{dc}	10 μF (film)	Inductor L	2.5 mH
Diode bridge	UF5404-E3/54	Diode D_A	SCS206AGC
S_A and S_B	AOT20S60	Current sensor	LTSR 6-NP

ICVC				
m	R_a	R_b	C_a	C_b
20	750 Ω	15 Ω	390 pF	22 nF

AMD							
τ_1	1/556	τ_2	1/45	τ_3	1/300	τ_4	1/300
R_1	150 kΩ	R_2	150 kΩ	R_3	1 MΩ	R_4	1 MΩ
C_1	1.2 nF	C_2	150 nF	C_3	3.3 nF	C_4	3.3 nF

Other Components			
OPA	Demultiplexer	Diode D_1–D_6	R
LM7171	74HC4052	CUS08F30	1 MΩ



(a) (b) (c)

Fig. 15. Measured waveforms of (a) the ICVC's output v''_L and its zoom-in waveforms at (b) point *A* (PPB capacitor charging phase) and (c) point *B* (PPB capacitor discharging phase).

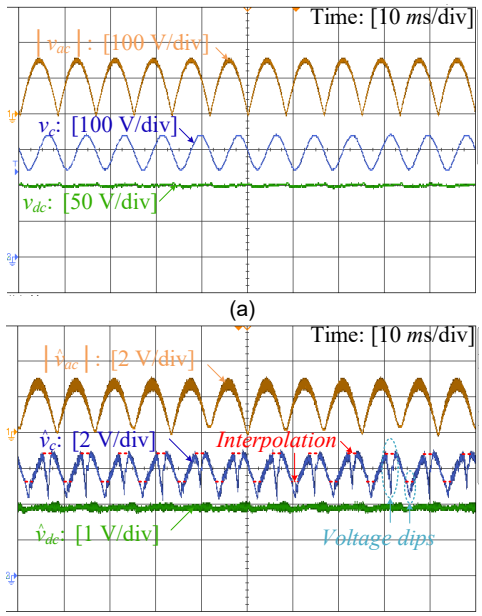


Fig. 16. Measured waveforms of the respective (a) actual voltages and (b) estimated voltages in steady state.

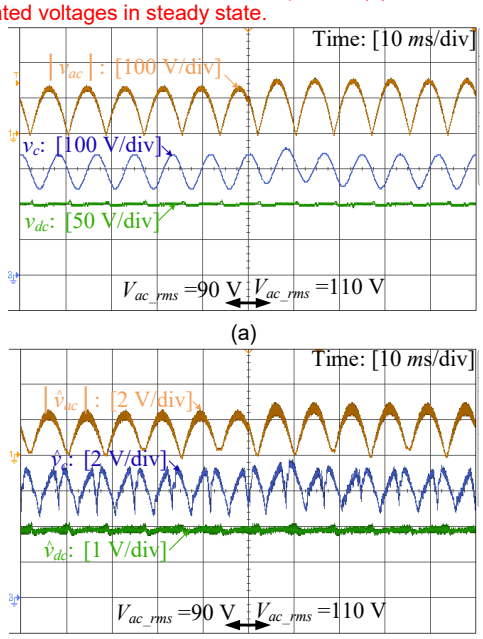
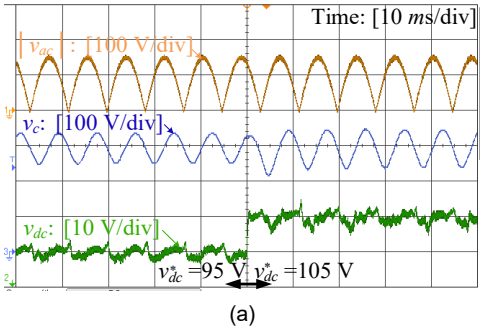


Fig. 17. The measured waveforms of the (a) actual and (b) estimated voltages during step changing v_{ac}.



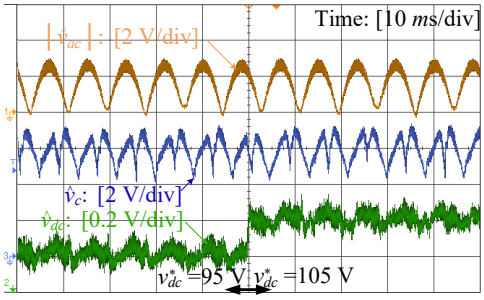
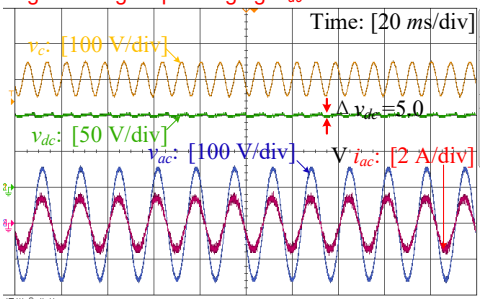
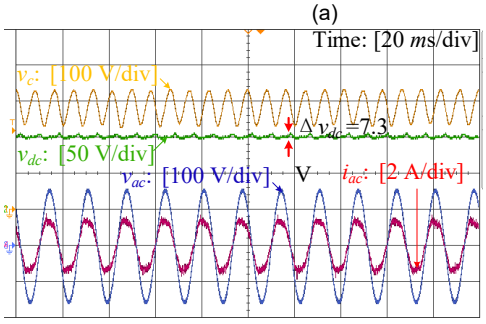


Fig. 18. The measured waveforms of the (a) actual and (b) estimated voltages during step changing v^*_{dc}.



PF = 0.990, THD = 3.6 %



PF = 0.982, THD = 4.7 %

Fig. 19. The measured waveforms of the rectifier (a) without (by using three isolated voltage sensors) and (b) with the voltage sensorless controller in steady state.

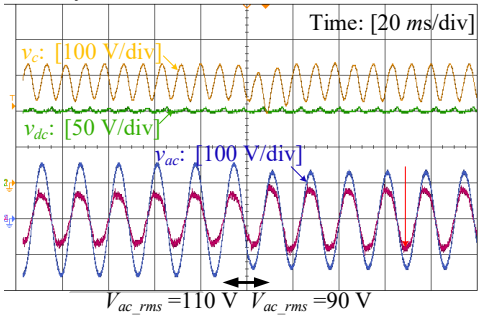


Fig. 20. Dynamic waveforms of the rectifier with voltage sensorless control under (a) v_{ac} step down and (b) v_{dc}^* step down.

Fig. 19 gives a comparison of the steady-state waveforms of the rectifier without (by using three isolated voltage sensors) and with the voltage sensorless controller. In both cases, (i) i_{ac} is sinusoidal and in phase with v_{ac}, (ii) v_{dc} is tightly regulated at 100 V with a small voltage ripple, and (iii) v_c is varying significantly at double-line frequency indicating pulsating power is being buffered. Compared to the waveforms without voltage sensorless controller, the performance of the rectifier with the designed sensorless controller is slightly degraded with (i) the peak-to-peak voltage ripple of v_{dc} being increased from 5.0 V to 7.3 V, (ii) the power factor (PF) being decreased from 0.99 to 0.98, and (iii) the total harmonic distortions (THD) being increased from 3.6% to 4.7%. The slight degradations in performance are attributed to the estimation errors.

The dynamic performances of the rectifier with the voltage sensorless control are further investigated by having a step change in the values of v_{ac} and v_{dc}^*. First, V_{ac_rms} is stepped down change from 90 Vrms to 110 Vrms, and then v_{dc}^* is stepped down from 105 V to 95 V. As shown in Fig. 20(a), i_{ac} quickly adjusts its magnitude to generate a 100-W output power without disturbing v_{dc} in the event of a step change of v_{ac}. Similarly, from Fig. 20(b), it can be seen that v_{dc} quickly tracks its set reference within a settling time of 2 ms in the event of a step change of v_{dc}^*. These results demonstrate the feasibilities of the designed voltage sensorless controller for practical applications.

V. Conclusions

Existing controllers for regulating single-phase PFC rectifiers with active pulsating power buffering function require the use of more than four sensors. For the first time, this paper reports a voltage sensorless control technique for regulating this emerging class of single-phase PFC rectifiers featuring only one current sensor. The basic operating principle of the proposed controller originates from that of the conventional voltage sensorless control methods for regulating a single-switch power converter. However, due to more switching states and state variables that must be measured, conventional voltage sensorless control methods cannot be readily employed for controlling this new type of PFC rectifier. The specific challenges involved are therefore detailed and the controller design guidelines (for the inductor current to voltage converter, the amplitude-modulation demodulators, and the compensation for the voltage dips) are explained. The feasibilities of exploiting the inductor's terminal voltage to predict all the voltage information are validated via a 100-W two-switch buck-boost PFC prototype. Future work, in particular the use of a coupled winding to obtain the inductor's terminal voltage for further performance advancement, will be investigated.

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