TECHNOLOGICAL SOLUTION BEYOND MOSFET AND BINARY LOGIC DEVICES

A Thesis in

Electrical Engineering

Presented to the Faculty of

University of Missouri Kansas City

in partial fulfilment of the requirements for the degree

MASTER OF SCIENCE

By

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Kansas City, Missouri 2018

TECHNOLOGICAL SOLUTIONS BEYOND MOSFET AND BINARY LOGIC DEVICES

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University of Missouri–Kansas City, 2018

ABSTRACT

Today's technology is based on the binary number system-based circuitry, which is the outcome of the simple on and off switching mechanism of the prevailing transistors. Consideration of higher radix number system can eradicate or lessen many limitations of binary number system such as the saturation of Moore's law. The most substantial potential benefits of higher radix approaches are the decrease of wiring complexity. Excessive scaling of the technologies has led the researchers beyond Binary Logic and MOSFET technology.

TFET considered as one of the most promising options for low-power application for beyond MOSFET technologies. Graphene Nano Ribbon, due to its high-carrier mobility, tunable bandgap and its outstanding electrostatic control of device gate becomes ideal choice for channel material of TFET. This paper proposes double gated ultra-thin body (UTB) TFET device model using Graphene nano ribbon as the channel material. In this paper evaluation of the model by performing the comparative analysis with InAs as the channel material in terms of Ec-Ev on and off state and Id-Vg characteristics is presented.

The feasibility of multi valued logic system in real-world rests on two serious aspects, such as, the easiness of mathematical approach for implementing the multivalued

logic into today's technology and the sufficiency of synthesis techniques. In this paper, we have focused on the different technology available for implementing multivalued logic especially ternary logic. Ternary logic devices are expected to lead to an exponential increase of the information handling capability, which binary logic cannot support. Memory capacitor or memcapacitor is an emerging device that exhibits hysteresis behavior, which can be manipulated by external parameters, such as, the applied electric field or voltage. One of the unique properties of the memcapacitor is that by using the percolation approach, we can achieve Metal-Insulator-Transition (MIT) phenomenon, which can be utilized to obtain a staggered hysteresis loop. For multivalued logic devices staggered hysteresis behavior is the critical requirement. In this paper, we propose a new conceptual design of a ternary logic device by vertically stacking dielectric material interleaved with layers of graphene nanoribbon (GNR) between two external metal plates. The proposed device structure displays the memcapacitive behavior with the fast switching metal-to-insulator transition in picosecond scale. The device model is later extended into a vertical-cascaded version, which acts as a ternary device.

APPROVAL PAGE

The faculty listed below, appointed by the Dean of the School of Computing and Engineering, have examined a thesis titled "Technological Solution beyond MOSFET and Binary Logic Device," presented by Jill Arvindbhai Patel candidate for the Master of Science degree, and certify that in their opinion it is worthy of acceptance.

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ACKNOWLEDGEMENTS

I would like to thank my academic adviser Dr. Masud Chowdhury for his guidance and support during the entire thesis work.

I would like to thank my parents, family, friends and team members for their support.

I would like to thank University of Missouri - Kansas City for providing me an opportunity to work on this thesis report.

CHAPTER 1
INTRODUCTION

With the exponential increase of the quantity and density of information the demands for extremely high data processing speed and storage requirements are rapidly moving beyond what binary logic based digital systems can offer. Binary logic-based computing machines are expected to face enormous challenge in the near future due to the severe thermal and reliability challenges. To mitigate this inevitable future limitation of the binary devices, researchers have already started exploring different multi-valued logic and memory devices. A fair amount of work on Multi-Valued Logic (MVL) has been done until now by different researchers. The main reason is that the concept of MVL holds a great possibility for improvement in present VLSI circuit design. The scope of application for MVL is profound and can be categorized into two major approaches. The first approach uses multiple valued logic domain to solve binary problems more efficiently. And the second approach is to design different electrical circuits based on prevailing and emerging technologies to get output signals having more than two unique values.

Multivalued logic holds many advantages over binary logic system. It allows a single digit to contain extensively more data than binary. If the signal values in the circuit can take up three or more levels rather than only two, on and off chip interconnect can be decreased, which in turn results lesser chip area and thus the pin-out problems that emerges with bigger chip area decreases. In the design of memory cell, if two bits of data is stored in the place of one bit of data, the density of the memory cell increases twice [1].

In spite of having several advantages, the concept of multi valued logic commences few disadvantages also. For example, with the continuously decreasing lower node technologies, which works with a maximum of 1.2 V as V_{DD} and 0 V as ground, it would

technologies, which works with a maximum of 1.2 V as V_{DD} and 0 V as ground, it would be quite difficult to maintain three or more distinct voltage levels and the intermediate voltage levels will become more prune to noises. Moreover, to implement a multi valued logic would require either a suitable enough technique to utilize CMOS circuitry to produce higher radix values or a whole new technology which can produce more than two discrete logic levels on its own.

Table 1: Table showing the density of information by 2, 3 and 4 valued logic

Highest Possible data that can be contained by:	**Binary (R=1)**	**Ternary (R=2)**	**Quaternary (R=3)**
1 bit	$2^1=2$	$3^1=3$	$4^1=4$
2 bit	$2^2=4$	$3^2=9$	$4^2=16$
3 bit	$2^3=8$	$3^3=27$	$4^3=64$
4 bit	$2^4=16$	$3^4=81$	$4^4=256$

In this, we have tried to explore and summarize all the different aspects of MVL design and the technology used to implement MVL in digital circuitry.

CHAPTER 2

MULTI-VALUED LOGIC

2.1 Definition and Numerical Representation

Multi valued logic system is the system comprising “R” distinct logic levels, where R>2. Whereas base 2 or binary numeral system works with only two values namely “true” and “false” or “1” and “0”, the MVL system may consists of a set of any number of logic levels, which is represented by some signal variables such as current, voltage or charge. These set of values can be illustrated using any of the two conventions: unbalanced and balanced. Unbalanced system is the extension of the binary number system in single direction, for instance 0, 1, 2, 3… (R-2), (R-1). And the balanced system needs an odd radix R=2K+1, with the values (-K), (1-K) … -1, 0, 1…, (K-1), K [2].

In the same way, ternary logic system uses three values to represent false, true and undefined. It can also be unbalanced: 0, 1, 2 or balanced: -1, 0, 1.

A simple ternary inverter can be implemented in three ways: Standard, positive and negative. The logic symbol and truth table for few of the operations of ternary logic system is given below in Table 2 [3]. Here, “0” stands for false, “1” stands for undefined and “2” stands for true:

Table2: Different logic levels for a ternary logic system

Logic level	Logic symbol
0	0
$0.5*V_{DD}$	1
V_{DD}	2

Table 3: Definition of different kinds of ternary inverter

Input	STI	PTI	NTI
0	2	2	2
1	1	2	0
2	0	0	0

Table 4: Basic logic functions of a ternary system

Input		OR	AND	XOR	Adder	
X_1	X_2				SUM	CARRY
0	0	0	0	0	0	0
0	1	1	0	1	1	0
0	2	2	0	2	2	0
1	0	1	0	1	1	0
1	1	1	1	1	2	0
1	2	2	1	1	0	1
2	0	2	0	2	2	0
2	1	2	1	1	0	1
2	2	2	2	0	1	1

A ternary function f(X) containing *n* variables $\{X_1, X_2 \ldots, X_n\}$ can be described as a logic function mapping $\{0, 1, 2\}^n$ to $\{0, 1, 2\}$, where $X = \{X_1, X_2, \ldots, X_n\}$. The elementary

algebraic operations of ternary logic can be described using equation, where, X_i, X_j = {0, 1, 3} [4].

$$X_i + X_j = \max\{X_i, X_j\} \quad (1)$$

$$X_i \bullet X_j = \min\{X_i, X_j\} \quad (2)$$

$$\bar{X}_i = 2 - X_i \quad (3)$$

Here, + and • represents the OR and AND operations respectively and – represents the arithmetic subtraction.

For a multi-valued logic system, the function minimization techniques become more complex with the increase of radix. In case of ternary, the minimization is a little bit complicated than that of binary but the use of Karnaugh map (K-map) for binary can be extended to ternary with little modification. The paper [5] presents a method to minimize a ternary function with the help of K-map. From table 4, the K-map for the Sum and carry of a ternary full adder are given in table 5:

Table 5: K-map for Sum and Carry

Sum					Carry			
X_1 / X_2	0	1	2		X_1 / X_2	0	1	2
0		1	2		0			
1	1	2			1			1
2	2		1		2		1	1

The equation for representing sum and carry from the k-map can be written as:

$$Sum = X_1^2X_2^0 + X_1^1X_2^1 + X_1^0X_2^2 + 1 \times (X_1^1X_2^0 + X_1^0X_2^1 + X_1^2X_2^2) \quad (4)$$

$$Carry = 0 + 1 \times (X_1^2X_2^1 + X_1^1X_2^2 + X_1^2X_2^2 \quad (5)$$

Besides K-map, there are some more synthesis techniques for MVL like Galois Field Polynomials, Arithmetic Polynomials and Linear Cellular arrays [6]. In [6] a novel approach for computing and analyzing MVL has been proposed, which is applicable and adaptable to any multivalued function. The process can be divided into three different steps: domain selection, linear regression and pattern matching for deriving selection criteria. In domain selection stage, the domain for the input, and output and parametric constants are fixed. Commonly, the radix of the input and output represents the domain of them. And the domain for the parametric constants depend on the number of inputs. These parametric constants domain vary with medium of implementation and requirements of the specific application. After the selection of domain, a linear regression is carried out on the input combinations through which a linear equation is derived which fits the majority of function outputs. On the residual unmatched outputs, linear regression is done again so that a set of linear expressions is acquired. Once all the outputs of the functions are matched with a linear expression, this step continues. For instance, if a multivalued function contains n-number of inputs as $x_0, x_1, x_2, \dots, x_{n-1}$ and there are n+1 number of parametric constants as $c_0, c_1, c_2, \dots, c_n$, the resulting linear equations obtained will be in the form of equation 4.

$$f' = c_0 + c_1x_0 + c_2x_1 + \cdots + c_nx_{n-1} \quad (6)$$

For the third stage, based on the sets of linear expressions obtained in Stage 2, individual selection conditions for individual expressions in the sets are derived. For a input combination, the hardware must be able to select the correct linear expression from the sets, through the selection conditions derived, to obtain the correct output. We propose a visual pattern matching scheme for the derivation of selection conditions. In this scheme, the input combinations of matched function outputs for individual linear expressions obtained from Stage 2, are plotted in the input domain space. Based on the distribution patterns obtained, certain boundary conditions are extracted, which can distinguish between individual linear expressions.

CHAPTER 3

OVERVIEW OF DIFFERENT MVL TECHNOLOGIES

Till now different new techniques and methods have been tried for implementing ternary logic. Among them, the work with CMOS technology is the oldest. After that comes ternary logic using Resonant tunneling diode. Ternary logic using Single Electron Transistor, FinFET, Quantum Dot Gate Field Effect Transistor, Memristor, CNTFET and MoS2 based memcapacitance modelling are more recent research work.

3.1 Ternary logic using CMOS

One of the main reasons for selecting CMOS for ternary logic is similarity and compatibility. And prevailing binary CMOS circuit can be modified with little effort to be converted into ternary circuit. There will be no need to devise any new types of transistors. The threshold values of MOS transistors can easily be changed during fabrication process which can be uses as a means to create multiple voltage or current levels. The concept of using CMOS for ternary logic has been utilized by many since its first inception by Mouftah and Jordan in 1974 [7], [8]. After that, many researchers have worked on this topic to come up with better and simpler circuits for ternary logic with CMOS.

Mostly, two different techniques have been explored for this purpose. One is to use a combination of enhancement and depletion type of MOSFETs in the same circuit [9]-[11] and the other is to use only enhancement type MOSFETs alongside some resistors in some cases to utilize the voltage divider rules to obtain multiple values [8]-[12].

From [9], figure 1 shows the circuit diagram of a STI, NTI and PTI respectively using first technique. For the STI, the output shows a balanced standard ternary inverter, i.e. for the input logic level of 1, 0 and -1, the output will have a value of -1, 0 and 1. When

the input is of high value (logic 1), Q1 will be off whereas Q2 will be on. And Q3 will be off though Q4 will be on. This setup will keep the output node at low value (-1 V). For the low input voltage (logic -1), Q1 and Q3 remains on, whereas, Q2 and Q4 becomes off so the output becomes high. For an intermediate input value, Q1 and Q2 will remain off and Q3 and Q4 will be on, thus making the output connected to ground (logic 0).

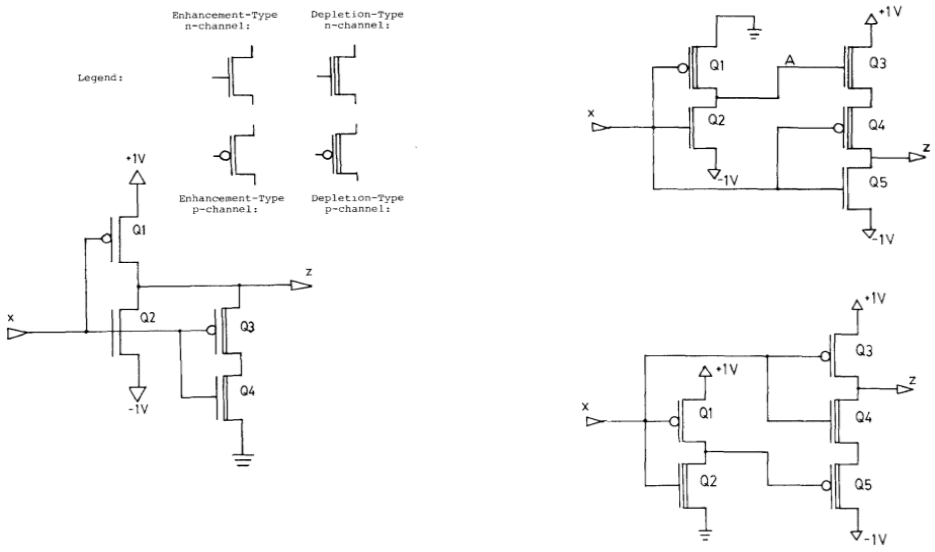

Figure 1: a) STI b) PTI and c) NTI

The condition for the STI circuit to work is:

$$V < V_T < 2 \qquad 7$$

$$0 < V_P < V \qquad 8$$

Where ±V = Value of the power supply

V_T= Threshold voltage of the enhancement MOS transistors

V_P = Pinchoff voltage of the depletion devices

For the ternary circuits with only enhancement type MOSFETs with resistors, a resistive value is inserted in between to get the required intermediate

voltage level (figure 2) [8]. Figure 3 shows the DC transfer characteristics of the circuit diagrams in figure 2.

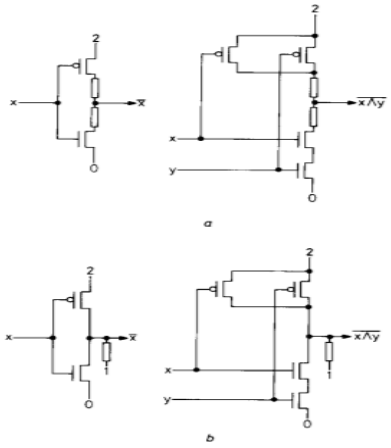

Figure 2: Ternary inverter and NAND gate

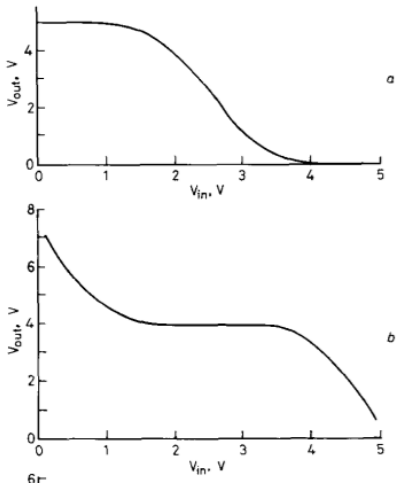

Figure 3: (a) Transfer characteristics with 2 resistors

(b) Transfer characteristics with 1 resistor [6]

The same circuit can be formulated without using the resistors and controlling the threshold voltage also [13]. And all the processes can be extended to create some other basic blocks like NAND, NOR, ALU etc.

3.2 Resonant Tunneling Diode (RTD) based ternary logic

A Resonant tunneling diode is a device in which there are different semiconductor materials which are present in alternate layers. Tunneling of electrons through different resonant states at certain energy levels causes the flow of current inside the device. The current-voltage (I-V) curve of a RTD demonstrations the negative differential resistance (NDR) feature. The decreasing part of the current curve with respect to the voltage gives rise to the negative differential resistance. This characteristic is very crucial to the circuit implementation as it can offer different voltage-controllable logic levels corresponding to the peak and valley currents. It consists of two heavily doped contacts made of a semiconducting material with a narrow energy gap (e.g. GaAs). These two contacts make the emitter and collector region. In between them there are two barriers made of a larger band gap material (e.g. AlGaAs). These two barriers encompass a quantum well which is made of the relatively smaller bandgap material, as shown in Figure 4 [14]. This type of structure is called a Double Barrier Quantum Well (DBQW) structure.

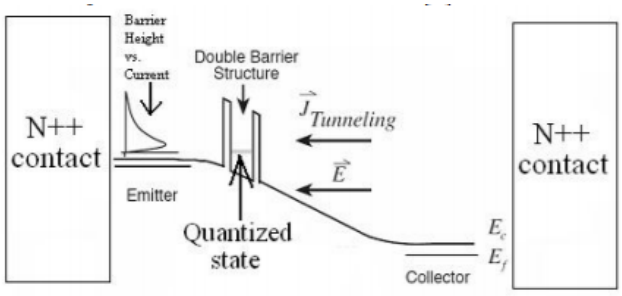

Figure 4: Resonant Tunneling Diode operation showing the quantum well (Gray area)

Before applying any forward bias, majority of the electrons and holes create an accumulation layer in the emitter and collector region respectively. With the application of a forward voltage bias, an electric field is generated. This field forces the electrons to travel from the emitter region to the collector by the process of tunneling through the scattered

states inside the quantum well. Due to the tunneling of electrons through these quasi-bound energy states, current is created.

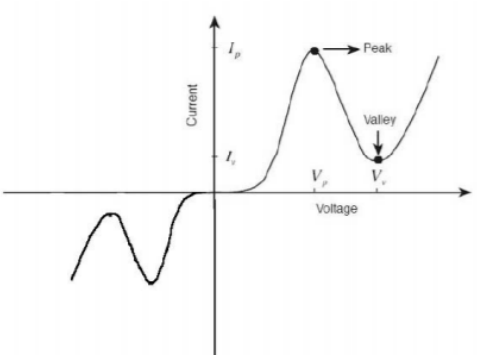

Figure 5: RTD I-V characteristics

As the number of electrons in the emitter with the same energy as the quasi-bound state increases, more electrons become able to tunnel through the quantum well. This results an increase of current corresponding to the applied voltage. At a point the energy level of the emitter electrons matches the energy level of the quasi-bound state. At that point the current reaches its' maximum value and resonant tunneling is said to happen. The occurrence of the resonant tunneling is observed at a certain resonant energy level which depends on the corresponding doping level and the quantum well width. As the applied bias keeps on increasing, more electrons obtain too much energy than the energy of the quantum well and the amount of current starts decreasing. After reaching a specific applied voltage, current rises again due to the substantial thermionic emission where it is possible for the electrons to tunnel through the non-resonant energy levels as well. The current at the minimum valley is termed as leakage current.

Different ternary and quaternary logic gates and memory devices have been proposed using different circuitry [15]-[17]. Among all of these, a very famous technique is the use of different combination of up and down literals to produce multiple valued

outputs. These literals can be obtained by using circuits called monostable-to-bi-stable transition logic elements (MOBILE) [17], [18].

Two RTD's connected in series combination creates a MOBILE, as shown in figure 6. Here, X has a gate which can module the peak current. The output voltage curve for respective input voltage can be seen in figure 6 (b). V1 is considered for low voltage and V2 is for high voltage. When V_{CLOCK}=V1, both the RTD's are ON and the circuit is in monostable state. When V_{CLOCK}=V2, the circuit transfers to bi-stable state. V2 is selected in such a way that either A or X switches to OFF state from ON state when V_{CLOCK} is set to V2. Depending on the ON and OFF states of A and X, high or low voltages can be seen in output.

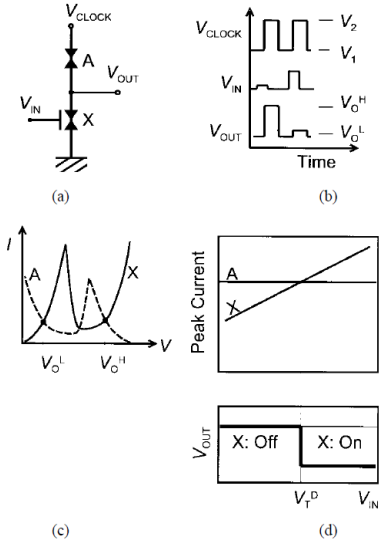

Figure 6: (a) Circuit diagram of a down literal MOBILE, (b) Voltage vs time graph of the operation, (c) current voltage curve showing the bi-stable state and (d) peak currents as a function of input voltage and output voltage

Here, the peak current of X increases with an increase in gate voltage V_{IN}. If $V_{IN}<V_T^D$, the peak current of X is less than peak current of A, which changes the state of

X from ON to OFF. Thus, the output voltage is found to be V_O^H (High). Again, when $V_{IN}>V_T^D$, the peak current of A is smaller than that of X. For that, A switches to OFF state making the output V_O^L (low).

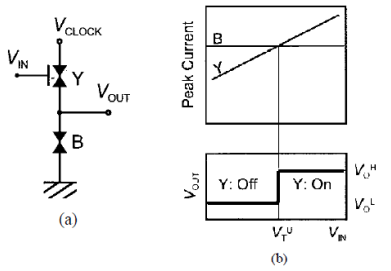

Figure 7: (a) Circuit configuration of an up literal MOBILE. (b) peak currents as a function of input voltage and transfer characteristics of up literal.

Similarly, an up literal can be obtained in a manner shown in figure 7.

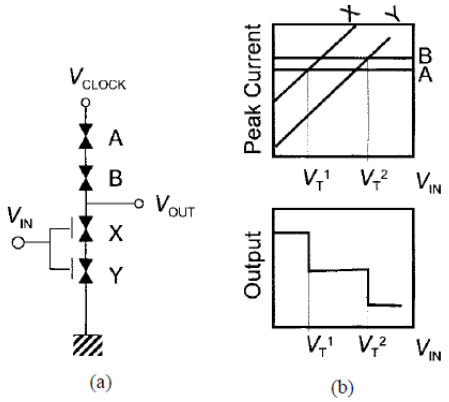

Figure 8: (a) Circuit configuration of ternary inverter and (b) peak currents as a function of input voltage and transfer characteristics of a ternary inverter.

By combining these up and down literals any transfer characteristics with multiple thresholds and multiple outputs can be presented. In [17], a ternary inverter was proposed using the combination of two down literals. In figure 8(a), the circuit configuration of a ternary inverter using only down literals is given. Here, one down literal is comprised of A and X with a threshold voltage of V_T^1 and another pair of is consisted of B and Y which

has the threshold voltage V_T^2. Peak current of A is smaller than peak current of B. When V_{CLOCK}=V2 (high), and $V_{IN}<V_T^1$, the output is at highest value (2). When $V_T^1<V_{IN}<V_T^2$, A and Y are switched off which results an intermediate output voltage (1). For $V_{IN}>V_T^2$, A and B are switched off and the output becomes low (0). The operating conditions and different states are summarized in Table 6.

Table 6 operating condition of different states

V_{IN}	Switched OFF RTDs	V_{OUT}
$V_{IN}<V_T^1$	X, Y	2
$V_T^1<V_{IN}<V_T^2$	A, Y	1
$V_{IN}>V_T^2$	A, B	0

There are few other ways which combine the RTD with some other technologies like HEMT (High Electron Mobility Transistors), HBT (Heterojunction Bipolar Transistor) or MODFET (Modulation Doped Field-Effect Transistor) to produce multiple valued logic circuits [17].

3.3 Ternary Logic using Single Electron Transistor:

Single Electron Transistor or SET is such a device which is based on Coulomb Blockade Effect. A SET comprises of two electrodes which work as the drain and the source. These electrodes are connected through tunnel junctions to a Quantum Dot (QD) which is also called the island. A third electrode, known as the gate, which is capacitively coupled to the island can be used to control the electrical properties of the island. The structural diagram of a SET can be seen from Figure 9[20].

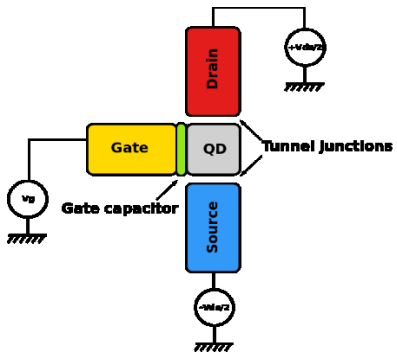

Figure 9: Single Electron Transistor

Figure 10, shows the working principle of a SET-in terms of energy levels. In the absence of an applied external bias, a blocking state prevails. Here, no available energy levels of the island are in the range of tunneling for the electrons in the source contact (in red). All the available or lower energy levels are occupied beforehand. Upon application of a positive voltage, the energy levels are lowered for the island electrode. At that point, the emitter electron (green 1) can tunnel through a previously vacant energy state of the island (green 2) to the drain electrode (green 3). Here it inelastically scatters and moves to the drain electrode fermi level.

The separation between the energy levels of the island electrode is ΔE which gives rise to a self-capacitance C of the island, which can be defined by the equation.

$$C = \frac{e^2}{\Delta E} \qquad 9$$

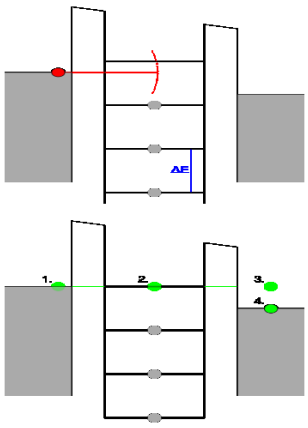

Figure 10: Left to right: energy levels of source, island and drain in a single-electron transistor for the blocking state (upper part) and transmitting state (lower part)

The remarkable characteristics of a SET is the possibility to include multiple gates and thus have a threshold voltage which is adjustable. Figure 11 demonstrates a dual gate single electron transistor. Here, C_{g1} and C_{g2} are the gates capacitances of gate 1 and gate 2 respectively. C_D and C_s are tunnel junction capacitors of drain and source. One gate is used for the voltage input port and another port is defined is threshold voltage adjusting port. The input for these two gates are V_{in} and V_{con} respectively. The voltage on the island V_{island} controls the current flowing through two tunnel junctions and can be represented by equation.

$$V_{island} = \frac{1}{C_\Sigma}(C_D V_{DS} + C_{g1} V_{in} + C_{g2} V_{con} - ne) \qquad 10$$

Here, $C_\Sigma = C_{g1} + C_{g2} + C_D + C_S$ and n is the number of electrons on the island [21].

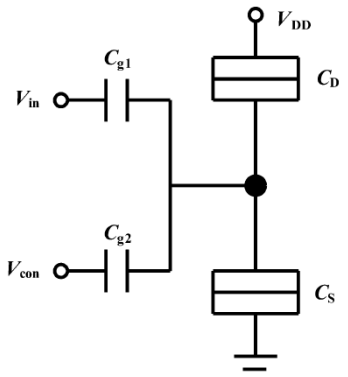

Figure 11: Dual gate SET

Considering the inherent threshold voltage of the island to be V_{th}, the condition for turning the SET on is:

$$V_{island} > V_{th} \tag{11}$$

$$\Rightarrow \frac{1}{C_\Sigma}\left(C_D V_{DS} + C_{g1} V_{in} + C_{g2} V_{con} - ne\right) > V_{th} \tag{12}$$

$$\Rightarrow V_{in} > \frac{C_\Sigma V_{th} - C_{g2} V_{con} - C_D V_{DS}}{c_{g1}} \tag{13}$$

Hence, the gate threshold voltage can be defined by the equation.

$$V'_{in} > \frac{C_\Sigma V_{th} - C_{g2} V_{con} - C_D V_{DS}}{c_{g1}} \tag{14}$$

Using the concept of SET [22] and [23] proposes a design to implement basic ternary gates. And [24] proposes a design for ternary logic-based gate by merging both Set and MOS transistors.

3.4 Fin Field Effect Transistor based ternary logic:

Whenever a lower node technology is introduced, it originates different kinds of short dimension effects like Carrier velocity saturation & mobility degradation, Drain Induced Barrier Lowering (DIBL), punch-through, hot carrier effects etc. If the channel length is small enough to compare with the source and drain depletion region, the

magnitude of these short channel effects increases manifold. Due to these effects the leakage current flows more easily through the channel and it is turning off the transistor becomes difficult. One way to alleviate this situation is to make the channel above the substrate making a fin like structure. The gate is wrapped around the fin shaped channel giving a better control of the channel. This gives rise to a vertical channeled device called FinFET in contrast to the horizontal channel of planer MOSFET. For FinFET, the height of the fin plays crucial role in determining the channel width. The channel width L for FinFET can be derived using equation [25].

$$L = 2 * Fin\ Height + Fin\ width \quad (15)$$

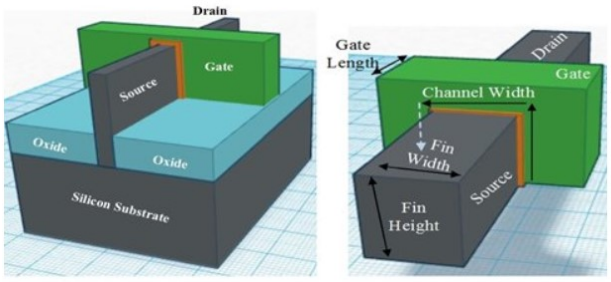

Figure 12: FinFET Structure

FinFET can be used to design ternary logic circuits like the CMOS ternary. The voltage transfer curve of FinFET shows three quite distinct voltage levels [26] which makes FinFET a suitable candidate for applying ternary logic. As FinFET is the best possible alternative for CMOS for the sub 22-nm technology, it is most convenient to implement ternary logic using FinFET also. The circuit diagram for applying ternary inverter, NAND, NOR etc. basic gates are like the binary CMOS gates [27]. More complex gates like ternary decoder, memory cells etc. are also possible to implement with Fin FET [26]-[28].

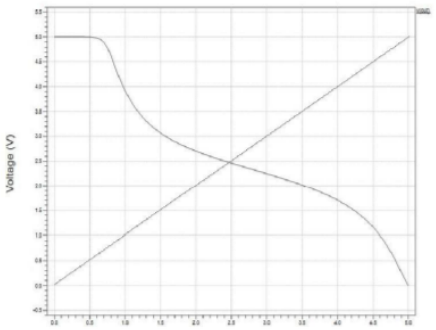

Figure 13: Voltage Transfer Curve of FinFET

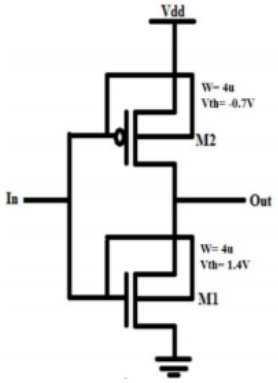

Figure 14: FinFET based STI

3.5 Ternary logic using Quantum Dot Gate Field Effect Transistor

Quantum Dot (QD): A quantum dot is a miniscule configuration of electrons enclosed in a three-dimensional potential well and the size of the well is in the range of the size of de Broglie wavelength of electrons. Any quarantined atom or a multi molecular collection of atoms can also be called quantum dots. A quantum dot exhibits similar discrete, quantized energy levels like an atom and sometimes called an “artificial atom”. By controlling the dimension of the quantum dots, the energy levels can be modified.

A QDGFET is a similar kind of structure like MOSFET and it can be fabricated with the conventional CMOS fabrication process, which makes this technology more

practical and reasonable [29]. In a QDGFET, on top the gate oxide layer, there remains two layers of quantum dots. Upon application of gate voltage, the charge carriers from the inversion channel moves through the gate insulator to the QD layers by means of resonant tunneling, thus creating a new intermediate state in between the two stable states. The device structure of a QDGFET is shown in figure 7.

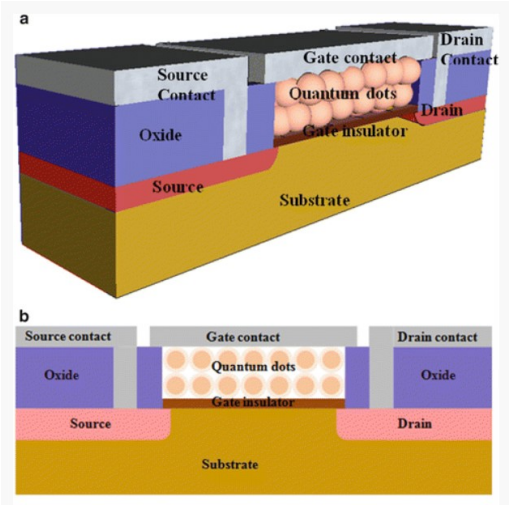

Figure 15: Structural diagram of QDGFET

The QDs which are deposited in the gate area are comprised of nanocrystals of silicon (Si) or geranium (Ge) which are cladded by their oxide. Due to the presence of tunnel oxide enclosing the semiconductor nanocrystal, the charge leakage is reduced [30].

For a QDGFET, when gate voltage V_{GS} is increased, because of resonant tunneling, the threshold voltage V_{th} also increases, keeping the overdrive voltage (V_{GS} - V_{th}) constant. The threshold voltage of a QDGFET can be expressed with the equations.

$$V_{Teff} = \begin{cases} V_T, & V_{GS} < V_{g1} \\ V_T + \alpha(V_{GS} - V_{g1}), & V_{g1} < V_{GS} < V_{g2} \\ V_T + \alpha(V_{g2} - V_{g1}), & V_{GS} > V_{g2} \end{cases} \quad 16$$

Where, V_{g1} and V_{g2} are respectively the lower and upper threshold voltage of the intermediate state and they are dependent on device structure. Within the range of V_{g1} and V_{g2} the threshold voltage changes linearly with gate voltage and the rate of linearity depends on the value of α. When α=0, the device acts like a simple FET and for α=1, the threshold voltage that changes linearly with $V_{GS.}$ Value of α can be controlled by changing the thickness of insulator or by changing the size and number of dots [31]. And the drain current equation is:

$$I_D = \begin{cases} 0, & V_{GS} < V_{Teff} \\ \frac{W}{L} C_o \mu \left(V_{GS} - V_{Teff} - \frac{V_{DS}}{2} \right) V_{DS}, & V_{DS} < V_{GS} - V_{Teff} \\ \frac{W}{L} C_o \mu \frac{(V_{GS} - V_{Teff})^2}{2}, & V_{DS} > V_{GS} - V_{Teff} \end{cases} \quad 17$$

The graph derived from the drain current equation is showed in figure 18.

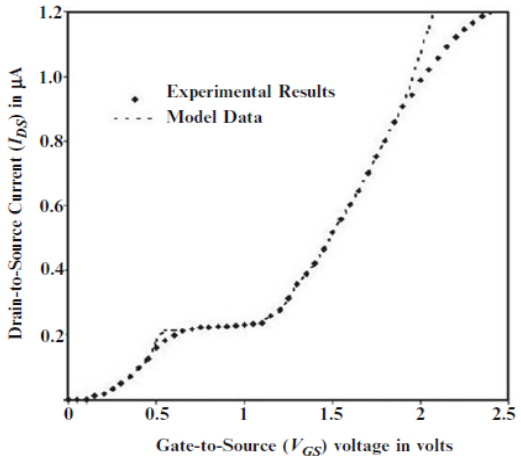

Figure 16: I_{DS} vs V_{GS} in QDGFET[31

And figure 17 and 18 shows a CMOS representation of a standard ternary inverter using QDGFET and its transfer characteristics:

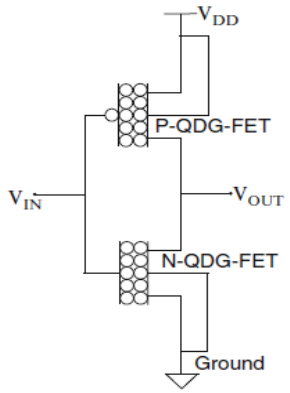

Figure 17: STI using QDGFET

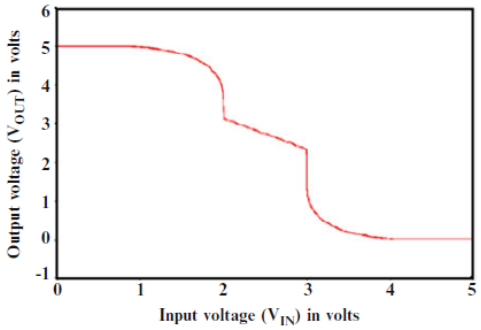

Figure 188: Transfer characteristics of QDGFET based STI [32]

Similarly, ternary NAND, NOR etc. basic gates can be designed using QDGFET following the similar circuit diagrams of binary CMOS. Being similar in circuit diagram and fabrication process, QDGFET based ternary circuits can be easily produced by prevailing binary logic gate architecture.

3.6 Ternary Logic using CMOS and memristor

Memristor is a nonvolatile passive memory element which can retain its information even if there is no power supply, which is introduced by Chan Leon in 1971. As per Leon Memristance is the missing relation between flux and charge. The relationship between the flux and charge can be describe as

$$M = \frac{d\emptyset}{dq} \quad (18)$$

Memristor is a very good alternative to the resistive-load ternary designs, because of its ability to handle more than two states with minimal hardware. Changes in the memristance depend upon the history of the device (e.g., the memristance may depend on the total charge passing through the device, or alternatively, on the integral over time of the applied voltage across the ports of the device).

Figure 19: Memristive device symbol

The thick black line on the left side of the device represents the polarity of the device. If the current flows into the device, the resistance of the device decreases which can be defined as R_{on}. If the current flows out of the device, the resistance increases and can be described as R_{off}.

Formally, a current-controlled time-invariant memristive system is represented by

$$\frac{dx}{dt} = f(x, i) \quad (19)$$

$$v(t) = R(x, i) \times i(t) \quad (20)$$

Where x is an internal state variable, $i(t)$ is the memristive device current, $v(t)$ is the voltage of the memristive device, $R(x, i)$ is the memristance, and t is time [33]. The symbol of a memristor is illustrated in Figure 19. Note that the polarity of the symbol defines the sign (positive or negative) of the current.

Memristor Based Ternary Inverter Design:

Memristor is a very suitable alternative to resistive load ternary designs. A deign to implement basic ternary logic gates like inverter, NAND and NOR gates using CMOS and memristor are given in [34]. A diagram of memristor based ternary inverter is seen from Figure 20.

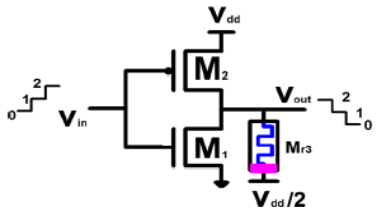

Figure 20: Ternary inverter using CMOS and Memristor.

3.7 Ternary Logic using CNTFET

CNTFET definition: The CNTFET is manufactured by depositing Carbon Nano-Tubes on to the silicon substrate, a CNT is a carbon material made from Graphene sheet. Rolling the graphene sheet in different chirality angels, can define the behavior of the CNT's. Depending on the chirality vector only, a CNT can act as a metal or semiconductor. n and m represents the chirality values of the CNT. If $n = m$ *or* $n - m = 3i$ (where i is an integer value) creates a metallic CNT, and $n - m > 3i$ creates a semiconductor CNT. For a single walled CNT with chiralities (m, n), diameter of the CNT can be expresses as D_{cnt}.

$$D_{cnt} = \frac{a\sqrt{n^2 + m^2 + nm}}{\pi} \quad (21)$$

Here, $a = 2.49$ Å is the interatomic distance between each two neighboring atoms. And the chiral angle can be defined as [32]:

$$\theta = \tan^{-1}\frac{\sqrt{3}n}{2m + n} \quad (22)$$

There exists quite similarity between I-V characteristics of a CNTFET and a MOSFET. The threshold voltage of a device can be described in terms of the voltage required to turn the device ON. In case of the CNTFET, the threshold voltage of the intrinsic CNT channel can be approximated to the first order as the half-bandgap that is an inverse function of the diameter [36].

$$V_{th} \sim \frac{Eg}{2e} = \frac{aV\pi}{\sqrt{3}\ \mathrm{x}\ \mathrm{eD_{cnt}}} \qquad 23$$

The parameter $V\pi$ (~ 3.033 eV) is the carbon π-π bond energy in the tight bonding model, e is the unit electron charge, and D_{cnt} is the diameter of a CNT.

For a (19,0), the D_{cnt} is found to be 1.487 nm. Putting all the values in equation, V_{th} is found to be 0.293V. Considering m in the chirality vector to be 0, it can be derived from the equation that the threshold voltage of the CNTFET is inversely proportional to the diameter of the CNT as well as the chirality vector n if the CNT.

$$\frac{V_{th1}}{V_{th2}} = \frac{D_{cnt2}}{D_{cnt1}} = \frac{n_2}{n_1} \qquad 24$$

Figure 21 gives a structural diagram of a CNTFET. Like a conventional CMOS, CNTFET also has four terminals. Here, the channel region is consisting of an undoped semiconducting carbon nanotubes or CNTs which is present under the gate region. And some heavily doped CNT segments are placed between gate and source/drain to permit for a low series resistance in the on-state.

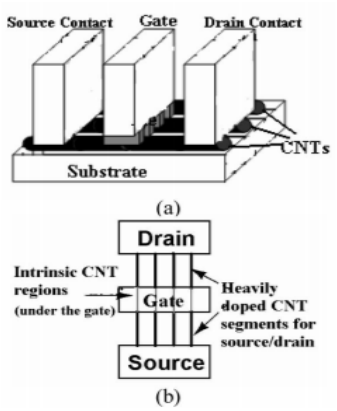

Figure 21: Fundamental structure of CNTFET (a) cross-sectional view (b) top view

CNTFET Based Ternary Inverter Design:

The main advantages of using CNTFET in a logic circuit is the opportunity of using transistors with different threshold voltage in the same circuit. Using this concept, two different standard ternary inverter (STI) were proposed in [37]-[38] which has their own merits and demits. The proposed design in [37] is shown in figure 21 and the design in [38] is shown in figure 22.

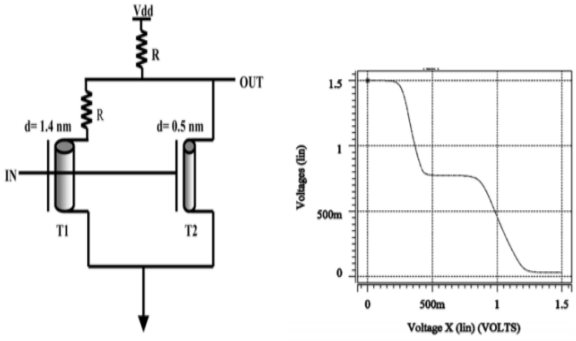

Figure 22: Proposed design CNTFET based inverter and its' transfer characteristics from [34]

In figure 21, two CNTFETs with diameter d_1=1.4nm and d_2=0.5nm are used. As a result, the threshold voltages of the two CNTFETs are V_{th1}=300mV and V_{th2}=840mV respectively. Two resistors both with the value 100kΩ are used. When the input voltage is

less than 300mV, both the transistors are in off-state and the output voltage is equal to V_{dd} (1.5V). For input voltage greater than 300mV, transistor T_1 becomes on and the output voltage reaches the value near to $V_{dd}/2$. As input voltage becomes equal to V_{th2}, second transistor is turned on and the output reaches an almost zero state.

The proposed design in [38] uses 6 transistors which can be observed from figure 22.

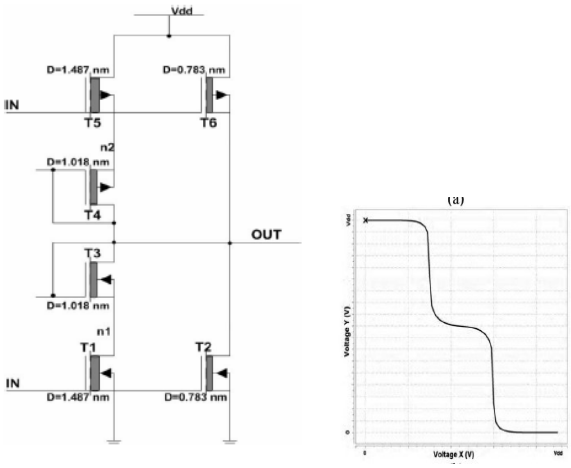

Figure 20: Design of CNTFET based inverter and its' transfer characteristics [35]

The properties of the 6 transistors are given below:

- The chiralities of the CNTs used in T1/T5, T2/T6, and T3/T4 are (19, 0), (10, 0), and (13, 0), respectively.
- The diameters of T1/T5, T2/T6, and T3/T4 are 1.487, 0.783, and 1.018 nm, respectively.
- The threshold voltages of T1, T2, and T3 are 0.289, 0.559 and 0.428 V, respectively.
- The threshold voltages of T5, T6, and T4 are –0.289, –0.559, and –0.428 V, respectively.

As the input voltage is increased from low to high (low being 0V and high being 0.9V), primarily the input voltage is lower than 300 mV. This turns ON both the transistors T5 and T6, and both T1 and T2 are turned OFF; the output voltage is 0.9 V, i.e., logic 2. When the input voltage rises to a value greater than 300 mV, T6 is OFF and T5 is still ON and T1 is ON and T2 is OFF. The diode connecting the CNTFETs T4 and T3 generates a voltage drop of 0.45V in between node n2 and output and in between output and node n1 due to the threshold voltages of T4 and T3. Therefore, the output voltage takes a value of half of the power supply voltage, i.e., 0.45 V. From table 1, it is seen that half V_{dd} represents logic 1. Once the input voltage goes above 0.6 V, both T5 and T6 are OFF, and T2 is ON to pull the output voltage down to zero. The transition from high to low is like the low to high transition.

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CHAPTER 4

GRAPHENE MEMCAPACITOR BASED TERNARY LOGIC DEVICE

Ternary logic devices are expected to lead to an exponential increase of the information handling capability, which binary logic cannot support. Memory capacitor or memcapacitor is an emerging device that exhibits hysteresis behavior, which can be manipulated by external parameters, such as, the applied electric field or voltage. One of the unique properties of the memcapacitor is that by using the percolation approach, we can achieve Metal-Insulator-Transition (MIT) phenomenon, which can be utilized to obtain a staggered hysteresis loop. For multivalued logic devices staggered hysteresis behavior is the critical requirement. In this paper, we propose a new conceptual design of a ternary logic device by vertically stacking dielectric material interleaved with layers of graphene nanoribbon (GNR) between two external metal plates. The proposed device structure displays the memcapacitive behavior with the fast switching metal-to-insulator transition in picosecond scale. The device model is later extended into a vertical-cascaded version, which acts as a ternary device.

4.1 Introduction

Modern computing devices based on binary logic circuits are expected to meet a massive challenge in the immediate future because of the exponential surge of information density and data handling and storage requirements. To alleviate this constraint of the binary devices, researchers have been exploring multi-valued-logic (MVL) technologies and its applications in logic and memory devices. MVL is the logic system, which uses more than two logic levels to define the state. Different materials and device technologies have been investigated to implement the MVL devices, and among them, graphene is one

of the most promising material platforms. Memcapacitor is an entirely new device that is being explored for many future nanoelectronics applications. Memcapacitor is fundamentally a capacitive device with memory capability, which upon applying an external stimulus like electric field or voltage, can exhibit different capacitance values. In this paper, we propose a ternary logic/memory device comprised of vertically stacked dielectric layers interleaved with graphene nanoribbon (GNR) layers placed between two external metal plates.

Emerging circuit elements like memristors, memcapacitors, and meminductors have a unique property of exhibiting memory capability along with the conventional electrical properties of resistance, capacitance, and inductance, respectively. The memristor, which was first introduced by Leon Chua in 1971, is considered as the fourth electrical element that provides the direct relation between the electrical charge and the magnetic flux of a device. Memristor can limit or control the flow of the electric current in a circuit and remember the amount of charge that has previously flowed through it. Memcapacitor and meminductor are two other memory elements, which have the similar memory characteristics. A memcapacitive system can either be voltage controlled or charge controlled. An n-order voltage-control system is defined by equations.

$$q(t) = C(x, V_c, t) \times V_c(t) \quad (25)$$

$$\dot{x} = f(x, V_c, t) \quad (26)$$

Here q(t) defines the charge on the capacitor at time t, $V_C(t)$ defines the corresponding voltage at time t, C defines the memcapacitance value and x = {x1, x2} is the set of internal state. To explore variables like position as well as velocities of all the

ions in the material. In the same way, an n-order charge control system is defined by the equations [39], [40].

$$V_c(t) = C^{-1}(x, q, t) \times q(t) \quad (27)$$

$$\dot{x} = f(x, q, t) \quad (28)$$

To explore the memcapacitive behavior, several methods have been researched. One of the ways to achieve memcapacitance is to utilize metal-insulator-transition (MIT) phenomenon. The band theory of material states that metals possess a partially filled band and insulators possess a fully filled band. Accordingly, the physical properties of the materials are quite stable, i.e., metals are always good conductor of charges and insulators are always bad conductors of charges [41]. The Metal-Insulator-Transition (MIT) phenomenon is the unusual property of a material to transit between the metallic and the insulating states of a material. It is possible to attain these transitions in the MIT materials by altering different ambient variables like pressure and doping in a semiconductor [42]. This paper discusses a new method of utilizing MIT phenomenon to achieve the memcapacitive behavior. In this paper, a voltage controlled memcapacitive device is modeled with GNR, which is later extended to create a ternary logic/memory device.

4.2 Fundamental concepts and the technological background of the Proposed Device

The proposed device is based on exploiting the memcapacitive behavior obtained by using the MIT phenomenon of a graphene-dielectric structure. The MIT behavior is mainly found in the dichalcogenide material. Several experiments show that graphene nanoribbon (GNR) exhibits MIT behavior under a specific condition. This MIT behavior

can be utilized to design memcapacitor and MVL device using GNR. In the next few subsections, the fundamental concepts behind this work are illustrated.

4.2.1 The Fundamentals of MVL Device

Multi valued logic system is the system comprising “R” distinct logic levels, where R>2. The traditional base 2 or binary numeral system in the digital world works with only two values namely “true” and “false” or “1” and “0”. However, the MVL system may consists of a set of any number of logic levels, which are represented by some signal variables, such as, current, voltage or charge. These set of values can be illustrated using any of the two conventions: unbalanced and balanced. Unbalanced system is the extension of the binary number system in single direction, for instance 0, 1, 2, 3… (R-2), (R-1). And the balanced system needs an odd radix R=2K+1, with the values (-K), (1-K) … -1, 0, 1…, (K-1), K. In the same way, ternary logic system uses three values to represent false, true and undefined. It can also be unbalanced: 0, 1, 2 or balanced: -1, 0, 1. In this paper, an unbalanced ternary device has been proposed.

4.2.2 Graphene Nanoribbon (GNR) as an MIT Material

MIT phenomenon, which can be explained in terms of the percolation probability, is described as the transition from the metallic to the insulating behavior of a material in picosecond time scale. These transitions can be attained by the alteration of various ambient parameters, for example, pressure [43], [44]. MIT materials can obtain any of the two given possible states defined as the metallic and insulating states, based on which capacitance of the model is changed. These two different behavioral states can be used as the electrical states. There are meta-materials, which exhibit this type of transition in μsec time scale using slow polarization approach. Dichalcogenide materials like MoS_2 generally

shows this kind of MIT phenomenon [45]. It is also discovered that GNR can exhibit MIT properties. Graphene is an allotrope of single layer carbon, which is found in group IV of the periodic table and has zero bandgap. Based on the hexagonal lattice structure, GNR can be of two types: Armchair and Zigzag GNR. For the case of aGNR (Armchair GNR), it has been proven that by controlling the physical properties like width, impurities etc. it is possible to introduce bandgap Fig. 24 shows the structure of both types of GNRs [46].

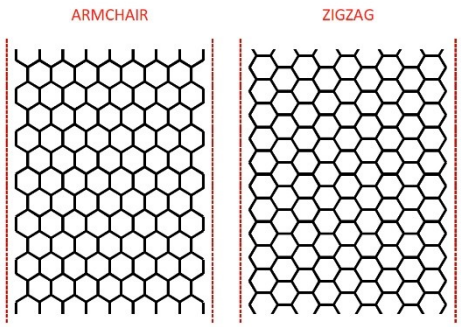


Figure 24: a) Armchair b) Zigzag GNR

In our proposed MVL device, we are considering GNR instead of 3D or bulk graphene because GNR has a finite bandgap that facilitates a transport gap induced by the percolation (i.e., two separate 2D MIT transitions for electrons and holes). GNR displays a 2D MIT for the low-carrier density system as an aftermath of the applied gate voltage [46]. Fig. 25 explains the percolation driven MIT on the naturally occurring GNR. For the finite systems, the percolation is defined as the emergence of a cluster of charge, which extends over the whole system. Conductance $G = (W/L)\sigma$ is the function of the applied gate voltage, which can be given by $V_g \propto n$. Here, W is the width, L is the length and σ is the conductivity of a given sample. For the 2D percolation university class (it is one of the many types of percolation), at low-density $\sigma = A(n - n^c)^{\delta}$, where δ=4/3 is defined as the critical exponent for the 2D percolation. For GNRs, we expect two of such percolation

transitions, one is stated for the electrons and the other is given for the holes, and is divided by the transport gap, which is defined as $\Delta_g = \gamma\sqrt{\pi(n_c^e - n_c^h)}$, where $n_c^{e(h)}$ is given as the critical density of the electrons (holes) and $\gamma = \hbar v_f$ as the graphene Fermi velocity. It is observed that for $W \geq \xi$ the material demonstrates 2D percolation behavior. Here, ξ is the size of the given electron or hole puddles.

2D MIT in GNR is based on the percolation transition instead of the quantum crossover phenomenon. To support this point, percolation density (n_p) can be estimated using the Nonlinear-screening argument of E_{FROS} [47]. The basis for this is that when inhomogeneous density fluctuation produced by the charged impurities cannot be conceived by the carriers anymore, at that time MIT takes place. This results in $n_p \sim \sqrt{n_{imp}}/d$, where n_{imp} is the concentration for the randomly charged impurities which are placed at the distance d from 2-Dimensional graphene plane. Assuming $d \sim 1nm$ and $n_{imp} \sim 2\text{-}5x10^{11}cm^{-2}$, the ideal value proposed from the mobility measurements is $n_p \sim 5x10^{12}cm^{-2}$.

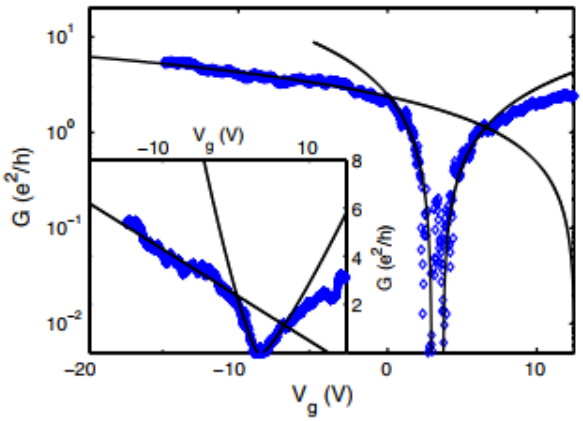


Figure25: Evidence of the percolation-driven MIT in GNR

4.2.3 Percolation based Memcapacitive Model using GNR

In our proposed ternary device, the MIT approach is utilized with GNR as the MIT material, which provides the memcapacitive behavior and makes the transition between the states achievable in psec. In Fig. 26, C_g is the gate capacitance and C_{mit} is the capacitance of the MIT material, which is initiated by the depletion and the misalignment of the charge puddle within the MIT material. To comprehend the condition of the MIT material and the boundary, an I_{offe} Regel-Mott criterion is used [48], [49].

The gate capacitance $C_g$of the device can be given by $C_g \approx \varepsilon_g/d_g$, where, $\varepsilon_g$is the gate dielectric and d_g is the thickness of the gate dielectric. For proposed device, $C_{mit}$is replaced with C_{GNR}, which is the capacitance of the GNR layer and can be described by $C_{GNR} \approx \varepsilon_{GNR}/d_{GNR}$, where, ε_{GNR} is the dielectric of the monolayer GNR and $d_{GNR}$is the thickness of the GNR layer. The total capacitance of the structure $C_{total} = ((1/C_{GNR}) + (1/C_g))^{-1}$. For the monolayer GNR layer, the carrier concentration n can be given by equation.

$$n = \frac{C_g(V_g - V_s - V_T)}{e} \quad (29)$$

Here, V_g is the gate voltage and $V_s = \int_0^{V_g}\left(1 - \frac{C_{total}}{C_g}\right)dV_g$ is the surface potential of the GNR layer which can be calculated by using the Poisson equation on the vertical structure in Fig26. V_T is the intrinsic threshold voltage at which, Metal to Insulator transition occurs for the GNR layer and *e* is the charge of an electrons.

The MIT state according to the Ioffe Regel-Mott criterion on the base of carrier concentration can be given by equation.

$$K_F \times l_e \approx 1; \text{for critical point of transition} \quad (30)$$

$$K_F \times l_e \ll 1 \text{ ; for the insulating state} \quad (31)$$

$$K_F \times l_e \gg 1 \text{ ; showss the metallic state} \quad (32)$$

In equation, $K_F = \sqrt{2\pi n}$ represents the Fermi wave vector and $l_e = {hk_F\mu}/{e}$ represents the mean free path of electrons. Here, h is the planks constant and μ is the mobility of electron.

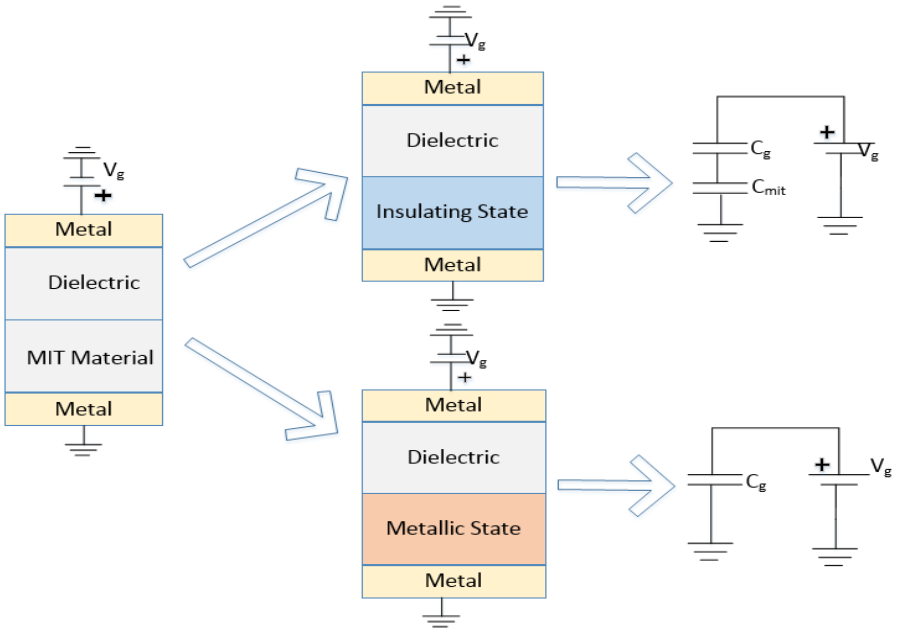
In this paper, a percolation-based modeling approach is used for the MIT material to illustrate the formation and the percolation of the metallic charge puddles. Due to this percolation phenomenon, a conducting channel consisting of charge is created, which sequentially converts the monolayer of MIT material from the insulating to the metallic phase. Equation describes the relation of the percolation probability with the gate voltage.

$$\frac{d}{dt}(p) \approx k \times (v_g - v_{gt}) \times (1 - (2p-1)^{2X}) \quad (33)$$

Here, p is the percolation probability of the monolayer MIT material that varies between zero and one ($0 \le p \le 1$), x = 1 and $k \approx 10^{10}$ are the constant values, and v_{gt} is the applied gate voltage to initiate the MIT transition. A percolation value equal to 1 suggests a conductive state and 0 suggests an insulation state. The value at which the transition happens is known as the critical percolation value p_c, which varies in each material. The term $(1-(2p-1)^{2X}$ in equation is used to show the smooth change between the two stable states to guarantee 0-time rate change of the percolation in a manner such as $\frac{d}{dt}(p) \approx 0$ for the given $p \approx 1$, 0. The memcapacitance value for the proposed device can be expressed as a function of the percolation as in equation. The defining characteristics of

the memcapacitance is that it is a memory element that can make transition between two states following a hysteresis loop.

$$C_{mem}(p) = C_{total} + (C_g - C_{total}) \times p(t) \quad 34$$



(a) (b) (c)

Figure26: MIT material based memcapacitance model that can be used as a binary device – (a) device structure, (b) insulating and metallic states of the device (c) capacitive model of the states [45]

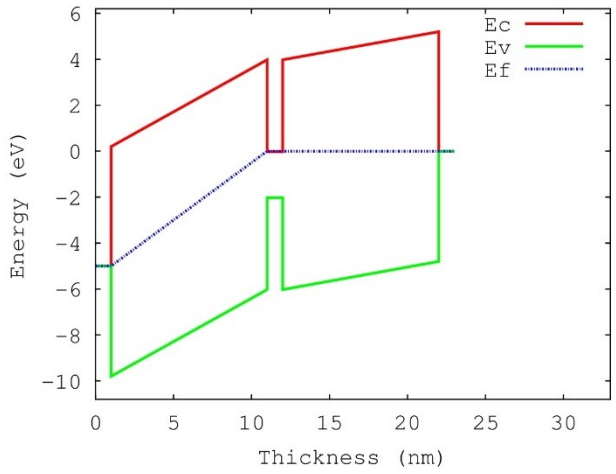


Figure 27: Energy band diagram of the binary device structure presented in Figure 26.

Fig.27, the energy band diagram of the device structure of Fig.26 is drawn. The device has an upper and a lower metal layer made of copper and an applied input voltage of 5V is used. In between the copper plates, a single layer of GNR with a donor doping concentration of 1×10^{11} and layers of dielectric material, Silicon Oxide (SiO_2), with a thickness of 10nm are placed. The simulation is done with the 2D simulation tool available through Nano-hub [50].

The analysis of the proposed MVL device is done in the basis of its relation with the percolation phenomenon and its I-V characteristics. We have also calculated the energy band diagram of the deivce and its comparision with the binary stacked device shown in Fig.26. To explain the electrical properties of the device in terms of the percoation phenomenon, conductivilty power law of percoaltion can be used. Equation states the relationship between the conductivity of the monolayer GNR in terms of the percolation threshold [45],[51].

$$\sigma(p) \approx \sigma_{ins}(p_c - p)^{-s}; \text{insulating region for } p < p_c \qquad 35$$

$$\sigma(p) \approx \sigma_{met}(p - p_c)^t; \text{metallic region for } p > p_c \quad (36)$$

$$\sigma(p_c) \approx \sigma_{met}\left(\frac{\sigma_{ins}}{\sigma_{met}}\right)^u ; \text{critical region for } p \approx p_c \quad (37)$$

The value of the critical exponents t and s depend on the type of conductivity [52] and they are choosen to be 0.3 and 0.2 for our case. Here, $u = \frac{t}{t+s}$ and the value for σ_{met} is taken to be the universal conductivity of GNR [53] and it is equal to $\frac{4}{\pi} \times e^2/h$. Fig.28a shows the relation between the conductivity and the percolation probabity based on equation. And Fig.28b shows the conductivity curve in logarithmic scale, which makes it easy to observe the effect of charge puddle based conductivity.The logarithmic curev shows the transition between each states clearly. With the increase of gate volate, the formation of charge puddle takes place, thereby making the device conducting.

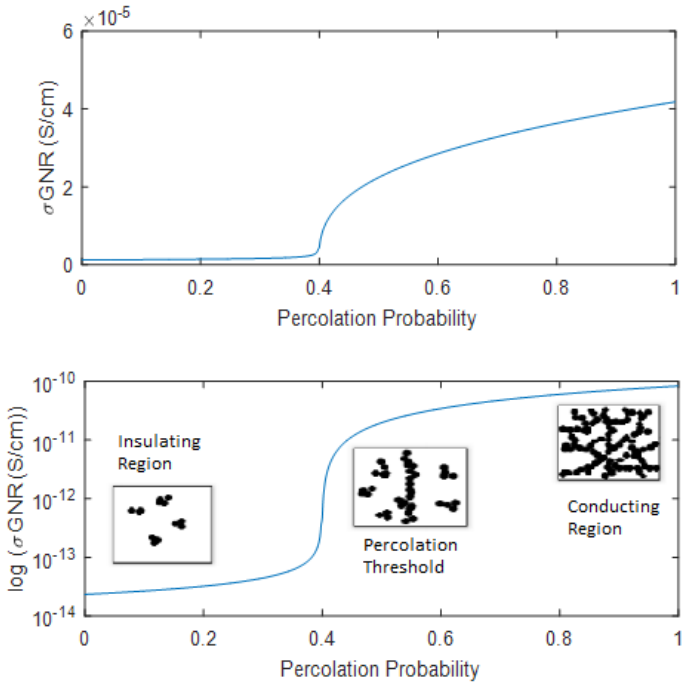


Figure 28: Conductivity of GNR as a function the percolation probability – (a) in linear scale and (b) in logarithmic scale.

4.3 Proposed Ternary Device

The previously explained memcapacitance model in Fig.3 can be vertically cascaded to obtain a staggered behavior with multiple electrical states, which can be utilized to design multi-valued logic or memory device as shown in Fig. 29(a). The individual memcapacitance shown in the Fig.29(c) is given by the equations.

$$C_{mem-1}(p1) = C_{total-1} + (C_{g-1} - C_{total-1}) \times p1(t) \quad 38$$

$$C_{mem-2}(p2) = C_{total-2} + (C_{g-2} - C_{total-2}) \times p2(t) \quad 39$$

Here, p1 and p2 illustrate the given percolative states for the top and the bottom GNR, respectively [43]. These two different percolative states that depend on the external voltage applied on the device generate three distinctive capacitive states for the device. The equivalent capacitance as shown in Fig.29(d) is given by equation.

$$C_{mem}(p1, p2) = \frac{C_{mem-1} \times C_{mem-2}}{C_{mem-1} + C_{mem-2}} \quad (40)$$

Theoretically and experimentally it can be proved that GNR possesses a MIT property and based on this property of GNR we are proposing a new ternary device as shown in Fig.29.

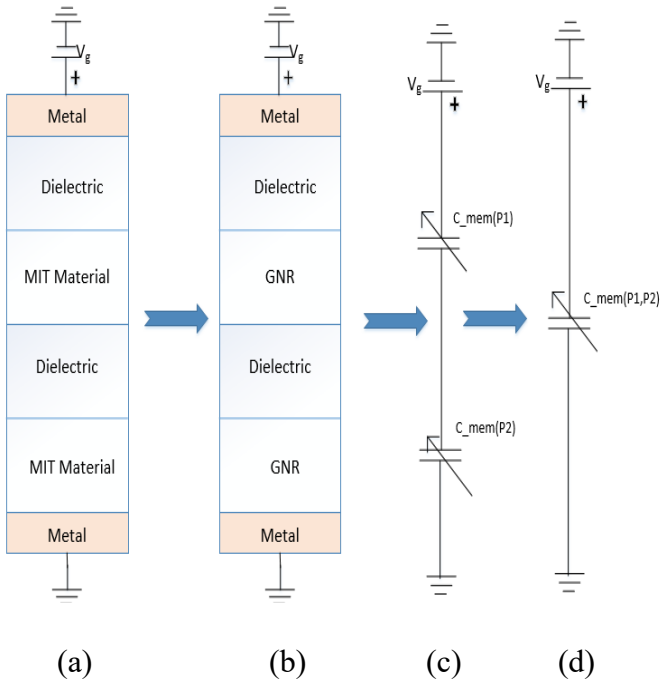


Figure 29. Proposed device structure and its equivalent capacitance model.

The proposed design structure is a vertically stacked structure, which consists of the layers of metal then dielectric then MIT material and then a layer of metal again. The MIT layer can have to possible states, insulating and the metallic, based on which the device equivalent capacitance is changed accordingly. When the voltage is applied the top electrode (metal plates) acts as a gate with a voltage applied to it as v_g to control the percolation of the charge puddles in MIT layer. According to percolation model, the charge puddles percolates to form a conducting channel which then in-turns transits the monolayer from insulating phase to metallic phase. Nanoscale metallic regions emerge from the

insulating host, increase in number and size to form percolative nature. When the carrier concentration in GNR reaches the critical concentration, the charge puddles start to percolate, which in-turns changes the percolation probability drastically. The percolation value near to 1 implies the conductive state of MIT material.

To determine the individual percolation states of both the top and bottom GNR layers, we need to calculate the carrier concentration in both MIT layers. For the structure in Fig.28, let's n_1 and n_2 be the carrier concentration in GNR-1 and GNR-2, respectively. Then according to the principle of electrostatic charge control, n_1 and n_2 with the help of (19) and (14) can be expressed as follows.

$$n_1 \propto C_{g-1} \times V_g \tag{41}$$

$$n_2 \propto \frac{C_{mem-1} \times C_{g-2}}{C_{mem-1} + C_{g-2}} \times V_g \tag{42}$$

In equation, at any instant "t", $n_2(t)$ will always be less than $n_1(t)$ for a given voltage V_g. This implies that after applying I_{offe} Regel criterion to both the GNR layers, the value of critical carrier concentration of layer 2 will always be higher than that of layer 1 such that $n_{c2} > n_{c1}$ and $V_{g2} > V_{g1}$. The difference between these two transition voltages is termed as ΔV_{gt}, which is directly proportional to the term $C_{g-1} - \frac{C_{mem-1} \times C_{g-2}}{C_{mem-1} + C_{g-2}}$. Fig 30 shows the plots for both the percolation states p1 and p2 and overall state of the device at any instant time "t" for a given gate voltage.

Initially both the GNR layers are in the insulating/semiconducting state and the percolation state value for both the layers is zero. This state of cascaded device is termed as state 2 with p1=1 and p2=0. When $V_{g2} > V_{g1}$ the bottom GNR layer undergoes MIT transition too and making the device in state 3 with p1, p2=1.

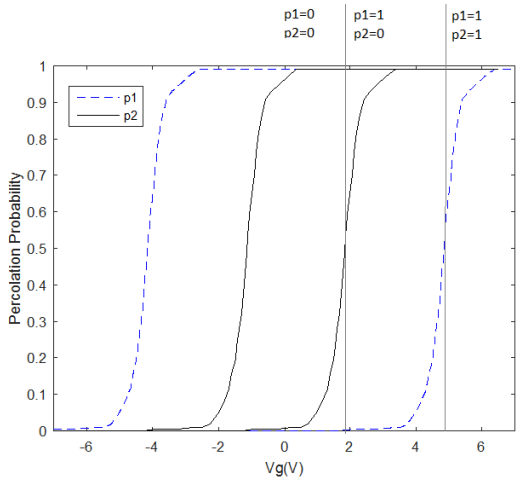


Figure 30. Hysteresis curve showing the percolation states of the individual GNR layer with respect to the changing gate voltages, which in turn forms three distinct states.

4.4 Analysis of the electrical behaviors of the proposed MVL device

Ultrathin 3D (bulk) semiconductors have dangling bonds that form traps for electrons and reduce the performance of field-effect transistors (FETs). By contrast, 2D materials have pristine surfaces. In 2D materials, charge carriers are confined in the atomically thin semiconductor, resulting in a narrower mobile charge distribution. This confinement of charge carriers allows the carriers to be easily controlled by the gate voltage, leading to excellent gate electrostatics [54]. However, despite their advantages, 2D materials do present some challenges. It is critical to control the surface interface and difficult to grow large and defect-free 2D films. The exceptional characteristics (very high charge carrier mobility and electrical conductivity, extraordinary high thermal and physical stability and MIT property) make graphene more suitable than the other 2D materials for our proposed MVL device design. The only limitation of working with graphene is the lack of distinct bandgap, which can be solved by modifying the ribbon width according to need.

Our proposed design is a two-terminal device whereas most of the existing devices are three-terminal devices. The presence of lesser number of input terminals makes the operation of the device simpler and reduces the fabrication process steps. In the case of three-terminal devices like MOSFETs, one terminal is used for controlling the ON-OFF state of the transistor and the other two terminals are used for the supply voltages (V_{dd} and GND). For our design, one terminal is used for controlling the ON-OFF state and the other one is always connected to ground. The presence of a substrate in the conventional devices makes the device size larger compared to our 2-terminal device.

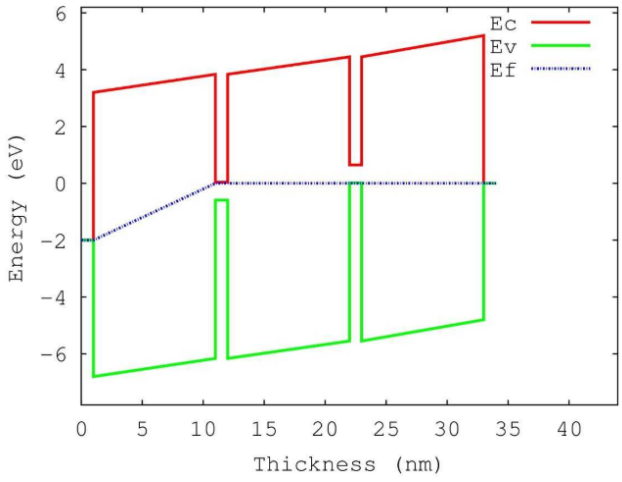


Figure 31: Energy band diagram of the proposed ternary device structure presented in Figure30

In Fig.31, the energy band diagram of the device structure of Fig. 29 is drawn. The structure is like that of Fig.27. The only difference is the number of GNR layer used.

4.5 Comparative Analysis

The theoretical understanding of multi-valued-logic (MVL) has been around since the beginning of the 20th century. Research on many different technologies and implementation approaches for MVL devices has been going on for the last four decades.

In this section, the prospects and the constraints of few of the most promising technologies and approaches have been discussed here. Among all the technologies, CMOS is the oldest one to be explored for the MVL device, mainly because CMOS MVL devices would be compatible to the current process. The prevailing binary CMOS circuits can be modified into ternary circuits through few modifications and new types of transistors are required. As the threshold values of the MOSFET transistors can be easily changed during the fabrication, multiple voltage or current levels can be created. In a current-mode circuits currents re usually defined to have a logic levels that are integer multiples of a reference current unit. In current-mode circuits, currents are usually defined to have logical levels that are integer multiples of a reference current unit. Currents can be copied, scaled, and algebraically sign changed with a simple current mirror. The frequently used linear sum operation can be performed simply by wiring, resulting in a reduced number of active devices in the circuit. Several prototype chips of current-mode CMOS circuits have been fabricated, showing better performance compared to corresponding binary circuits [64]-[68]. It is believed that current-mode designs can allow better noise margin than voltage-mode CMOS designs. Regrettably, the unique characteristics of CMOS binary logic, namely that of zero static power dissipation in either stable state, similar output impedance in either state are not carried over to MVL CMOS circuits. Instead, such circuits are usually characterized by rail-to-rail current flow in one or more static state and higher output impedance in one state compared to other states. Two solutions to these problems have been suggested recently. In current mode CMOS MVL circuits based on dual-rail source-couple logic have been introduced. The use of a complementary input pair and source-coupled logic allows high-speed circuits with low power dissipation. An alternative

solution is proposed in where low-voltage and low-power current-mode MVL circuits are designed using a neuron-MOS transistor. Another problem with CMOS MVL circuits is that, unlike binary CMOS circuits, they are not self-restored. A level restorer circuit must be used every certain number of stages to recover the signal. To overcome this problem, a novel self-restored architecture has been recently presented. It uses both current-mode MVL circuits and voltage-mode binary circuits to implement MVL functions and to restore output signal simultaneously. Binary gates are used within the design architecture so that MVL-binary or binary-MVL conversion circuits are not required to interface with binary circuits. The average size of the resulting circuits is about 50% smaller than previously proposed MVL circuits, while the average power dissipation and time delays are comparable. CMOS multivalued circuits are expected to share the three key advantages of the CMOS binary circuits - zero static power dissipation in the stable states, low-output impedance in the stable states and the elimination of the passive elements (resistors). Any multivalued signal can be transmitted through a CMOS transmission gate. In contrast with the bipolar junction transistors, the ability to change the threshold voltage of the MOS transistors simplifies the task of responding to a multilevel input signal. The first CMOS ternary circuits were proposed in 1974.

An alternative way to implement MVL circuits is to utilize resistors to achieve multiple voltage levels. However, the electrical properties of the resistor based MVL circuits are not desirable [58]. Memristor is a very good alternative to the resistive-load ternary circuit designs because of its ability to handle more than two states with minimal hardware. Changes in the memristance depend upon the history of the device (e.g., the memristance may depend on the total charge passing through the device, or alternatively,

on the integral over time of the applied voltage across the ports of the device). Power dissipation is a crucial parameter for a digital circuit. When both inputs are similar, current does not flow in the circuit and the power dissipation is zero. If different input vectors are considered, current flows and significant amount of power is dissipated in the circuit. The power is dissipated during switching of the memristors and it's depended on the resistance offered by both memristors and changes during the computational process. For cascaded logic gates, the output voltage is depending on the voltage divider action across series connected two memristors. This voltage divider action degrades the output signal; however, this degradation is minor, hence, it can be neglected particularly when Roff>>Ron [59].

CNTFET can act as both metal and semiconductor based on the chirality values. As CNFETs inherit – characteristics that are qualitatively like silicon MOSFETs, most of the present-day MOS circuits can be translated to a CNFET based design [60]. The carbon nanotube field-effect transistor (CNTFET) is a promising alternative to a traditional bulk silicon transistor for low-power and high-performance designs due to the ballistic transport and the low OFF-current properties. Moreover, in a CNTFET, the threshold voltage is determined by the CNT diameter; therefore, a multi-threshold design can be accomplished by employing CNTs with different diameters (chirality) in a CNFET [61].

Other than the circuit level implementation research has been done for the device level implementation. Research has been done for the beyond CMOS technology for the multi valued logic as well. Few of the most promising technologies and approaches have been mentioned here.

As the scaling down of the CMOS technology beyond 22nm is discussed the short-channel effects, unnecessary noise and leakage current comes into picture. In order to reduce these effects, the one of the most promising devices are FINFETs. FINFET are the latest mass-produced Si based transistors used in production of ULSI products.

FINFETs are used to overcome various performance issues on the planar transistor. FINFET have significantly better performance in terms of V_t, Speed and leakage because of its major geometrical change in channel design. FINFET are harder to manufacture and have more complex challenges like design reliability as compared to the planar devices [57].

The other device for the beyond CMOS technology is Single-Electron Transistors have low power consumption, they are compact in size highly sensitive high operating speed it has simplified circuits, operating principle is simple, and it has straight forward cointegration with the traditional CMOS circuits Low energy [55].

To operate SETs at room temperature, large quantities of mono dispersed Nano particles less than 10nm in diameter must be synthesized. But it is very hard to fabricate large quantities of SETs by traditional optical lithography and semiconducting process. It is difficult to link SETs with the outside environment. Practically difficult to fabricate Single electron transistors (SETs) [55]. The major problem with the SET technology us it suffers from the background charge problem [56].

Quantum Dot Gate Field Effect Transistor have the kind of similar structure as Single electron transistor and works on the same operating principle as SETs. Unlike SET it does not suffer from the background charge problem. Moreover, it can be designed in the same way as the CMOS, reducing the design complexity to design ternary logic [56].

CHAPTER 5

GRAPHENE NANORIBBON BASED TUNNEL FIELD EFFECT TRANSISTOR

5.1 Introduction

It has been more than half a century since Moore's law, the idea that the number of transistors that can be placed on an integrated circuit doubles approximately every 18 months, was postulated, but only recently did it begin to slow down. As we continue to reduce the size of the MOSFET we face many challenges. 1)The threshold voltage required to switch the states (between ON and OFF states) and 2) the increasing leakage currents (I_{off}) that degrades the I_{on}/I_{off} ratio. To lower the threshold voltage, the sharpness of the switching must increase. This sharpness is inversely proportional to the subthreshold swing (the amount of the voltage necessary to increase the current by a factor of 10). In a MOSFET, switching requires a fundamental minimum subthreshold swing of 60 mV/decade at room temperature due to the diffusion current of the device in weak inversion state. As the energy barrier of the device gate decreases, the leakage current increases exponentially. A current voltage curve of the MOSFET is illustrated in Fig.32.

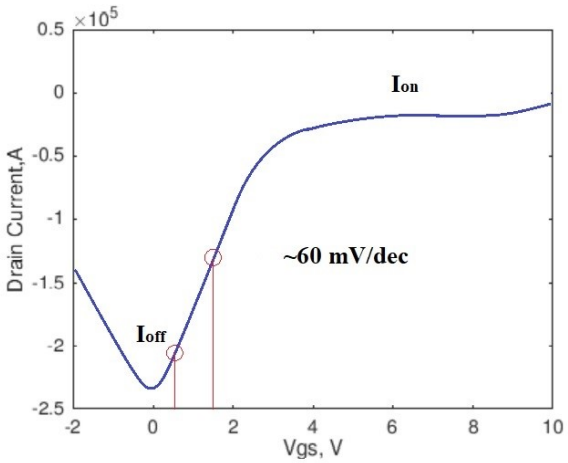


Figure 32: Current (I) –Voltage (V) curve for a typical MOSFET [75]

The device is on when the current is relatively high compared to off. The subthreshold swing is calculated using the voltage difference between 10-7 A and 10-6 A, which is about where the steepest slope is [70-74].

The expression for the dynamic power loss is explained as shown in equation

$$CV_d^2 f + V_d I_{off} \quad (43)$$

where V_d is the amount of voltage required to switch the device on (related to V_{gs}), C is the switch capacitance, f is the operation frequency, and I_{off} is the leakage/off current. This equation explains why it has not been possible to increase clock speed *f* (typically around 2 GHz) due to its proportionality to power. Further increase would cause too much power to be dissipated as heat. V_d is limited by the subthreshold swing and if it can scale down, f and CPU's clock speed can be amplified accordingly without generating more heat.

To bypass the 60 mV/decade subthreshold swing limit, several techniques have been investigated out of them TFET is one of the promising techniques.

5.2 TFET device structure and operation

The tunnel field-effect transistor (TFET) belongs to the family of so-called steep-slope devices that are currently being investigated for ultra-low-power electronic applications.

The fundamental challenge for realizing commercially competitive TFETs is a limited on-current level, which is typically addressed by creating higher doping levels and abrupt doping profiles. [75] Fig.33 shows a schematic of an n-channel TFET architecture

which incorporates a highly doped p+ source region, a near intrinsic channel region and n+ drain region.

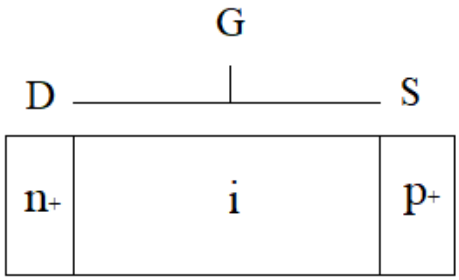


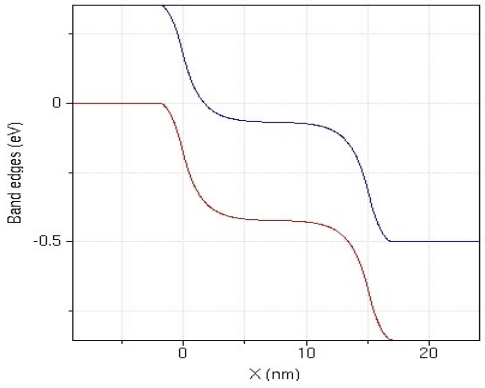
Figure: 33 A schematic of an n-channel TFET architecture [75]

Operation of TFET

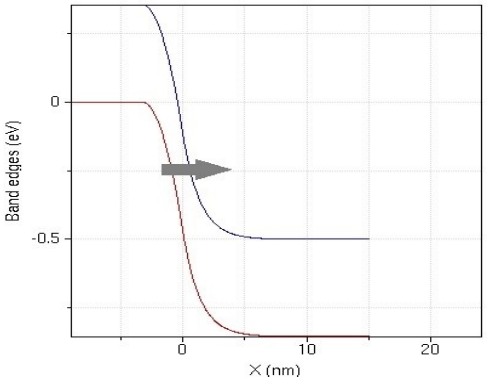
TFET is simply a gated p-i-n diode, which is operating under reverse bias condition. In a MOSFET the source of carrier injection mechanism is thermal injection but a TFET utilizes band-to-band tunneling as a source carrier injection mechanism Fig.34 shows the band diagrams of the n-channel TFET in the OFF and ON states. In the OFF state, there is a wide potential barrier between the source and the channel, as a result no tunneling is occurring.

Only a very small leakage current exists. But when the gate voltage exceeds the threshold voltage, the potential barrier between the channel and the source becomes narrow enough to allow a significant tunneling current, which is called ON state. FET is an ambipolar device, it will show p-type behavior with dominant hole conduction and n-type behavior with dominant electron conduction. But this ambipolarity can be suppressed by designing an asymmetry in the doping level or profile, or by restricting the movement of one type of charge carrier using Heterostructures. In principle, because of the asymmetry TFETs can achieve much higher I_{ON}-I_{OFF} ratio over a given gate voltage swing compared

to the MOSFETs, making the TFET architecture an attractive vehicle to implement low supply voltage (VDD) digital logic circuits.



(a)



(b)

Figure 34 The band diagrams of the n-channel TFET in the (a)OFF and (b) ON states [75]

When a TFET is in its off state (Fig.34 a), the valence band edge of the channel is located below the conduction band edge of the source, so BTBT is suppressed, leading to very small TFET off-state currents that are dictated by the reverse-biased p-i-n diode. Applying a negative gate voltage pulls the energy bands up.

A conductive channel opens as soon as the channel valence band has been lifted above the source conduction band because carriers can now tunnel into empty states of the

channel. Because only carriers in the energy window ΔΦ can tunnel into the channel, the energy distribution of carriers from the source is limited; the high-energy part of the source Fermi distribution is effectively cut off, as shown in Fig.33. Thus, the electronic system is effectively 'cooled down', acting as a conventional MOSFET at a lower temperature. This filtering function is the reason why we can achieve an S of below 60mV per decade. However, the channel valence band can be lifted by a small change in gate voltage, and the tunneling width can effectively be reduced by the gate voltage. S in a TFET is not constant, as a consequence of the BTBT mechanism, but it depends on the applied gate-source bias, as indicated in Fig. 35, increasing with the gate-to-source bias. In a TFET S remains below 60 mV per decade over several orders of magnitude of drain current and that's why you have a better voltage scaling of a TFET than a MOSFET. One challenge in TFETs is to realize high on currents because ION critically depends on the transmission probability, TWKB, of the inter band tunneling barrier. This barrier can be approximated by a triangular potential, as indicated by the grey shading in Fig.33, so "T" can be calculated using the Wentzel-Kramer's-Brillouin (WKB) approximation as given in equation:

$$T_{WKB} = exp\frac{4\lambda\sqrt{2m * E_g^3}}{3q\hbar(E_q + \Delta\phi)} \qquad 44$$

Where m* is the effective mass and Eg is the bandgap. Here, λ is the screening tunneling length and describes the spatial extent of the transition region at the source-channel interface; it depends on the specific device geometry. In a TFET, at constant drain voltage, VD, the VG increase reduces λ and increases the energetic difference between the conduction band in the source and the valence band in the channel (ΔΦ),

TFETs represent the most promising steep-slope switch candidate, having the potential to use a supply voltage significantly below 0.5 V and thereby offering significant power dissipation savings. Because of their low off currents, they are ideally suited for low-power and low-standby-power logic applications operating at moderate frequencies. Other promising applications of TFETs include ultralow-power specialized analog integrated circuits with improved temperature stability and low-power SRAM.

The biggest challenge is to achieve high performance (high ION) without degrading IOFF, combined with an S of less than 60 mV per decade over more than four decades of drain current. This requires the additive combination of the many technology boosters which are available or under research [75].

5.3 Graphene Nano Ribbon

TFET can achieve subthreshold swing below 60mv/decade. But there are many tradeoffs present in this device while achieving the steep subthreshold swing. To overcome this trade off research in the materials used in the manufacturing of the TFETs is going on. To enhance the ON-state tunneling current, narrower bandgap materials with smaller effective masses are being considered. The structure of GNR is shown in the Fig.35

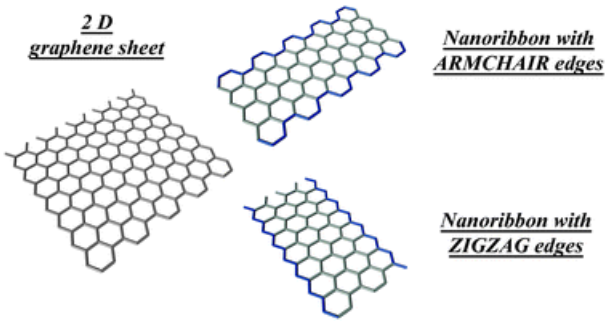


Figure 35 Structure of GNR with different edges.

Properties of GNR

It exhibits ambipolar carrier conduction, a carrier mobility as high as ~2×106 cm2/V--sec, and a defect density of ~1×1010/cm2. This mobility is better than the mobility reported for small gap InSb his mobility is also practically independent of temperature, thus opening the possibility of room temperature ballistic transport at the sub-micrometer scale.

Graphene is intrinsically a semi-metal or zero-gap semiconductor. Graphene has a remarkably high electron mobility at room temperature: - The mobilities for holes and electrons are nearly the same. The mobility is nearly independent of temperature between 10 K and 100 K. The resistivity of the graphene sheet is measured to be 10−6 Ωcm. This is less than the resistivity of silver, the lowest resistivity substance known at room temperature. [71]

Graphene appears to be one of the strongest materials ever tested. Graphene has a breaking strength over 100 times greater than a hypothetical steel film of the same (incredibly thin) thickness. The tensile modulus (stiffness) of graphene is 1 TPa (150,000,000 psi) Graphene is very light, weighing only about 0.77 milligrams per square meter [71]. The energy band diagram and the density of states of the GNR for Armchair ribbons and zigzag ribbons are shown as below.

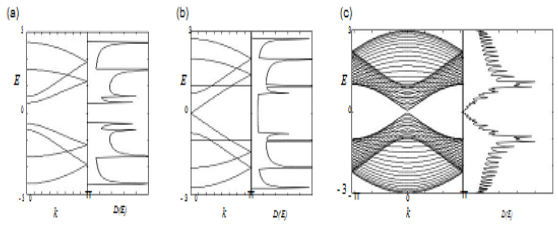


Figure 36 Energy band structure E(k) and density of states D(E) of armchair ribbons of various widths [(a) N = 4, (b) 5 and (c)30[71]

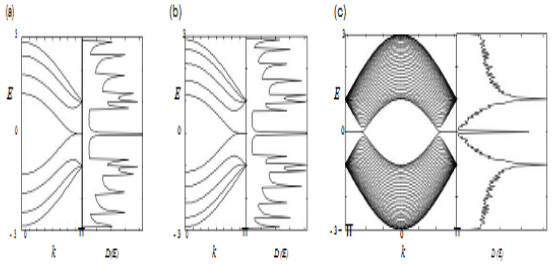


Figure. 37 Energy band structure E(k) and density of states D(E) of zigzag ribbons of various widths (a) N = 4, (b) 5 and (c) 30. [71]

For the semiconducting ribbons, the direct gap decreases with increasing ribbon width and tends to zero in the limit of very large N [71]

Optimization Parameters of GNR.

The GNR TFET are basically simulated using the Vgs = +/- 0.2V, Fermi level = 0.07, Chirality = 3, Tilt angle = 0, energy grid points=400, length =40nm, width=5nm, Vd=0.1V, and doping = 0.24 eV. From the simulation results, Subthreshold swing was extracted as 6.4 mV/decade and an Ion to Ioff ratio of more than ~25,000 were obtained for given parameters as compared to the typical MOSFET has ~70mV/decade subthreshold swing and ~1000 I_{on} and I_{off} ratio. The result of the subthreshold swing and Ion and Ioff ratio can be varied by varying several parameters [74]. Varying channel length

As length of the device increases Ioff decreases and hence ion/ioff increases but the subthreshold swing decreases significantly up to the length of 40nm. The best subthreshold swing of 6mv/decade and an Ion /Ioff was more than 50,000. [74]

A. Varying channel width

As the width increases, the bandgap decreases, yielding a large increase in Ioff and small increase in Ion and increase in subthreshold swing. If Ion is too small, it cannot be

used to drive another transistor: widths of 1.25 nm and 2.5 nm are not practical. Ion for a width of 1.25 nm or below is too noisy. Hence, Ion/Ioff ratio of width below 3.75nm would be inaccurate. Above width of about 3.75 nm, Ion to Ioff ratio is exponential correlated with width. This is due to exponential correlation of off leakage current to width. Subthreshold swing is also affected similarly. [74]

B. Varying contact doping

As the doping profile increase, Ion/Ioff ratio increases initially and then decreases because of passing of the valence band of the drain and the conduction band of the channel between doping of 0.28eV and 0.32 eV. Subthreshold swing remains about the same until 0.28 eV and then degrades above that doping. [74]

C. Varying drain bias

As the drain bias (Vd) increases, Ion also increases. The trade-off is that Ioff increases faster. Hence the Ion to Ioff ratio reduces as Vd increases. Subthreshold swing fluctuates and increases. A minimum drain bias is required to maintain a high Ion. [74]

5.4 Proposed Device Structure

In the proposed device structure, we have used the double-gated ultra-thin body (UTB) TFET model is used as shown in the Fig.38 GNR is used as the channel. Where the channel length is 15 nm, channel thickness is 1.2nm, oxide thickness on both the side is 1nm, VDD is given as 1V with the source and drain doping as 1e20. As for as the material parameters of the GNR is considered we have used.

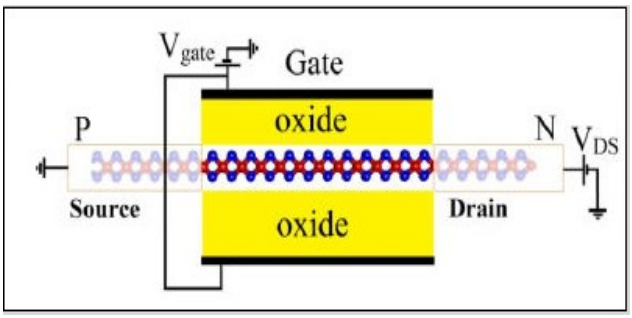
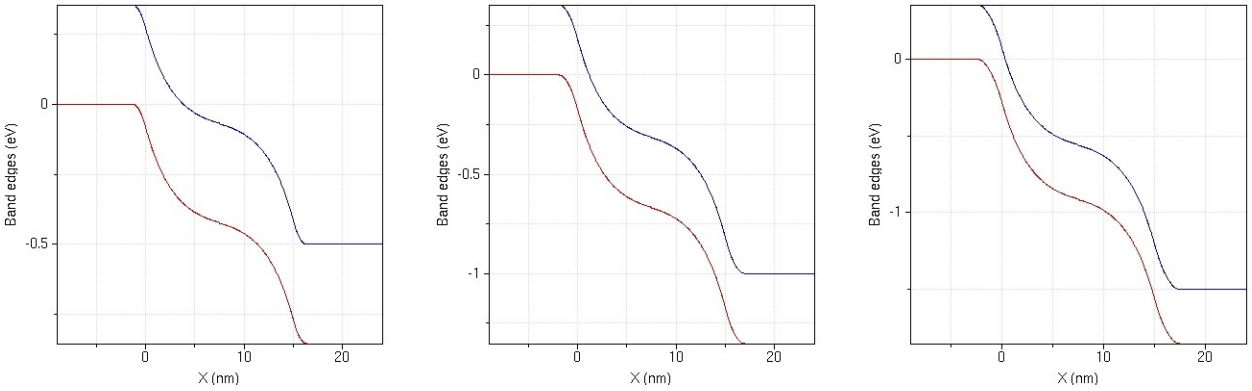


Figure. 38 Proposed device structures

5.5 Result and analysis

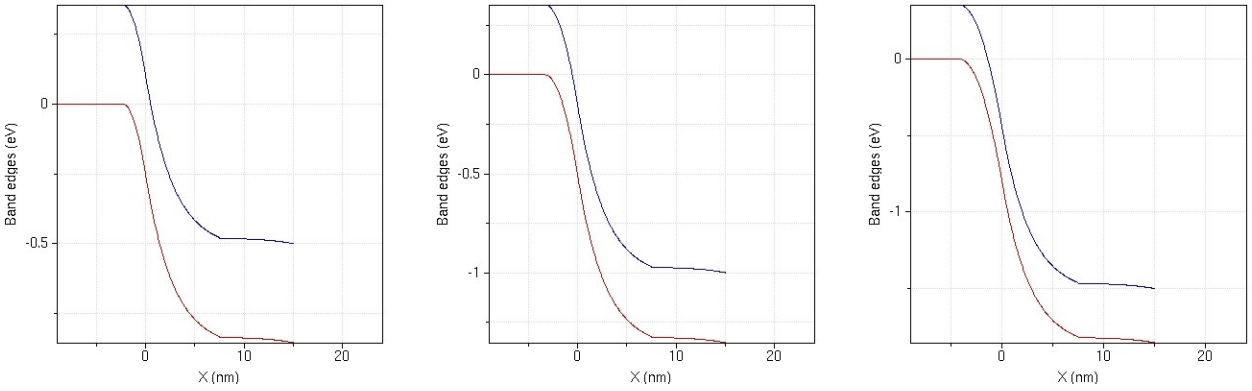
Fig.39 shows the comparison for the Ec-Ev off characteristics for the InAs as the channel material as we can see, as the voltage increases the bandgap between conduction and valence band decreases which results in better tunneling effect now in order to obtain the better tunneling effect we have compared the results for the voltage 0.5,1and 1.5V for both InAs and GNR as a channel material. Now if we compare the result of the Fig39 with the fig 43 it is shown that at the applied voltage GNR gives much less band gap as compared to InAs.

As we can see from the below-mentioned graph GNR shows much sharper curve in comparison of InAs for the corresponding Voltage. Which proves the at GNR gives way more efficient results as a channel material as compared to the standard InAs.



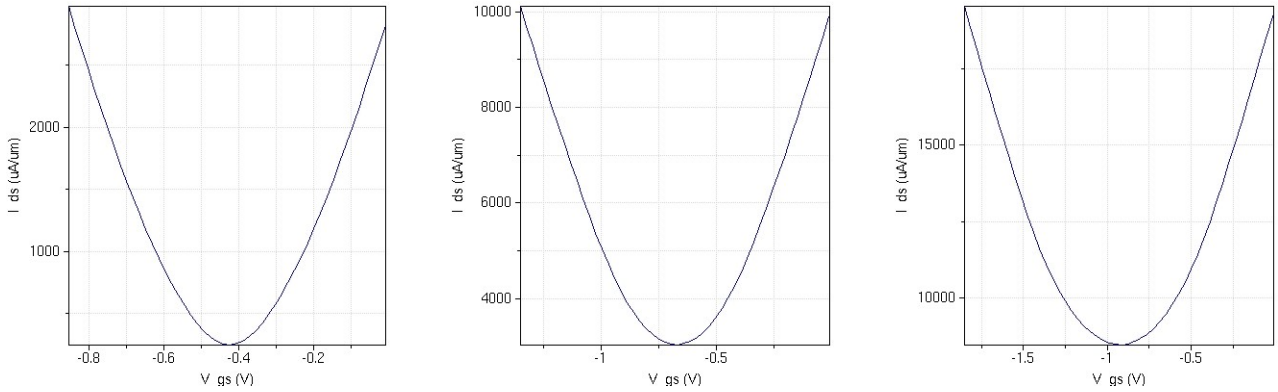
(a) (b) (c)

Figure. 39 Ec-Ev off for (a)VDD=0.5, (b) VDD=1.0, (c) VDD=1.5



(a) (b) (c)

Figure. 40 Ec-Ev on for (a)VDD=0.5, (b) VDD=1.0, (c) VDD=1.5



(a) (b) (c)

Figure. 41 Id-Vg on for (a)VDD=0.5, (b) VDD=1.0, (c) VDD=1.5

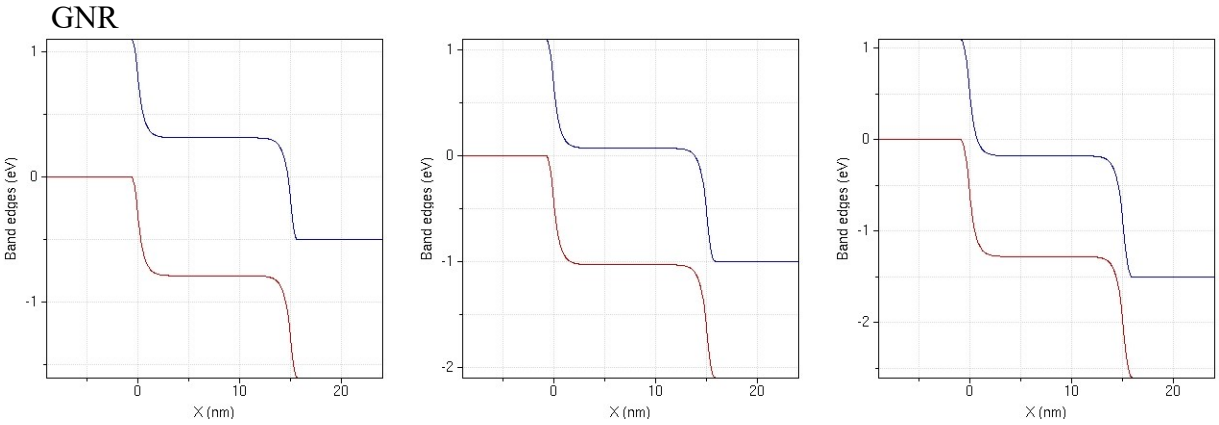


Figure. 41 Ec-Ev off for (a)VDD=0.5, (b) VDD=1.0, (c) VDD=1.5

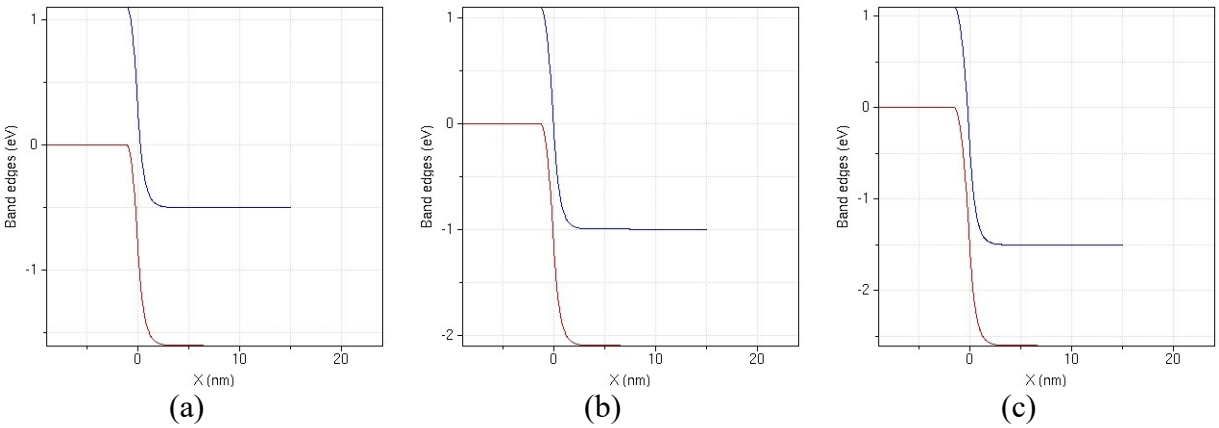


Figure. 43 Ec-Ev on for (a)VDD=0.5, (b) VDD=1.0, (c) VDD=1.5

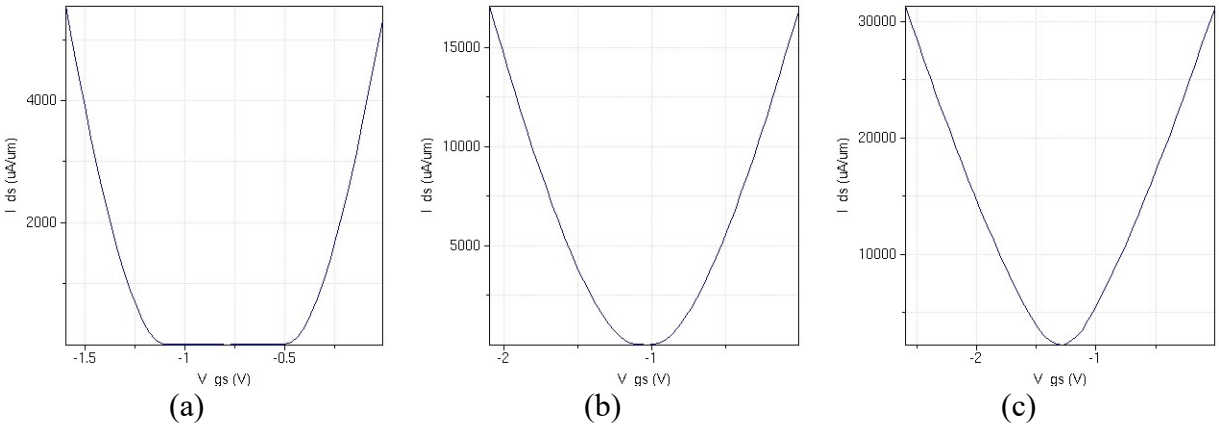


Figure. 42 Id-Vg for (a)VDD=0.5, (b) VDD=1.0, (c) VDD=1.5

Comparative analysis

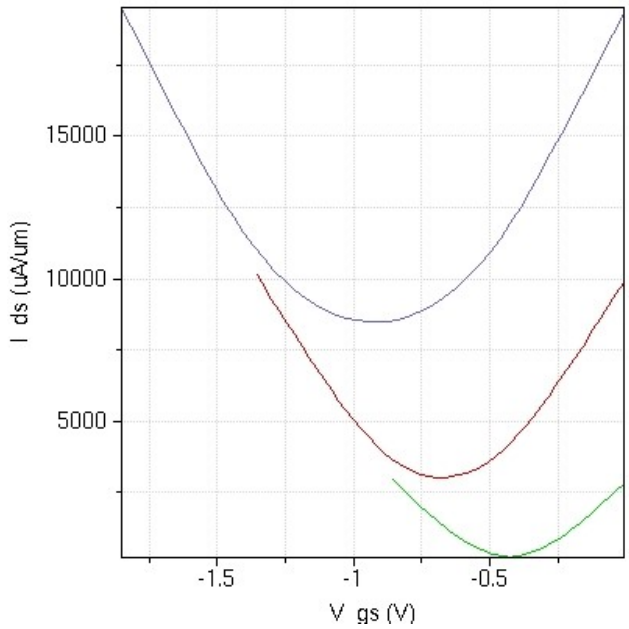


Figure. 45 Comparative analysis of Id-Vg characteristics InAs

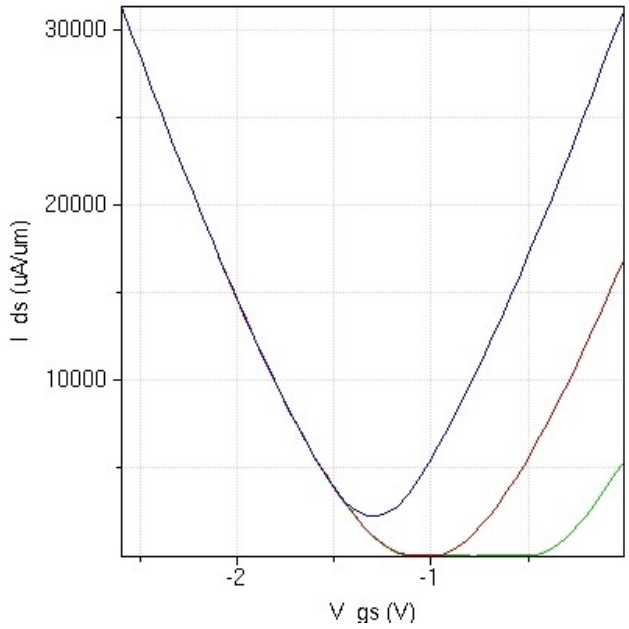


Figure. 46 Comparative analysis of Id-Vg characteristics GNR

CHAPTER 6

CONCLUSION AND FUTURE WORK

Increasing dependence of the modern human civilization on artificial intelligence, IoT and machine learning applications supported by a highly interactive cloud-based infrastructure will push data processing and handling requirements to an unprecedented level. Multi-valued-logic and memory devices are going to be the future of the computing machines to support the extreme scale information density and data handling capabilities. This paper presents a new conceptual design of graphene nanoribbon (GNR) based ternary device, which takes advantage of the percolation driven Metal-Insulator-Transition (MIT) phenomenon exhibited by GNR and some other 2D nanomaterials like MoS2. The design utilizes the memcapacitance obtained from a vertical structure of a dielectric layer and an MIT material layer placed between a pair of metal conductors as illustrated above. Here, we have just presented the basic concept and a summary of the underlying physics of the proposed device illustrated above s. To the best of our knowledge, this is the first GNR based ternary device proposal that utilizes the memcapacitance exhibited by the GNR with MIT behavior. The investigation revealed that by controlling the hysteresis properties of GNR, it is possible to achieve the memcapacitance behavior. Hysteresis in graphene can be controlled by different environmental and external stimuli like vacuum annealing, intrinsic doping, and dipolar adsorbates. Our future work will present the detail validations of this theoretical design.

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