Minimizing The Risk Qualification Test Wafers Have On The Manufacturing Readiness Of A New Microprocessor Fabrication Site Through Data Driven Processes

By

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B.S. Biomedical Engineering, Rensselaer Polytechnic Institute 1995

Submitted to the Sloan School of Management and the Department of Mechanical Engineering in partial fulfillment of the Requirements for the degrees of

Master of Science in Management
And
Master of Science in Mechanical Engineering

In conjunction with the Leaders for Manufacturing program at the
Massachusetts Institute of Technology

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Abstract:

Intel continues to aggressively ramp up new fabrication sites to ensure that the supply of its new process technology can meet the demand. Test wafer readiness for the qualification of the ramping equipment at these new fabrication sites has consistently been at high risk. The primary test wafer risk is ensuring that the right test wafers are available when the tools are ready for qualifications.

This project looks to identify opportunities that will minimize the risk in the test wafer readiness process. Once these opportunities are identified, recommendations are made to minimize this risk for future fabrication sites.

Specifically three opportunities were identified to minimize the risk: a tracking tool to monitor the test wafer, a capacity allocation tool and a build ahead hedging policy. The tracking tool will reduce the risk by capturing data that can provide performance against the plan metrics. The capacity allocation tool identifies which fabrication site is in the best position to build the test wafers. The build ahead hedging policy identifies the test wafer build ahead quantity that will maximize Intel's profits.

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Chapter 1.0: Introduction

1.1: Problem Statement

The goal of this project is to minimize the risk that the test wafer readiness process has on the manufacturing readiness of a ramping fab.

As Intel continues to aggressively ramp up new fabrication sites (fabs), it strives to reduce the time needed to obtain manufacturing readiness and to improve its speed to market. With a shorter ramp time, Intel is more flexible and can more accurately meet the market demand. Compressing the time line can require new thinking and processes. From lessons learned in past ramps, there are some tasks that are currently at high risk of failure. As the project time line is compressed, these tasks will present an even higher risk to the manufacturing readiness of a new fab.

Test wafer (TW) readiness for the qualification of the ramping equipment has consistently been high risk for manufacturing readiness. The primary TW risk is ensuring that the right TWs are available on time. This requires a robust TW process that integrates forecasting, allocating, tracking, receiving, and distributing the qualification TWs.

1.2: Fab 17 Background

Intel designates each of its fabrication sites (Fab) with a number. The site number in Hudson, Massachusetts is Fab 17. Intel acquired Fab 17 in May of 1998 when it bought out Digital Corporation's fabrication sites and its processing technology. Intel has continued to operate the Hudson site manufacturing Digital's processing technology. In mid 1999, Intel prepared a plan to manufacture its own microprocessor technology at Fab 17. During the internship period, Fab 17 was ramping up Intel's P858 microprocessor technology and finalizing preparations for production readiness.

1.3: The Semiconductor Manufacturing Process

A microprocessor is an integrated circuit. The microprocessor is built on and in the surface of a silicon wafer. The four primary stages to semiconductor manufacturing are material preparation, crystal growth and wafer preparation, wafer fabrication, and packaging (Van Zant, 1997). During the material preparation stage, the semiconductor raw materials are obtained and purified. In the second stage, a crystal structure is grown from the raw material and formed into a silicon wafer. In the wafer fabrication stage, the integrated circuits are built on and in surface of the wafer. Some fabrication processes can build several thousand identical integrated circuits on one wafer (Van Zant, 1997). Finally the integrated circuits are tested and cut up into individual microprocessors in the packaging stage.

At Intel, the wafer fabrication stage is performed at dedicated sites. Intel obtains bare silicon wafers from its vendors, processes the wafers at the fab, and sends the wafers to a

different location for packaging. Fab 17 in Hudson was responsible for the wafer fabrication stage of Intel's P858 microprocessor technology.

There are four generic operations to the wafer fabrication stage, layering, patterning, doping, and heat treatment (Van Zant, 1997). Layering adds insulating, semiconductive, or conductive material to the wafer surface. Patterning removes selected portions of the layers. Layering adds the material to the wafer and then patterning removes selected portions. Doping adds dopants to layers. These dopants allow the microprocessor to perform the transistor operations of the integrated circuit. The heat treatment operations heat and cool the wafer to achieve the desired material property results. The four operations are sequenced and performed several times to create the microprocessor.

1.4 Ramping a New Fab

Ramping a new fab that will perform the wafer fabrication stage is a very expensive and complicated process. Fabs can cost billions of dollars to make operational. The site for the fab must be cleared and prepared for a building. A building is put up and the support facilities are installed. The clean room where the process is performed has to be certified. Particulates can destroy the functionality of a microprocessors; therefore, the fabrication process is performed in a clean room that limits the particulate count.

The equipment used in the wafer fabrication operations needs to be installed. Equipment that performs similar operations are typically co-located and are called tool sets. Each piece of equipment is defined as a particular tool. To install the tools a general safety test

is performed. During the safety test, the tool is turned on and checked to make sure that there are no malfunctions that could injure a person. After the safety test, the tool is tested for functionality. Many of the tools use test wafers for functionality checks.

Finally after all of the tools are individually tested, a validation run is performed. During the validation run, wafers are fabricated. The wafers are tested and the yield of functional microprocessors on each wafer is measured.

1.5: Test Wafers

Test Wafers (TWs) are used for two different purposes; qualification of a new tool and sustaining a tool. Qualification TWs are needed to verify and validate that the tool is capable of performing to manufacturing specifications. Sustaining TWs are used for preventive maintenance tasks and to ensure that a tool that is building production product continues to operate within the manufacturing specifications. This thesis focuses on qualification TWs.

Intel segregates TWs into two main categories; bare silicon and preprocessed. Bare silicon TWs come directly from Intel's vendors and do not require any additional processing. Preprocessed TWs require some amount of processing on Intel's equipment before the TWs are in a usable state. There is a large variation in the complexity of preprocessed TWs. Some tool sets use several different TW types. In order to keep track of the different types of test wafers, Intel designates each unique test wafer with its own specific identification number. This thesis focuses on the readiness of preprocessed TWs.

1.6: Virtual Factory Structure

At Intel, several fabrication sites make microprocessors with the same processing technology. Intel's Copy Exactly (CE) policy dictates that the same process technology among the fabrication sites have identical processes. This CE policy makes cross processing of the microprocessors and the sharing of best known practices easier. Cross processing is a method that allows wafers that are partially built at one site to be processed at a different site. Since the processes at each site are identical, process variation is minimized. Intel has defined this cross processing ability of its fabrication sites as the virtual factory (VF). Every fabrication site that produces a particular microprocessor technology is part of a single VF. Wafer processing can start at one of the VF fabs and completed at differ VF fab. This cross processing capability of the VF creates a more flexible manufacturing process that allows Intel to improve its equipment utilization and wafer throughput. The VF concept is symbolic of the fact that the microprocessors for a given process can be manufactured at any of the sites that are within the VF.

1.6.1: Joint Engineering Team Overview

The organizational structure of each work unit throughout the sites has the essence of the CE policy. Intel has Joint X Teams (JXTs) that are responsible for various functional activities. The JXT report to Joint X Mangers (JXM). The JXM are represented throughout the VF.

There are two main types of JXT, the joint engineering team and the joint operational team. The difference between the engineering teams and the operational teams is the scope of work. An operational team is more task oriented, whereas the engineering teams are responsible for more complicated problem solving activities.

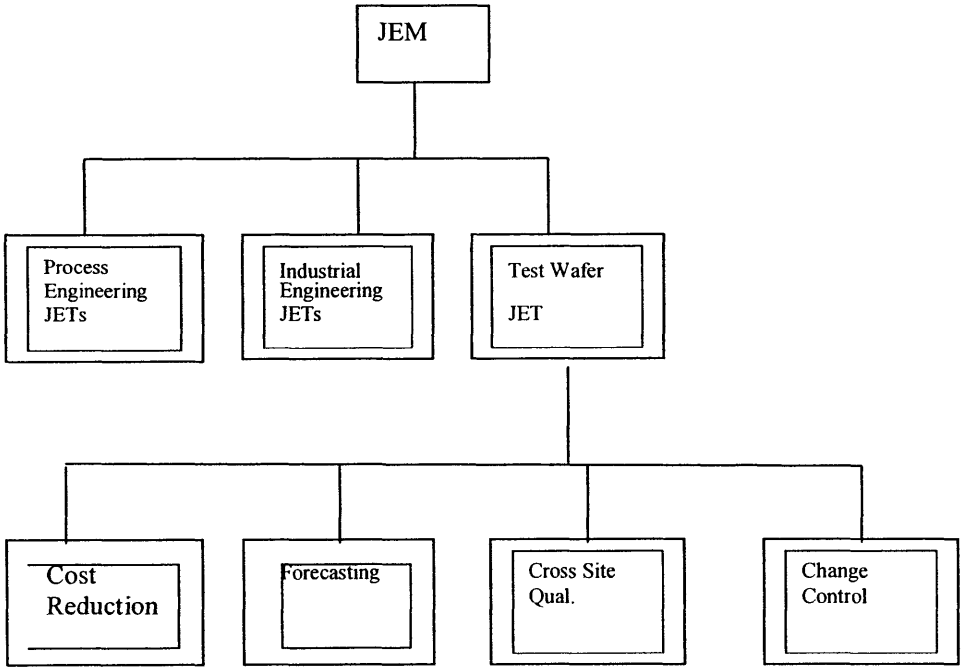
There are several types of JETs; industrial engineering, process engineering, yield, test wafer, etc. There are also subgroups within each functional JET. For example, the process engineering team breaks the JET teams into tool types. The lithography process JET is responsible for working on the lithography tools. The lithography JET has representatives from each fabrication site that is part of the VF.

1.6.2: Test Wafer JET

The purpose of the TW JET is to address VF issues dealing with test wafers. There are several responsibilities of the TW JET. Sub-teams drive these responsibilities. The forecasting sub-team monitors the test wafer usage at each site and develops forecasts of the test wafer usage. The cost reduction sub-team works on cost reduction projects related to test wafer usage and inventory policies. The change control sub-team is responsible for ensuring that the test wafer processing complies with the documented process. When there are changes to the process, the TW change control sub-team is part of the approval process and the local TW members are responsible for implementing the changes. The TW JET organizational design is depicted in figure 1.

The TW JET primarily focuses on the sustaining process. The qualification process is less integrated into the TW JET's systems. As the speed to production becomes more important and multiple factories are coordinating the processing of qualification TW, the TW JET focus on qualification test needs to increase. Within the last year, a cross-site qualification sub-team (CQT) was formed to address processing of qualification TW.

Figure 1: Test Wafer JET Organizational Design.



The skills and background of the members of local test wafer teams differ from site to site. Some sites' members have more of an operational and logistics background while others have engineering backgrounds. Some of the more established sites have had members working on test wafers for more than 4 years. However, these tenure individuals are rare and the majority of test wafer members have had less than one and a half years of experience working in the TW JET.

1.7: Fab 17 Organizational Structure

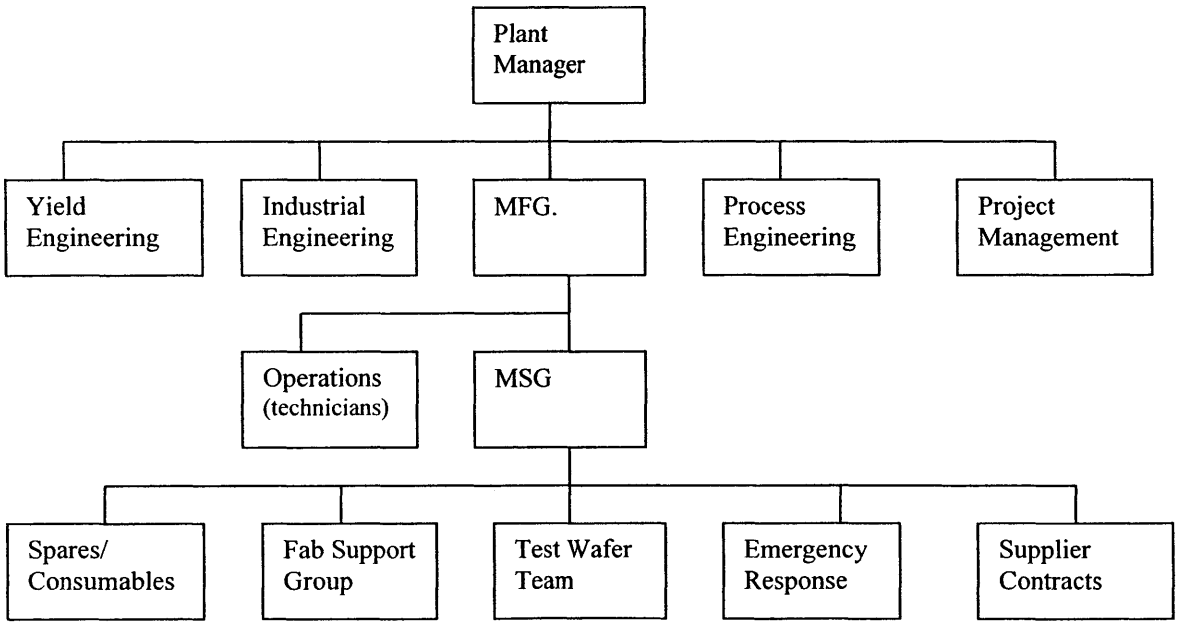
The FAB 17 manufacturing support group (MSG) manager was responsible for the local test wafer team. The MSG manager had a vision for the ideal structure of a test wafer team. It would include at a minimum a logistic expert, an industrial engineer, and a chemical engineer. One of the main functions of the test wafer team is to coordinate the test wafer inventory levels and ensure that the test wafers were sent to the right tool stations on time. A person skilled in logistics can manage the inventory and the test wafer orders. A responsibility of the test wafer team that is well suited to an industrial engineer is to build systems that can monitor the test wafer usage, and to look for cost reduction opportunities. Finally, a chemical engineer's background is well suited for understanding the composition of the test wafers. There is a lot of chemistry that goes into making the test wafer and it is important to understand how this chemistry impacts the performance of the test wafer.

The organizational chart for FAB 17 is located in figure 2. Figure 2 details only a part of the organizational chart, placing emphasis on those groups that impact the test wafer team and those groups that impact the operations of the fab. The plant manager oversees the entire organization. There are five main functional areas: industrial engineering, process engineering, yield engineering, project management, and manufacturing. The industrial engineering group is responsible for the factory layout and ensuring that proper quantity of tools are ordered to meet output requirements. The process engineers are divided up into tool types and process steps. The process engineers ensure that the process is

capable of making a high quality product. The yield engineering group is responsible for the quality of the wafers. The yield engineers track the batch performances and perform root cause analysis on lots with low yields. The project management group focuses on implementation of new process technology.

The manufacturing group is responsible for operating the machines and coordinating the manufacturing support functions. Specifically there are five manufacturing support functions. The spares and consumables group ensures that all of the spare parts and items that are used in production are available when needed. The fab support group assists in miscellaneous logistic functions. The emergency response team tracks and resolves reportable incidences. The supplier contract groups works with the suppliers on the equipment and vendor support personnel contracts. The test wafer team is responsible for the management of the test wafer needs.

Figure 2: FAB 17 Organizational Chart



1.8: Scope and Objectives

This thesis focuses on developing data driven methods that will enable the TW JET to minimize the risk that the TW readiness process imposes on the manufacturing readiness. While a cross-functional analysis helped identify what methods would be the most useful to the TW JET, there was little consideration of developing methods that required changes to these cross-functional boundaries. By itself, the TW JET has a relatively large number of constituents, which makes it difficult to effect change. It was felt that attempting to pull in more cross-functional stakeholders into the change process would diminish the chance to realize improvements. The methods that are developed in this thesis are intended to help the TW JET with their internal decision making process. The TW JET should then be in a better position to effect changes that require cross-functional participation. The first step in improving the test wafer readiness process is to get the TW JET's internal processes in order. The second step is to work cross-functionally to optimize the readiness process. This thesis focuses on step one.

The local TW team and the TW JET are the key stakeholders responsible for the TW readiness. By incorporating data driven processes into the TW readiness process, the local TW team and the TW JET are able to make more informed decisions. Three specific opportunities were identified that could improve the TW JET's internal processes. These opportunities were an improved tracking system, an allocation tool, and a buffer inventory policy – a TW build ahead policy. An improved tracking system for the qualification TWs will reduce the risk by capturing data that can provide performance against the plan metrics. These metrics can provide insight on tools that may require

additional TW quantities for future tool qualifications. An allocation tool that identifies which supply fab is in the best position from a capacity perspective to build the qualification TWs will minimize the risk. A supply fab with more capacity is less likely to have delays in processing the TWs. A buffer strategy minimizes the risk by ensuring that additional TWs are already processed and available for times when tools have excursions from the forecasted quantities.

This thesis develops the allocation tool and the buffer inventory policy in detail. The improved tracking system was not a primary focus for this thesis. Other people in the TW JET were focusing on the improved tracking system. The current tracking system and some opportunities for improvement are discussed in appendix 1.

While Intel is in general a data rich culture, there is little data on the test wafer readiness process that is useful for making informed decisions. The allocation tool and the buffer inventory policy provide the TW JET with methodologies and tools that will help them make informed decisions. However, it is difficult to quantify the improvement value because of the long lead-time between site qualifications. Some projected savings are calculated based on the implementation of these information systems.

1.9: Chapter Summary

The remaining chapters of the thesis address the problem statement. Chapter 2 describes the current test wafer readiness process. Specifically, the current forecast preparation, and the allocation and build process are reviewed in chapter 2. In chapter 3, the

methodologies used to develop the tools and policies are presented. The methods for applying these tools and policies are also illustrated in chapter 3. In chapter 4, the build ahead policy is applied to a data set of forecasted test wafer requests and the results are analyzed. Several "what if" scenarios are considered in chapter 4. The effects of a generalized build ahead plan are assessed in chapter 4. Finally, the conclusions and recommendations are presented in chapter 5. Conclusions are drawn about both the allocation tool and the build ahead policy. Recommendations are given and future opportunities are explored in chapter 5.

Chapter 2: Current Qualification Test Wafer Process

2.1 Introduction:

This chapter reviews the current process for coordinating qualification test wafer build requests. There are three components essential for coordinating the request; the forecast preparation, the allocation and build process, and the tracking of the test wafers. This chapter focuses on the forecast preparation and the allocation and build process. The tracking process is described in appendix 1.

During the forecast preparation phase, the ramping test wafer team identifies the quantity of each qualification test wafer route that is needed for each tool set. In the allocation and build phase, the local test wafer team works with a TW JET sub-team to obtain build commitments from the supply fabrication sites for the qualification test wafers. Throughout the entire process, the requests are tracked using a spreadsheet database.

2.2 Forecast Preparation:

Intel has a documentation control policy that describes the qualifying process for each tool needed to ramp a new fabrication site. These documents are called White Papers. Within each tool qualification, the White Paper provides detailed information on the type, quantity and acceptance criteria for each test wafer. A tool may use several different types of test wafers to complete the qualification process. A route number identifies each unique type of test wafer.

Changes to the White Paper require Virtual Factory approval. This Virtual Factory approval not only requires sign off at the ramping site, but can also require all of the other sites that are currently running the process and the development site to sign off on changes. This can make changes to the White Paper tedious and efforts are made at Intel to avoid having to make changes.

The development sites are responsible for creating the initial White Papers. Typically, several development engineers in the lithography department are responsible for developing the White Paper for the lithography tools. Likewise, the other process development engineers create the White Papers for their process areas. In creating these initial White Papers, the development engineers are responsible for identifying the type, quantity and acceptance criteria of the test wafers used to qualify the tools.

In interviews with some of the process development engineers, it became clear that there was no robust process for determining the quantity of test wafers for each test wafer route. Typically, the quantity of test wafers for a given route was based on the development engineer's personal experience in qualifying the tool. There was little consideration for tool variation. Tool variation could create the need for additional wafers when the same tool type is qualified at one of the high volume manufacturing sites.

The only consistent message given by the development engineers that suggests that they consider the effects of tool variation was in rounding lots. For example, if a particular tool required nineteen wafers for a given tool, the development engineers would routinely round the wafer quantity to twenty-five wafers, a full lot of wafers. There was no documentation that justified the lot rounding, nor was it possible for a high volume manufacturing (HVM) engineer to discern the size of the buffer –or if there even was a buffer.

Once an HVM site started preparing for its ramp, a local member of the test wafer team was responsible for preparing a test wafer forecast. In addition to referencing the white paper, the test wafer team member would solicit input from several other stakeholders. If another HVM site had already gone through the ramp, it was possible to obtain some insight from both process engineers and test wafer engineers that already completed the ramp. This insight was often obtained in an informal manner. For example, one of the test wafer engineers at the HVM site that already went through the ramp might recall that for a particular tool, XYZ tool used twice as many ABC wafers during qualification than called for in the White Paper. If the local test wafer engineer felt that it was likely that her XYZ tool could experience the same issue with ABC wafer, then it was left to the discretion of the local test wafer engineer to increase the quantity of ABC wafers.

Another group that influenced the test wafer forecast was the local process engineers. The local process engineers were seen as the customers who needed the test wafers. The local process engineers were the key stakeholders. The local process engineers used the

test wafers to qualify the tool. It was the responsibility of the test wafer team to make sure that the local process engineers received the correct quantity of test wafer on time. Unfortunately, during the forecast and planning stage, test wafers were not a priority for the local process engineers. The local process engineers had other priorities such as learning about how the actual tool performed a particular process.

The standard test wafer forecast would plan to provide test wafer for two tools of each tool set. The first tool was known as the early tool set (ETS). The second tool was a redundant tool and described as the early tool set plus one (ETS+1). The test wafer readiness process generally forecasted test wafer for both the ETS and the ETS+1 tool. However, production readiness typically only needed one qualified tool for each tool set. Since management was driven by the production readiness date, the test wafers for the ETS+1 tool could be considered a buffer for the ETS. If the ETS+1 test wafers were needed for the ETS tool, there was usually enough time to replace the ETS+1 test wafers before they were needed.

Determining the needed date for the test wafers was not a trivial matter. Intel had a master schedule that provided a rough timeframe for when the tools were going to qualify. However, this schedule was constantly being changed. Most of the changes to the schedule were beyond the control of the tool owners who were qualifying the tools. Factors such as electrician availability and actual construction of the clean room space where the tool was going to be located had a major impact of the schedule. These changes made it difficult to establish a firm need date for the test wafers. Furthermore,

constant changes to the schedule made it difficult to determine which tools were on the critical path. Without knowing which tools were on the critical path, it was not possible to determine which tools could cause a delay in production readiness if a tool was not qualified on time. This made it difficult to know which test wafers were the most important.

2.3 Allocation and Build Process:

Once a reasonable draft of the forecast was created, the local test wafer team began requesting VF support with producing the qualification test wafers. The local test wafer team brought the qualification test wafer build requests to one of the TW JET sub-teams, the Cross-site Qualification Team (CQT). Each site from the VF was represented on the CQT.

The CQT met weekly to review any new or outstanding test wafer build requests and to obtain commitments from the supply fabrication sites to build the requests. Each supply fabrication site was in charge of determining whether or not it would commit to build a particular test wafer request. The entire allocation process was informal and there were no metrics that guided the CQT in determining which supply fabrication site was in the best position to build the test wafer requests.

Most of the test wafer requests were not a significant strain on the supply fabrication sites production throughput and these types of request were easily accommodated. It was difficult obtaining commits from the supply fabrication sites for test wafer requests that

strained production throughput. These test wafer requests required processing on constraint or near constraint tools. Intel's production process used the Theory of Constraints to dictate its tool capacity. Constraining the capacity on specific strategic tools allowed Intel to focus on only a small number of tools that could affect throughput (Goldratt, 1992). If a supply fabrication site committed to building these difficult test wafers, it could negatively effect production wafer throughput.

The operations group, responsible for production throughput and in charge of the lot dispatching process that dictates which lot processing order, wanted to minimize any negative affect to production throughput. The operations group's performance was measured on production wafer throughput and producing test wafers did not count towards the production throughput. This meant that there was little incentive for the operations group to agree to any test wafer build that could limit throughput.

Ultimately, the operations group understood that the difficult test wafer builds that required processing on the constraint tools were needed, but the current process created a hold out opportunity. If the operations group could reject the test wafer build request long enough, another fabrication site might eventually agree to build the difficult test wafers. Since there were no metrics that measured which supply fabrication site was in the best position from a capacity perspective to build the difficult test wafer requests, each supply fabrication site would hold out as long as possible.

A typical difficult test wafer request received a commitment in the following manner. The requesting site would introduce the request at the CQT meeting and ask for any volunteers to build the test wafers. Two or three of the supply sites would immediately deny the request, stating that this type of test wafer went through one of their constraint tools that has recently been problematic. There was silence for several seconds, as the other two possible supply sites waited to see if the other site would agree to commit. Eventually, the representative from one of the sites would agree to check with her operations group to determine if a commitment could be made. Normally both sites would agree to check with their operations group and report back at the following CQT meeting. Approximately fifty percent of the time, at the next CQT meeting at least one of the sites was able to get a commitment to build the difficult test wafers. The other fifty-percent of the time, no resolution was obtained. Sometimes the request would be pushed back to the entire CQT to see if any of the sites that originally rejected the request were now capable. Other times, the request was escalated to the TW JET group leaders. The group leaders had more positional authority than the CQT representative. The group leaders could sometimes use this positional authority to convince their operations group to commit to the test wafer request.

Ultimately, commitments were obtained for all test wafer requests. However it could take several weeks of negotiations and meetings. The longer it took to get build commitments for all of the test wafers, the longer the ramping fabrication site's risk assessment for obtaining test wafer remained high. The ramping fabrication site's management team reviewed the risk assessment periodically. The more time test wafers were at a high risk

level, the more pressure the ramping fabrication site's test wafer team felt from the management team. There seemed to be an unwritten rule about how long test wafers could stay at the high risk level before the management team would get involved. When the management team got involved, the performance of TW JET and the operations group was often considered poor. Most people at Intel were over-achievers who had a desire to outperform. The potential of being regarded as poor performers would often overcome the desire to hold out and let another site build the difficult test wafers. Unfortunately, it took time for the threat of being viewed as a poor performer would overcome the desire to hold out.

Chapter 3: Methodology and Application

3.1: Test wafer allocation decision tool:

In chapter 1, it was suggested that a method for improving the allocation process would improve the test wafer readiness process. The purpose for the allocation tool is to provide the cross-site qualification team (CQT) with information on each of the VF sites' constraint tool excess capacity. This information will allow the CQT to make a more informed decision in allocating test wafer requests to VF supply sites.

In this section, an allocation decision tool is developed. First the process for collecting the data is described. A method for comparing site capacity is then generated. Finally, a process for interfacing between the TW JET and the tool is suggested.

The initial goal for developing the allocation tool was to provide the CQT with a tool that would dictate with 100% accuracy, which VF site would build the difficult test wafer requests that are processed on constraint tools. Unfortunately, the tool is not capable of achieving this goal. There are some limitations with the tool and other limitations with the allocation process. The limitations are identified in section 3.1.3 and a method for applying the allocation tool is proposed in 3.1.4.

3.1.1: Data collection:

Intel has a data rich culture. One of Intel's internal databases tracks virtual factory performance on several metrics. The database is capable of pulling up historical data in 13-week increments for each of the performance metrics. The critical performance metrics for this analysis are:

- Tool availability
- Tool utilization
- Number of tool in process
- Processing time

Tool availability is a measure of the percentage of time that the tool is in the up to production status to the total time. Let A be the percentage of time that the tool set is up for production.

Tool utilization is a measure (U) of the percentage of time that the tool set is processing wafers to the total time.

The number of tools (N) measures the quantity of tools that were up to production.

The processing time is a measure of the average time it takes for the tools in the tool set to process one lot of wafers. There are twenty-five wafers in each lot. Let P be the average processing time measured in hours.

The database is capable of filtering the data in the following sub-categories:

- Process technology
- VF site
- Workweek performance
- Performance metric
- Tool type

By filtering the data by these five sub-categories, it is possible to develop insight into the excess tool capacity at each site. Comparing the tool set excess capacity provides data that the CQT can uses to determine which site is in the best position to commit to a test wafer build.

3.1.2: Capacity Methodology

Using the performance metrics from the database, the site's excess capacity for each tool type is calculated. The excess availability is defined as the gap. Excess availability is defined as the difference between the availability and utilization. To convert the

availability and utilization measurements into hours per week, the gap is multiplied by 168 hours. Let G be the gap. Then

$$G = (A-U)*168 \qquad (1)$$

Excess capacity per tool is defined as the gap divided by the processing time. Let C be the excess capacity per tool measured in wafer lots per week. Then

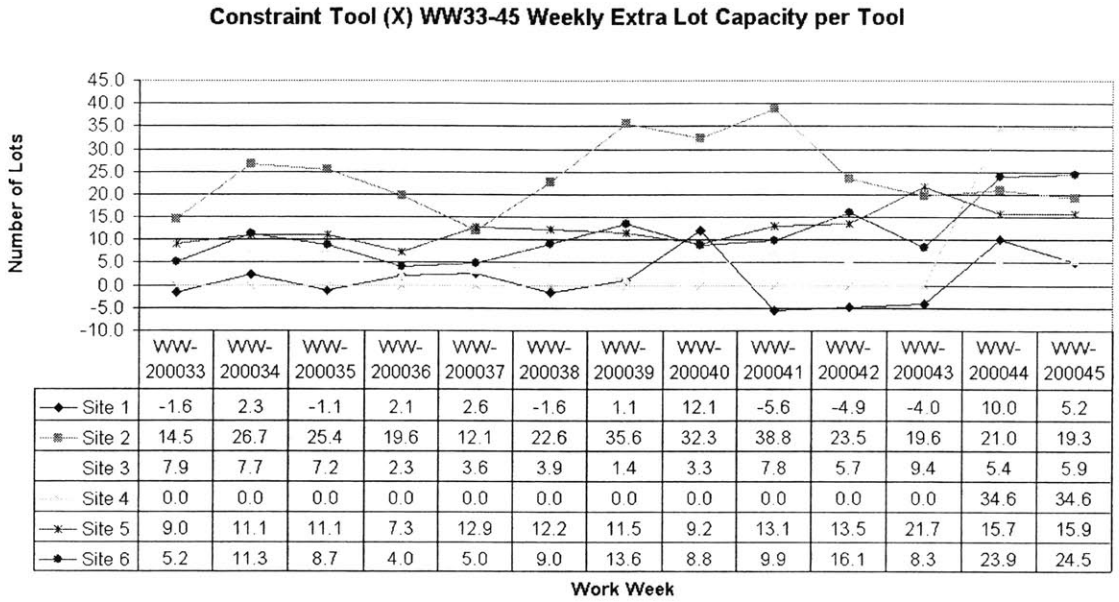
$$C = G/P \qquad (2)$$

The tool set excess capacity is defined as the excess capacity per tool times the number of tools. Let TC be the tool set excess capacity in wafer lots per week. Then

$$TC=C*N \qquad (3)$$

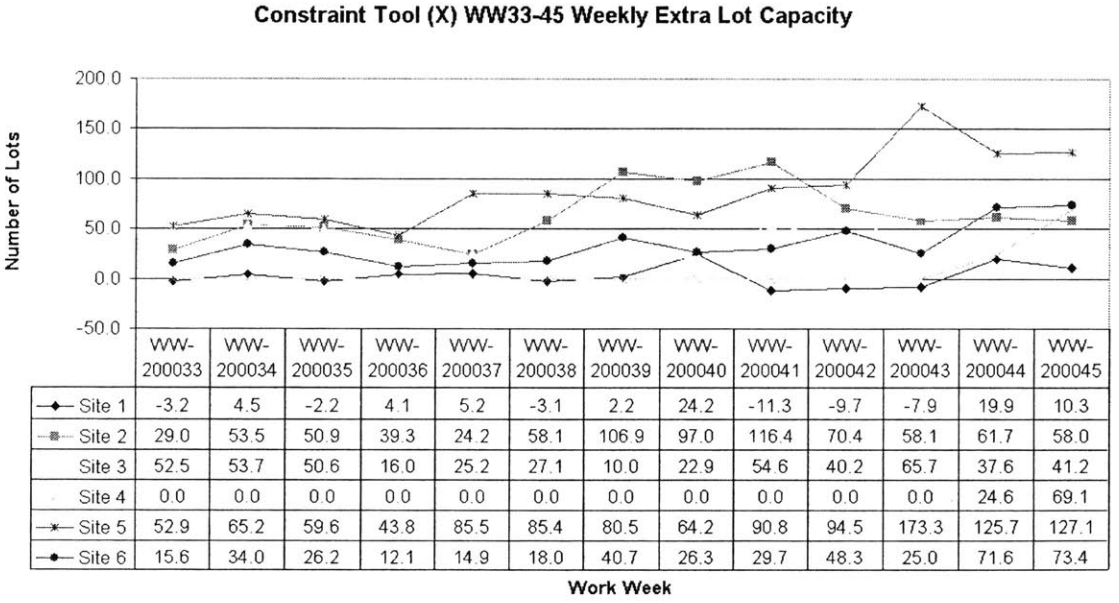
These two excess capacity measurements, C and TC, are calculated for each constraint tool set for each site over a 13-week period. A sample calculation of the excess capacity is located in Appendix 2. Note the data is disguised for proprietary purposes. Figure 3 and 4 are plots of the two excess capacity measurements for each of the six sites for one of the constraint tools (X) over workweeks (WW) thirty-three through forty-five.

Figure 3: Constraint Tool (X) Excess Capacity per Tool



	WW-200033	WW-200034	WW-200035	WW-200036	WW-200037	WW-200038	WW-200039	WW-200040	WW-200041	WW-200042	WW-200043	WW-200044	WW-200045
Site 1	-1.6	2.3	-1.1	2.1	2.6	-1.6	1.1	12.1	-5.6	-4.9	-4.0	10.0	5.2
Site 2	14.5	26.7	25.4	19.6	12.1	22.6	35.6	32.3	38.8	23.5	19.6	21.0	19.3
Site 3	7.9	7.7	7.2	2.3	3.6	3.9	1.4	3.3	7.8	5.7	9.4	5.4	5.9
Site 4	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	34.6	34.6
Site 5	9.0	11.1	11.1	7.3	12.9	12.2	11.5	9.2	13.1	13.5	21.7	15.7	15.9
Site 6	5.2	11.3	8.7	4.0	5.0	9.0	13.6	8.8	9.9	16.1	8.3	23.9	24.5

Figure 4: Constraint Tool (X) Total Excess Capacity



	WW-200033	WW-200034	WW-200035	WW-200036	WW-200037	WW-200038	WW-200039	WW-200040	WW-200041	WW-200042	WW-200043	WW-200044	WW-200045
Site 1	-3.2	4.5	-2.2	4.1	5.2	-3.1	2.2	24.2	-11.3	-9.7	-7.9	19.9	10.3
Site 2	29.0	53.5	50.9	39.3	24.2	58.1	106.9	97.0	116.4	70.4	58.1	61.7	58.0
Site 3	52.5	53.7	50.6	16.0	25.2	27.1	10.0	22.9	54.6	40.2	65.7	37.6	41.2
Site 4	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	24.6	69.1
Site 5	52.9	65.2	59.6	43.8	85.5	85.4	80.5	64.2	90.8	94.5	173.3	125.7	127.1
Site 6	15.6	34.0	26.2	12.1	14.9	18.0	40.7	26.3	29.7	48.3	25.0	71.6	73.4

3.1.3 Allocation tool limitations:

There are two types of tool limitations, accuracy and applicability. Intel's database has some accuracy issues in measuring tool utilization. Tool utilization is actually a calculation based on expected performance and the processing time. Since utilization is a calculation, it is not completely accurate; however, the internal group at Intel that created the database has estimated that the average utilization error is small. A second generation of the database is in development that will measure utilization instead of calculating it. This second-generation database will have a more accurate measurement of the tool utilization.

It is unclear which of the two excess capacity measures is the most appropriate to use for allocating test wafer request to VF sites. Some sites may have a moderate amount of excess capacity per tool, but several tools. These sites typically have a larger amount of excess capacity for the tool set relative to the other sites. For example, one site (A) may only have one tool and another site (B) may have five tools. The tool at site (A) may have an average weekly excess lot capacity of fifty. Site B may only have an average weekly excess lot capacity of twenty-five per tool, but site B's total weekly excess lot capacity is one hundred and twenty-five. In general, the sites with the largest excess capacity for the tool set are most likely in the best position to build the test wafer request.

The allocation tool only identifies each site's excess capacity for the constraint tool set. While this information is useful in establishing the best candidate to allocate the request

to, there are other factors that can influence the allocation decision. Several of these factors are beyond the control of the CQT. With input from the CQT, a list of these factors was generated. Table 1 is the list of these factors.

Table 1: Allocation Decision Factors

Factor	Negative impact on the supply fab's ability to commit
A requested TW is processed on a constraint tool	Yes
Supply fab constraint tool capacity	Yes
Supply fab TW human resource availability	Yes
Supply fab tool operator resources	Yes
VF manufacturing management commitment (Lack of support/supply fab charters for start up/requesting fabs)	Yes
Availability of bare Si	Yes
Business policy decision #1 (Development fab's will not utilize there capacity as much as an HVM site)	Yes
Business policy decision #2 (A copper fab will not build TW for a non-copper fab)	Yes
Having the requested route at the supply fab	Yes

3.1.4: Applying the allocation tool

In order to minimize these limitations, the following process is recommended for allocating requests.

1. Determine an initial VF allocation site by comparing the request to the tool set excess capacity graph. The site with the largest excess capacity agrees to consider the request.

2. If the initial site can not commit to the request, proceed to the site with the next largest excess capacity.
3. Record the incidences when a site can not commit. Use the factors listed in Figure 3 to categorize the incidences.
4. Record the amount of time it takes to get a commitment for each of these difficult test wafer request.
5. Periodically review the frequency of each incident relative to each factor. If a particular category has a high incidence rate, estimate the amount of extra time the allocation process takes because of this factor.
6. Perform a cost benefit analysis that will assess if changes that minimize the effect of this factor on the allocation process are reasonable.

3.2: A build ahead policy

In this section, a build ahead policy for setting the appropriate quantity of test wafers is developed. This build ahead policy is based on a hedging strategy. It is similar to the Newsboy Model and a decision analysis. The necessity for a build ahead policy is summarized. The details of the Newsboy Model and the decision analysis are reviewed. Finally, build ahead policy is developed for this specific application.

3.2.1: A need for a build ahead policy

In chapter 1, a risk opportunity was identified regarding how the decision for determining the amount of test wafer was made. Chapter 2 described the current process for establishing the test wafer forecasted quantities. The test wafer quantity was set through an informal process that was based on an initial estimate made by the development group.

This initial estimate was adjusted when the local test wafer team obtained insights from various HVM groups (VF test wafer team members, VF process engineers, and local process engineers). The frequency and magnitude of adjustment of the test wafer quantities were largely dependent on how well the local test wafer team's network of contacts was established. If the local test wafer team had established good contacts within the VF and the local process engineers, then more of the wisdom for adjusting the test wafer quantities was passed along.

Even if the test wafer team had established a good contact network, the test wafer team typically did not track the actual test wafer usage versus the forecasted quantities. Without this tracking, it was not possible to establish performance metrics. Fortunately, one of the VF test wafer teams that recently ramped a fabrication site did track the actual test wafer usage and the forecasted quantities. This data was used to obtain an estimate of the forecasting accuracy.

3.2.2: The Newsboy Model

The Newsboy model considers a single-period stochastic inventory policy. The objective of a one-period model is to balance the cost of ordering too much with the cost of ordering too little (Nahmias, 1997). A classical application of this one-period model is determining how many newspapers to stock at a newsstand, hence the Newsboy model.

There are three factors that must be calculated in order to optimize the Newsboy model. The demand for the item must be characterized. The cost of ordering too much (cost of

overage) has to be determined and the cost or ordering too little (cost of underage) must also be assessed.

The normal distribution is a popular continuous distribution used to approximate the demand. The advantage of the normal distribution is that it is fully characterized by its mean and standard deviation. Estimates for the mean and standard deviation are calculated from the demand history.

There are several factors that can contribute to the cost of ordering too much of an item. These factors can included the raw material, assembly, transportation, and holding cost. In addition there can be opportunity costs associated with ordering too much of an item. The newsboy illustration can provide a good example of these opportunity costs. Suppose that the tools that are used to manufacture the newspaper could also produce brochures. For this example assume that the brochures have a deterministic demand and that there is not enough capacity to satisfy all demand for both the brochure and newspapers. The lost revenue from the brochures is an opportunity cost that should factor into ordering too many of the newspapers.

The cost of not ordering enough of an item is an opportunity cost. This opportunity cost is the lost revenues. If the newsstand is out of newspapers and one more person wants to buy the paper, then this is lost revenue.

Optimization software is useful in determining the ideal number of newspapers to order to maximize profits. An objective function is established for maximizing the profits that are related to the demand, the cost of overage and the cost of underage. The decision variable is the number of newspapers to order. Constraints can be added to reflect reality.

One specific constraint is the hurdle rate. Companies want to maximize the productivity of their limited capital resources. Even if an investment can provide an expected positive return, the company may not want to allocate capital resources toward this investment. The company may be able to allocate the capital resources towards a better investment. The hurdle rate is the minimum percent return on the capital investment that is acceptable (Brealey and Myers, 2000). If the expected return on an investment is lower than the hurdle rate, then the company should not allocate resources toward the investment.

Assume that the cost of a newspaper is twenty-five cents and that the expected net gain of having one additional newspaper is five cents. This is a twenty- percent net gain over the cost of the additional newspaper. If the hurdle rate is less than or equal to twenty percent, then having the additional newspaper is a good investment. If the hurdle rate is greater than twenty percent, it does not make sense to have the additional newspaper. When the hurdle rate is greater than twenty percent, the twenty-five cents spent to get the newspaper could have been used in a more productive manner.

3.2.3: A Decision Analysis

A decision analysis is a systematic method for structuring and analyzing decisions that have uncertainty (Bertsimas and Freund, 2000). A decision tree is the model that is used to structure the decision analysis. The method presented here for creating and analyzing the decision tree is adapted from the book Data, Models and Decisions, by Bertsimas and Freund.

A decision tree is made up of nodes and branches. A node is like a fork in the road. At each node either a decision is made or an event happens that takes the outcome down a particular road. Each branch that comes from the node represents a possible outcome that could occur. The branches represent all of the roads that could possibly be taken at the node. There are two types of nodes. A decision node represents a choice that has to be made. A box depicts a decision node. An event node represents an uncertain event and is depicted by a circle.

A branch that does not lead to another node is called a final node. Associated with each final node is a monetary value. By summing the weighted averages of each branch that goes out of a node, the expected monetary value (EMV) for the node is calculated. The EMV of an uncertain event is the weighted average of all possible numerical outcomes, with the probabilities of each of the possible outcomes used as the weights (Bertsimas and Freund, 2000). The EMV of a decision node is the maximum of the EMV's for all of its branches. Starting at the end nodes and working backwards, an EMV is calculated for each node.

3.2.4: Applying the models to the build ahead policy,

The purpose of modeling the build ahead policy is to gain insights into where the greatest opportunities for improving the expected costs associated with the test wafer forecast quantities. The build ahead policy is similar to the Newsboy methodology described in section 3.2.2 in that the build ahead policy has a test wafer overage and underage cost. Using the decision analysis technique described in section 3.2.3, an expected cost for each possible quantity of test wafers is determined. Choosing the test wafer quantity that has the lowest expected cost minimizes Intel's cost. The following sections will provide modeling assumptions, define the parameters, and develop the optimization problem.

3.2.5: Build Ahead Policy Assumptions

The model makes assumptions based on the current forecasting process. In addition, there are some assumptions that simplify the analysis. For example, the demand is assumed to be normal. In reality there is limited data on the demand distribution, which makes it difficult to verify normality. While these simplifying assumptions may results in a sub-optimal solution, the assumptions should provide reasonable approximations so that intuition on policies can form. The following is the set of assumptions, as well as illustrative parameters, for the example:

- The demand is normally distributed with a mean of 91% of the plan and a standard deviation of 74% of the plan

- There are two types of test wafers, test wafers that are processed on at least one constraint tool and test wafers that are not processed on any constraint tool.
- Test wafers that are processed on constraint tools have a lead time of 14 days
- Test wafers that are processed on non-constraint tools have a lead time of 2 days
- The baseline cost for a test wafer is $60/wafer
- The opportunity cost to produce a test wafer that is processed on a constraint tool is $200,000/wafer
- It is not possible to determine which tools are on the critical path for ramping the fab; therefore, a delay in any tool is equally likely to delay the ramp
- There are 165 early tool sets (ETS) to qualify before the ramp is completed and operations can begin to manufacture production wafers
- Since each tool is equally likely to delay the ramp and 165 tools must qualify before the ramp is completed, there is a 1 in 165 chance (0.61%) that a given tool is on the critical path and any delay in qualifying that tool will delay the ramp
- The opportunity cost for a delay to the ramp is $2,000,000/day
- The build ahead for the ETS+1 is a sunk cost since the current policy is to build these test wafers (note: the ETS+1 is a redundant tool, see section 2.2 for a detailed description)
- Test wafers are only ordered in lot quantities of twenty-five
- Test wafers have no salvage value

3.2.6: Build Ahead Policy Definitions

The demand parameter: Percentage of Plan

The percentage of plan is defined as the percentage of the actual quantity of test wafer used of a given test wafer route to qualify a tool over its forecasted test wafer quantity. Let %P equal the percentage of plan. Then

$$\%P = \text{Actual Usage/Forecasted Usage}$$

The percentage of plan is the demand parameter for test wafer consumption. Based on data from the VF, the percentage of plan has an average value of 91% and a standard deviation of 74% (see appendix 3).

Cost of overage:

For the build ahead policy, there are two costs associated with the test wafers. There is a raw material cost and an opportunity cost for the test wafers. Only test wafers that are processed on the supply sites' constraint tools have an opportunity cost. The constraint tools could make production wafers that generate income for Intel. By making test wafers on the constraint tool, Intel is forgoing the potential income from the production wafers. Let the cost of overage per lot equal C_o. For non-constraint test wafers, C_o is \$1500/lot (\$60/wafer) of test wafers. For constraint test wafers, C_o is \$5,000,000/lot (\$200,000/wafer) plus \$1500/lot (\$60/wafer) of test wafers. A lot contains twenty-five

wafers. The total cost of overage is the product of the C_o times the number of build ahead lots.

Cost of underage:

For the build ahead policy, the cost of underage is an opportunity cost due to possibly delaying the completion of the fab ramp. Let C_u be the expected opportunity cost of underage. C_u is a cost per event and is a function of the number of build ahead lots (as will be seen). If there is an insufficient quantity of test wafers to qualify the tool, more test wafers will need to be ordered. The additional test wafers have a certain lead-time. Let LT equal the lead-time to acquire the additional test wafers. If the qualifying tool is on the critical path, the ramp will be delayed by this lead-time. A delayed ramp means that Intel cannot produce production wafers and production wafers provide income.

The expected opportunity cost of underage depends on the product of two probabilities: the first probability is the probability that for given TW route, additional wafers are necessary to qualify the tool. This probability is calculated based on the distribution of the %P. Based on the original forecasted quantity, the test wafer order quantity and the %P distribution, a coverage level for a given route is determined. For example, route X has a forecasted quantity of 50 and an order quantity of 100. This order quantity means that 200% of the request is on hand. Based on a normal %P distribution with mean of 91% and standard deviation of 74%, this 200% of the request means that there is only an 7% chance that more test wafers will be needed. This means that the order quantity has a coverage level of 93% (100%-7%). Let CL equal the coverage level.

The second probability relates to the likelihood that the tool that needs additional TW is going to be on the critical path. Recall that due to extraneous circumstances, it is difficult to determine when a tool is available for qualification. Let P_{CP} equal the probability that a tool is on the critical path. If there is an estimate of the opportunity cost for delaying the ramp, then a cost of underage can be determined. Let OC equal the daily opportunity cost for a delay in the ramp. The expected cost of underage is the product of one minus the coverage level, the probability that the tool is on the critical path, the daily opportunity cost for a delay in the ramp, and the lead time to acquire the additional test wafers. Then

$$C_u = (1\text{-}CL)*P_{CP}*OC*LT \qquad (4)$$

For example, assume that for a given non-constraint test wafer route (X), the forecasted test wafer quantity is 100. In this example, assume that there is no forecasted ETS+1 quantity. The first decision made in the decision tree model is to determine the % of plan (Figure 5). Each % of plan is associated with an event node that has a particular coverage level (CL). The coverage level is the probability of whether or not more test wafers will be needed. In the event that more test wafers are needed, there is another event node associated with whether or not the test wafers are needed for a tool that is on the critical path. The probability that the tool is going to be on the critical path (P_{CP}) is set at 0.61%. The opportunity cost for a delay in the ramp is four million dollars (two million dollars a day with a two day lead time for non-constraint test wafers).

A decision tree model provides a visual representation for establishing the expected opportunity cost (Bowersox, 1974). Figure 6, provides a decision tree model for test wafer route (X) for when the % of Plan is 125%. This decision tree model provides a visual representation of the cost of underage for test wafer route (X) when the % of Plan is 125%. The expected cost of underage for test wafer route (X) is $7829. With a forecasted quantity of 100, a 125% of Plan equates to twenty-five build ahead test wafers. Since test wafer route (X) is a non-constraint route, twenty-five wafers have a cost of overage of $1500. The total cost for test wafer route (X) when the % of plan is 125% is the sum of the cost of overage and the expected cost of underage; $9329. By choosing the % of Plan that minimizes the total cost for each test wafer route and that also satisfies the constraints, an optimal build ahead policy is created. Alternatively, a solution that maximizes the savings is used for the optimal build ahead policy. Using the initial forecasted test wafer quantity as a baseline for the % of Plan, the savings is calculated as the difference between the baseline cost and cost for a given % of Plan. Table 2 provides the costs and savings for various % of Plan choices for test wafer route (X). In this example, a build ahead with a 175% of Plan is the least cost option for test wafer route (X).

Figure 5: Decision Tree Stage One

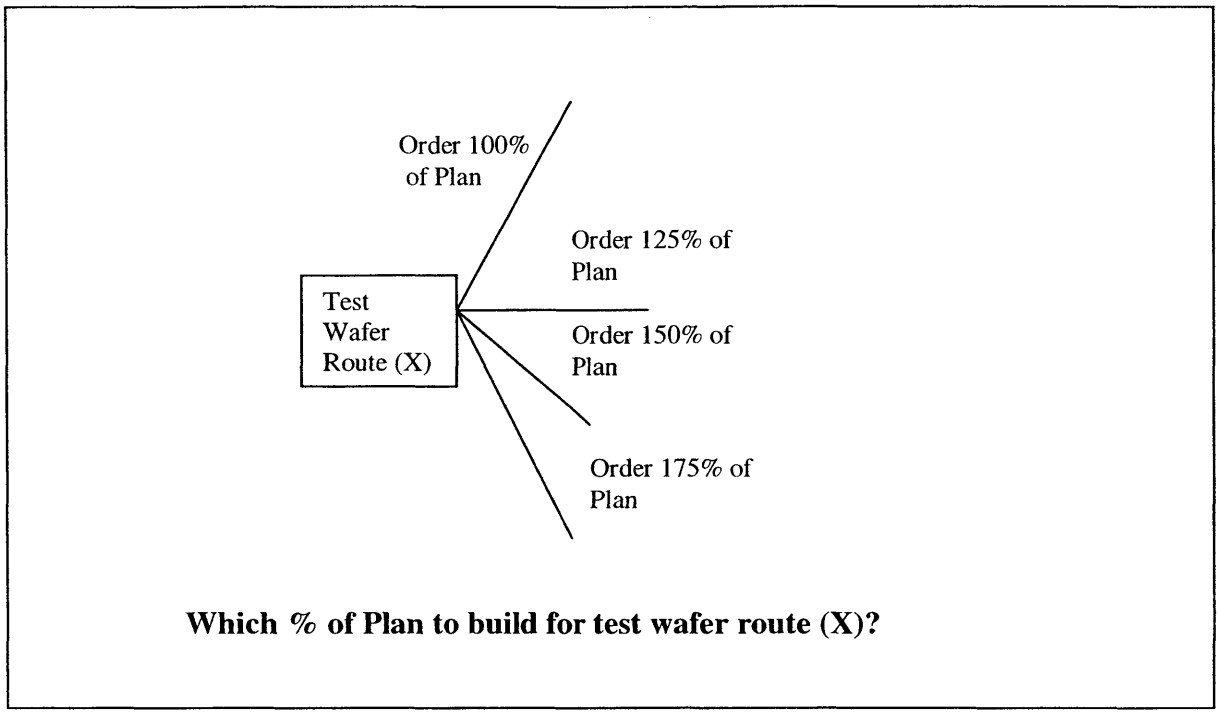


Figure 6: Decision Tree Analysis for 125% of Plan

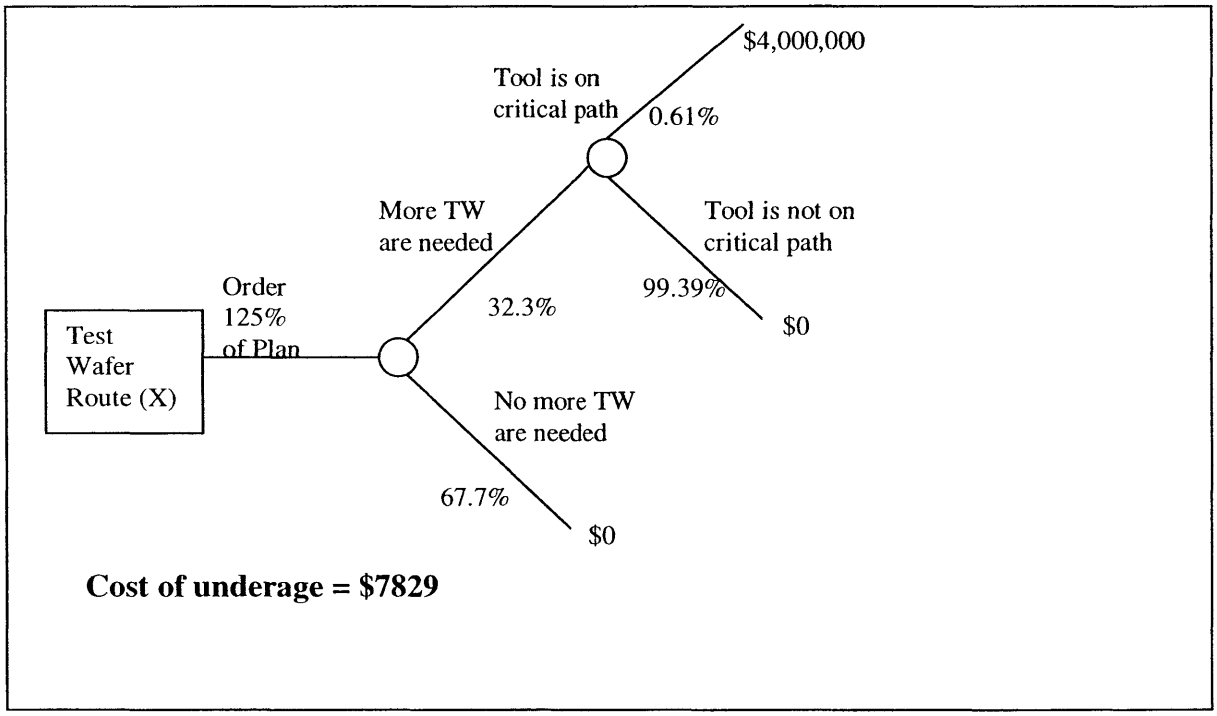


Table 2: Test Wafer Route (X) Costs and Savings

% of Plan	Cost of Overage	Coverage Level	Expected Cost of Underage	Total Expected Cost	Total Savings
100%	$ 0	55%	$10948	$10948	$0
125%	$1500	67.7%	$7829	$9329	$1619
150%	$3000	78.7%	$5155	$8155	$2793
175%	**$4500**	**87.2%**	**$3107**	**$7607 (Min. Cost)**	**$3341 (Max. Savings)**
200%	$6000	93.0%	$1706	$7706	$3242
225%	$7500	96.5%	$851	$8351	$2597

Hurdle rate:

The hurdle rate used in this analysis is fifteen percent. Recall that the hurdle rate is the minimum percent return on the capital investment that is acceptable (Brealey and Myers, 2000). Let H equal the hurdle rate. Then

$$H = 15\% \qquad (5)$$

A hurdle rate is used in this analysis to ensure that Intel is making good use of its capital. Without the hurdle rate as a constraint, the decision analysis could provide an optimal build ahead quantity that does not have a fifteen percent return on the capital. Recall that in the example above for a non-constraint test wafer route (X), the forecast quantity is 100 test wafers. With a % of Plan of 100% there is no additional test wafers built and the cost of overage is zero. The expected cost of underage is $10,948. If an additional lot of test wafers were built for test wafer route (X) as a buffer, route (X) would have a % of Plan of 125%. This extra lot would have a cost of overage of $1500. This extra lot of

test wafers lowered the expected cost of underage by $3119, which is an expected return of 208%. A savings of at least $1725 is necessary to provide a fifteen percent return. Having a hurdle rate of fifteen percent ensures that Intel gets at least a minimum return on its capital investment.

3.2.7: Optimizing the Savings

In order to optimize the savings, the objective function, the decision variables and the constraints must be defined.

Decision Variable:

The quantity of additional lots to be produced for the given test wafer route is the decision variable. The decision variable is defined as the lot modifier. Let L equal the lot modifier. L is an integer that is greater than or equal to zero, and equals the number of additional lots that are built.

Let TC_o equal the total cost of overage for a given test wafer route. TC_o is L times C_o. Then

$$TC_o = L*C_o \qquad (6)$$

The forecasted quantity of test wafers for a given route is defined as F. The forecasted quantity is the early tool set quantity. The initial forecasted request quantity of test wafers for a given route is defined as R_I. The initial forecasted request quantity is the early tool

set quantity plus the ETS+1 quantity. Let $\%R_I$ be R_I divided by F multiplied by 100. Then

$$\%R_I = (R_I/F)*100 \qquad (7)$$

In the example above, the $\%R_I$ for test wafer route (X) was 100%. Based on the distribution of the %P, this $\%R_I$ will provide a particular coverage level. The initial mean, μ_i, of the test wafer request beyond the initial plan is the difference between the mean %P and the $\%R_I$. In the example above, μ_i is –9% (91%-100%). The standard deviation, σ, of the test wafer request beyond the initial plan is the standard deviation of %P (74%). The coverage level is defined as the probability for the given test wafer route with the specified %R, no additional test wafers will be required. The initial coverage level is a function of μ_i and σ and is calculated based on the normal distribution. Let CL_I be the coverage level. Then

$$CL_I = \Phi(-\mu_i/\sigma) \qquad (8)$$

In the example above, this $\%R_I$ provided a coverage level of 55% for test wafer route (X).

The initial expected cost of underage is defined as C_{uI}. In the example, the C_{uI} was \$10948. Let C_{uI} be the product of one minus CL_I, P_{CP}, OC and LT. Then

$$C_{uI} = (1\text{-}CL_I)*P_{CP}*OC*LT \qquad (9)$$

Let $\%R_M$ be the modified percent requested for a given test wafer route. In the example above, the optimal $\%R_M$ for test wafer route (X) was 175%. Let $\%R_M$ be the sum of L time 25 plus R_I divided by F multiplied by 100. Then

$$\%R_M = (((L*25)+R_I)/F)*100 \qquad (10)$$

Based on the normal distribution of the %P, this $\%R_M$ will provide a particular coverage level. The modified mean, μ_m, of the test wafer request beyond the initial plan is the difference between the mean %P and the $\%R_M$. A $\%R_M$ of 175% results in a μ_m of –84% (91%-175%). The standard deviation, σ, of the test wafer request beyond the initial plan is still the standard deviation of %P (74%). The modified coverage level is a function of μ_m and σ and is calculated based on the normal distribution. Let CL_M be the coverage level for $\%R_M$. Then

$$CL_M = \Phi(-\mu_m/\sigma) \qquad (11)$$

In the example above, this $\%R_M$ provided a coverage level of 87.2% for test wafer route (X).

The modified cost of underage is defined as C_{uM}. In the example, the optimal solution with a $\%R_M$ of 175%, the C_{uM} was $ 3107. Let C_{uM} be the product of one minus CL_M, P_{CP}, OC and LT. Then

$$C_{uM} = (1 - CL_M) * P_{CP} * OC * LT \quad (12)$$

The total modified saving from the cost of underage is the difference between the initial cost of underage (C_{uI}) and the modified cost of underage (C_{uM}). In the example, the optimal solution had a total modified savings of $7841 ($10948 - $3107). Let TMS equal the difference between of C_{uI} and C_{uM}. Then

$$TMS = C_{uI} - C_{uM} \quad (13)$$

The saving is defined as S. Let S equal the difference between TMS and TC_o. Then

$$S = TMC - TC_o \quad (14)$$

Constraints:

The lot modifier L is greater than or equal to zero.

$$L >= 0 \quad (15)$$

Additional test wafers are only produced in full lot sizes.

$$L = \text{integer} \qquad (16)$$

The hurdle rate is greater than or equal to 15%.

$$H >= 15\% \qquad (17)$$

Objective Function:

The objective is to maximize the total projected savings for each test wafer route. Let z equal the objective function. Let j index the test wafer routes. Let N equal the total number of test wafer routes. Then z equals the sum of the difference between S and TC_o for each test wafer route for j equal 1 to N. Then

$$\max z = \sum_{j=1}^{N} (S)_j \qquad (18)$$

Additional Metrics:

There are additional performance metrics that can help the TW JET assess the impact of the optimized build ahead plan. The metrics are the total quantity of additional build ahead test wafers, the percent increase in test wafers over the initial request, and the expected payback on the optimized solution.

Chapter 4: Results

4.1: Build Ahead Results

A build ahead policy was developed for one of the preliminary test wafer forecasts. The preliminary test wafer forecast had 20 test wafer route requests. Each route was a non-constraint route. Using the optimization process described in section 3.2.7, an additional build ahead quantity was determined that maximized the total projected savings for each route. The sum of the savings from the individual routes is the projected savings for the build ahead policy. Table 3 summarizes the initial forecast information. Table 4 provides the optimal build ahead analysis.

Table 3: Initial Forecast Quantities

Route #	ETS Forecast Quantity	ETS+1 Forecast Quantity	$\%R_I$	Coverage Level (CL_I)	Initial Cost of Underage (C_{uI})
1	50	50	200%	93%	$ 1,706
2	75	0	100%	55%	$ 10,948
3	75	75	200%	93%	$ 1,706
4	75	0	100%	55%	$ 10,948
5	75	75	200%	93%	$ 1,706
6	250	175	170%	86%	$ 3,463
7	50	50	200%	93%	$ 1,706
8	50	0	100%	55%	$ 10,948
9	50	50	200%	93%	$ 1,706
10	25	25	200%	93%	$ 1,706
11	75	75	200%	93%	$ 1,706
12	65	65	200%	93%	$ 1,706
13	125	125	200%	93%	$ 1,706
14	50	0	100%	55%	$ 10,948
15	100	100	200%	93%	$ 1,706
16	125	125	200%	93%	$ 1,706
17	25	0	100%	55%	$ 10,948
18	25	0	100%	55%	$ 10,948
19	50	25	150%	79%	$ 5,155
20	25	25	200%	93%	$ 1,706

Table 4: Optimized Build Ahead

Route #	Lot Modifier	**Additional Build Ahead Quantity**	%RM	Modified Coverage Level (CLM)	Total Cost of Overage (TC_o)	Total Modified Savings (TMS)	Savings (S)	Payback
1	0	**0**	200%	93.0%	$0	$ 0	$ 0	0%
2	3	**75**	200%	93.0%	$4,500	$ 9,242	$ 4,742	105%
3	0	**0**	200%	93.0%	$0	$ 0	$ 0	0%
4	3	**75**	200%	93.0%	$4,500	$ 9,242	$ $ 4,742	105%
5	0	**0**	200%	93.0%	$0	$ 0	$ 0	0%
6	0	**0**	170%	85.7%	$0	$ 0	$ 0	0%
7	0	**0**	200%	93.0%	$0	$ 0	$ 0	0%
8	2	**50**	200%	93.0%	$3,000	$ 9,242	$ 6,242	208%
9	0	**0**	200%	93.0%	$0	$ 0	$ 0	0%
10	0	**0**	200%	93.0%	$0	$ 0	$ 0	0%
11	0	**0**	200%	93.0%	$0	$ 0	$ 0	0%
12	0	**0**	200%	93.0%	$0	$ 0	$ 0	0%
13	0	**0**	200%	93.0%	$0	$ 0	$ 0	0%
14	2	**50**	200%	93.0%	$3,000	$ 9,242	$ 6,242	208%
15	0	**0**	200%	93.0%	$0	$ 0	$ 0	0%
16	0	**0**	200%	93.0%	$0	$ 0	$ 0	0%
17	1	**50**	300%	99.8%	$3,000	$ 10,890	$ 7,890	263%
18	1	**50**	300%	99.8%	$3,000	$ 10,890	$ 7,890	263%
19	1	**25**	200%	93.0%	$1,500	$ 3,449	$ 1,949	130%
20	0	**0**	200%	93.0%	$0	$ 0	$ 0	0%

The projected savings was $39,696. The build ahead policy required an additional 375 wafers, which was a 15.1% increase over the initial request quantity. The average payback for the build ahead policy was 176%. Table 5 summarizes the results.

Table 5: Results Summary

Total Savings	$ 39,696
Additional build ahead Wafers	375
% of Additional Wafer	15.1%
Payback ((Savings-Cost)/Cost)	176%

4.2: What if Scenarios

In order to develop intuition about the impact of the factors that affect the build ahead policy, several what if scenarios were developed. Table 6 states the what if scenarios. Table 7 shows the what if scenario results.

Table 6: What If Scenarios

Scenario	Description
A	Baseline: no changes to the assumptions
B	The opportunity cost if additional test wafers are needed is doubled (either by doubling the lead time, the opportunity cost for a delay or the chance that a tool is on the critical path)
C	The opportunity cost if additional test wafers are needed is reduced by half (either by doubling the lead time, the opportunity cost for a delay or the chance that a tool is on the critical path)
D	The standard deviation on the demand is doubled
E	The standard deviation on the demand is reduced by half
F	Relax the full lot build assumption
G	Constrain the percent of Additional Wafers to less than or equal to 10%

Table 7: What If Scenario Results

P860 What if Scenarios							
	A	B	C	D	E	F	G
Route #	**Additional Build Ahead**	Additional Build Ahead	Additional Build Ahead	Additional Build Ahead	Additional Build Ahead	Additional Build Ahead	Additional Build Ahead
1	0	25	0	25	0	3	0
2	75	100	0	25	50	67	25
3	0	25	0	0	0	0	0
4	75	100	0	25	50	67	25
5	0	25	0	0	0	0	0
6	0	0	0	0	0	0	0
7	0	25	0	25	0	3	0
8	50	75	25	75	25	55	50
9	0	25	0	25	0	5	0
10	0	25	0	25	0	9	0
11	0	25	0	0	0	0	0
12	0	25	0	0	0	0	0
13	0	0	0	0	0	0	0
14	50	75	25	75	25	55	50
15	0	0	0	0	0	0	0
16	0	0	0	0	0	0	0
17	50	50	25	50	25	34	25
18	50	50	25	50	25	34	25
19	25	50	0	50	0	30	25
20	0	25	0	25	0	9	0
Total Savings	**$ 39,696**	$ 116,111	$ 10,940	$ 31,968	$ 42,966	$ 42,443	$ 35,059
Additional build ahead Wafers	**375**	725	275	800	200	422	225
% of Additional Wafer	**15%**	29%	11%	32%	8%	17%	9%
Payback ((Savings-Cost)/Cost)	**176%**	267%	66%	67%	358%	167%	260%

Table 8 summarizes the performance of each scenario relative to baseline.

Table 8: What If Scenario Performance Summary

Performance	Scenario B	Scenario C	Scenario D	Scenario E	Scenario F	Scenario G
Change in Total Savings	2.9	0.3	0.8	1.1	1.1	0.9
Change in additional wafers	1.9	0.7	2.1	0.5	1.1	0.6
Change in Payback	1.5	0.4	0.4	2.0	0.9	1.5

The results from scenarios B and C demonstrate the impact that changes in the cost of underage have on the optimized solution. The cost of underage is the product of three factors, the coverage level, the probability that the tool is on the critical path and the opportunity cost for a delay in the ramp. All else being equal, a larger cost of underage creates larger total savings. The results of scenario D and E demonstrate the impact of the standard deviation on the optimized solution. An in depth discussion of the effects of the standard deviation on the optimal build ahead quantity is in section 4.3. When the full lot assumption was relaxed in scenario F, the changes in the performance metrics were small. When the percent of additional wafer is constrained to 10% in scenario G, there is a small reduction to the total savings. The 10% constraint is only marginally different than the baseline result of a 13% increase in additional wafers. The payback in scenario G was higher than the payback for the baseline. With a 10% constraint on the increase in additional wafers, the optimization of the total savings throws out the builds with the

worst savings. The builds with the worst savings have lower paybacks, so the payback for the constrained scenario G actually looks better.

4.3: Generalize Build Ahead Plan

During the test wafer forecast preparation phase, the forecast changes frequently. Additional routes are being added. Occasionally an ETS+1 tool set is dropped from the ramp schedule. At times the original forecast for a route is updated. A generalized build ahead plan that allows the test wafer team to quickly determine the optimal test wafer order quantity could minimize the chaos created by all of these types of changes to the forecast. If a member of the test wafer team could simply look up the optimized build ahead plan for a given forecasted test wafer quantity, changes to the forecast would be easier to handle. In this section a generalized build ahead plan is developed.

There are eight input variables used to optimize the build ahead plan. These variables are summarized here:

- Opportunity cost for a delay to the ramp
- If additional test wafers are needed, the chance that they are needed for the tool that is on the critical path
- The lead time for obtaining additional test wafers
- The mean percent of plan
- The standard deviation for the percent of plan
- The minimum hurdle rate
- The ETS+1 quantity

The product of the first three variables is the expected cost of underage.

With accurate estimates of these eight input variables, it is possible to determine an optimal build ahead quantity for any ETS quantity. Using Microsoft Excel's macros capability, it is easy to create a build ahead look up tool. An example of the build ahead look up tool is located in appendix 4.

There are four steps that the user must follow to operate the build ahead look up tool.

Step 1:

- Verify and update the eight input variable

Step 2:

- Input the ETS quantity in question

Step 3:

- Initiate the Excel solver by clicking on the button linked to the macro

Step 4:

- Order the optimal build ahead quantity

This look up tool calculates the optimal build ahead quantity that maximizes the projected savings.

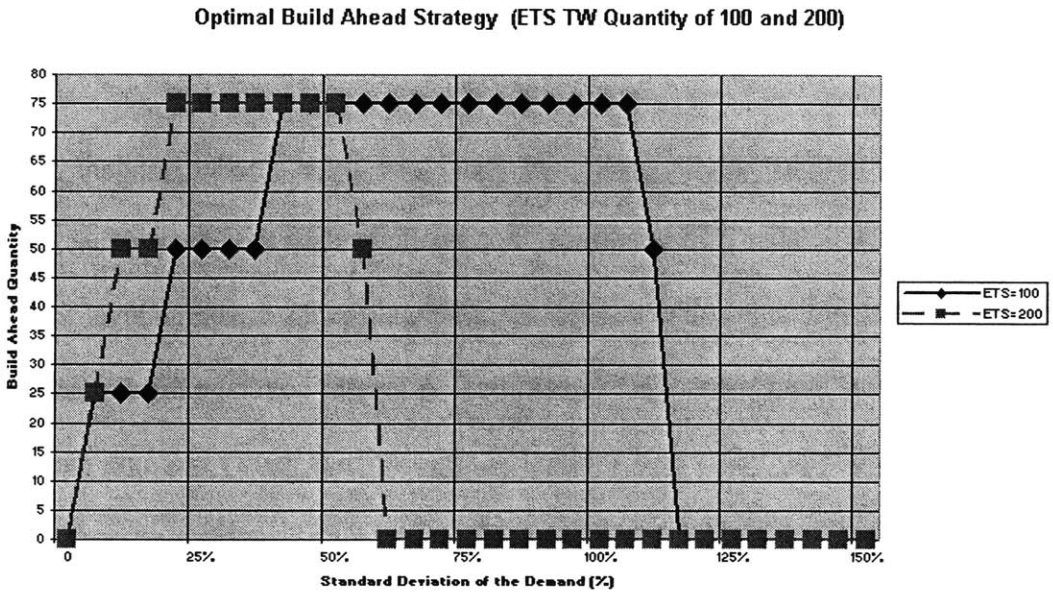
Using the generalized build ahead plan, additional insights on the effect that the standard deviation of demand has on the build ahead plan are obtained. Holding the other seven

input variables constant according to the values located in table 9, the standard deviation is varied. Figure 7 shows the results for ETS quantities of 100 and 200.

Table 9: Input variables

Input Variable	Value
Daily opportunity cost of a delay to the ramp	$1,650,000
Chance that an insufficient quantity of test wafers will impact the critical path	0.61%
Mean %P	100%
Test wafer lead time (days)	2
Test wafer cost	$60
Hurdle rate	15%
ETS+1 quantity	0

Figure 7:

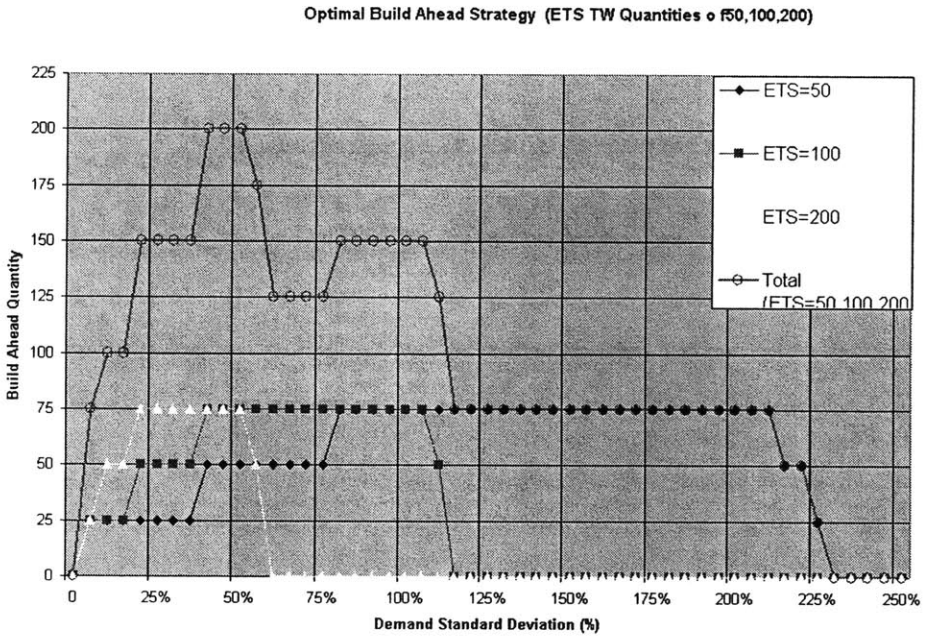


Several observations are made from figure 7. The optimal build ahead quantity has a step function. This step function is due to the full lot constraint. There is a peak build ahead quantity of 75 test wafers, which is a function of the test wafer cost and the expected opportunity cost if additional test wafers are needed. Eventually the test wafer cost for an additional lot is greater than the savings. At this point, the marginal savings are negative. Since the objective is to maximize the savings, it does not make sense to build additional lot of wafers. This result depends on the assumptions about the expected cost of underage, specifically that there is a fixed cost regardless of the extent of the shortage in test wafers.

The larger ETS quantities reach the peak build ahead quantity at smaller standard deviation values than smaller ETS quantities. For small standard deviation values, an additional lot of test wafers provides a larger marginal gain in the coverage level for larger ETS quantities than for small ETS quantities. A greater coverage level means that more of the expected opportunity cost is saved. Larger savings justify building the lots. Likewise, build ahead wafers do not make sense for larger ETS quantities when the standard deviation is high. When the standard deviation is high, one extra lot of test wafers increases the coverage level to a small degree. This small increase in coverage level leads to a small savings, which does not justify the cost for the lot of wafers.

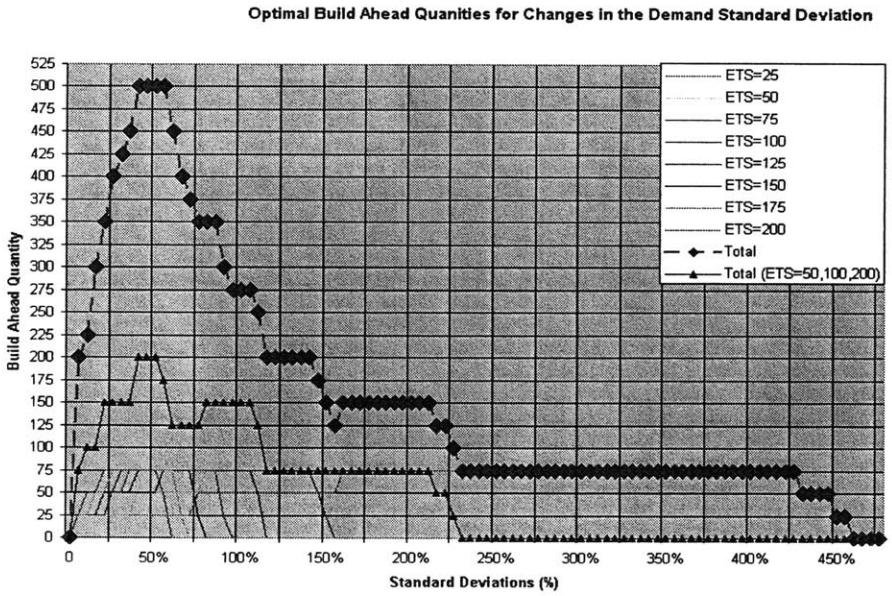
An additional observation is made when considering several ETS quantities. Figure 8 shows the results for 50, 100 and 200 ETS quantities and the sum of the three ETS values. The sum of the three ETS values reaches a maximum build ahead quantity of 200 test wafers. The build ahead quantity decreases for standard deviations between 50% and 60%. From 60% to 75%, the optimal build ahead quantity is level at 125 test wafers; however, the build ahead quantity increases to 150 at a standard deviation of 80%. The total build ahead quantity remains at 150, until the standard deviation reaches 105%. Beyond a standard deviation of 105%, the optimal build ahead quantity for the 100 ETS value decrease and quickly drops to zero.

Figure 8:



This intermediate increase in the optimal build ahead quantity is also seen when a larger quantity of ETS values are considered. Figure 9 provides the optimal build ahead quantities when there are 8 ETS quantities between 25 and 200. This rise then fall and then rise again in the optimal build ahead quantity observed in figures 8 and 9, suggest an important relationship between the test wafer team and their incentives. The TW JET has incentives for reducing the test wafer quantities. The plots in figure 8 and 9 suggest that this incentive may not always maximize Intel's savings. As the standard deviation decreases, the expected opportunity cost will decrease. This smaller standard deviation reduces the risk that the test wafer readiness will delay the fab ramp; however, there are situations when improvements to the standard deviation indicate that building more test wafers provide maximized savings. This is in conflict with the TW JET's current incentives and could create mix motive opportunities.

Figure 9:



Chapter 5: Conclusions and Recommendations

The goal of this thesis was to minimize the risk that the TW readiness process has on the manufacturing readiness of a ramping fab. The primary TW risk is ensuring that the right test wafers are available on time. The tools and policies developed in this thesis enable the TW JET to make informed decisions that will improve the test wafer readiness process. The allocation tool helps the CQT choose the supply site in the best position to process the test wafers. The build ahead policy and look up tool identifies the optimal test wafer quantity.

This chapter briefly reviews Intel's current test wafer readiness process. Conclusions are drawn and recommendations are made based on the analysis of the three opportunities discussed in this thesis. Finally, suggestions for future opportunities are made for when Intel masters the opportunities discussed in this thesis.

5.1: Current test wafer readiness process summary

Test wafer (TW) readiness for the tool qualification has consistently been high risk for manufacturing readiness. The primary TW risk is ensuring that the right TWs are available on time. There are two phases to the TW readiness process, the forecast preparation and the build allocation phases.

The test wafer forecast preparation process is summarized as an informal process that is based on a White Paper quantity and then modified by high volume manufacturing (HVM) people who have either already gone through the qualification process at a

different site or are the local process engineers. The initial test wafer forecast was based on the White Paper. The development engineers went through an informal process for determining the quantity of test wafers stated in the White Paper. The local test wafer team used the White Paper as a starting point for generating a forecast. The quantity of test wafers in the forecast was modified through insights the local test wafer team gained from other HVM test wafer engineers, HVM process engineers, and local process engineers. While the local process engineers where the key customer, getting an accurate quantity of test wafers was not a priority of the process engineers during this planning phase of generating the forecast.

The cross-site qualification team (CQT), a sub-team of the TW JET, coordinated the test wafer build allocation process. The CQT was composed of members from each of the virtual factory (VF) sites. The process for obtaining build commitments was informal. The local test wafer team member presented the build request to the other VF sites. If the request required processing on a constraint tool, it was difficult to obtain a commitment. There was no mechanism that provided the CQT with information on which site was in the best position to build these difficult requests. Typically several weeks passed before a VF site committed to build one of the difficult request.

5.2: Allocation tool conclusions

The allocation tool provides information that can be used, as a baseline by the CQT for determining which VF site should build a test wafer request. In the past, the CQT would receive a request and it could take several weeks to determine which site would build the

wafers. There was also no indication if the site that committed to the request was in the best position to build the wafers. It was possible for a site to feel like it was committing to more than its fair share of the request and unilaterally stop committing to any additional request. This was not an optimal policy. The allocation tool will allow each member of the CQT to compare each site's excess capacity. The ability for each site to see the excess capacity of all the sites should minimize the political jockeying of getting a site to commit.

5.3: Build Ahead Conclusions

The what-if scenarios provide insight on where to focus operational efforts. With limited resources, it is difficult to address everything at once. Changes to the three input variables that affect the cost of underage have the largest impact on the total savings. Of these three variables, the lead-time and the chance that a tool is on the critical path have opportunities for operational improvements. The TW JET can measure its lead-time and look for ways to improve the lead-time. Working with the project management team, the TW JET can better characterize the likelihood that a tool is on the critical path.

Intel has little control over the third variable, opportunity cost for a delay. Market forces drive the opportunity cost for a delay. In fact a high opportunity cost for a delay suggests that Intel's microprocessors are in high demand. While it is important to have an accurate measurement of the opportunity cost, it does not make sense to try to change it.

From the analysis of the generalized build ahead plan, it was observed that there are scenarios when building more test wafers maximizes Intel's savings. The TW JET's current incentive is to minimize the test wafer quantity. The TW JET's current incentive does not optimizes Intel's savings in all scenarios.

5.4: Recommendations

The recommendations focus on improving the test wafer readiness process by developing data driven processes. These data driven processes provide the TW JET with decision-making tools. Armed with these decision making tools, the TW JET is capable of making informed choices that will improve the test wafer readiness process and minimize the risk that the test wafers will delay the manufacturing readiness process.

While not fully developed in this thesis, an improved tracking system is needed that will capture data that can provide usage versus forecasted TW quantities. This metric can provide insight into which tools that may require additional TW quantities for future tool qualifications. This metric will improve the accuracy of the buffer inventory policy.

The CQT should use the allocation tool to identify which VF supply site is in the best position to build the qualification TWs. The current allocation process takes several weeks to identify a site that can commit to the difficult requests that require processing on constraint tools.

Implementation of a TW buffer inventory strategy will improve the test wafer readiness process by ensuring that additional TWs are already processed and available for times when tools have excursions from the WP quantities. The buffer inventory strategy is a hedging practice that maximizes Intel's savings. The buffer inventory strategy demonstrates that every TW route does not need an additional buffer.

The TW JET should align its incentives so that Intel can maximize its savings. Reducing the test wafer quantity was traditionally assumed to always result in savings. The conclusions from section 5.3, identify at least one situation where reducing the test wafer quantity does not result in maximizing savings.

5.5: Future Opportunities

Once the TW JET implements the recommendations from this thesis, additional opportunities become available. The allocation tool process described in section 3.1.2, suggests that the CQT record the incidences where the site that has the most excess capacity is unable to commit to a specific request. Recording these incidences and tallying up the most prevalent incidence provides the CQT with valuable information. The CQT can then share this information with the operations group and the project management teams. By working cross-functionally with the operations and project management, it is possible to make an informed decision on whether or not changing policies can minimize the prevalence of the incident.

The buffer inventory policy identifies several opportunities for improvement. The high variability of the demand parameter creates a large cost of underage. Part of the reason the variability is high is because the development sites have an informal process for establishing WP test wafer quantities. Now that the cost of this informal process is exposed, a cross-functional team of development and test wafers engineers can look for improvement opportunities. If the cost for improving the variability could be estimated, it could be compared to the expected opportunity cost and rational trades could be made.

References

Bertsimas, D. and R. Freund, Data, Models, and Decisions. South-Western College Publishing, 2000

Bowersox, D. J., Logistical Management. Macmillan Publishing Co., Inc., 1974

Brealey, R. A. and S. C. Myers, Principles of Corporate Finance, 6th edition. Irwin McGraw Hill, 2000

Goldratt, E. M., The Goal. North River Press, 1992

Nahmias, S. Production and Operations Analysis, 3rd edition. McGraw Hill, 1997

Newlin, A. W., "Equipment Protective Capacity Optimization Using Discrete Event Simulation." Masters Thesis, Cambridge, MA: Massachusetts Institute of Technology, June, 2000

Van Zant, P., Microchip Fabrication, 3rd edition. McGraw Hill, 1997

Winston, W. L., Introduction to Mathematical Programming, 2nd edition. Duxbury Press, 1995

Appendix 1

Tracking and Performance Metrics:

The local test wafer team tracked the qualification forecast in an excel spreadsheet database. This database was cumbersome and had several inefficient features. The database lacked the following capabilities:

- Unique row identifiers
- A centralized database were all new information was updated
- Links to the supply fabrication sites
- Tracking capability to monitor a request status
- Performance metrics

The database was cumbersome because of the first three bulleted items. Without the unique row identifiers, it was difficult to query the request. Since querying was difficult, one had to recall minute details for several atypical requests. Furthermore, the centralized database did not automatically update any of the smaller detailed summary sheets. There were several summary sheets that tracked individual supply fabrication sites commitments. In addition, the supply fabrication sites had their own databases for tracking the test wafer request. This separate database was not link to the main forecast database.

This cumbersome database was prone to errors. For example, some requests were split and built by two supply fabrication sites. The centralized forecast database did not have the capability to sub-divide the request. A note was attached in the notes column in the centralized forecast database that indicated the request was split between two sites. In addition, the smaller detailed summary sheets tracked commitments for each of the two supply sites. If the status of a particular request was questioned, someone would need to lookup three different databases for proper verification. Often times one of the databases was not updated - either properly or on time-, which caused confusion and made people question the accuracy of the database.

The database did not track the status of the request through the entire process. The centralized forecast database kept track of all of the needs and the detailed summary sheets identified which supply fabrication site committed to which request. However, there was no method for knowing the location of a request at any given time. If the ramping site received a particular lot of wafers, the lot was not verified against the forecast. Without verifying against the forecast two potential problems were created. If a lot of wafers went missing, it was not possible to determine where it was lost. If a lot of test wafers were needed by a particular date, it was not possible to verify that lot was in on time.

The centralized forecast database did not measure any typical performance metrics. Neither on time delivery performance, nor test wafer usage statistics were captured.

Without measuring performance, it was difficult to track trends and make improvements to the process.

Appendix 2

Excess Capacity Tables for Constraint tool (X):

Availability

Site	Process	WW-200033	WW-200034	WW-200035	WW-200036	WW-200037	WW-200038	WW-200039	WW-200040	WW-200041	WW-200042	WW-200043	WW-200044	WW-200045	Avg
Site 1	P858	0.8	0.61	0.47	0.82	0.74	0.8	0.63	0.85	0.59	0.85	0.72	0.81	0.81	0.73
Site 2	P858	0.57	0.82	0.72	0.7	0.41	0.72	0.9	0.88	0.97	0.86	0.54	0.76	0.67	0.73
Site 3	P858	0.61	0.67	0.6	0.58	0.61	0.62	0.59	0.68	0.75	0.63	0.76	0.72	0.76	0.66
Site 4	P858	0	0	0	0	0	0	0	0	0	0	0	0.78	0.7	0.11
Site 5	P858	0.64	0.66	0.75	0.76	0.77	0.79	0.73	0.76	0.68	0.64	0.83	0.75	0.76	0.73
Site 5	P858	0.59	0.64	0.74	0.72	0.65	0.9	0.73	0.87	0.91	0.8	0.72	0.9	0.86	0.77

Utilization

Site	Process	WW-200033	WW-200034	WW-200035	WW-200036	WW-200037	WW-200038	WW-200039	WW-200040	WW-200041	WW-200042	WW-200043	WW-200044	WW-200045	Avg
Site 1	P858	0.87	0.57	0.49	0.78	0.69	0.83	0.61	0.6	0.68	0.93	0.79	0.64	0.73	0.71
Site 2	P858	0.21	0.19	0.14	0.18	0.13	0.18	0.09	0.12	0.03	0.11	0.07	0.23	0.21	0.15
Site 3	P858	0.44	0.5	0.44	0.53	0.53	0.53	0.56	0.61	0.58	0.5	0.56	0.6	0.62	0.54
Site 4	P858	0	0	0	0	0	0	0	0	0	0	0	0.31	0.2	0.04
Site 5	P858	0.51	0.46	0.57	0.65	0.58	0.57	0.53	0.6	0.46	0.39	0.5	0.46	0.43	0.52
Site 5	P858	0.45	0.39	0.55	0.63	0.55	0.7	0.3	0.64	0.69	0.44	0.48	0.41	0.33	0.5

Process Time

Site	Process	WW-200033	WW-200034	WW-200035	WW-200036	WW-200037	WW-200038	WW-200039	WW-200040	WW-200041	WW-200042	WW-200043	WW-200044	WW-200045	Avg
Site 1	P858	7.43	2.96	3.08	3.26	3.22	3.21	3.11	3.47	2.68	2.77	2.97	2.87	2.6	3.36
Site 2	P858	4.17	3.96	3.83	4.45	3.88	4.01	3.82	3.95	4.07	5.37	4.02	4.24	4	4.14
Site 3	P858	3.61	3.72	3.72	3.67	3.73	3.91	3.53	3.6	3.66	3.8	3.58	3.75	4	3.71
Site 4	P858	0	0	0	0	0	0	0	0	0	0	0	2.28	2.43	0.36
Site 5	P858	2.43	3.04	2.72	2.53	2.48	3.03	2.92	2.93	2.82	3.11	2.56	3.1	3.49	2.86
Site 5	P858	4.52	3.71	3.65	3.76	3.38	3.74	5.33	4.4	3.73	3.76	4.84	3.45	3.64	3.99

IP Tools

Site	Process	WW-200033	WW-200034	WW-200035	WW-200036	WW-200037	WW-200038	WW-200039	WW-200040	WW-200041	WW-200042	WW-200043	WW-200044	WW-200045	Avg
Site 1	P858	2	2	2	2	2	2	2	2	2	2	2	2	2	2
Site 2	P858	2	2	2	2	2	2.57	3	3	3	3	2.96	2.94	3	2.57
Site 3	P858	6.64	7	7	7	7	7	7	7	7	7	7	7	7	6.97
Site 4	P858	0	0	0	0	0	0	0	0	0	0	0	0.71	2	0.21
Site 5	P858	5.89	5.9	5.36	6	6.64	7	7	7	6.93	7	8	8	8	6.82
Site 5	P858	3	3	3	3	3	2	3	3	3	3	3	3	3	2.92

Extra Capacity per Tool

Site	Process	WW-200033	WW-2000	WW-2000	WW-2000	WW-2000	WW-2000	WW-2000	WW-2000	WW-2000	WW-2000	WW-2000	WW-2000	WW-2000	Avg
Site 1	P858	-1.6	2.3	-1.1	2.1	2.6	-1.6	1.1	12.1	-5.6	-4.9	-4.0	10.0	5.2	1.0
Site 2	P858	14.5	26.7	25.4	19.6	12.1	22.6	35.6	32.3	38.8	23.5	19.6	21.0	19.3	23.5
Site 3	P858	7.9	7.7	7.2	2.3	3.6	3.9	1.4	3.3	7.8	5.7	9.4	5.4	5.9	5.4
Site 4	P858	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	34.6	34.6	32.7
Site 5	P858	9.0	11.1	11.1	7.3	12.9	12.2	11.5	9.2	13.1	13.5	21.7	15.7	15.9	12.3
Site 5	P858	5.2	11.3	8.7	4.0	5.0	9.0	13.6	8.8	9.9	16.1	8.3	23.9	24.5	11.4

Total Extra Capacity

Site	Process	WW-200033	WW-2000	WW-2000	WW-2000	WW-2000	WW-2000	WW-2000	WW-2000	WW-2000	WW-2000	WW-2000	WW-2000	WW-2000	Avg
Site 1	P858	-3.2	4.5	-2.2	4.1	5.2	-3.1	2.2	24.2	-11.3	-9.7	-7.9	19.9	10.3	2.0
Site 2	P858	29.0	53.5	50.9	39.3	24.2	58.1	106.9	97.0	116.4	70.4	58.1	61.7	58.0	60.5
Site 3	P858	52.5	53.7	50.6	16.0	25.2	27.1	10.0	22.9	54.6	40.2	65.7	37.6	41.2	37.9
Site 4	P858	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	24.6	69.1	6.9
Site 5	P858	52.9	65.2	59.6	43.8	85.5	85.4	80.5	64.2	90.8	94.5	173.3	125.7	127.1	84.1
Site 5	P858	15.6	34.0	26.2	12.1	14.9	18.0	40.7	26.3	29.7	48.3	25.0	71.6	73.4	33.2

Appendix 3:

VF Percentage of Plan Data:

Tool Type	Tool ID	VF Route	BS/PR	F18 Plan	Actual	% of Plan
LRCst	LRC010	ET.858	PR	15	50	333%
AWBso	AWB015	ET.812	PR	8	25	313%
AWBso	AWB008	ET.819	PR	8	25	313%
OXAxx	OXA002	ET.829	PR	8	25	313%
GAS	GAS002	ET.851	PR	8	25	313%
LRCst	LRC010	ET.862	PR	8	25	313%
OXAxx	OXA002	ET.840	PR	25	75	300%
LRCns	LRC007	ET.881	PR	10	25	250%
SSPss	SSP001	LT.806	PR	4	10	250%
SPTxx	SPT002	TF.X98	PR	188	400	213%
HITxx	HIT001	ET.825	PR	5	10	200%
DL xx	DL 008	LT.863	PR	50	100	200%
DL xx	DL 008	LT.833	PR	50	100	200%
DL xx	DL 008	LT.859	PR	25	50	200%
HITxx	HIT 002	ET.889	PR	14	25	179%
CMPil	CMP011	PL.898	PR	250	425	170%
HITxx	HIT003	ET.883	PR	15	25	167%
NSXxx	NSX031	LT.882	PR	75	125	167%
HITxx	HIT003	ET.886	PR	8	13	163%
HITxx	HIT003	ET.889	PR	8	13	163%
HITxx	HIT003	ET.890	PR	8	13	163%
SPTna	SPT001	TF.X98	PR	200	325	163%
DL xx	DL 008	LT.860	PR	25	38	152%
SPTco	SPT014	TF.X98	PR	175	250	143%
DL xx	DL 008	LT.861	PR	25	35	140%
CMPst	CMP001	PL.896	PR	25	35	140%
ADHlt	ADH001	TF.821	PR	54	75	139%
ADHlt	ADH001	TF.820	PR	475	650	137%
RTAbp	RTA003	DI.802	PR	225	300	133%
RTAbp	RTA003	DI.X77	PR	225	300	133%
AWBga	AWB001	ET.814	PR	75	100	133%
NSXxx	NSX031	LT.883	PR	75	100	133%
WMPxx	WMP001	PL.803	PR	225	300	133%
OXAxx	OXA 001	ET.896	PR	12	13	108%
OXAxx	OXA 001	ET.897	PR	12	13	108%
HITxx	HIT001	ET.883	PR	12	13	108%
VDFte	VDF025	DI.XD1	PR	25	25	100%
VDFni	VDF016	DI.XN1	PR	25	25	100%
VDFpo	VDF014	DI.XY1	PR	50	50	100%
PLYxx	PLY001	ET.804	PR	6	6	100%
HITxx	HIT 002	ET.887	PR	18	18	100%

Tool Type	Tool ID	VF Route	BS/PR	F18 Plan	Actual	% of Plan
HITxx	HIT001	ET.887	PR	18	18	100%
AWBso	AWB008	ET.834	PR	4	4	100%
OXAxx	OXA002	ET.897	PR	3	3	100%
GAS	GAS003	ET.839	PR	5	5	100%
HITxx	HIT001	ET.890	PR	3	3	100%
HITxx	HIT 002	ET.886	PR	25	25	100%
HITxx	HIT 002	ET.883	PR	25	25	100%
AWBbe	AWB013	ET.813	PR	15	15	100%
HITxx	HIT001	ET.886	PR	25	25	100%
HITxx	HIT001	ET.889	PR	50	50	100%
LRChm/pa	LRC001 + LRC003	ET.802	PR	125	125	100%
LRCns	LRC008	ET.810	PR	25	25	100%
AWBso	AWB015	ET.818	PR	25	25	100%
OXAxx	OXA 001	ET.829	PR	25	25	100%
GAS	GAS003	ET.832	PR	15	15	100%
LRCst	LRC010	ET.859	PR	15	15	100%
LRCst	LRC010	ET.863	PR	15	15	100%
OXAxx	OXA 001	ET.840	PR	25	25	100%
NSAxx	NSA001	LT.869	PR	25	25	100%
NSXxx	NSX031	LT.875	PR	75	75	100%
NSXxx	NSX031	LT.876	PR	5	5	100%
NSXxx	NSX031	LT.885	PR	50	50	100%
HBTxx	HBT001	LT.806	PR	12	12	100%
DSBxx	DSB041	LT.897	PR	50	50	100%
DUVxx	DUV001	LT.865	PR	25	25	100%
DUVxx	DUV001	LT.866	PR	25	25	100%
NSAxx	NSA001	LT.868	PR	25	25	100%
NSXxx	NSX031	LT.882	PR	10	10	100%
DUVxx	DUV001	LT.867	PR	50	50	100%
NSXxx	NSX031	LT.886	PR	100	100	100%
SSPss	SSP001	LT.805	PR	15	15	100%
CMPst	CMP001	PL.893	PR	3	3	100%
WMPxx	WMP001	PL.815	PR	15	15	100%
AMSps	AMS001	TF.889	PR	18	18	100%
NVWxx	NVW001	TF.826	PR	3	3	100%
SPTco	SPT014	TF.X97	PR	75	75	100%
HDPxx	HDP001	TF.886	PR	100	100	100%
NVWxx	NVW001	TF.891	PR	125	125	100%
NSXxx	NSX031	LT.874	PR	50	41	82%
DSBxx	DSB041	LT.872	PR	25	20	80%
OXAxx	OXA002	ET.896	PR	4	3	75%
PLYxx	PLY001	ET.854	PR	100	75	75%
DSBxx	DSB041	LT.877	PR	100	75	75%
RTAsa	RTA001	DI.X77	PR	500	350	70%
AWBsc	AWB003	ET.814	PR	25	17	68%

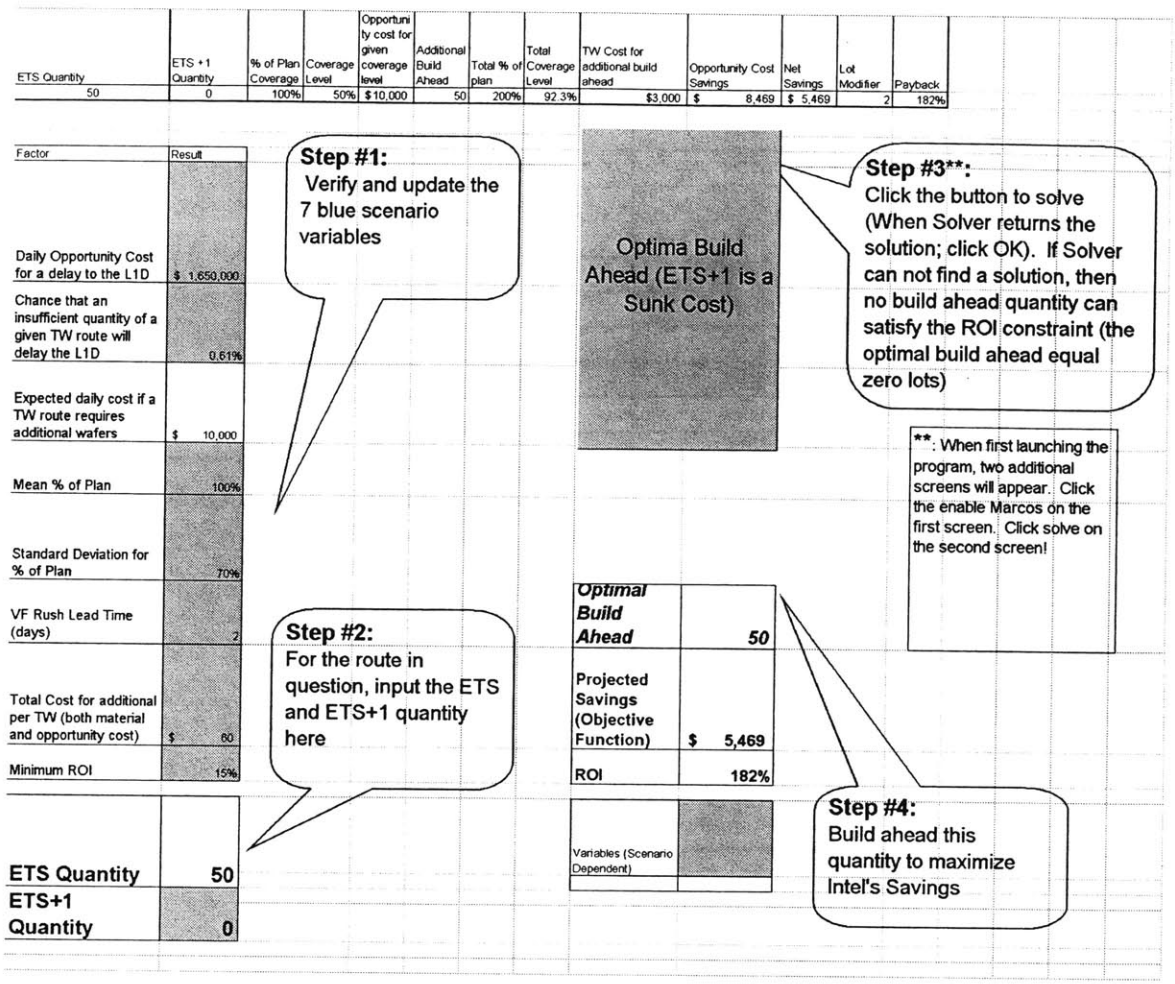
Tool Type	Tool ID	VF Route	BS/PR	F18 Plan	Actual	% of Plan
AWBbe	AWB013	ET.817	PR	25	17	68%
DSBxx	DSB041	LT.878	PR	25	17	68%
DSBxx	DSB041	LT.879	PR	25	17	68%
NSXxx	NSX031	LT.884	PR	25	17	68%
BCTli	BCT041	LT.X29C	PR	25	17	68%
LRCst	LRC010	ET.891	PR	75	50	67%
AWBbe	AWB013	ET.821	PR	75	50	67%
DSBxx	DSB041	LT.870	PR	75	50	67%
WMPxx	WMP001	PL.817	PR	75	50	67%
STIxx	STI001	tf.893	PR	75	50	67%
LRChm/pa	LRC001 + LRC003	ET.837	PR	16	10	63%
AWBso	AWB015	ET.822	PR	25	15	60%
DSBxx	DSB041	LT.871	PR	125	75	60%
DSBxx	DSB041	LT.873	PR	50	28	56%
NCTli	NCT031	LT.X29C	PR	150	83	55%
VDFal	VDF027	DI.850	PR	50	25	50%
VDFga	VDF015	DI.XA1	PR	100	50	50%
AWBso	AWB015	ET.814	PR	100	50	50%
AWBga	AWB001	ET.820	PR	100	50	50%
HITxx	HIT003	ET.825	PR	100	50	50%
GAS	GAS002	ET.832	PR	100	50	50%
WMPxx	WMP001	PL.802	PR	150	75	50%
HDPxx	HDP001	TF.887	PR	50	25	50%
HDPxx	HDP001	TF.888	PR	100	50	50%
AMPxx	AMP001	TF.890	PR	100	50	50%
AWBso	AWB008	ET.882	PR	25	12	48%
AWBsc	AWB003	ET.846	PR	25	12	48%
HITxx	HIT003	ET.887	PR	25	10	40%
GAS	GAS002	ET.839	PR	5	2	40%
LRChm/pa	LRC001 + LRC003	ET.861	PR	5	2	40%
HDPxx	HDP001	TF.828	PR	25	10	40%
AMSps	AMS002	TF.889	PR	50	20	40%
LRCns	LRC008	ET.850	PR	8	3	38%
CMPpo	CMP009	PL.896	PR	25	9	36%
AMPxx	AMP002	TF.890	PR	50	17	34%
RTAsa	RTA001	DI.890	PR	25	8	32%
RTAbp	RTA003	DI.891	PR	25	8	32%
VDFal	VDF013	DI.850	PR	25	8	32%
HITxx	HIT 002	ET.825	PR	25	8	32%
RTAga	RTA005	DI.892	PR	100	25	25%
ADHlt	ADH001	TF.892	PR	100	25	25%
CMPil	CMP011	PL.894	PR	50	5	10%
RTAsa	RTA001	DI.893	PR	25	0	0%
RTAsa	RTA001	DI.X75	PR	25	0	0%

Tool Type	Tool ID	VF Route	BS/PR	F18 Plan	Actual	% of Plan
RTAbp	RTA003	DI.X75	PR	25	0	0%
RTAga	RTA005	DI.X76	PR	25	0	0%
VDFga	VDF002	DI.XA1	PR	25	0	0%
VDFex	VDF024	DI.XA1	PR	25	0	0%
VDFft	VDF026	DI.XB1	PR	50	0	0%
VDFni	VDF003	DI.XN1	PR	100	0	0%
VDFbt	VDF005	DI.XZ1	PR	250	0	0%
VDFte	VDF025	DI.XD2	PR	25	0	0%
AWBbe	AWB013	ET.833	PR	5	0	0%
PLYxx	PLY001	ET.847	PR	25	0	0%
LRCns	LRC008	ET.881	PR	5	0	0%
AWBbe	AWB013	ET.814	PR	75	0	0%
HITxx	HIT 002	ET.890	PR	13	0	0%
LRCns	LRC007	ET.810	PR	10	0	0%
LRCns	LRC007	ET.850	PR	10	0	0%
GAS	GAS003	ET.851	PR	10	0	0%
PPIxx	PPI003	LT.806	PR	100	0	0%
CMPil	CMP011	PL.895	PR	50	0	0%
WSWwt	WSW001	PL.815/pl. 817	PR	15	0	0%
WSWwt	WSW001	PL.803	PR	50	0	0%
NVWxx	NVW001	TF.803	PR	25	0	0%

Average % of Plan for Preprocessed	91%
Stdev	74%

Appendix 4:

Build Ahead Look Up Tool



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