Investigation of Lateral Gated Quantum Devices in Si/SiGe Heterostructures

by

Andrew P. Lai

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Author .....
Department of Physics
May 10, 2013

Certified by .....
Marc A. Kastner
Donner Professor of Physics and Dean of the School of Science
Thesis Supervisor

Accepted by .....
John W. Belcher
Professor and Associate Department Head for Education

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Abstract

Quantum dots in Si/SiGe have long spin decoherence times, due to the low density of nuclear spins and weak coupling between nuclear and electronic spins. Because of this, they are excellent candidates for use as solid state qubits. The initial approach towards creating controllable Si/SiGe quantum dots was to fabricate them in delta doped heterostructures. We provide evidence that the delta doping layer in these heterostructures provides a parallel conduction path, which prevents one from creating controllable quantum dots. Instead, it may be more favorable to supply electrons in the 2DEG through capactive gating, instead of a delta doping layer. We therefore discuss efforts to fabricate Si/SiGe quantum dots from undoped heterostructures and the difficulties encountered. A new method for fabricating ohmics in undoped heterostructures is discussed. We also discuss parallel conduction which occurs in the Si cap layer of these undoped heterostructures, which appears to be a major obstacle towards achieving workable devices in undoped Si/SiGe heterostructures.

Thesis Supervisor: Marc A. Kastner
Title: Donner Professor of Physics and Dean of the School of Science

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Chapter 1

Introduction

In this chapter, we explain the motivation for pursuing this research, followed by a brief review of 2 dimensional electron gases (2DEGs) in semiconductor heterostructures. We cover how lateral quantum dots can be made from a 2DEG, and explain the benefit of using Si/SiGe quantum dots over the more traditional GaAs/AlGaAs quantum dots for qubits. We then explain how the excess spin of Si/SiGe quantum dots can be used as qubits, and the implementation of the needed quantum logic gates to allow for universal quantum computation.

1.1 Motivation

Quantum computers have the potential to revolutionize computing by providing polynomial time solutions for problems once considered intractable in classical computing [1]. For example, through the use of Shor's algorithm, quantum computers can efficiently solve for the prime factors of an integer, a computationally difficult problem

for classical computers [2]. Additionally, quantum computers are significantly more efficient in simulating quantum mechanical systems than classical computers [3]. On a classical computer, the run time of simulating quantum systems scales exponentially with the number of atoms, while on a quantum computer, this time scales polynomially. Many problems in chemistry and solid-state physics, such as the calculation of the energy of a large number of molecules in a chemical reaction, can therefore be computed quickly with a quantum computer. Due to its potential for quickly solving intractable problems in classical computing, there is a significant interest in the realization of a large-scale quantum computer [1, 4].

1.1.1 Quantum Computing

Traditional classical computers store information in bits, which can be one of two states, either a $|0\rangle$ or a $|1\rangle$. Computation on these bits occurs by manipulation with logic gates, which can be implemented through electronic circuits. In contrast, quantum computing stores information in qubits, which are a superposition of two states:

$$|\psi\rangle = a|0\rangle + b|1\rangle \text{ where } |a|^2 + |b|^2 = 1$$

The system of qubits evolves deterministically and its evolution can be described by the time evolution operator, $U(t) = \exp[i \int_0^t H(t')dt']$. This operator is unitary, and the quantum logic gates needed for universal quantum computation can be implemented by manipulating the system Hamiltonian, H (t'). In order to obtain information from the system, a measurement on the qubits must be performed, which breaks

the superposition of the qubit system and brings it to a single state. The outcome of the measurement is random, but the probabilities for each outcome are known in advance. The property of qubits to consist of a superposition of states, combined with the ability to entangle qubits, provide quantum computers with tremendous computation power. One can think of quantum computation as a superposition of classical computing occurring in parallel [5].

1.1.2 Implementing a quantum computer

However, constructing a physical implementation of a quantum computer is a non-trivial problem. While any two-level quantum system in principle can be used as a qubit, there are a number of additional factors that need to be considered for successful quantum computation. First, the qubits must be able to maintain a coherent quantum state for a time long enough to enact the needed quantum gate operations. This requires the qubits to be well isolated from their outside environment. However, in order to enact gate operations, a very high degree of control over the system Hamiltonian is required, meaning that we must have a certain level of accessibility to the quantum system. To further complicate matters, in order to obtain information of the resulting quantum computation, one must perform a measurement of the qubits, which also requires accessibility to the quantum system. Finding and implementing physical systems that have this balance between isolation and accessibility with their surrounding environment can be quite challenging [1].

There are several proposed architectures for quantum computers, such as ion traps

[6], nuclear spins [7], superconducting qubits [8] and optical lattices [9]. Many of these architectures have already been successful in the implementation of a few qubits. However, for these systems, there is uncertainty about whether the architecture would be scalable to large scale quantum computing involving more than 50 qubits. A particular architecture that could be scalable is the use of electron spins in quantum dots [5] . The realization of qubits from quantum dots has additional appeal due to the existing fabrication technologies for quantum dots prevalent in the semiconducting industry.

Quantum dots can be fabricated from semiconductor heterostructures with a 2 dimensional electron gas (2DEG). Confinement to 2 dimensions can be established in the junction(s) of two semiconductors with different band gaps. The 2DEG can be depleted locally using gates on the surface to form a small puddle of electrons. Quantum dots formed through this method are known as lateral quantum dots. At low temperatures, the electrons occupy quantized energy states, and therefore quantum dots can be thought of as "artificial atoms" [10]. Because the spin-1/2 degrees of freedom in the quantum dots are insensitive to fluctuations in the electric potential, they tend to have longer decoherence times than the charge degrees of freedom. Therefore, qubits can be realized from the excess spin in quantum dots and quantum gate operations can applied through spin manipulations achieved with applied magnetic and electric fields [5, 11].

Si/SiGe quantum dots (lateral quantum dots made from a Si/SiGe heterostructure) have particularly long spin relaxation and decoherence times. For comparison, the spin decoherence time in Si/SiGe quantum dots is estimated to be longer by a

factor of 300 than that of Gallium Arsenide quantum dots [12] . Therefore, Si/SiGe quantum dots are a very promising candidate for the realization of qubits [11, 13]. The work done in this thesis was aimed towards achieving controllably Si/SiGe quantum dots that could be used as qubits.

1.2 Two Dimensional Electron Gases

The lateral quantum dots investigated in this research were fabricated from semiconductor heterostructures that contain a two-dimensional electron gas. A two-dimension electron gas (2DEG) is a system where electrons can move freely in two spatial dimensions, but have restricted movement in the third. This confinement is achieved by placing electrons in a quantum well in one of the spatial dimensions, resulting in quantization of the energy levels for motion in that direction. At low temperatures, electrons occupy the ground state of the energy levels, and therefore their motion in that direction is constrained.

1.2.1 2DEG's in semiconductor heterostructures

A quantum well can be created in a semiconductor heterostructure by growing semiconductors with different band gaps next to each other. According to the electron affinity rule, at a heterojunction, the bands of the semiconductors will line up such that their vacuum levels match (1-1). When the semiconductors have different band gaps, there will be discontinuities in the valence and conduction bands at the junctions, allowing one to engineer quantum well structures from these discontinuities.

Electrons for the quantum well/2DEG can be added either through doping, or by applying a positive bias to a metallic gate at the top of the heterostructure.

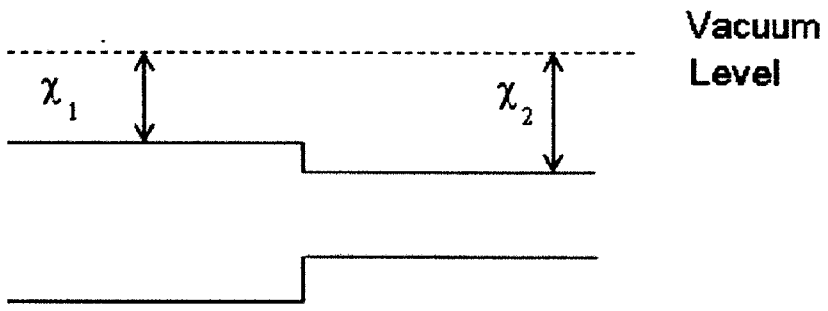

Figure 1-1: Here, we have two semiconductors with different band gaps. At the heterojunction, the conductance and valence bands will line up such that the vacuum levels of both semiconductors match, resulting in a discontinuity for both bands. In this figure, χ_1, and χ_2 are the electron affinities of each semiconductor.

In the situation where electrons in the 2DEG are supplied through doping, it is advantageous to spatially separate ionized electrons from their donors. This will reduce scattering of electrons from ionized donors, resulting in higher 2DEG mobility. Spatial separation of ions from donors can be achieved through a process known as modulation doping [14]. In modulation doping, dopants are added to a small region of the heterostructures, and a spacer layer of undoped material exists between the doped region and the 2DEG. For optimal increases in mobility, it is best to add doping in a localized layer that is close to only one atom in thickness, a process known as delta doping [15]. With delta doping, all the ionized dopants are now in a very concentrated region far from the 2DEG, resulting in little scattering of electrons with ionized donors, and therefore higher 2DEG mobility. With modulation/delta doping, one has to be cautious about adding too many donors, as a parallel conduction channel

to the quantum well can be created if this happens.

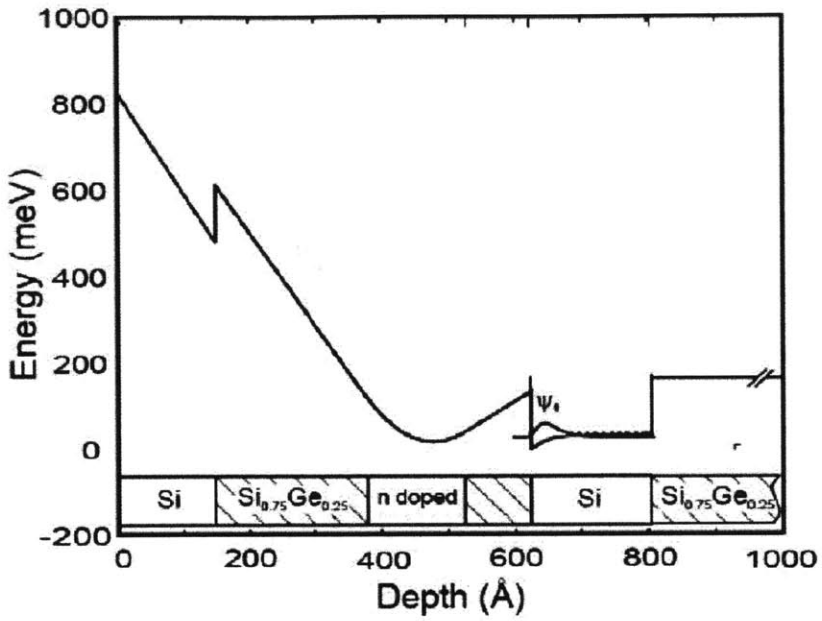

Figure 1-2: The electronic band structure of a modulation doped Si/SiGe heterostructure. The quantum well is at depth of 600 - 800 A, and the doping occurs between 400-500 A. Note that there is a dip in the electronic band structure around the doping. If the doping concentration is too high, a parallel conduction band can occur here. Image taken from reference[16]

One can also induce a 2DEG in a heterostructure without using intentional doping [17]. By adding a metallic top gate to the surface of the heterostructure and adding a positive bias, an electric field pointing towards the top gate is created. At a large enough bias, the semiconductor bands will bend such that the Fermi level of the system is above the quantum well, but below the energies of the bands neighboring the well. When this occurs, there will be a 2DEG in the quantum well. The advantage of a system where the 2DEG is induced capacitively by a top gate is that it allows one to easily control the density of the 2DEG. Additionally, it allows one to remove

donor layers from the heterostructure, removing scattering from ionized dopants, and the possibility of a parallel conduction channel forming in a donor layer.

The most common heterostructure used to study 2DEG's is the GaAs/AlGaAs heterostructure. This is due to the fact that GaAs/AlGaAs 2DEGs have the highest measured 2DEG mobilities, upwards to 20,000,000 V / (cm * s). However, there is significant interest in 2DEG's created from Si/SiGe heterostructures, largely in part due to higher mobilities than purely silicon structures, and compatibility with silicon processing.

The 2DEG samples studied in for the research in this thesis are Si/SiGe heterostructures, with a Si quantum well in between SiGe layers containing 20 % Ge. The heterostructure was grown through molecular beam epitaxy. For samples with dopants, delta doping with antimony (Sb) donors is added in the top SiGe layer. These excess electrons from the donors fall into the Si quantum well, where band bending from the donors and their ionized atoms, and band discontinuities from the different band gaps of the semiconductors trap the electrons in the quantum well. For the undoped heterostructures, a Ti/Au top gate deposited at the top of the heterostructure is used instead to supply electrons into the quantum well.

1.2.2 Quantum Hall Effect

When studying 2DEGs and nanoscale devices fabricated from them, it is useful to have techniques to characterize their properties. A convenient way to measure the density and mobility of a material is through a phenomenon known as the Hall effect.

In the Hall effect, a magnetic field is applied in a direction perpendicular to the current flow in a conducting material (1-3). The Lorentz force acting on the electrons is:

$$\vec{F} = q\vec{v} \times \vec{B} + q\vec{E} \tag{1.1}$$

If we have for our current $\vec{I} = nevL_xL_y\hat{x}$ and $\vec{B} = B\hat{z}$ in the steady state with $\vec{F}$ we have:

$$E\hat{y} = vBy \implies V_{\text{Hall}} = vL_yB = \frac{IB}{neL_z}$$

This is a transverse voltage, known as the Hall voltage, which develops in the y direction. The hall resistance is:

$$R_{\text{Hall}} = \frac{V_{\text{Hall}}}{I} = \frac{B}{L_zne} \tag{1.2}$$

In a 2DEG, our density is $L_zn = n_{2DEG}$ and therefore we have $R_{\text{Hall}} = \frac{B}{n_{2DEG}e}$. By measuring the hall resistance, one can plot it as a function of the magnetic field, and extract the electron density from the slope of the resulting plot.

When a magnetic field is applied perpendicular to a 2DEG, at sufficiently high magnetic fields and low temperatures an interesting phenomenon known as the Quantum Hall Effect can be observed. One can get a sense of what happens by considering the Hamiltonian of an electron confined to 2 dimensions in a magnetic field. We are free to choose the gauge of the field, so in this case, we choose $A = \langle 0, Bx, 0\rangle$ For our Hamiltonian, we have:

$$\hat{H} = \frac{\hat{p}_x^2}{2m} + \frac{(\hat{p}_y - \frac{qBx}{c})^2}{2m} \tag{1.3}$$

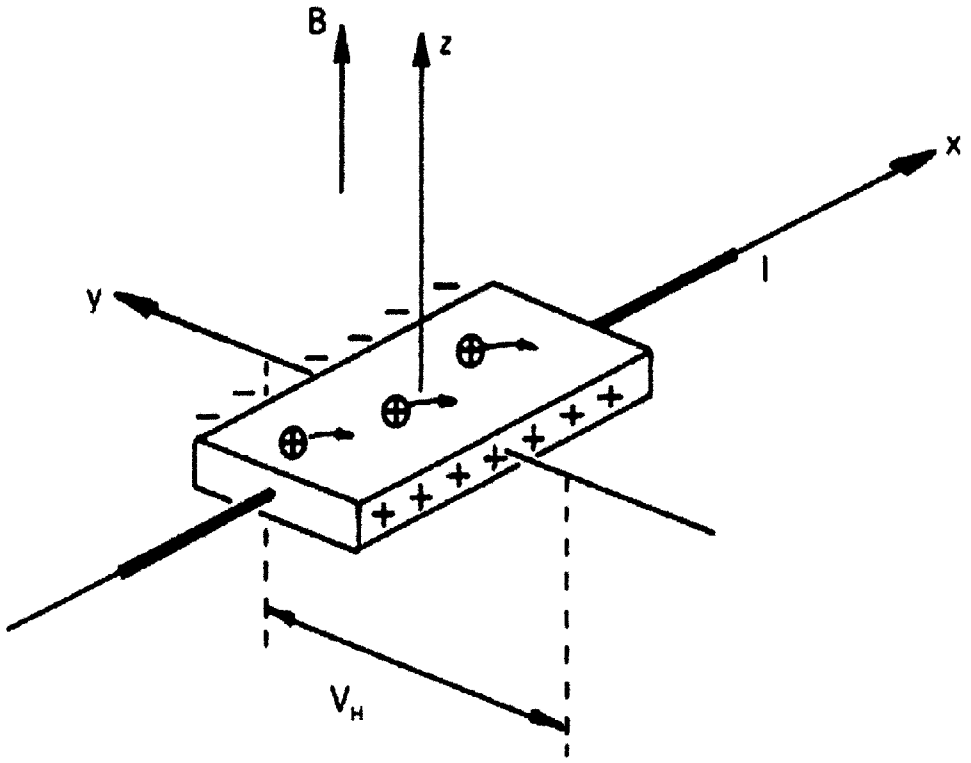

Figure 1-3: Classical Hall Effect. A current is passed through the sample, with a magnetic field perpendicular to the current. Due to the Lorentz force from the magnetic field, a voltage transverse to both the current and the field develops, known as the Hall Voltage. Figure taken from reference [18]

The p_y operator commutes with the overall Hamiltonian, so we can replace it with its eigenvalues:

$$\hat{H} = \frac{\hat{p}_x^2}{2m} + \frac{1}{2}m{\omega_c}^2\left(x - \frac{\hbar k_y}{m\omega_c}\right)^2 \tag{1.4}$$

This is simply the quantum harmonic oscillator problem, with cyclotron frequency of $\omega_c = eB/mc$, and the oscillators centered at $\hbar k_y/m\omega_c$. The eigenstates of our Hamiltonian are of the form:

$$\Psi_{j,k_y}(x,y) = e^{ik_y y}\phi_j(x - x_o) \tag{1.5}$$

where ϕ_j are the normalized eigenstates of the harmonic oscillator. The eigenenergies of our system are $E_j = \hbar\omega_c(j + 1/2)$. Therefore, we can see that the electrons now occupy discrete energy levels, called Landau levels, and we can no longer describe our Hall effect classically. We can estimate the degeneracy of each Landau level as follows. Assuming that we have periodic boundary conditions, we have for our allowed values,

$$k_y = \frac{2\pi m}{L_y}, \text{ where m is an integer}$$

Now, assuming x_o must lie within the system, we have:

$$0 < x_o < L_x \text{which means that } 0 < m < \frac{L_x L_y eB}{hc} \tag{1.6}$$

Therefore, the degeneracy per unit area of each Landau level is B/ϕ_o, where $\phi_o = hc/e$ is the flux quantum.

Semi-classically, one can imagine that as the magnetic field is increased, electrons in the 2DEG become increasingly localized as they coalesce into discrete orbits/landau levels. Eventually, the orbits of the electrons in the bulk are completely localized, and the only conduction of the system occurs along the edges. The number of conduction channels on the edges corresponds to the number of Landau levels filled. Because the propagation is now along the edges, the conduction in the system occurs through one-dimensional channels. Therefore, when the hall conductance is plotted as a function of magnetic field, instead of a straight line, there are now hall plateaus, which occur at integer multiples of e^2/h or $\nu e^2/h$ where ν is an integer known as the filling factor. Because the conduction is occurring in one-dimensional channels and the direction of propagation is opposite on opposite sides of the sample, there is no back-scattering and zero longitudinal resistance. Therefore, the longitudinal resistance drops to zero whenever there is a hall plateau.

At high enough magnetic fields, and samples with very high electron mobility, fractional values of the filling factor, ν, are observed. This phenomenon is known as the fractional quantum Hall effect, and it can be described by taking into account electron-electron interactions, which was previously ignored in our derivation of the integer quantum Hall effect. One can think of the fractional quantum Hall effect as the integer quantum Hall effect for composite fermions, which are quasiparticles formed from electrons and magnetic flux quanta [19].

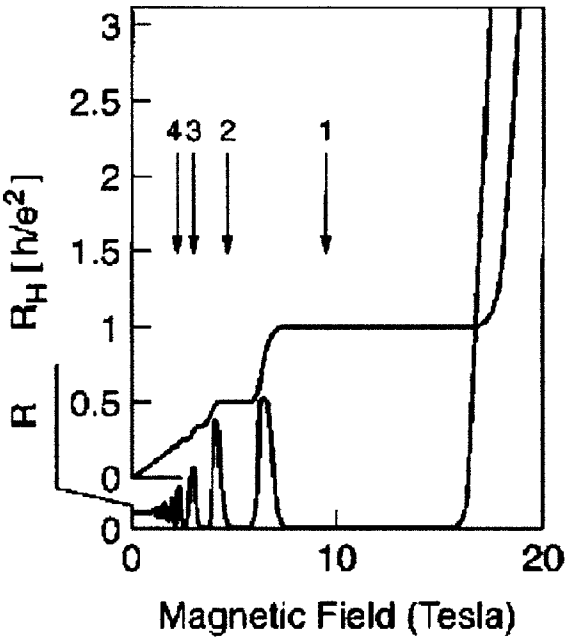

Figure 1-4: Example of the integer quantum hall effect. Here, we can see the plateaus in the hall resistance, each corresponding to the number of landau levels filled. Note that the longitudinal resistance drops to zero at each of the hall plateaus. Figure taken from reference [18]

1.3 Lateral Quantum Dots

By placing metallic gates on top of the 2DEG heterostructure, and applying a negative bias on these gates, one can deplete the electrons in the 2DEG underneath the gates. With appropriate gate placement, one can isolate electrons in the 2DEG into a local puddle and effectively confine the electrons in all three spatial dimensions. Such a device is known as a lateral quantum dot. One can achieve a fine enough level of control over the number of electrons in the puddle to the point where only one electron at a time is removed or added. The energy scales that we use to study lateral quantum dots cannot be resolved at room temperatures. For example, the energy needed to add an electron to a quantum dot, the charging energy $U \sim \frac{e^2}{c}$ is around 1 meV for a dot with dimensions around 0.5 microns. This roughly corresponds to a temperature of 10 K. Additionally, the energy relaxation times and decoherence times are thought to increase in duration at sub-kelvin temperatures. Such low temperatures can be reached with a He_3 fridge or a dilution refrigerator.

1.3.1 Coulomb Blockade

To see how we can achieve a fine enough control of a quantum dot to where we can add/remove one electron at a time, we can treat the lateral gates, source and drain as a system of capacitances between the dot and the environment [20] . The total energy of our dot is the sum of the electrostatic energy, interaction energy and energy from the discrete energy levels. Let us first calculate the electrostatic energy. In a quantum dot, there is a capacitance between the dot, and each gate. We can use the

superposition principle by first considering V_{dot} when all but one of the capacitances, C_i, are grounded. In this situation, the capacitance network acts as a voltage divider, and we have:

$$V_{\text{dot}} = \frac{C_i}{\sum C_i} V_i$$

Therefore if we have a voltage applied to each gate, we have, for the electrostatic energy of the dot:

$$E = -NeV_{\text{dot}} = -Ne\sum \alpha_i V_i \tag{1.7}$$

where N is the number of electrons in the dot, and $\alpha_i = C_i / \sum C_i$. The interaction energy of the dot is:

$$E_i = \sum_{i=1}^{N} e\phi_i \tag{1.8}$$

With $\phi_i = -\frac{e(i-1)}{\sum C_i}$ being the electrostatic potential between the ith electro, and the previous i - 1 electrons added to the system, this give us:

$$E_i = \frac{e^2}{\sum C_i} \sum_{i=1}^{N} i - 1 = \frac{e^2 N(N-1)}{\sum C_i} \tag{1.9}$$

Finally, E_{QM} will be:

$$E_i = \sum_{i=1}^{N} \epsilon_i$$

where ϵ_i is the energy of an electron occupying the ith energy level. Therefore, we have:

$$E(N) = -Ne\sum \alpha_i V_i + \frac{e^2 N(N-1)}{\sum C_i} + \sum_{i=1}^{N} \epsilon_i \tag{1.10}$$

Now, let us consider the electrochemical potential of the dot, which is $\mu_{\text{dot}}(N) = E(N) - E(N-1)$. From 1.10, we get:

$$\mu_{\text{dot}}(N) = -e\sum \alpha_i V_i + \frac{e^2(N-1)}{\sum C_i} + \epsilon_N \tag{1.11}$$

The value of N will be such that $\mu_{\text{dot}}(N)$ is less than μ_{source} and μ_{drain}. For now, let us consider the situation where $\mu_{\text{source}} = \mu_{\text{drain}} = 0$. When $\mu_{\text{dot}}(N+1) > 0$ there will be no conduction across the quantum dot. However, if we increase the voltage on one of the gates, we can see that this reduces the value of $\mu_{\text{dot}}(N+1)$ and eventually we will reach a point where $\mu_{\text{dot}}(N+1) = 0$. By definition, this means that $E(N+1) = E(N)$, and therefore electrons can hop on and off the dot without a change in the total quantum dot energy. In this case, conduction is allowed across the dot, and we have a conduction peak. If we increase the gate voltage, $\mu_{\text{dot}}(N+1)$ will drop below 0, and again we have no conduction. From this, we can see that there will be conduction peaks whenever $\mu_{\text{dot}}(N+1)$ lines up with $\mu_{\text{source}} = \mu_{\text{drain}} = 0$. These conductance peaks as a function of gate voltage are known as coulomb blockade oscillations.

Now, let us consider the situation when $\mu_{\text{source}} \neq \mu_{\text{drain}}$. In this situation, conductance can occur whenever μ_{dot} is between μ_{source} and μ_{drain}. Therefore, if we plot the differential conductance as a function of μ_{dot} and μ_{source} (with $\mu_{\text{drain}} = 0$)), we will end up observing diamond shaped conductance patterns (1-6).

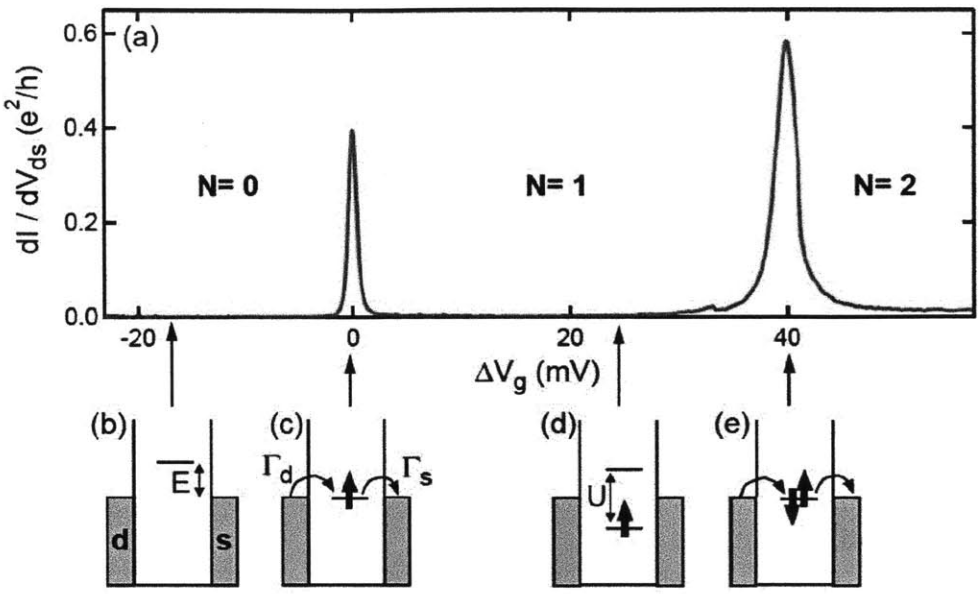

Figure 1-5: An example of coulomb blockade in a quantum dot. Conductance is plotted as a function of gate voltage, with $V_{\text{source}} = V_{\text{drain}}$. Image taken from reference [21]

1.3.2 Spin physics of quantum dots

Due to the fact that spin fluctuations in a quantum dot are much more stable than charge fluctuations, the excess spin of the dot is the best candidate to use as a qubit. Additionally, the spin state of a quantum dot is already a two-level system, with $\Delta E = g\mu_B B$. There are two main limiting factors to how long the spin state can be maintained. The first is the energy-relaxation time, T_1, which is the time it takes an excited spin state to relax back to its ground state. The second is the decoherence time, T_2, which is how long the phase of the spin state can be preserved.

There will always be a nonzero overlap between the wave functions of the electrons and nuclei. In particular, hyperfine coupling, which is the interaction between the

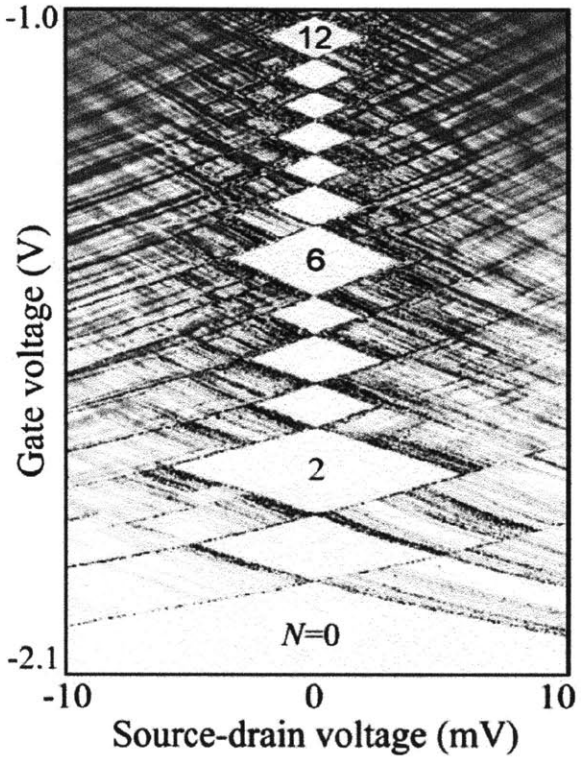

Figure 1-6: An example of coulomb blockade diamonds. The diamonds in the center each correspond to having a discrete number of electrons in the dot, with N=0 for the diamond at the bottom, and N=12 for the diamond at the top. Image taken from reference [22]

spin and nuclear magnetic moments, has the effect of reducing both T_1 and T_2. Additionally, spin-orbit coupling, which causes the spin and orbital states to be mixed, also has the effect of reducing T_1 and T_2.

1.3.3 Advantages of Si dots over GaAs dots

The wavefunctions of electrons in GaAs have a large overlap with those of the nuclei, resulting in a strong hyperfine coupling. This hyperfine coupling causes both spin relaxation and decoherence. In comparison, there is significantly less overlap between the wavefunctions of electrons and nuclei for Si/SiGe quantum dots, and a much lower concentration of magnetic nuclei (in principle, isotropically pure Si can be used). Both of these factors result in much longer T_1 and T_2 times for Si/SiGe quantum dots. It is estimated that the T_2 time in Si/SiGe quantum dots is around 300 times longer than the T_2 time of GaAs quantum dots [12]. In principle, it would be possible to use isotropically pure Si for the quantum well, further increasing the T_2 time.

1.3.4 Implementation of quantum computation from spin

For universal quantum computation, we will need a method for implementing the XOR gate, and single qubit operations. One potential implementation would involve the use of excess electron spin of the quantum dot as the qubit. Two qubit operations could then be applied through electrostatic gating of the tunnel barrier between quantum dots [5]. If we implement a low voltage pulse for our electrostatic gating, according to the Hubbard Model [23], there will be a transient Heisenberg coupling

as follows:

$$H_s(t) = J(t)\vec{S}_1 \cdot \vec{S}_2 \tag{1.12}$$

where $J(t) = 4t_o{}^2(t)/u$, the time-dependent exchange constant can be controlled by turning on and off the tunneling matrix element $t_o(t)$. If we apply our pulse duration such that: [5]

$$\int J(t)dt = J_o\tau = \pi \mathrm{mod}(2\pi) \tag{1.13}$$

with our time evolution operator, $U(t) = exp[i\int_0^t H(t')dt']$, we end up with:

$$U(t_1) = \exp\left[i\pi\vec{S}_1 \cdot \vec{S}_2\right] = \exp\left[i\pi(S_{1z}S_{2z} + S_{1x}S_{2x} + S_{1y}S_{2y})\right] \tag{1.14}$$

This turns out to be:

$$U(t_1) = \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{pmatrix} \tag{1.15}$$

which is the SWAP gate operation. If we apply the pulse, t_1, for half its duration, we can perform the $\sqrt{\mathrm{SWAP}}$ operation. We can achieve single quit manipulations by local magnetic field manipulation (perhaps with a scanning tip probe). Through the technique of electron spin resonance (ESR), an oscillating B field is applied for a duration sufficient to create any superposition of $|\uparrow\rangle$ and $|\downarrow\rangle$. Therefore, with single qubit operations and the $\sqrt{\mathrm{SWAP}}$ operation, we can perform the XOR gate operation

as follows: [5]

$$U_{XOR} = \exp[\frac{i\pi S_{1z}}{2}] \exp[-\frac{i\pi S_{2z}}{2}] U_{\sqrt{\text{SWAP}}} \exp[i\pi S_{1z}] U_{\sqrt{\text{SWAP}}} \tag{1.16}$$

From the XOR gate and single qubit manipulations, we would have the ability to perform universal quantum computation. Therefore, quantum computing in quantum dots could potentially be implemented through electrostatic gating of the tunnel barrier, and magnetic field pulses acting on the qubits. (Figure 1-7)

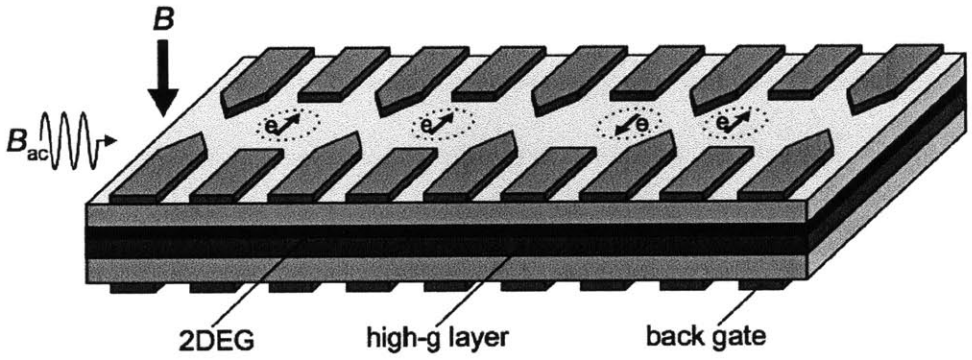

Figure 1-7: The implementation of a quantum computer using the spin of quantum dots. Here, lateral gates are used to deplete the 2DEG underneath, forming quantum dots. Electrical pulses are applied on the tunnel barrier of between each dots for two-qubit operations, while a pulsing magnetic field B is used to perform single qubit operations. Figure from [24]

Chapter 2

Experimental Methods

In this chapter, we briefly cover the experimental methods used in this research. Section 2.1 discusses the heterostructures used for the devices and the methods of fabrication that went into creating the devices. Section 2.2 discusses the low temperature systems that were used when characterizing the devices.

2.1 Fabrication Methods

The heterostructures used to fabricate the devices studied in this thesis were grown at UCLA by the research group of Professor Ya-Hong Xie. The heterostructures were grown through the use of molecular beam epitaxxy. They consist of a thin Si cap layer around 4-5 nm on the surface, followed by 40-45 nm spacer layer $Si_{0.8}Ge_{0.2}$, a 10 nm Si quantum well, another layer of $Si_{0.8}Ge_{0.2}$, and a SiGe graded buffer grown on top of a Si substrate (2-1). For heterostructures where electrons in the Si quantum well are supplied through doping, there is a delta doping layer of Sb atoms around in

the middle of the SiGe spacer layer.

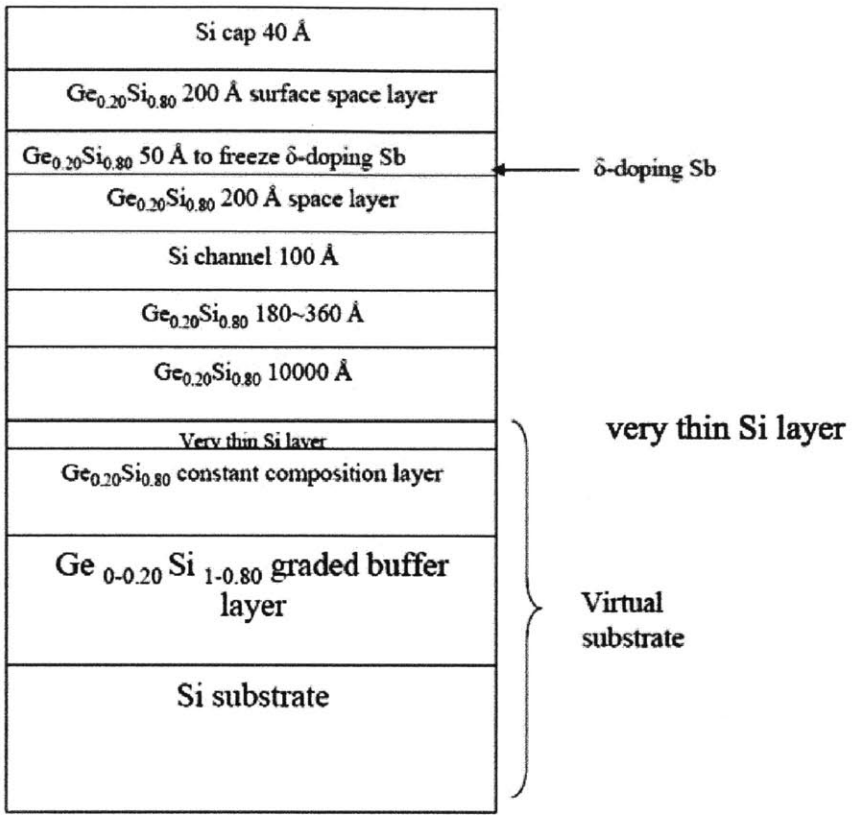

Figure 2-1: An example of a doped Si/SiGe heterostructure. This particular sample was grown by the research group of Professor Ya-Hong Xie. The undoped heterostructures used in this research were similar to the one above, but without a delta doping layer in the spacer SiGe layer above the Si quantum well. Figure taken from [12]

For our devices, we performed patterning of our ohmics, gates, etc through photolithography or e-beam lithography.

2.1.1 Photolithography

Photolithography was used for the patterning of the ohmics, mesa, and large gates. It involves the depositing of photoresist, often by spinning it on a coater for uniform

deposition. The thickness of the deposited photoresist is dependent on the angular velocity of the coater. There are two types of photoresist used, positive resist and negative resist. With positive resist, the regions that are exposed to UV light become soluble in a developer. In the case of negative resist, the regions that are not exposed to the UV light are soluble in the developer. Positive resist was used to pattern the mesa, and negative resist was used to pattern the ohmics, and larger gates.

2.1.2 E-beam lithography

For features which required higher resolution, such as our small gates, e-beam lithography was used to define the patterns. Since UV light has a diffraction limit, we are limited to defining patterns at the smallest sizes of around a few hundred nanometers with photolithography. Therefore, for smaller features, it is preferable to use E-beam lithography. E-beam lithography works by emitting a beam of electrons at regions of photoresist, where either exposed or non-exposed regions are removed with a developer. For the patterning of small gates, we used a positive e-beam resist, so exposed regions are removed with a developer.

2.1.3 Overall outline of fabrication procedure

The devices are made on Si/SiGe samples of size 0.5 mm by 0.5 mm, which are cleaved using the scriber at the Harvard cleanroom. Each sample contains multiple devices, which are electrically isolated in mesas. The mesas are pattered with photolithography and 100 nm of the heterostructure from the surface is etched with reactive ion

etching. For devices fabricated from the doped heterostructures, electrical contacts to the 2DEG are patterned with photolithography, and through e-beam evaporation, 295 nm of Au/Sb is deposited onto the surface. The device is then annealed at 325 C for 5 minutes. E-beam lithography is used to pattern the small gates, and 5/20 nm of Cr/Au is evaporated onto the surface with E-beam evaporation. Finally, connector gates to the small gates are patterned with photolithography, and 20 nm / 120 nm Cr/Au is deposited on the surface with E-beam evaporation. The final sample is then glued onto a sample holder with PMMA, and aluminum wires are used to make electrical connection between electrodes on the sample and the sample holder.

For devices fabricated on undoped Si/SiGe heterostructures, there are additional fabrication steps that have been added to the procedure. Since the 2DEG is induced through the use of a top gate, this top gate must be electrically isolated from the lateral side gates. This is accomplished by depositing a 100 nm thick layer of aluminum oxide through atomic layer deposition (ALD) on the surface of heterostructure. After the ALD deposition, a top gate is patterned with photolithography, and 5 nm/295 nm Ti/Au is deposited through e-beam evaporation. However, the addition of an aluminum oxide layer and metallic top gate were not the only alterations to the recipe that are made. When fabricating devices from undoped heterostructures, ohmics made with the Sb/Au recipe used in the doped devices ended up being very spiky in topography and would poke through the ALD aluminum oxide layer. This leads to a direct conduction path between the ohmics and the top gate, therefore causing leakage. To remedy this, the ohmic contacts are instead fabricated through ion implantation. Phosphorous ion implants are added at 40 keV, at a concentration of

$2 \cdot 10^15$ per cm^2, and after ion implantation, the device is annealed at 600 C for 30 minutes. Contact pads to the ohmic contacts have been patterned with photolithography, and 200 nm of aluminum is deposited with E-beam evaporation. This new recipe for the ohmics was successful in eliminating leakage between the metallic top gate and ohmics.

For a more detailed fabrication procedure, look at Appendix A.

2.2 Low Temperature Systems

The experiments done for the research related to this thesis were conducted at temperatures of 4K or 300 mK, using either flow through cryostats or a He^3 refrigerator. The operation of a flow-through cryostat is quite simple. The device is attached and wire bonded to a sample holder, mounted onto an inset, which is loaded into a cryostat. The cryostat is connected with a transfer rod to a Helium dewar. The warm transfer rod boils off helium in the dewar, pressurizing the system, and eventually forcing liquid helium to flow from the dewar, through the transfer rod, and into the cryostat. The flow through cryostat system is capable of reaching temperatures of 4K, which is the temperature of liquid helium, and was used whenever simple conductance measurements of the devices were needed.

Whenever magnetic field measurements and/or lower temperatures were needed, the He^3 refrigerator would be used. The He^3 system is capable of reaching 300 mK, and has a magnet which can reach B fields of up to 8 T. The cooling mechanism of the He^3 system is the evaporating of liquid He^3. One can reach lower temperatures

from He^3 cooling as compared to He^4 cooling, because He^3 has a much larger vapor pressure and a larger specific heat when its temperature is less than 1.5 K [25]. The operation of a He^3 fridge is more involved than the cryostat, but nonetheless not too complicated. Once again, the sample is attached and wire bonded to a sample holder, mounted onto the He^3 inset, which is then lowered into a dewar. Liquid nitrogen is transferred into the dewar to bring the system to 77 K, and liquid helium is transferred to bring the He^3 inset to 4 K. The 1K pot is then pumped on with a vacuum, while a little bit of He^4 is allowed to enter it. The pumping action causes the 1K pot and its surroundings to reach temperatures of around 1.5 K. The sorb is then heated to 40 K so that it does not absorb any helium, and as the He^3 gas travels through the 1K pot, it liquefies, and condenses. The sorb is cooled back down to 4 K, and therefore starts to pump on the He^3. The evaporation of the He^3 brings the He^3 chamber temperature down to 0.3 K, and this temperature can be maintained for about 10 hours. If further time is needed continue operation at 0.3 K, the He^3 can be re-condensed by heating the sorb to 40K.

Chapter 3

Characterization of lateral gated quantum devices in doped Si/SiGe heterostructures

In this chapter, we discuss characterization of lateral gated quantum devices in Si/SiGe heterostructures with single layer delta doping. To better understand the difficulties delta doping causes in fabricating controllable quantum dots, we fabricate a set of quantum point contacts on a heterostructure with low doping concentration. We carry out conductance and capacitance measurements on the device and fit the data with a simple circuit model. From our results, we conclude that there is a parallel conduction channel, most likely the delta doping layer itself, which is responsible for the difficulty in creating controllable Si/SiGe quantum dots.

The results in this chapter have been published as:

"The effect of surface conductance on lateral gated quantum devices in Si/SiGe heterostructures", Xi Lin, Jingshi Hu, **Andrew P. Lai**, Zhenning Zhang, Kenneth MacLean, Colin Dillard, Ya-Hong Xie, and Marc A. Kast- ner, J. Appl. Phys. 110, 023712 (2011) [26].

3.1 Difficulties in fabricating Si dots from delta-doped heterostructures

In this section, we discuss difficulties encountered in fabricating controllable lateral quantum dots with a doped Si/SiGe heterostructure. The Si/SiGe heterostructure consists of a 10 nm Si quantum well sandwiched between SiGe layers. The SiGe layers contain 20 % Ge and are relaxed, having been grown epitaxially on a graded, relaxed SiGe buffer. The 2DEG residing in the quantum well is 50 nm beneath the surface, and the electrons are provided by the delta doping layer of Sb. Devices are fabricated on mesas created through reactive ion etching in order to provide electrically isolation from one another. To make electrical contact to the 2DEG, an ohmic pattern is defined photolithographically, and Au/Sb is deposited on the surface through e-beam evaporation. Afterwards, the device is annealed at 325 C for 5 minutes. Lateral metallic gates are patterned through e-beam lithography, and 5/15 nm of Ti/Au is deposited on the surface through e-beam evaporation.

In most cases, when a negative bias is added to the lateral gates of the quantum dots to deplete the underlying 2DEG, the resulting dots become completely insulating.

This means that the 2DEG is the region of the quantum dot has become completely depleted, and the lateral gates have a much larger depletion range than intended. A possible explanation for this is that a parallel conducting layer is forming in the Sb delta doping layer.

Additionally, there appears to be significant telegraph noise, also possibly from the Sb delta doping layer, which could interfere with the observation of coulomb blockade. Figure 3-1 depicts a device made from a sample with electron density of 4.0×10^{11} cm^{-2} and doping concentration of 2×10^{12} cm^{-2}. The doping density of this sample is particularly chosen to be fairly low. Measurements of this sample were taken in a He_3 refrigerator, at a temperature of 0.4 K. For a preliminary charge motion measurement, a quantum point contact (QPC) is made on this device by applying a negative bias to the highlighted gates in Figure 3-1. QPCs are excellent probes of charge motion as they are highly sensitive to their surrounding electrostatic environment. The conductance through the QPC is then measured as a function of the bias on the QPC's gates. The conductance is a two-lead measurement between a pair of ohmics on either side of the QPC, and a current with an AC excitation voltage of 92 μV and a frequency of 103 Hz is used. A pinch off profile measuring conductance through the QPC as bias on the QPCs increased is obtained. The bias is then set to -1.3 V, while the DC current through the QPC is measured. As see in (Figure 3-1b), there are jumps in the conductance due to telegraph noise. The conductance change in these jumps when compared to the pinch off profile, however, occur with a corresponding voltage of 200 mV (Figure 3-1a). This is 10 times the magnitude of the expected coulomb blockade peaks of a quantum dot of similar size. Therefore,

in order for the QPC to accurately measure charge motion, the quantum dot would have to be 10 times smaller, sizes which would be rather difficult to fabricate with current lithographic technologies.

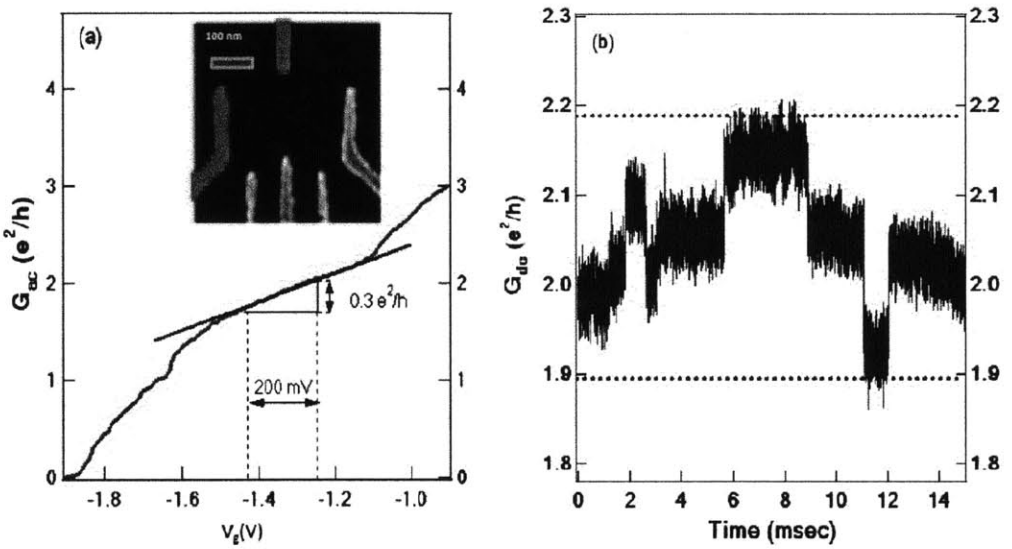

Figure 3-1: a) Conductance through the channel, with negative bias applied to a pair of gates, forming a QPC. (b) Telegraph noise of magnitude 0.3 e2/h. measured at Vg = -1.3 V, with a bandwidth from 0 - 300 kHz. Figure taken from [26]

3.2 Capacitance Measurements

In order to measure how large of a region of the 2DEG the surface gates were depleting, a device with the geometry depicted in 3-2 was fabricated. The device contains QPCs of various constriction sizes ranging from 3 μm to 10 μm, all of which are larger than that those in previous samples where we attempted to fabricate quantum dots. The electron density and mobility of the sample are 2.0×10^{11} cm^{-2} and

2.2×10^4 cm$^2/V * s$, with a doping concentration of 3×10^{11} cm^{-2}. The doping concentration of this sample was purposely chosen to be lower than the previous samples in which we attempted to fabricate quantum dots. Initial two-lead conductance measurements were taken between ohmics on opposite sides of the gate structures, using an AC excitation of 92 μV and a frequency of 130 Hz. It was found that applying a bias of around -6 V to any pair of gates would cause this conductance to drop to zero. Upon further investigation, it was discovered that this negative bias needed to be applied to only a single gate in order to turn off conductance between the ohmics. This vanishing conductance means that the gate is not only depleting the 2DEG region directly underneath it, but also the narrowest region of the 2DEG at the very least. In order for this to happen, the gates would have to have to be depleting a region of at least 30 μm in diameter, which is a very large area. Such a large range depletion, however, makes it clear why it was difficult to create quantum dots in doped heterostructures in the first place. The cause for this unintended depletion is possibly leakage from the gate to a conducting layer parallel to the 2DEG. Various attempts were made to measure the leakage between this layer and the surface gates, but they were unsuccessful. The likeliest candidate for this parallel conducting layer is the delta doping Sb layer.

In addition to conductance measurements between ohmics, capacitance measurements between gate 2 (inset in Figure 3-2) and an ohmic connected to the underlying 2DEG are also made. The measurements were taken with frequency of 130 Hz and an AC excitation of 92 microV, while a negative DC bias is applied to the gate. The capacitance is calculated as the imaginary component of the measured AC current

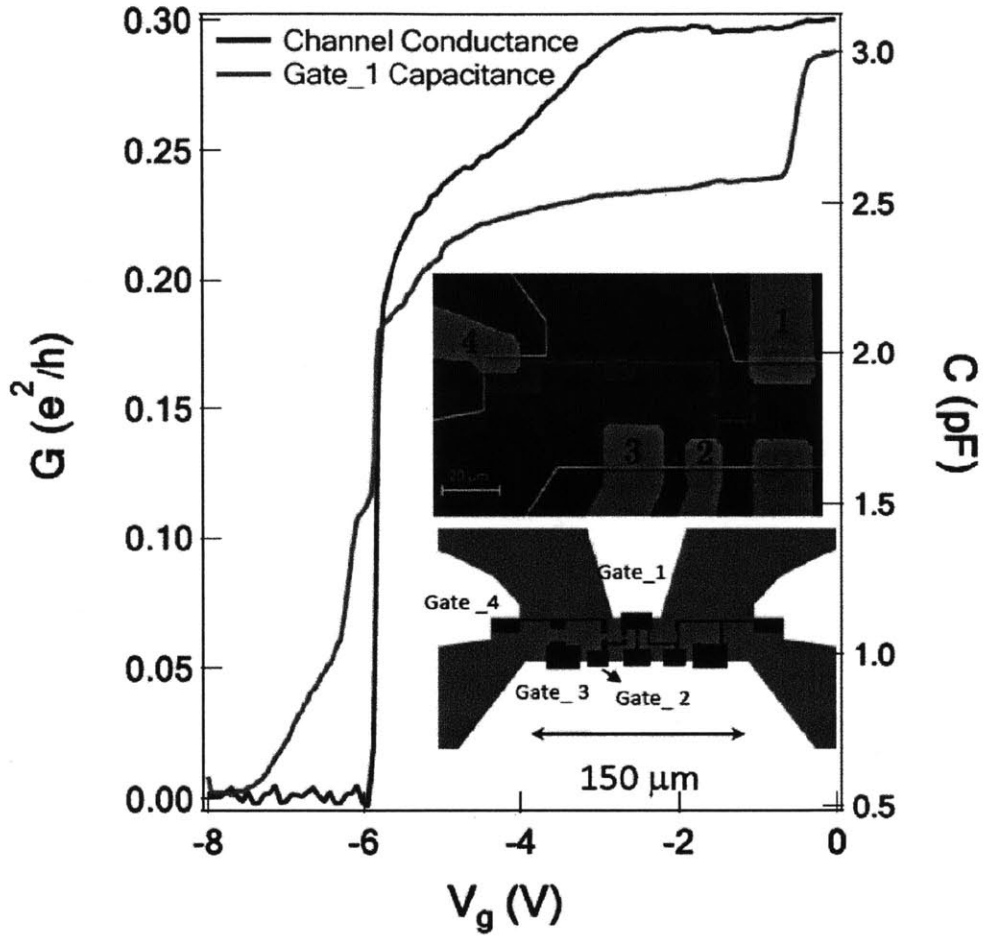

Figure 3-2: a) A negative DC bias is applied to gate 2, and the capacitance of the gate with the underlying 2DEG, and the conductance of the 2DEG are measured. An initial drop in the capacitance occurs at around Vg = -0.4 V, and this drop is equal to the theoretically calculated capacitance of gate 2. As the negative bias is increased in magnitude, around -6 V, both the capacitance and conductance drop to zero, indicating that the 2DEG has been completely depleted. Figure taken from [26]

normalized with frequency and excitation voltage. The expected capacitance between gate 2 and the 2DEG is 0.3 pF. However, from Figure 3-2, we can see that at Vg = 0, the capacitance is around 2.8 pF. This indicates that there is another source of capacitance in the system, perhaps involving the delta doping layer. As the magnitude of the DC bias increases and approaches -1 V, a sizable drop in the capacitance occurs. The value of this capacitance drop is 0.31 pF, which matches up quite nicely with the expected capacitance of 0.3 pF for gate 2. This drop seems to indicate that as the DC bias is approaches -1 V, the 2DEG directly underneath the gate is depleted, and the system is left with the background capacitance of 2.5 pF. There is little change to this background capacitance as the magnitude of the DC bias is increased further, until at Vg = -6 V, when the entire capacitance and conductance of the system drops to zero. This corresponds to complete depletion of the 2DEG in a large region surrounding gate 2, as the source of the background capacitance is removed.

3.2.1 Circuit Fitting

To further characterize the device and attempt to figure out the source of the background capacitance, measurements were taken of the current with the DC bias varied from 0 to -1 V and AC frequencies varied from 130 to 9700 Hz. DC biases below -1 V were avoided, due to the fact that there is significant hysteresis in the device beyond that voltage. As seen in Figure 3-5, as the frequency of the AC current is increased, the real component of the measured current increases, while the imaginary component normalized with frequency and voltage decreases. A system which exhibits such

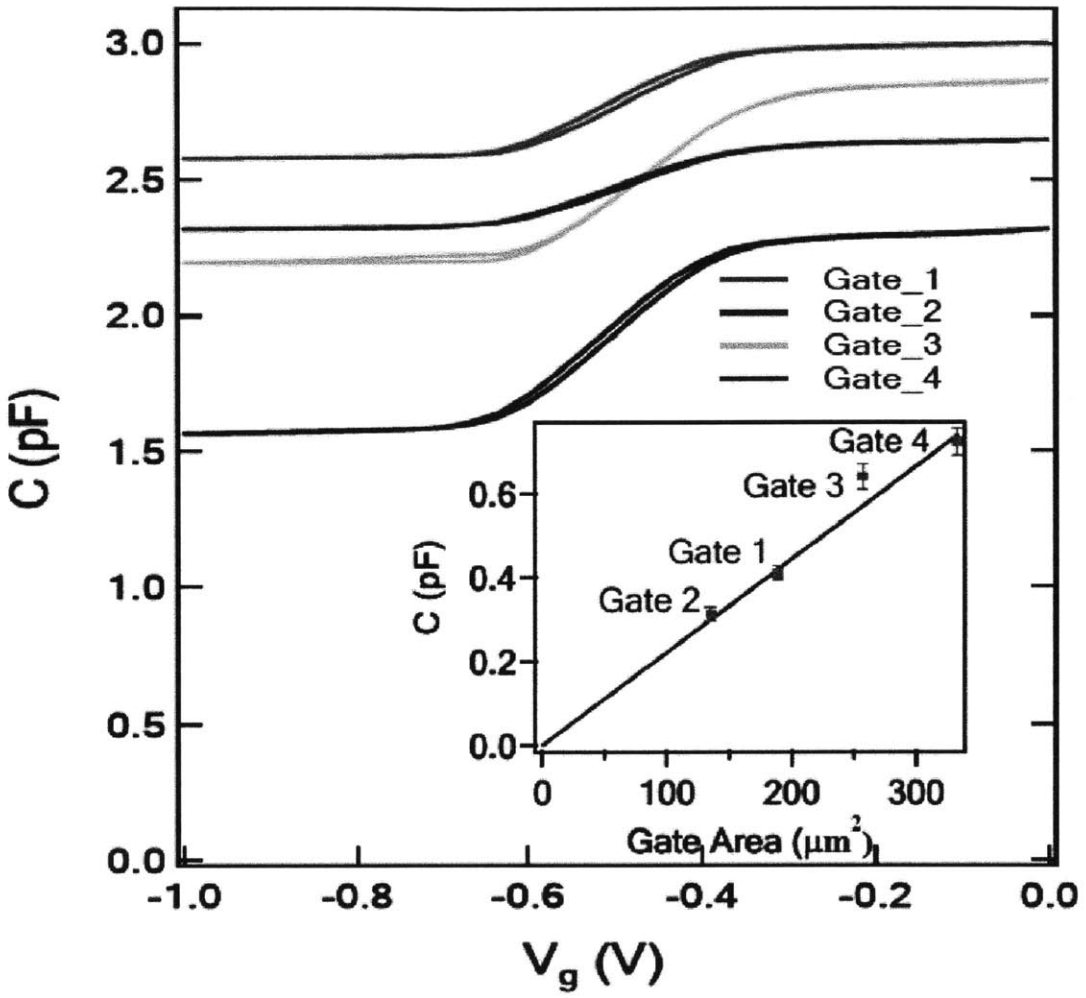

Figure 3-3: Capacitance measurements of each gate, as a function of gate voltage applied. As the magnitude of Vg is increased, there is a corresponding drop in the capacitance. This experimental drop matches up quite nicely with the theoretical capacitance of each gate. Figure taken from [26]

behavior is indicative of a capacitance in series with a large resistance. To see this, we can consider such a circuit. We have an overall excitation voltage, V, and an impedance of $Z = R + \frac{1}{iC\omega}$. Therefore, our current is simply:

$$I = \frac{V}{Z} = \frac{V}{R + \frac{1}{iC\omega}} = \frac{V(R + \frac{i}{\omega C})}{R^2 + \frac{1}{\omega^2 C^2}} \tag{3.1}$$

Thus, we have:

$$I_{\text{real}} = \frac{V}{R + \frac{1}{RC^2\omega^2}} \tag{3.2}$$

$$\frac{I_{\text{imaginary}}}{V\omega} = \frac{C}{R^2\omega^2C^2 + 1} \tag{3.3}$$

As we can see, as the frequency increases, the real current will increase, while the imaginary current normalized with frequency will decrease. Using the basic premise of a resistor in series with a capacitor, we were eventually able to arrive at the following circuit model depicted in Figure 3-4, which does a fairly accurate job of modeling the behavior.

In this model, we have a capacitance between the gate and the 2DEG, C_1, a capacitance between the donor layer and the 2DEG, C_3, and a fringe capacitance between the gate and the donor layer, C_2. Additionally, we have a leakage resistance from the gate to the donor layer, R_1, and an overall resistance of the donor layer, R_2. As we increase the gate bias from 0 V to -1 V, we deplete the 2DEG directly underneath the gate, so at this voltage, the circuit model no longer includes C_1. Fitting the data at $V_g = 0$ and $V_g = -1$ to the circuit model in Figure 3-4, we find for

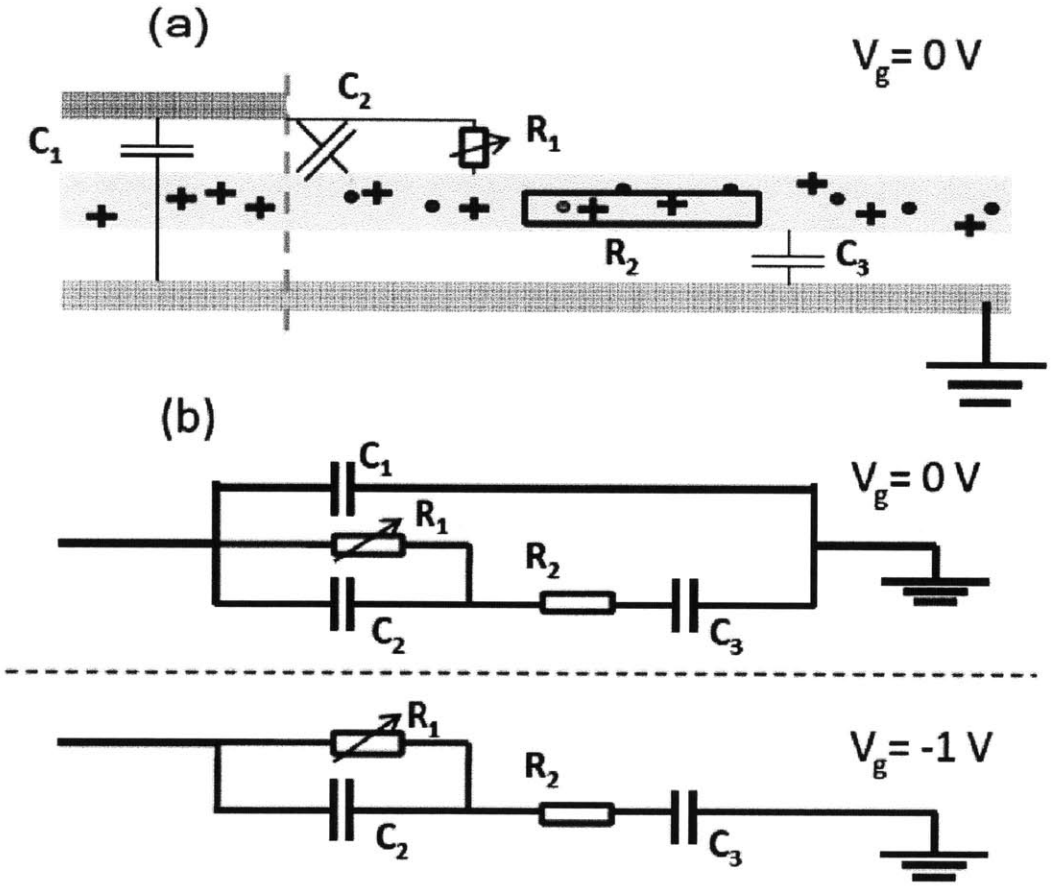

Figure 3-4: The proposed circuit model to describe the observed behavior. At Vg = 0, we have the capacitance C1 between the gate and the 2DEG. We also have the fringe capacitance, C2 between the 2DEG and the donor layer (underneath the gate, the donor layer is depleted), and a leakage resistance, R1, also between the gate and the donor. This is in series with the donor layer resistance, R2, and the capacitance between the donor layer and the 2DEG, C3. As we reach Vg = -1, the 2DEG directly underneath the gate is deleted, and therefore, we can ignore C1. Figure taken from [26]

the values of our capacitances and resistances, $C_1 = 0.3 \pm 0.1pF$, $C_2 = 02 \pm 0.9$ pF, $C_3 = 2.5 \pm 0.1pF$ and $R_1 = 8 \pm 14M\Omega$, $R_2 = 12 \pm 15M\Omega$. There is little uncertainly in the values for C_1 and C_3, and we find that C_1 matches up quite nicely with the expected theoretical value of 0.3 pF. Our value of R_2 would indicate that while the donor layer is conducting, it is still highly resistive. Additionally, if C_3 is a capacitance between the donor layer and the 2DEG, its value of 2.5 pF would correspond only to a region of the 2DEG in the mesa. Combined with the high value of R_2, our model suggests the donor layer consists of regions of highly conducting patches. Leakage between the lateral gates and these conducting regions in the donor layer are then what cause the extended depletion of the underlying 2DEG.

3.3 Conclusions

Overall, there is evidence that the conduction in the delta doping layer is responsible for the difficulty in creating controlled quantum dots in Si/SiGe heterostructures. Depletion of the 2DEG with a range greater than 30 microns occurs by applying a negative bias on just one gate, indicating that there exists a leakage path from the gate to the 2DEG. Despite being unable to identify the source of this leakage path, the fact that depletion of the 2DEG can occur over such large regions makes it clear why fabricating controllable dots in doped Si/SiGe heterostructures is difficult. There are groups which have been successful in creating controllable quantum dots formed doped heterostructures; however this is most likely done by careful control of the delta doping layer. Such fine tuning is not a preferable way to create Si/SiGe quantum dots,

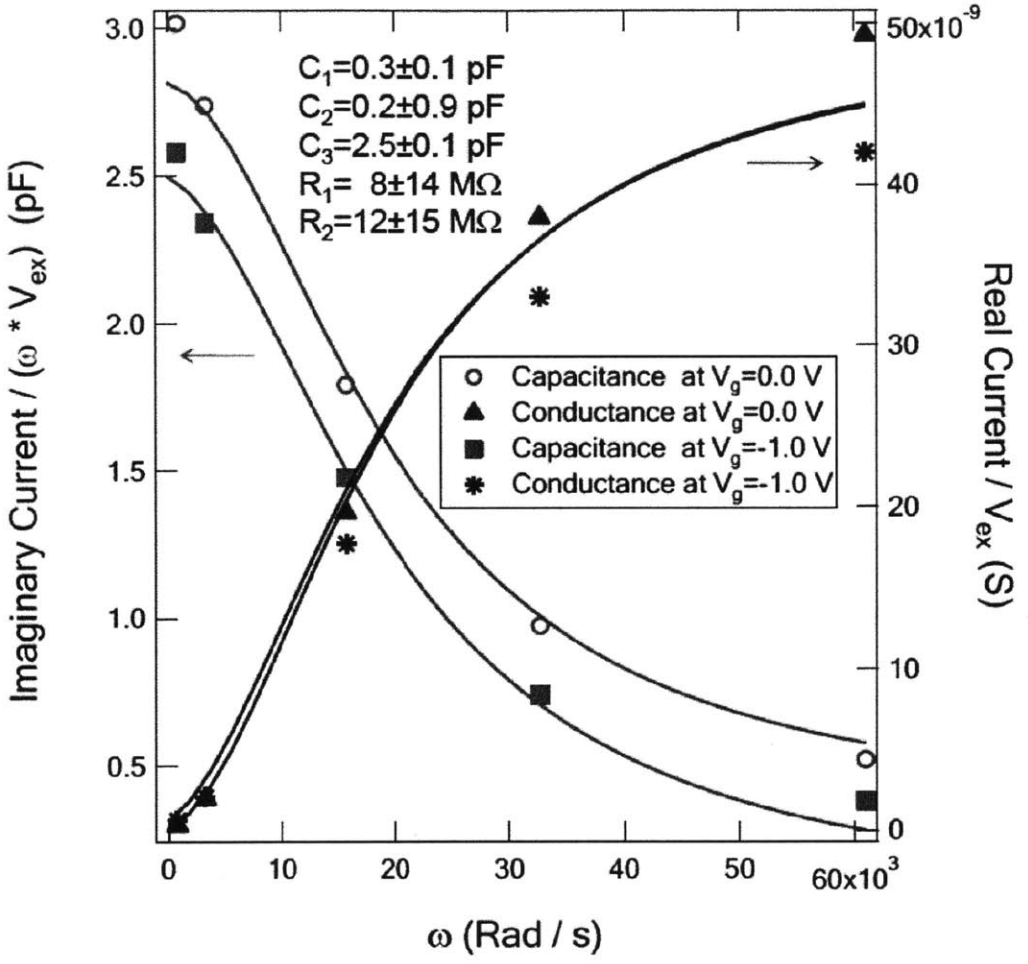

Figure 3-5: Fits of current as a function of frequency using the circuit model depicted in Figure 3-4. As we can see, there is a decent agreement in the fit and the experimental data. The value of $C_1 = 0.3 \pm 0.1pF$, which corresponds to the capacitance between the gate and the 2DEG matches up quite nicely with the theoretically expected value of 0.32 pF. Figure taken from [26]

particularly for their use as qubits. Therefore, it appears to be preferable to instead to induce such quantum dots capacitively, by creating the 2DEG through applying a positive bias to a metallic top gate at the top of the heterostructure. This method eliminates the need for a donor layer, and therefore the associated problems that accompany it.

Chapter 4

Undoped Si/SiGe Heterostructures

In this chapter, we discuss attempts to make Si/SiGe dots in undoped heterostructures. We mention initial difficulties in fabricating ohmic contacts to the 2DEG and how these difficulties were resolved. We also discuss further difficulties that arose in attempts to make a field effect transitor (FET) in undoped heterostructures due to a parasitic coeducation channel forming in the Si cap layer.

4.1 Initial Changes to Heterostructure

When we first changed from a doped heterostructure to a undoped heterostructure, there were a few changes made immediately in the fabrication process. First, since the 2DEG is now induced capacitively, a metallic top gate over the active region is needed. However, since the quantum dots are defined by lateral surface gates, a layer of insulation is needed between these lateral gates and the top gate. For this layer of insulation, we deposited 100 nm of aluminum oxide on top of the surface gates

and silicon cap using atomic layer deposition. After the ALD deposition of aluminum oxide, the top gate is patterned with photolithography, and a 5 nm / 295 nm Ti/Au layer is deposited with E-beam evaporation.

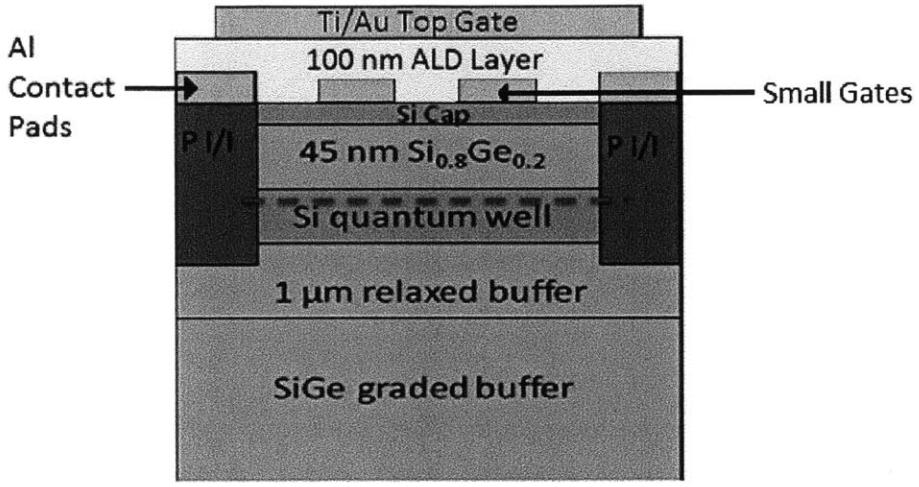

Figure 4-1: Side view schematic of devices fabricated in a undoped Si/SiGe heterostructure

4.1.1 Ohmics Contacts

To first make sure that we could induce a 2DEG capactively, we fabricated field effect transistors in the undoped heterostructure. Our fabrication procedure for field effect transistors is the same as that for the quantum dots, except we do not need to make lateral surface gates. In our field effect transistors, there were problems with the Au/Sb ohmics, which turned out to be very spiky in topography. As a result, the aluminum oxide layer was unable to provide sufficient insulation between the ohmic contacts and the top gate, resulting in the leakage between the two. Attempts were made to reduce the region of overlap between the ohmic contacts and top gates.

However, despite reducing the number of leaking ohmics, a single device only needed one leaking ohmic to become non-functional. Therefore, the majority of devices still remained unusable and a new method for fabricating ohmics was desired. Instead of using annealed Au/Sb contacts, we went with the method of ion implantation to fabricate ohmic contacts. The ohmic contacts are first patterned with photolithography, and afterwards phosphorous ions are implanted at energies of 40 keV and concentrations of 2e15 per cm^2 to create n-doped regions. After implantation, the sample is annealed at 600 C for 30 minutes. During annealing, the damage to the lattice structure caused by the ion implantation is corrected. To make contact to these n-doped regions, contact pads are again patterned with photolithography, and aluminum is deposited with e-beam evaporation. We fabricated a few test devices with this new ohmic recipe and in most devices, there was no longer leakage between the top gate and ohmics.

4.2 Conduction in cap layer

In these new test devices, we performed simple conduction tests to see whether we could induce a 2DEG capacitively. To do this, we measure the two-lead conductance between a pair of ohmics, while a positive DC bias is applied to the metallic top gate. For the conductance measurements, an AC excitation with a frequency of 103 Hz and voltage of 92.3 μV is used, while the DC bias on the top gate is varied from 0 to 10 volts. In our measurements, we observe that at around 4 V, there is a turn on in conductance (4-2). Initially, we were hopeful that this conduction was occurring in

the silicon quantum well. However, our field effect mobility from these measurements is much lower than expected. The field effect mobility can be computed as follows:

$$\mu = m_{\text{lin}} \frac{L}{W V_{\text{DS}} C_i} \tag{4.1}$$

where m_{lin} is the slope of the current vs voltage, C_i is the gate capacitance per unit area, and V_{DS} is the excitation voltage. Using Eqs. 4.1 and 4-2, we compute a field effect mobility of around 70 $\frac{\text{cm}^2}{V \cdot s}$. This is much lower than the expected value, which should be at least 100,000 $\frac{\text{cm}^2}{V \cdot s}$ [12].

Given this low value of mobility, it is likely that conductance is not occurring in the Si quantum well, but in the Si cap layer instead. To see where this conduction is occurring, we performed capacitance measurements on our devices, in the same manner as in Chapter 3. If conduction is occurring at the Si quantum well, treating the system of the resulting 2DEG and metallic top gate as infinite metal plates, the expected capacitance between the two should be around 175 pF. If this capacitance is instead occurring at the Si cap layer, the expected capacitance would be around 240 pF. As seen from the measurements in Figure (4-3), and based on the expected capacitance, it appears that conduction is actually occurring in the Si cap layer instead of the Si quantum well.

Conduction occurring in the Si cap layer results in much lower electron mobilities, as a lot scattering occurs at the interface between the Si and oxide. One possibility for why conduction is occurring in the cap layer instead of the 2DEG is that the ohmics, while making contact with the cap layer, are not making proper contact with the

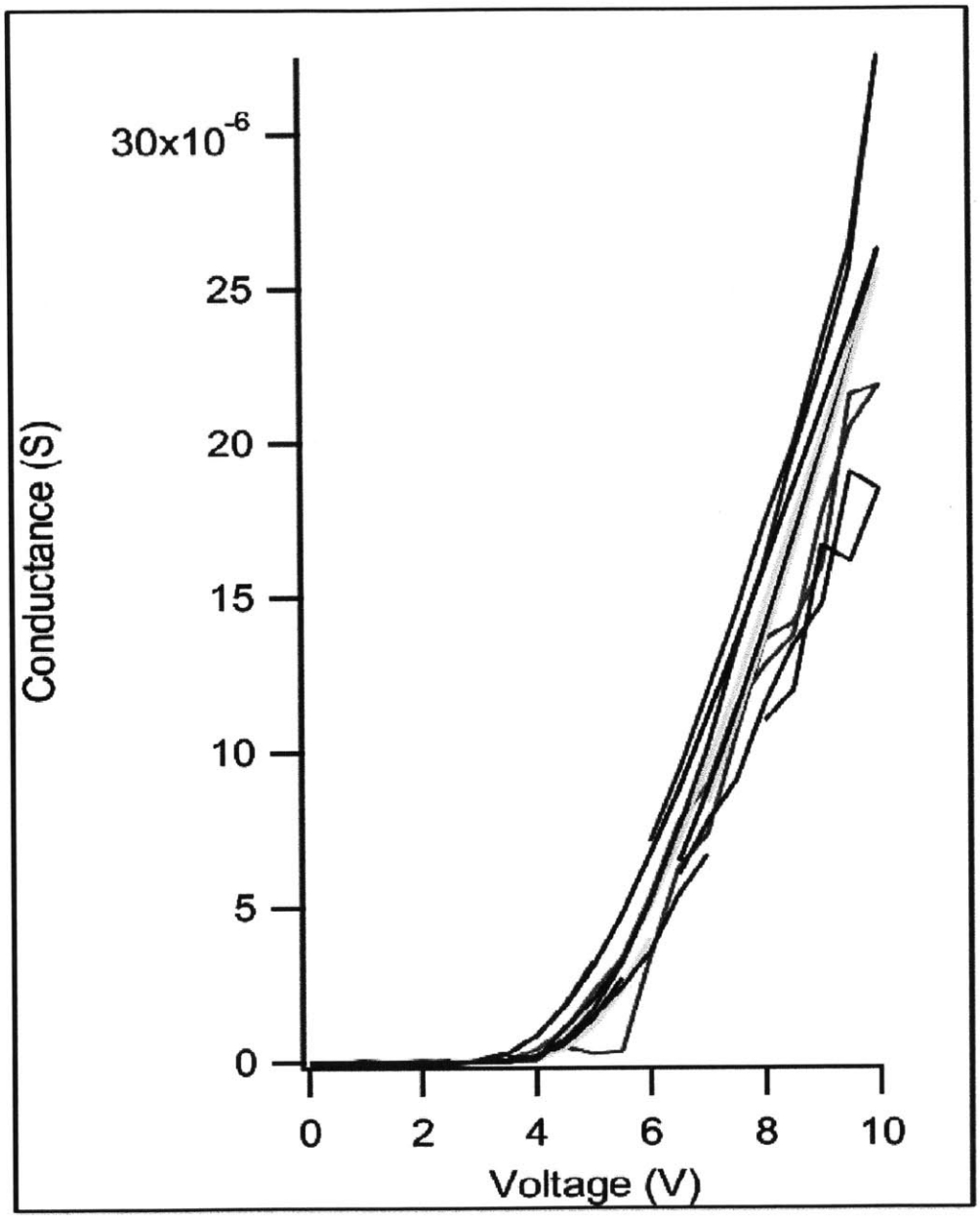

Figure 4-2: Conductance measurements of devices fabricated with an undoped heterostructure. The field effect mobility of these devices is around 70 $\frac{cm^2}{V \cdot s}$, several magnitudes lower than expected.

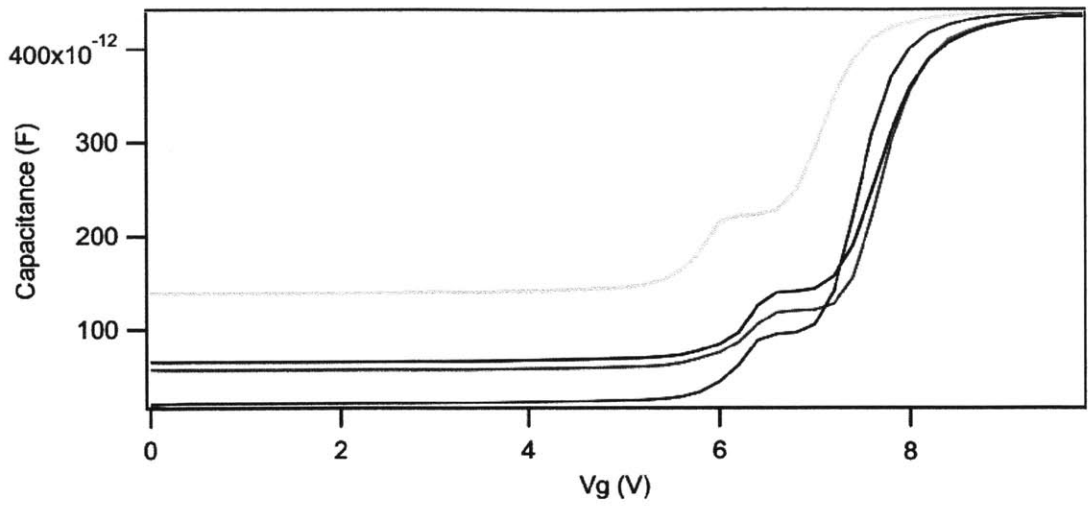

Figure 4-3: Capacitance measurements of devices fabricated with an undoped heterostructure. The capacitance is measured between the metallic top gate, and one of the ohmics. From the data, it appears that initially, there is are electrons populating the Si quantum well; however, as the gate voltage is increased, the electrons move very quickly to populate the Si cap layer instead.

2DEG. However, this seems unlikely, as successful ohmics have been fabricated from ion implantation to similar heterostructures as ours, with the same concentration (2e15 cm^{-2} and slightly lower energies (40 keV) [27]. Additionally, in the situation that the lattice structure had not been properly restored after annealing, various samples were annealed at higher temperatures, going all the way to 830 C, but none resulted in any improvement in the electron mobility.

4.2.1 Simulations of band structure

Since it appears our ohmics are making contact with the 2DEG, the likeliest scenario for why conduction is occurring in the Si cap layer instead of the quantum well is the Si cap layer is energetically favorable for electrons. We can explore this further

by first considering the zero-point energies of both the quantum well, and the Si cap layer. The Si quantum well can be modeled simply as a 10 nm finite square well, with barriers of energies around 200 meV. The Si cap layer, similarly, can be modeled as a square well, with infinite boundaries on one side, and an energy barrier of 200 meV on the other. Both of these square wells are well known problems in 1 dimensional quantum mechanics [28]. The finite square well has eigenenergies which occur at:

$$\alpha = k \tan(\frac{kL}{2}) \text{ for symmetric wavefuctions} \tag{4.2}$$

$$\alpha = -k \cot(\frac{kL}{2}) \text{ for antisymmetric wavefuctions} \tag{4.3}$$

where $\alpha = \frac{\sqrt{2m(V_o - E)}}{\hbar}$, k is the wavevector inside the well, and L is the length of the well. Therefore, for our zero-point energy, we can consider the lowest energy solution to the symmetric case, and with $V_o = 200$ meV, and L = 10 nm, we arrive at a value of $E_o = 3.21$ meV. Similarly, to find the ground state the square well with infinite boundaries on one side, and a finite barrier on the other, we can consider a finite square well of twice its length, and consider the lowest energy solution to the antisymmetric case. Doing this, with L = 4 nm, we arrive at a value of $E_o = 19.1$ meV. If we reduce L to 1 nm, are value of E_o increases to 158.8 meV.

As we can see, there is not too much of an energy difference between these values for a 4 nm well with infinite boundaries on one side, and a 10 nm finite square well, though it is nonetheless energetically favorable for electrons to reside in the larger 10 nm square well. However, for a more complete picture, we must consider the overall effects of the band structure in the heterostructure. In order to see the effect the

cap layer has on conduction, we ran a few simulations with the program NextNano. Nextnano is used to solve the self-consistent 1-dimensional Poisson-Schrodinger equation for the undoped Si/SiGe heterostructure. In the program, the band structure of the various regions of Si, SiGe, and Aluminum oxide as a function in the z direction are provided as input for the potential. With this potential and an applied gate voltage, the electron density over these various regions is calculated. According to the simulations, when Si cap layer is 4 nm, the Si quantum well is more energetically favorable until the gate voltage is 0.25 V. From then onwards, it is more energetically favorable for an electron to reside in the cap layer as opposed to the Si quantum well. If the Si cap layer is reduced to 1 nm, the Si cap layer becomes more energetically favorable once the gate voltage is 0.7 V. Of course, this simulation is may be too simplistic, as it does not take into account possible effects which could occur at the interface between the cap layer and the aluminum oxide layer. However, it nonetheless demonstrates that reducing the Si cap layer can only improve the likely hood that conduction occurs in the Si quantum well.

4.2.2 Attempts at reducing the cap layer

Based on the simulations, it seems necessary to reduce the cap layer as much as possible to increase the threshold voltage for conduction in the cap layer. Since the cap layer is only 4 nm is size, we wanted a method which would etch silicon very slowly, so as not to accidentally remove the entire cap layer in the process. Eventually, we went with using a buffered oxide etch (BOE). BOE etches are used to

remove oxides. The Si cap naturally will oxidized and a thin layer of silicon dioxide forms on its surface. During this oxidation process, a small amount of the Si cap layer is consumed, usually around 0.7 nm [29]. Therefore, through the process of performing a BOE etch, growing an oxide on the cap layer, and repeating, we have a controllable method for removing small fractions of the 4 nm Si cap at a time, without removing it entirely. The BOE etch was typically done for 10 seconds, while the oxide on the cap layer was grown through exposure to UV light and ozone for about 5 minutes.

With this method, we made various attempts to thin the Si cap layer, going as far as to etch off almost the entire cap. However, in all of our attempts, we were unable to induce a 2DEG in the Si quantum well. We either still had conduction in the Si cap layer, or behavior which seemed indicative of charge trapping occurring in the oxide layer (4-4). The latter gives an indication that perhaps a large portion of our problems are occurring at the interface between the Si cap layer, and the ALD aluminum oxide layer. Various methods to passivate this interface between the Si cap layer and ALD layer, such as heating the sample with forming gas, were attempted, but none were successful.

4.3 Conclusions

Overall, there appear to be significant difficulties in fabricating controllable quantum dots in undoped Si/SiGe heterostructures. The previous recipe of using Sb/Au ohmics was causing leakage through the insulating ALD layer. This difficulty was resolved

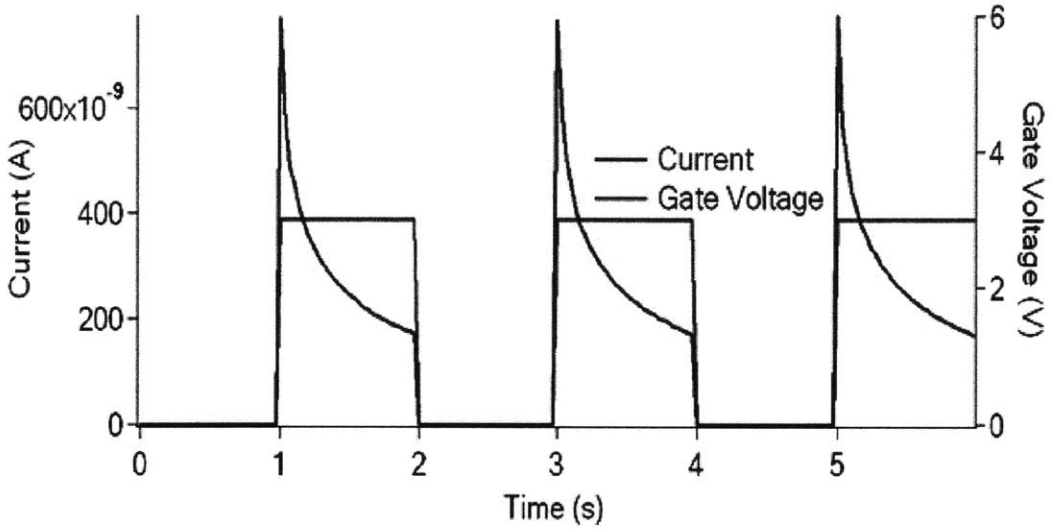

Figure 4-4: Evidence of possible charge trapping in the oxide layer. Here, the DC current is measured between a pair of ohmics, while the gate voltage on the top gate is changed from 0 V to 3 V. Immediately, a current appears, however, this current exponentially decays as a function of time. A possible explanation for this exponential decay in current is charge trapping in the oxide layer.

once the ohmics were fabricated with ion implantation of phosphorous ions. However, it appears that more work is needed to passivate the interface between the ALD layer and the Si cap. Achieving this, along with using a heterostructure with a thin Si cap layer, would hopefully prevent conduction on a parasitic channel, and charge trapping in the oxide layer, allowing us to populate electrons in the Si quantum well. With an undoped heterostructure capable of inducing a 2DEG in the Si quantum well capacitively, lateral quantum devices fabricated from it should not have the issue of a conducting donor layer that was found in devices build from doped heterostructures. This would move us closer towards the goal of creating controllable quantum dots in Si/SiGe heterostructures.

Appendix A

Fabrication Procedure

A.1 Fabrication procedure for devices on doped Si/SiGe heterostructure

We provide a more detailed fabrication procedure here. First, here is the fabrication procedure for devices made with doped Si/SiGe heterostructures.

I. Wafer Cleaving and cleaning

- Cleave wafer into approximately 10x10 mm pieces using diamond scribe.
- Sonication in Acetone/methanol/IPA for 5 minutes each
- Blow dry with nitrogen and Dehydration Bake.

II. Mesa Isolation

The purpose of this step is to define an active conducting region in the heterostructures. Baked photo-resist is used as the masking material for dry etch.

- Coat positive resist, OCG-934, using the standard TRL recipe (30 s, 4000 RPM), followed by pre-bake in the oven for 30 minutes at 90 C.

- Exposure for 1.75 seconds with the EV1

- Develop for 1 min using the OCG-934 1:1 developer.

- Dry-etch to define Mesa (Plasmaquest, Cl2 + Ar for 23 seconds at 80 degree C. Name of the recipe: SIGEETCH).

- Remove resist using Acetone/methanol/IPA (Photo-wet-Au), followed by 15 seconds of ashing (asher-TRL).

III. Ohmic Contacts

The purpose of this step is to provide ohmic contacts to the active region defined in the first layer. Negative photo-resist is used for pattern generation, and Ebeam-Au to deposit metal. The pattern will be annealed to form ohmic contacts.

- Clean sample in Acetone/IPA, 5 minutes each, blow dry with N2.

- Hotplate for 2 minutes at 110 C.

- Coat negative resist, AZ5214, with the coater using the standard TRL recipe (30 s, 4000 RPM), followed by pre-bake for 30 minutes at 90 C.

- Exposure for 1.5 seconds with the EV1.

- Post-Bake for 30 minutes at 90 C.

- Flood exposure for 60 seconds with the EV1.

- Develop for 2 minutes using the AZ422 MIF developer.
- Buffered Oxide Etch (BOE) dip for 1 min to remove native oxide in the acid-hood.
- Attach samples to metal slides with PMMA, and do an E-beam (E-beam Au) evaporation of 200nm Ohmic metal (Au0.99/Sb0.01 alloy purchased from Good Fellow Inc).
- Place sample in acetone, and do a liftoff overnight.
- Anneal at 325 degree C for 10 minutes in forming gas (H2/N2).

IV. Small Gates The purpose of this step is to provide small metallic gates above the mesa, which will be used to deplete the 2-dimensional electron gas underneath. E-beam lithography is used for the patterning, followed by brief dry etch and metal deposition.

- Small Gate Lithography
  - Resist process (PMMA spinner):
    * Dehydration bake for 2 minutes on the hotplate at 180 C.
    * Spin coat 1st layer of 950-A2 PMMA at 4000rpm for 60 seconds.
    * Bake 3 minutes at 180 C.
    * Spin coat 2nd layer of 950-A2 PMMA at 4000rpm for 60 seconds.
    * Bake 6 minutes at 180 C.

- Exposure (Raith-150) using cleanroom compatible holders and tweezers. (WF: 100 um at 550X; Dose: 420 uC at 30 kV; Aperture size 30 um; Step size 12-15 nm).
- Develop for 90 seconds using developer, followed by 15 seconds of ashing (asher-TRL).

- Metal deposition (eBeam Au) Cr/Au 5 nm/15 nm.
- Lift-off in Acetone.

V. Large Gates The purpose of this step is to provide extended bond pads of the small gates structure.

- Clean sample in Acetone/IPA, 5 minutes each, blow dry with N2.
- Hotplate for 2 minutes at 110 C.
- Coat negative resist, AZ5214, using standard TRL recipe (30 s, 4000 RPM), followed by pre-bake for 30 minutes at 90 C.
- Exposure for 1.5 seconds (EV1).
- Post-Bake for 30 minutes at 90 C.
- Flood exposure for 60 seconds (EV1).
- Develop for 2 minutes.
- E-beam (E-beam Au) evaporation of 20 nm Cr/ 120 nm Au.
- Lift-off in Acetone (Photo-wet-Au).

A.2 Fabrication procedure for devices on undoped Si/SiGe heterostructure

For undoped heterostructures, steps I and II (cleaving and mesa isolation) stay the same. For our ohmic contacts in step III, we use the following updated recipe:

III. Ohmic Contacts

The purpose of this step is to provide ohmic contacts to the active region defined in the first layer. We use ion implantation to form the ohmic contacts. An aluminum contact pad is then deposited on top of the ohmic contacts.

- Photolithography process
  - Clean sample in Acetone/IPA, 5 minutes each, blow dry with N2.
  - Hotplate for 2 minutes at 110 C.
  - Coat negative resist (AZ5214E) using standard TRL recipe (30 s, 4000 RPM) followed by pre-bake for 30 minutes at 90 C.
  - Exposure for 1.5 seconds (EV1).
  - Bake again for 30 minutes at 90 C.
  - Flood exposure for 60 seconds (EV1).
  - Develop for 2 minutes with AZ422 developer.
  - Post-bake at 120 C for 30 minutes.
- Ship sample to Innovion for P+ ion implants (40 keV, 2e15 per cm2).

- Remove resist using Acetone/IPA, followed by 1 hour of ashing (asher-TRL). Then dip in Nanostrip for 10 minutes to remove residual photoresist (acid-hood-TRL).

- Anneal sample at 600 C for 30 minutes to activate implants. (Harvard RTP)

- Contact Pads for ohmics

  - Clean sample in Acetone/IPA, 5 minutes each, blow dry with N2.

  - Photoresist Process in TRL

    * HDMS-TRL for 30 minutes, use recipe 5.

    * Coat 2 layers of positive resist (OCG) using standard TRL recipe (30 s, 4000 RPM), followed by pre-bake for 30 minutes at 90 C.

    * Exposure for 1.75 seconds (EV1). Develop with 934 developer for 1 min.

    * Post-Bake (post-bake-oven) at 120 C for 30 minutes.

  - Thermal evaporation of 200nm Aluminum. (TE-3, Harvard)

  - Liftoff: Leave in acetone over night. Use Sonication if needed. Clean in IPA and then blow dry.

After the small gates and connector gates are patterned, (Steps IV and V), we deposits the ALD layer.

Step VI. The purpose of this step is to deposit an insulating layer of aluminum oxide between the small lateral gates on the surface, and the top gate.

- Perform an RCA clean (Rinse sample in DI water after each step)
- 10 minutes in mixture of Hydrogen Peroxide, Ammonium Hydroxide and DI water, in 2:2:7 ratio. Temperature = 70 C
- 10 minutes in mixture of HCL, Hydrogen Peroxide, and DI water, in 2:2:7 ratio. Temperature = 70 C
- 40 second etch in diluted HF, 1:50.
- Perform 10 minute UV ozone clean (This also grows a thin layer of silicon dioxide). (Harvard UV Ozone)
- Deposit aluminum oxide using ALD machine. 900 cycles at 250 C. (Harvard ALD Machine)

Step VII. Our last step is to provide the top gate, which will be used to attract electrons into the quantum well.

- Clean sample in Acetone/IPA, 5 minutes each, blow dry with N2.
- Photoresist Process in TRL:
- Place on hotplate for 2 minutes at 110 C.
- Coat negative resist (AZ5214E) using standard TRL recipe, followed by pre-bake for 30 min at 90 C.
- Exposure for 1.5 seconds (EV1). Post-Bake for 30 min at 90 C. Flood exposure for 60 seconds (EV1). Develop for 2 minutes with AZ422 developer

- Thermal Evaporation of 200 nm of Aluminum (TE-3, Harvard).
- Lift-off in Acetone overnight. Use Sonication if needed. Clean in IPA and then blow dry.

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