Thesis for the Degree of Doctor of Philosophy

Analytical Approaches to Load Modulation Power Amplifier Design

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Abstract

In future mobile communication networks, there will be a shift toward higher carrier frequencies and highly integrated multiple antenna systems. The system performance will largely depend on the available radio frequency (RF) hardware. As such, RF power amplifiers (PAs) with improved performance, e.g. energy efficiency, are needed. Active load modulation (ALM) is one of the most common PA efficiency enhancement techniques. Unfortunately, different ALM techniques come at the cost of degrading other PA attributes. Through investigation of new ALM design techniques, the overall objective of this thesis is to improve upon different attributes and performance trade-offs in ALM PAs for future wireless systems.

The working principle of ALM PAs is determined by both how the individual transistors are operated and how their outputs are combined. In the first part of the thesis, an analytical approach, where the output combiner is assumed to be an arbitrary black-box, is applied to the Doherty PA. The fundamental interaction between the main and auxiliary transistors is analyzed and generalized. New solutions with improved performance are identified, such as higher gain and an improved efficiency-linearity trade-off. This approach also introduces improved integration possibilities, which are demonstrated by a transmitter where the antenna acts as both the radiator and the Doherty combiner. Additionally, the analytical approach is applied to an isolated two-way power divider. This unlocks many new possibilities, such as improved integration and layout flexibility.

In the second part, one embodiment of the emerging ALM architecture, the load modulated balanced amplifier (LMBA), is proposed: the RF-input Doherty-like LMBA. Design equations are derived and the fundamental operation is studied. This variant presents several advantages over other known architectures, such as higher gain and device periphery scaling of the different transistors.

The third part proposes a new measurement-based ALM PA design procedure, which emulates the full behavior of the transistors in any ALM architecture using active load-pull measurements. This method can predict the intricate behavior in ALM PAs and it gives measurement-based insights into the internal operation of the circuit already at the design stage. This facilitates the design for optimal ALM PA performance.

The thesis contributes with several promising techniques for reducing performance trade-offs and improving the overall performance of ALM PAs. Therefore, the results will contribute to the development of more energy efficient and high capacity wireless services in the future.

Keywords: Active load-pull, Doherty, load modulation, energy efficiency, linear, microwave, load modulated balanced amplifier (LMBA), power amplifier (PA), radio frequency (RF), Wilkinson power divider.

List of Publications

Appended Publications

This thesis is based on work contained in the following publications:

[A] O. Iupikov, W. Hallberg, R. Maaskant, C. Fager, R. Rehammar, and M. Ivashina, "A dual-fed PIFA antenna element with non-symmetric impedance matrix for high-efficiency Doherty transmitters: Integrated design and OTA-characterization," submitted to *IEEE Trans. Antennas Propag.*, Feb. 2019.

[B] W. Hallberg, M. Özen, D. Gustafsson, K. Buisman, and C. Fager, "A Doherty power amplifier design method for improved efficiency and linearity," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 12, pp. 4491–4504, Dec. 2016.

[C] W. Hallberg, M. Özen, D. Kuylenstierna, K. Buisman, and C. Fager, "A generalized 3-dB Wilkinson power divider/combiner with complex terminations," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 10, pp. 4497–4506, Oct. 2018.

[D] P. H. Pednekar, W. Hallberg, C. Fager, and T. W. Barton, "Analysis and design of a Doherty-like RF-input load modulated balanced amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 12, pp. 5322–5335, Dec. 2018.

[E] W. Hallberg, D. Nopchinda, C. Fager, and K. Buisman, "Emulation of Doherty amplifiers using single amplifier load-pull measurements," Manuscript.

Other

The content of the following material partially overlaps with the appended publications or is out of the scope of this thesis.

[a] M. Özen, W. Hallberg, and C. Fager, "Combiner synthesis for active load modulation based power amplifiers," Chapter contribution in A. Grebennikov, *RF and Microwave Power Amplifiers: Theory, Design & Applications,* to be published.

[b] D. Fishler, T. Cappello, W. Hallberg, T. W. Barton, and Z. Popović, "Supply modulation of a linear Doherty power amplifier," in *Proc. Eur. Microw. Conf.*, Sep. 2018, pp. 519–522.

[c] C. Fager, M. Ivashina, O. Iupikov, R. Maaskant, and W. Hallberg, "Integrated active Doherty antenna transmitter," Patent application, PCT/EP2018/064387, Jun. 2018.

[d] W. Hallberg, P. E. de Falco, M. Özen, C. Fager, Z. Popović, and T.W. Barton, "Characterization of linear power amplifiers for LTE applications," in *Proc. IEEE Topical Conf. RF/Microw. Power Amplif. Radio Wireless Appl.,* Jan. 2018, pp. 32–34.

[e] C. Fager, W. Hallberg, M. Özen, K. Andersson, K. Buisman, and D. Gustafsson, "Design of linear and efficient power amplifiers by generalization of the Doherty theory," in *Proc. IEEE Topical Conf. RF/Microw. Power Amplif. Radio Wireless Appl.,* Jan. 2017, pp. 29–32.

[f] W. Hallberg, M. Özen, and C. Fager, "Current scaled Doherty amplifier for high efficiency and high linearity," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2016, pp. 1–4.

[g] W. Hallberg, M. Özen, and C. Fager, "Class-B/C Doherty power amplifier," U.S. Patent, US14759528B2, Jul. 2015.

[h] W. Hallberg, D. Gustafsson, M. Özen, C. M. Andersson, D. Kuylenstierna, and C. Fager, "A class-J power amplifier with varactor-based dynamic load modulation across a large bandwidth," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2015, pp. 1–4.

Thesis

[i] W. Hallberg, *Frequency Reconfigurable and Linear Power Amplifiers Based on Doherty and Varactor Load Modulation Techniques*, Licentiate dissertation, Dept. of Microtechnology and Nanoscience, Chalmers University of Technology, Gothenburg, Sweden, Oct. 2016.

As part of the author's doctoral studies, some of the work has previously been published in [i]. Text, figures and tables from [i] may therefore be fully or partially reproduced in this thesis.

Notations and Abbreviations

Notations

β	Normalized gate-source voltage drive level
β_{bo}	Backed-off drive level
η	Drain efficiency
γ	The ratio $P_{\mathrm{del,max}}/P_{\mathrm{del,bo}}$
ζ	Waveform constant
C_{ds}	Drain-source capacitance
i_{DS}	Drain-source current, time domain
I_{DS}	Drain-source current, DC component
I_{ds}	Drain-source current, fundamental frequency component
$I_{\mathrm{ds,max}}$	Maximum fundamental drain-source current
I_{MAX}	Maximum DC drain-source current
P_{DC}	DC power
P_{del}	Power delivered to the fundamental load termination
$P_{\mathrm{del,max}}$	Maximum delivered power
$P_{\mathrm{del,bo}}$	Backed-off delivered power
R_{l}	Fundamental load termination resistance
R_{on}	On-resistance
$\Re$	Function that gives the real part of a complex number
S_{aux}	Relative size of the auxiliary transistor
v_{DS}	Drain-source voltage, time domain
V_{DS}	Drain-source voltage, DC component
V_{ds}	Drain-source voltage, fundamental frequency component
$V_{\mathrm{ds,max}}$	Maximum fundamental drain-source voltage

Abbreviations

ACPR	Adjacent Channel Power Ratio
ALM	Active Load Modulation
AUT	Antenna Under Test
CW	Continuous Wave
DC	Direct Current
DLM	Dynamic Load Modulation
DPD	Digital Pre-distortion
DSM	Dynamic Supply Modulation
DUT	Device Under Test
EA	Envelope Amplifier
ET	Envelope Tracking
FET	Field-effect Transistor
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
ICT	Information and Communication Technology
IM	Intermodulation
LTE	Long Term Evolution
MIMO	Multiple Input Multiple Output
OMN	Output Matching Network
OPBO	Output Power Back-off
PA	Power Amplifier
PAE	Power Added Efficiency
PAPR	Peak to Average Power Ratio
RF	Radio Frequency
SISO	Single Input Single Output

Contents

Chapter 1

Introduction

The future of humanity is dependent on sustainable development. Sustainable development can be divided into three pillars: economic and social development while preserving the environment. Many efforts are required in all human activities to achieve sustainable development. Information and communication technology (ICT) is evermore present in society and has the potential to both enable and restrain sustainable development. Therefore, developing ICT to meet future demands must be done responsibly, keeping sustainable development in mind. While one of the biggest concerns of the development of ICT is high energy consumption, the benefits are plentiful. ICT can contribute in many ways to all pillars of sustainable development. The contributions are often analyzed with regards to direct and indirect effects. The direct economic effects are quite significant. In 2015, the ICT sector, including manufacturing and services, represented 3.9% of the total GDP in the EU. That same year, 2.5% of all employees in the EU worked in the EU ICT sector [1]. ICT also enables faster and better means of communications and access to information, which in itself is a great social development. The many indirect effects of ICT on sustainable development have been analyzed by the International Institute for Sustainable Development (IISD) [2]. One such indirect effect is ICT enabling distant communication, which is more energy efficient from a transport point of view.

ICT is a broad term including, mobile communications, computer technologies and software. Among these, mobile communications is an exponentially growing technology under constant development [3].

1.1 Trends in Mobile Communications

The development of mobile communications is pushed by the need for enhancing existing experiences and by the expansion to new use cases, such as internet of things (IoT). Future demands put new requirements on wireless infrastructures, which in turn put new technical implications on the digital and radio frequency (RF) front-end hardware. Some key future infrastructure requirements for future mobile communications are listed below [4–7]:

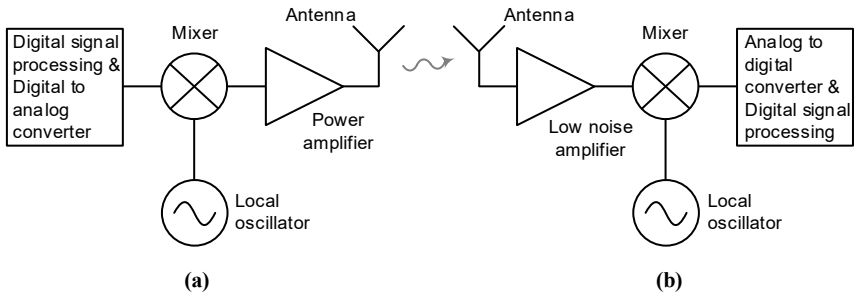


Figure 1.1: Illustration of a wireless (a) transmitter and (b) receiver.

- **Diverse services and devices**. A vast amount of different devices and scenarios will have various requirements, e.g. output power and data rate demands will differ significantly between IoT devices and cell phones.

- **Diverse spectrum**. In order to support higher data rates, much larger signal bandwidths will be employed. This will lead to increased usage of higher operational frequencies. Lower frequency bands will still be maintained due to previously defined standards, different requirements (e.g. IoT), improved spectral efficiency, and spectrum sharing. Furthermore, frequency bands below or beyond 6 GHz possess different benefits in terms of range, interference, complexity, cost, etc. The fragmented spectrum may also necessitate inter-band carrier aggregation.

- **Diverse deployments**. Deployment will be diversified beyond macro-, micro- and pico-base stations. Single and multi-antenna transmitters, and signals with different orders of modulation will be utilized.

The key aspect of these requirements is diversity, meaning that the technical implications on the wireless hardware are also diverse.

Figure 1.1 shows an illustration of a traditional single-input-single-output (SISO) wireless transmitter and receiver. In the transmitter, the data is first processed and converted into an analog signal. Thereafter, it is upconverted to a carrier frequency through a mixer and a local oscillator. The upconverted signal is then amplified by a power amplifier (PA) and transmitted through the air by an antenna. The wireless receiver has similar functionality but in the opposite order. The multiple-input-multiple-output (MIMO) technique has been utilized frequently in the evolution of mobile communications [8, 9]. In a MIMO capable transmitter, i.e. a multi-antenna transmitter, multiple coherent transmission paths are spaced closely together. One single DSP block transmits multiple signals through individual branches of mixers, PAs and antennas. The antennas are typically placed in an array. Such a transmitter is shown in Figure 1.2. The MIMO capable receiving block is scaled in the same way, although not necessarily with the same number of branches as the transmitter. MIMO provides many advantages over SISO, such as spatial multiplexing for higher spectral efficiency and beam forming for increased capacity and/or higher system energy efficiency [10–13]. MIMO transmission where the number of transmit branches is significantly larger than the number of receiving branches, i.e. massive MIMO, is believed to be a key technology for future mobile communications [13].

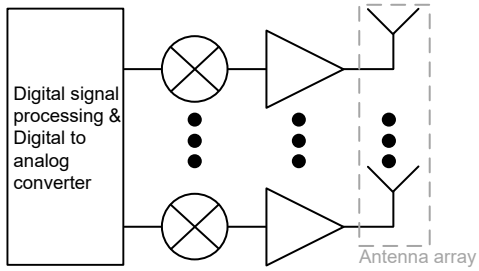


Figure 1.2: Illustration of a multi-antenna transmitter capable of multiple-input-multiple-output (MIMO) communication. All mixers are connected to the same local oscillator.

In the transmitter, the PA constitutes one of the biggest challenges in wireless infrastructures [14], making RF PA research crucial for future mobile communications. RF PAs are not only central in mobile communications, they are also relevant in: other wireless communication systems, such as Bluetooth or WiFi; other wireless technologies, such as radar systems [15]; or other microwave technologies, such as portable microwave ovens [16]. The PAs in these types of technologies also share some of the challenges with PAs for future mobile communications.

1.2 RF Power Amplifier

There are many things to consider in PA design, both inherent properties and system level aspects, such as: output power, energy efficiency, linearity, gain, bandwidth, operational frequency, and cost. The design is dictated by trade-offs: improving one property will often compromise others. The following future wireless infrastructure aspects impose especially large challenges in PA design: signals with high order of modulation having a large peak to average power ratio (PAPR); large signal bandwidths, carrier aggregation, and frequency agility; high operational frequency; and multi-antenna transmitters. These challenges are discussed briefly below.

Signals with large PAPR put stringent requirements on PA energy efficiency. Efficiency is of utmost importance since the PA is one of the most power hungry components in the transmitter [17, 18]. Low energy efficiency results in high operational costs, large heat dissipation and an increased environmental footprint. A PA operating in its most energy efficient mode typically presents a very nonlinear behavior. As systems often have strict linearity requirements in terms of spectral regrowth and in-band distortion, either the raw linearity of the PA must be improved or the PA must be linearized - digitally or by analog circuitry. For "conventional" PAs (e.g. class-B), backing off the output power level typically improves linearity. This, unfortunately, comes at a great energy efficiency cost. Linearization techniques, e.g. digital pre-distortion (DPD), enable high power operation with improved linearity. Linearization, however, increases complexity and consumes power. A conventional PA is often not efficient enough for modern communication signals with a large PAPR. Therefore, *efficiency enhanced* PAs are required. There are many different efficiency enhancement techniques/architectures, which all come at the cost of degrading other PA properties, e.g. complexity and size. A higher complexity makes it more challenging to model the PA. Accurate PA modeling is requisite

for meeting stringent performance requirements. Inaccurate models can lead to long and costly design cycles.

The diversity of carrier frequencies requires either different PAs per band or fewer broadband PAs. Many different PAs require a larger size, resulting in higher material consumption, higher cost and less practical deployment. On the other hand, with known techniques, it is not an easy task to maintain an acceptable PA performance across large RF bandwidths. Large signal bandwidths also necessitate broadband PAs. Furthermore, large signal bandwidths increase cost and complexity of digital signal processing (DSP), e.g. linearization, which could make other PA properties, such as linearity, more important.

To increase the operational frequency, transistor technologies with higher cutoff frequencies f_T are required. In a simplified field-effect transistor (FET) model, f_T is inversely proportional to the gate-source capacitance [19]. Thus, this capacitance must be reduced to enable higher frequencies, which is challenging and degrades other transistor properties. In particular, output power and gain suffer as the frequency is increased. Trying to increase the output power is challenging due to, for instance, large impedance transformation ratios. A low gain decreases system level efficiency and makes it challenging to implement some efficiency enhancement techniques. The gain and output power are also degraded due to larger losses in the matching networks as the frequency increases. When the operational frequency increases, cost typically goes up, making compact designs crucial. Furthermore, measurement accuracy typically decreases, due to, for example, sensitivity to coupling and high loss passives. As a result, it can be difficult to extract accurate transistor and system models.

Compared to SISO, splitting the output power into several PA-antenna branches in MIMO reduces the output power requirement of each individual PA, which could facilitate the PA design. This reduction enables the use of low-power silicon technology (e.g. complementary metal oxide semiconductor, CMOS) for the PAs, which, in turn, enables a higher level of integration, imposing both new possibilities as well as new design challenges. Using a single technology in integration (homogeneous integration) is challenging since one technology is often not the optimal choice for all blocks. Therefore, heterogeneous integration is an emerging strategy [20]. Nevertheless, integration is important to keep size and cost down. Having individual DPD linearization for each PA consumes an unneglectable amount of power. Therefore, improved linearity of the PAs is required to reduce DPD complexity or omit it completely. Heat dissipation becomes a problem if the individual PAs are closely spaced together, making efficiency important. Cross-talk between antennas might reduce PA linearity, but when the number of antennas increases, averaging effects might reduce out-of-band distortion [21]. System and PA modeling also becomes more challenging due to cross-talk.

All PA properties are deeply connected to each other and trade-offs always have to be made. It is often very difficult to determine how to prioritize between the different properties to reach the most cost- and complexity-efficient solution for a certain application. Therefore, PA research consists of concurrently improving PA properties and reducing trade-offs. A profound understanding of the fundamental operation of different PA architectures provides knowledge of how trade-offs can be made and is key for any improvements.

1.3 Thesis Contributions and Outline

The overall research goal of this thesis is to provide new understanding of different PA architectures, related circuits and design methods through analytical approaches. It will be shown that these analytical approaches, together with minimizing unnecessary restrictions in topology and functionality, lead to expanded design spaces. With an expanded design space, it is possible to identify novel solutions with improved trade-offs between different properties. In addition, these analytical approaches provide better understanding of the fundamental operation of a given architecture/circuit, which gives insights into its possibilities and limitations. Overall, the thesis presents different promising techniques for improved performance in high-efficiency PAs, such as improvements in linearity, gain, integration, losses, and design methodology.

In Chapter 2, the most common efficiency enhancement PA architectures are discussed, and relevant theoretical background is provided. Focus is put on the active load modulation (ALM) category of PA efficiency enhancement techniques. The chapter discusses the working principle of ALM PAs, which is determined by both the operation of the individual transistors and the combining networks.

Chapter 3 focuses on a core concept in this thesis: the generalization possibilities when using an analytical approach in the combiner design. In this approach, the combiner topology is first assumed to be an unknown network – a *black box*. The parameters of the black-box network are then solved in terms of defined boundary conditions, such as transistor loading conditions for high efficiency. After that, with the network parameters solved, the black-box combiner is synthesized. The black-box approach is first applied to the Doherty PA. It is shown how this contribute with better understanding of the working principle of the architecture, and how it can be used for improved performance. In particular, improved efficiency and integration by using an antenna as the combiner [Paper A] and an improved efficiency-linearity trade-off are demonstrated [Paper B]. Furthermore, the black-box approach is applied to an isolated two-way power divider [Paper C]. This approach unlocks many new possibilities, such as improved integration and layout flexibility.

Chapter 4 presents an analytical approach to the emerging efficiency enhancement PA architecture: the load modulated balanced amplifier (LMBA) [22]. One particular embodiment of the LMBA is the Doherty-like RF-input LMBA [Paper D]. This variant is derived analytically and is compared to the Doherty PA – its closest competitor. The Doherty-like RF-input LMBA presents some interesting advantages compared to the Doherty PA, such as higher gain.

Chapter 5 presents a new measurement-based design methodology for ALM PAs [Paper E]. An active load-pull measurement setup excites a single device under test in different states in turn, the states corresponding to the different transistors in an ALM PA. This allows for a performance prediction in an early design stage where the full ALM PA behavior is captured by measurements. Moreover, the new methodology provides measurement-based insights into the internal operations of the different transistors, which can provide knowledge of the ALM PA working principle beyond the ideal theory, which in turn can facilitate designing ALM PAs for optimal performance.

Chapter 6 concludes the thesis and discusses future work.

Chapter 2

Efficiency Enhancement Techniques

In order to meet mobile communications demands, many different strategies for PA design have been implemented. Energy efficiency enhancement is on the top of the list of required attributes, and it can be accomplished by various techniques that come with different pros and cons. This chapter gives a brief overview of the most common energy efficiency enhancement techniques, with a focus on load modulation architectures.

2.1 Goal of Efficiency Enhancement

In the evolution of wireless communication systems, the need for higher spectral efficiency has led to higher order modulation schemes [23]. The large amplitude variation of these schemes results in a large difference between the signal peak power and average power. For example, in long term evolution-advanced (LTE-Advanced), a single downlink carrier has roughly 9 dB PAPR, and up to 12 dB PAPR for a two-carrier aggregation [24].

The large variations in the instantaneous transmitted power result in severe degradation of the average energy efficiency of conventional PAs, since the PA has to operate at the average power to avoid clipping of the signal. This is because the drain efficiency is, by default, reduced as the delivered power is backed off. The drain efficiency, i.e. the ratio of delivered power P_{del} over the DC power P_{DC}, of an ideal transistor [i] can be expanded to[1,2]:

$$\eta = \frac{P_{\mathrm{del}}}{P_{\mathrm{DC}}} = \frac{0.5 R_{\mathrm{l}} |I_{\mathrm{ds}}|^2}{V_{\mathrm{DS}} I_{\mathrm{DS}}} \tag{2.1}$$

where R_l is the fundamental load termination, I_{ds} is the fundamental drain current, V_{DS} is the supply voltage and I_{DS} is the DC current. For class-B,

[1] Throughout this thesis, signals are denoted the following way. Time domain: lower case letter with upper case subscripts (v_{DS}). DC component: upper case letter with upper case subscripts (V_{DS}). Fundamental frequency component: upper case letter with lower case subscripts (V_{ds}).

[2] FET terminology is used throughout this thesis although the derivations are technology independent.

both the fundamental drain current I_{ds} and the drain DC current I_{DS} are proportional to the normalized input voltage drive level β [i]. As a result, the drain efficiency is proportional to β, i.e.

$$I_{\mathrm{ds}} \propto \beta \text{ and } I_{\mathrm{DS}} \propto \beta \;\Rightarrow\; \eta \propto \beta. \tag{2.2}$$

Thus, the drain efficiency is maximum at the maximum drive level and it decreases as the drive level decreases. Since the ideal class-B transistor is linear, the delivered power is proportional to the square of the voltage drive level.

To address the problem of low average energy efficiency of the PA for signals with high PAPR, different methods of making the drain efficiency less dependent on the drive level (or delivered power) have been implemented. The goal is to maintain a constant high efficiency for a large range of drive levels. The two most common categories of energy efficiency enhancement are dynamic supply modulation (DSM) and dynamic load modulation (DLM). These two categories are discussed in detail in this chapter.

DLM and DSM come with different benefits and disadvantages, and are suitable for different applications. Although both categories can be implemented with transistors operating in any PA class, they are, for simplicity, demonstrated here using class-B mode transistors. Nonetheless, the operating class has a big impact on the overall performance of the efficiency enhanced PA. Since efficiency enhancement aims to maintain an efficiency level over a large dynamic range of delivered powers, this efficiency level should be as high as possible. Selecting a switched mode PA class can yield very high efficiencies, but is increasingly challenging as the frequency becomes higher and might make broadband designs more challenging.

In addition to DLM and DSM, other types of high energy efficiency PA configurations exist. There are architectures that fully exploit switch-mode PAs. Examples of such are class-S [25, 26] or pulse width modulation (RF-PWM) [27–29]. There is also the sequential PA [30, 31], where auxiliary transistors boost the total output power without affecting the main transistor. Even though many of these "other" types of efficiency enhanced PAs can be used in conjunction with DLM or DSM, or are related to DLM or DSM, they are out of scope of this thesis.

2.2 Dynamic Supply Modulation (DSM)

The first presented DSM technique is envelope elimination and restoration (EER) [32]. EER is a polar transmitter, where the PA is fed with a phase only modulated input signal, and supply voltage modulation introduces the amplitude modulation of the output signal [33]. Nowadays, the most common DSM technique is envelope tracking (ET), where a both phase and amplitude modulated RF signal is fed to the PA, and the supply is dynamically modulated along with the envelope variations of the input signal [34, 35]. In other words, V_{DS} is made proportional to the drive level β, i.e.

$$V_{\mathrm{DS}} \propto \beta. \tag{2.3}$$

As a result, the drain efficiency becomes independent of β. The DSM principle is illustrated in Figure 2.1. It is, however, important to recognize the limits of

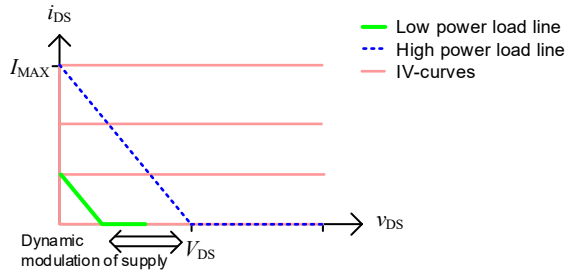


Figure 2.1: Load lines for supply modulation of class-B operation. The drain bias is modulated dynamically as a function of the drive level.

the ideal transistor model here. For real transistors, when the value of V_{DS} is low, the drain efficiency can be approximated by the following equation [36,37]:

$$\eta = \frac{\eta_{max}}{1 + \zeta_1 \frac{R_{on}}{R_l}} \tag{2.4}$$

where η_{max} denotes the maximum possible drain efficiency for the operation of choice. R_{on} is the on-resistance. ζ_1 is a constant depending on the current and voltage waveforms, i.e. a constant depending on the operation of choice, e.g. 2 for class-B. It is also important to mention that the envelope amplifier (EA) providing the supply modulation constrains the performance of the whole circuit. For example, the EA consumes power and therefore degrades the energy efficiency of the whole circuit.

ET provides high efficiency and a large RF bandwidth [38]. ET does, however, have limited signal bandwidth and output power capabilities due to the EA. The EA tracking bandwidth, relative to the signal bandwidth, is determined by an envelope shaping function, which in turn is determined from trade-offs between efficiency, linearity, bandwidth expansion and complexity [39]. Furthermore, efficient ($> 90\%$) EAs are limited to around 100 MHz of bandwidth [38]. Recently, it has been shown that it is possible to use the sum of the envelope of a plurality of signals in concurrent operation as the EA tracking signal, making it feasible to employ efficient ET for multiple signals widely spaced apart [40–42]. In this approach, the tracking bandwidth is approximately the same as the largest single signal bandwidth. However, as the number of concurrent signals increases, the efficiency enhancement, over a constant supply, decreases.

2.3 Dynamic Load Modulation (DLM)

In DLM, the fundamental load termination is modulated dynamically as an inverse function of the envelope variations of the signal. In other words, R_l is made inversely proportional to the drive level β, i.e.

$$R_l \propto 1/\beta. \tag{2.5}$$

As a result, the drain efficiency becomes independent of β. The DLM principle is illustrated in Figure 2.2. Again, it is important to recognize the limits of the ideal transistor model. For real transistors, one mechanism that limits

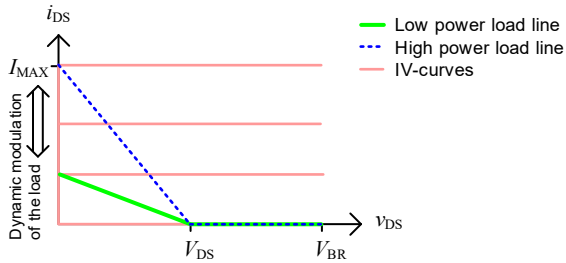


Figure 2.2: Load lines for load modulation of class-B operation. The fundamental load termination resistance is modulated dynamically as an inverse function of the drive level.

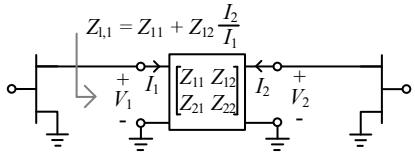


Figure 2.3: Illustration of a two-way ALM PA and the load presented to the first transistor. The load termination is absorbed into the combiner.

the drain efficiency of a DLM PA is parallel losses [36, 43, 44]. This can be expressed as

$$\eta = \frac{\eta_{\max}}{1 + \zeta_2 \omega_0^2 C_{\mathrm{ds}}^2 R_{\mathrm{p}} R_{\mathrm{l,p}}} \tag{2.6}$$

where C_{ds} and R_{p} are in series elements representing parallel losses at the transistor output. $R_{\mathrm{l,p}}$ is the effective parallel resistance of the load termination. ζ_2 is a constant depending on the current and voltage waveforms. It is easy to see how the drain efficiency enhancement at backed-off power levels is limited as $R_{\mathrm{l,p}}$ increases. Furthermore, in [43] it was shown that the waveforms are not constant during load modulation, making ζ_2 nonlinear versus drive level. After all, the waveforms interact with the knee-voltage differently at different drive levels. Proper harmonic terminations therefore play a crucial role for maintaining high efficiency throughout the dynamic range of load modulation [45–47].

DLM can be divided into varactor-based DLM (VDLM) and active current injection-based DLM - also called active load modulation (ALM). VDLM utilizes varactors to tune the load [48], whereas ALM utilizes active current injection to tune the load, as in for example Chireix outphasing [49], the Doherty PA [50], and the load modulated balanced amplifier (LMBA) [22].

In ALM, the outputs of a plurality of transistors are connected by a combiner, the combiner also being terminated with a load. If the load is absorbed into the combiner, the load presented to the first transistor out of N can be expressed in terms of individual transistor fundamental drain currents and the lossy N-port combiner as

$$Z_{\mathrm{l},1}(\beta) = Z_{11} + \sum_{i=2}^{N} Z_{1i} \frac{I_i(\beta)}{I_1(\beta)}. \tag{2.7}$$

An illustration of a two-way ALM PA is shown in Figure 2.3. It can be seen that an asymmetry between currents versus the drive level, together with an appropriate combiner, results in variation of $Z_{\mathrm{l},1}$. The asymmetry in the currents can be in magnitude and/or phase. Different number of transistors

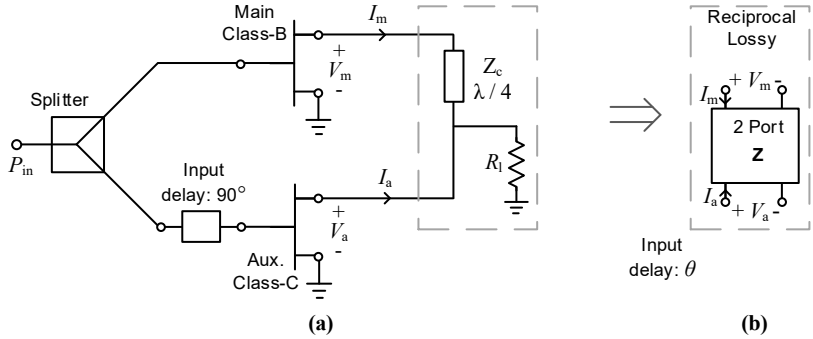


Figure 2.4: (a) Conventional ideal two-way Doherty PA with single RF-input. (b) A generalized representation of the combiner and the input phase delay.

and different current profiles versus the drive level is the basis for different ALM architectures. If the phase difference between the currents is static versus drive level, but the magnitude ratio between the currents varies versus drive level, the operation corresponds to the working principle of the Doherty PA. The other way around, a static magnitude ratio but varying phase difference versus drive level corresponds to the working principle of the mixed-mode Chireix outphasing PA. It is also possible to design an ALM PA using a mix of amplitude and phase asymmetry [51, 52]. The load modulated balanced amplifier (LMBA) can be seen as two-way (two branches) ALM PA where one branch comprises a balanced amplifier. In the LMBA, load modulation can be achieved by amplitude and/or phase asymmetry versus the drive level. It should also be mentioned that the combiner in an ALM PA can be selected such that asymmetries in the currents are cancelled out, such that there is no load modulation for the main branch, as is the case for the sequential PA [30, 31].

Different DLM architectures present different advantages and challenges over each other. The common challenges for all ALM architectures are to find a suitable way to generate the current profiles (with low complexity, low loss, etc.) and to realize an appropriate combiner (low loss, large bandwidth, compact, etc.). The most important challenges of the VDLM PA are to find suitable varactors (with low loss, high power handling, etc.) and to incorporate the varactors into the variable output matching network (OMN) effectively (presenting low loss and a large bandwidth, being compact, etc.).

2.3.1 Doherty PA

The Doherty PA was first introduced in 1936 [50]. A schematic of this "conventional" implementation is shown in Figure 2.4(a). It is characterized by the quarter-wave transformer output combiner and the 90 degree input phase delay. The load modulation of the main transistor, achieved by magnitude asymmetry between output currents of the two transistors versus drive level, is often achieved by having the main transistor in class-B operation and the auxiliary transistor in class-C operation. For low drive levels, the auxiliary transistor is not conducting, causing the current magnitude ratio to be zero, see (2.7). At some intermediate drive level, the auxiliary transistor starts to conduct and the current magnitude ratio starts to increase versus drive level. The conventional Doherty PA was designed to have one efficiency peak at peak

power and one at 6-dB output power back-off (OPBO). This high efficiency range (denoted γ) can actually be arbitrary if a certain relationship between the main and auxiliary transistor currents is met (typically by increasing the size of the auxiliary transistor) [53, 54]. Although the conventional Doherty PA topology consists of an input power splitter between the main and auxiliary transistor, the Doherty PA operation can also be achieved with individually controlled dual RF-inputs [55, 56].

It is not necessary to base the topology and phase delay on the conventional configuration in order to achieve the "Doherty-like" behavior. A generalized way of looking at the output combiner and phase delay is shown in Figure 2.4(b). Treating the combiner as a *black-box* was first described in [57]. This approach is beneficial in many different ways: improved efficiency [57, 58] [Paper A]; expanded design space [g]; or improved linearity [Paper B]. This is discussed in detail in Chapter 3.

One drawback of the conventional Doherty PA is the limited RF bandwidth, constrained by the quarter-wave transformer and transistor parasitics. This problem has been studied extensively in literature. The RF bandwidth can be improved by parasitic absorption into the combiner [59,60] and/or modifications to the quarter-wave transformer [61–65].

The single RF-input Doherty PA typically sacrifices a substantial amount of gain compared to a single-ended class-B PA. At back-off, when the auxiliary transistor is off, all power split into the auxiliary transistor is just wasted. To make things worse, the class-C bias of the auxiliary transistor necessitates a large fraction the input power being split into it. Typically, the gain degradation becomes larger for increasing values of the range γ, as the auxiliary transistor grows in size, which typically lowers the gain of an individual transistor. The gain degradation becomes a huge problem at millimeter-wave frequencies, as the transistor gain is often limited to begin with. Chapter 3 [g] addresses this problem by proposing a modification of the Doherty PA for improved gain.

Another drawback of the conventional Doherty PA is linearity. Despite the architecture being linear when using ideal transistors, real transistors present severe nonlinearities. Typically, the transistors are driven into deep compression to achieve high efficiency, and load modulation causes a nonlinear phase response due to the feedback-capacitance [66–68]. This problem is often overcome by linearization using DPD. Unfortunately, DPD increases complexity and cost, which limits its usage in some applications. Chapter 3 [Paper B] proposes a modification to the Doherty PA that makes the phase response more linear, which, in turn, makes it possible to reduce DPD complexity - or possibly omit it completely.

Losses in the combiner limit the performance at millimeter-wave frequencies. This naturally degrades the efficiency and gain, which both are scarce to begin with at those frequencies. This can be mitigated by incorporating different technologies for the transistors and the combiner and bonding them together [69] or by modifying the combiner [70].

The auxiliary transistor has an inherently suboptimal load modulation at intermediate power levels, meaning that the voltage swing is not maintained at the maximum level. This causes a drop in efficiency between the two efficiency peaks. This dip becomes more severe for large values of the range γ. This problem can be overcome by introducing additional auxiliary branches, e.g.

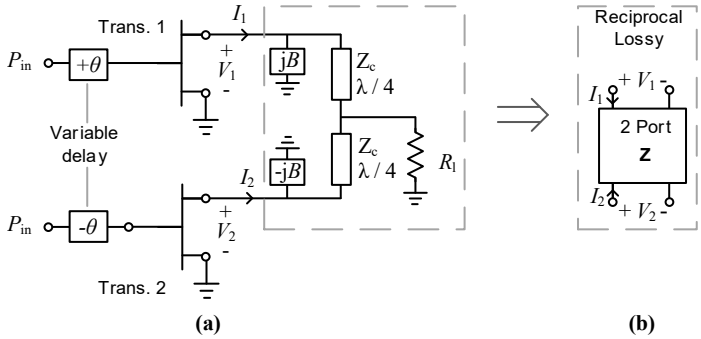


Figure 2.5: (a) Conventional ideal Chireix outphasing PA. (b) A generalized representation of the combiner.

a three-way Doherty PA [71–73]. This approach complicates the combiner, decreases the gain in the single RF-input case, or increases complexity in the multiple RF-input case.

For a single RF-input Doherty PA, the phase difference between the main and auxiliary transistor currents is static at the input. The nonlinear transfer functions of the phase for the two transistors versus drive level, however, causes the phase difference between the drain currents to be nonlinear versus drive level. The combiner can still be solved to present optimal impedances at peak output power and at back-off (where the auxiliary transistor is off). The nonlinear phase difference at the output, unfortunately, causes sub-optimal load-modulation at intermediate power levels for both transistors. This effect can be compensated for by using a nonlinear phase difference at the input in a dual RF-input Doherty PA [74,75], which, of course, is an increase in complexity. Interestingly, this strategy makes the input driving functions become more similar to the ones of mixed-mode Chireix outphasing.

2.3.2 Chireix Outphasing

The Chireix outphasing PA is, like the Doherty PA, an architecture introduced long time ago (1935) [49]. A schematic of a typical implementation [76] of the architecture is shown in Figure 2.5(a). This combiner is characterized by two quarter-wave transmission lines and two opposite susceptive "compensation" elements. The load modulation of both transistors is achieved by phase asymmetry between the output currents of the transistors (I_1 and I_2). The two currents have an equal magnitude. These current profiles are often achieved by having both transistors equal in size and operation, e.g. class-B, and with phase control of the two separate RF-input signals. Compared to the Doherty PA, the suboptimal load modulation at intermediate power levels can in theory be made less severe in the Chireix outphasing PA, making it possible to obtain an overall higher efficiency in the high power region.

The original version of the architecture has a constant power into the two branches, and the output power is controlled only by outphasing. This mode is typically referred to as pure-mode. A drawback of pure-mode outphasing is the difficulty to achieve perfect cancellation of the branch signals at the load through outphasing, thus limiting the dynamic range of the possible signals [76]. This can be overcome if the input amplitude is also modulated and the phase

asymmetry is made a function of the input drive level [77]. This mode is typically referred to as mixed-mode. In this mode, the phase difference between the two currents is fixed for low drive levels and then starts to vary versus drive level. Furthermore, mixed-mode outphasing typically presents higher efficiency at deep OPBO compared to pure-mode [76].

Most Chireix outphasing PAs utilize two individually controlled RF-inputs [76]. Nevertheless, it is possible to generate the mixed-mode driving profiles using a nonlinear analog input signal splitter with diodes [78–81]. Two challenges in this approach are the diode losses – a problem that typically increases as the frequency increases – and limited bandwidth.

Similar to the combiner of the Doherty PA, it is not necessary to base the outphasing combiner on the Chireix topology. A generalized way of looking at the combiner is shown in Figure 2.5(b) [82, 83]. This black-box approach was applied using empirical load-pull data in [82], demonstrating that this approach leads to an easier realization of the circuit and a more compact combiner. In [83], the method was applied analytically using transistors operated in class-E mode. It was demonstrated how the method allows a more broadband combiner, when the design is not constrained by the conventional topology, while still maintaining high efficiency. The black-box approach has been demonstrated to yield excellent performance when either extracting loading conditions at the extrinsic (package) plane [82] or at the intrinsic (current source) plane [84].

The conventional Chireix combiner limits the RF-bandwidth severely. The two quarter-wave transmission lines naturally limit the bandwidth, but the two opposite sign susceptive compensation elements – often implemented in an inductive and capacitive fashion – also limit the bandwidth. Modifications of the combiner can improve the bandwidth [83]. Yet, the best reported bandwidth of Chireix outphasing PAs (33% in [83]) comes nowhere near the best reported bandwidth of Doherty PAs (87% in [65]), despite [83] having dual RF-inputs and [65] only having one. It should also be mentioned that the signal bandwidth is limited in Chireix outphasing since different RF frequencies often require different phase asymmetries in the input signals.

2.3.3 Load Modulated Balanced Amplifier

The load modulated balanced amplifier is a very recent architecture (2016) [22]. A schematic of the architecture is shown in Figure 2.6. The idea is to have a quadrature balanced amplifier and to inject a control signal at the isolation port of the output coupler. This control signal modulates the loads presented to the two equal main transistors in the balanced branch. In one way, this architecture can be seen as a two-way ALM architecture where the main branch comprises a balanced amplifier. The control signal from the auxiliary transistor can induce load modulation presented to the main transistors using magnitude and/or phase asymmetry versus drive level (in respect to the main transistor currents). Thus, the architecture can be used in many different ways, e.g. like a Doherty PA or more like an outphasing PA. In Chapter 4 [Paper D], one particular embodiment of the LMBA is presented, analyzed and discussed: the Doherty-like RF-input LMBA. A comprehensive literature survey of the LMBA is saved for that chapter. In the next section, some properties of the Doherty-like RF-input LMBA are compared to the other DLM architectures, where

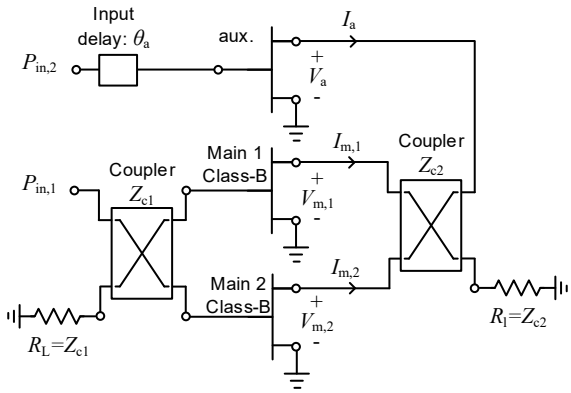


Figure 2.6: (a) Ideal load modulated balanced amplifier.

it is shown that the Doherty-like RF-input LMBA presents some interesting advantages.

2.3.4 Varactor-Based DLM

Compared to the Doherty PA and Chireix outphasing PA, VDLM is a more recent architecture (2003) [48]. The VDLM operation is illustrated in Figure 2.7. A voltage across the varactor tunes its capacitance. This voltage is controlled by a high speed and highly efficient voltage amplifier. In contrast to DSM, this signal envelope tuning does not affect transmitter energy efficiency significantly, since the voltage amplifier provides an insignificant amount of power. Tunable OMNs can have other uses in addition to load modulation. They can be used for, e.g., compensate for antenna mismatch, for increasing power transfer [85] or for improving digital linearization [86]. It has been shown that antenna mismatch compensation can be used concurrently with load modulation [87]. It has also been shown that the load modulation, enabled by VDLM, can be selected for linearity improvements [88, 89].

As mentioned, the challenges in VDLM are in the varactor(s) itself and how to incorporate it into the tunable OMN. Low breakdown voltage of varactors limited the delivered power in early VDLM PA designs. However, as new varactors with higher breakdown voltage while maintaining tuning capabilities emerged, delivered power levels have been scaled up to 86 W [90]. The varactor must present high tuning capabilities if a single varactor control signal is used for DLM across a large bandwidth. On the other hand, a tunable OMN consisting of two varactor control signals allows the tuning capabilities of the varactors to reduced significantly, but at the cost of circuit complexity [91]. The effective tuning range across a large bandwidth for single varactor control can be extended by reconfiguring the drain bias versus frequency [92]. It should be mentioned, however, that the efficiency enhancement is degraded for large signal bandwidths if different RF frequencies require different varactor control signals. One of the major drawbacks of VDLM is the varactor losses, which can severely degrade the efficiency compared to the ideal theory [93].

In many designs, e.g. [94–97], optimum load trajectories have been found empirically by load pull measurements, resulting in limited understanding of the best way of realize the tunable OMN. However, theoretical analyses

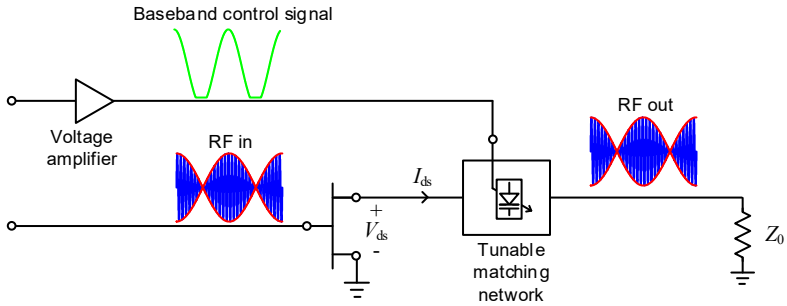


Figure 2.7: Varactor-based dynamic load modulation architecture.

for effective OMNs have been explored for: single varactor control class-E PAs in [48]; single varactor control class-J PAs in [93]; and single varactor control wideband class-J PAs [h], [98]. These analyses have provided better understanding of how to incorporate the varactor(s) into the design and how the tunable OMN should be realized in the best ways.

2.4 Comparison of DLM Architectures

It is rather difficult to compare different DLM architectures in a fair way, especially since there are a vast number of modifications to each architecture addressing different drawbacks. In particular, Doherty, Chireix outphasing, and Doherty-like LMBA can all be realized either with single RF-input or dual RF-inputs. Nevertheless, in this section, the different DLM architectures are compared in their basic forms. The following architectures are compared: two-way Doherty, pure-mode Chireix outphasing, VDLM, and Doherty-like RF-input LMBA. In this comparison, the main transistor refers to: the main transistor in the Doherty PA; either of the two transistors in the Chireix outphasing PA; the one transistor in the VDLM PA; and one of the two equal main transistors in the LMBA. The main transistor is in class-B operation and the auxiliary transistor is in class-C operation. All transistors are assumed to have the same supply voltage unless otherwise specified.

Figure 2.8(a) shows an example of the drain efficiency versus delivered power for the different architectures, targeting a second efficiency peak at 8 dB OPBO (i.e. $\gamma = 8$ dB). For the LMBA and Doherty PA, the efficiency has been calculated assuming a piece-wise approximation of the class-C current [Paper D, g,i]. The Chireix outphasing PA efficiency is calculated using the equations from [99]. The VDLM assumes perfect class-B load modulation. It can be seen that the Chireix outphasing PA and VDLM both present the highest efficiency in the load modulation region, and that the Chireix outphasing PA efficiency is lower at deep back-off.

Other relevant metrics for these ideal versions of the architectures are summarized in Figure 2.8 and are discussed below. These metrics are gathered from [Paper D, g,i]. A table summarizing the analytical functions of these metrics is presented in [Paper D].

Range of efficiency enhancement

One interesting thing to compare is how much parallel losses degrade the efficiency, see (2.6). Due to the parallel losses, it is only effective to utilize load modulation across a certain dynamic range below the maximum delivered power ($P_{\mathrm{del,max}}$). This dynamic range can be defined as

$$\frac{P_{\mathrm{del,max}}}{P_{\mathrm{del,bo}}} = \gamma \tag{2.8}$$

where $P_{\mathrm{del,bo}}$ is the backed-off power level where the second efficiency peak occurs. The range γ is typically selected to maximize the efficiency for a modulated signal with a given probability density function. Often, that translates to selecting γ close to the PAPR of the signal [100]. Since parallel losses limit the dynamic range where high efficiency is possible for a single transistor, it is interesting to study how much the individual transistors have to be backed-off in an ALM PA. The ratio of peak and backed-off power for one main transistor can be expressed as

$$\frac{P_{\mathrm{del,m,max}}}{P_{\mathrm{del,m,bo}}} = \frac{1}{\beta_{\mathrm{bo}}}. \tag{2.9}$$

This parameter β_{bo} can be expressed in terms of the range γ for the different architectures [Paper D]. One function of the auxiliary transistor can be seen as improving the high efficiency range for the whole PA (over a single transistor). This comes from the auxiliary transistor contributing power to the load at maximum drive level, but not any power at back-off.

Figure 2.8(b) shows β_{bo} versus the range γ. It can be seen that for $\gamma = 6$ dB, the main transistor has to backed-off 3 dB for the Doherty PA, 4.8 dB for the LMBA and 6 dB for the Chireix outphasing PA and VDLM PA. In terms of being affected by parallel losses, the Doherty PA comes out as the clear winner in this idealized comparison. Thus the Doherty PA should present the highest back-off efficiency for large values of the range γ. However, it should be mentioned that it is highly important to maintain optimal waveforms throughout the load modulation in a more realistic scenario, see the discussion around (2.6).

Gain compression and gain

Figure 2.8(c) shows the gain compression, i.e. the gain at the maximum drive level relative to the small signal gain, versus the range γ. It can be seen that the Doherty PA has a linear gain, the VDLM PA is severely nonlinear, and that the LMBA is somewhere in-between. The gain compression due to load modulation is less severe when real transistor models are used. However, all architectures typically present nonlinear gain when real nonlinear transistor models are used, since they are typically driven into compression to reach high efficiency. The gain characteristic of the pure-mode Chireix outphasing PA makes it difficult to compare with the others. The small signal gain of the Doherty PA and Doherty-like RF-input LMBA is lower compared to a single-ended PA, since the auxiliary transistor is not conducting at back-off. The Chireix outphasing and VDLM PAs do not have this issue.

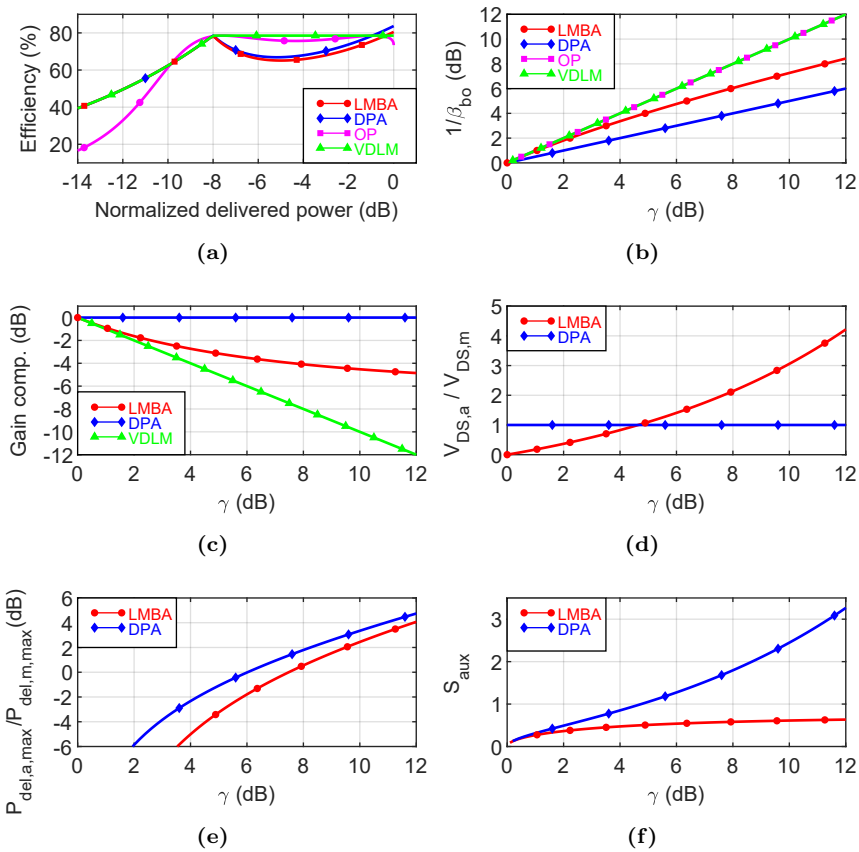


Figure 2.8: Metrics for the RF-input load modulated balanced amplifier (LMBA), the Doherty PA (DPA), the Chireix outphasing PA (OP), and the varactor-based dynamic load modulation PA (VDLM). (a) Efficiency example for $\gamma = 8$ dB. (b-f) metrics versus the range of efficiency enhancement γ.

Supply voltage ratio

Figure 2.8(d) shows the supply voltage of the auxiliary transistor, relative to the main transistor, versus the range γ. This demonstrates one of the drawbacks of the Doherty-like LMBA. Since the coupler mainly is selected to optimize the impedances for the balanced branch, the load of auxiliary transistor cannot be selected freely. To overcome this, the supply voltage of the auxiliary transistor can be adjusted such that an optimal impedance is presented. This, however, limits the possible values of γ in a realistic scenario.

Power and size ratio

Figure 2.8(e) shows the maximum power delivered from the auxiliary transistor, relative to the maximum power from the main transistor, versus the range γ. Figure 2.8(f) shows the size of the auxiliary transistor relative to the main. The size is referring to the maximum DC current of a transistor. These figures demonstrate a drawback of the two-way Doherty PA. For large values of γ, the auxiliary-main power ratio becomes large. Consequently, the relative size of

the auxiliary transistor also becomes large. In practice, this leads to a large fraction of input power into the auxiliary transistor, which in turn leads to lower gain. The Doherty-like RF-input LMBA has the same problem but it is less severe. The auxiliary transistor size of the LMBA is low for large values of γ since the auxiliary transistor supply voltage is unreasonably large.

Discussion

Among the presented idealized DLM architectures, the Doherty PA is most linear and is the least affected by parallel losses. The nature of the auxiliary branch makes the architecture less sensitive to parallel losses, but at the cost of a dip in the efficiency in the load modulation region (due to the suboptimal load modulation of the auxiliary transistor). A drawback of the Doherty PA is the gain degradation for large values of γ. The Doherty-like RF-input LMBA is similar to the Doherty PA but where both the positive and negative aspects are less severe. The drawbacks of the Doherty-like RF-input LMBA are the limited values of γ and gain compression. The Chireix outphasing PA has high efficiency in the load modulation region, is more flexible for different values of γ but is quite affected by parallel losses. The VDLM PA has high efficiency in the load modulation region but presents a severe gain compression and is quite affected by parallel losses.

Having dual RF-inputs necessitates two complete baseband to RF up-conversion paths. This extra circuitry is not viable in many applications. In the applications where it is viable, there is no need whatsoever to limit the operation of the two transistors to either Doherty or mixed-mode outphasing. A combiner designed for a mix of phase and amplitude asymmetry in the output currents versus drive level was demonstrated in [51, 52]. This dual RF-input two-way ALM PA is one of the best performing broadband and efficient PAs reported, especially when considering the theoretical results. It should be mentioned that this concept has not been studied as much as it deserves, although it has gotten some traction recently [101].

Chapter 3

Analytical Combiners for Active Load Modulation PAs

The working principle of ALM PAs is determined by both how the individual transistors are operated and how their outputs are combined. If the output combiner topology is first assumed to be fixed, the available ways to operate the transistors for high efficiency becomes limited. A new design space of possible ways of operating the transistors opens up, if, on the other hand, the combiner is first assumed to be an arbitrary *black-box*. The black-box approach starts off with only a few assumptions of the transistor operation, e.g. if the operation should be Doherty-like or like mixed-mode outphasing. The exact operation of the transistors, e.g. phase delays, the transistor size ratios, and the network parameters of the combiner are then solved in terms of predefined boundary conditions, such as transistor loading conditions for high efficiency. With the network parameters of the combiner solved, the circuit realization of the combiner can be based on well-known techniques.

The black-box approach was first demonstrated on a two-way Doherty PA [57]. It was shown that the new design space allows for improved efficiency when using two identically sized transistors. Later it was also demonstrated for a mixed-mode Chireix outphasing PA [82]. In this chapter, the new two-way Doherty PA design space enabled by the black-box approach is studied further. The whole continuum of solutions for maximum efficiency operation [g] and a new set of solutions for improved linearity [Paper B] are derived analytically. It is also shown that the black-box approach can be used for increased integration in a transmitter. This chapter shows that a dual-fed antenna can be used as both the Doherty PA combiner and the radiator [Paper A]. It is possible to design the antenna to present the two-port network parameters for optimal transistor loading conditions, where the parameters are derived from the black-box equations. Finally, the chapter shows that the black-box approach is equally suitable for expanding the design space of isolated dividers. Design equations for a two-way isolated divider are analytically derived and explored [Paper C].

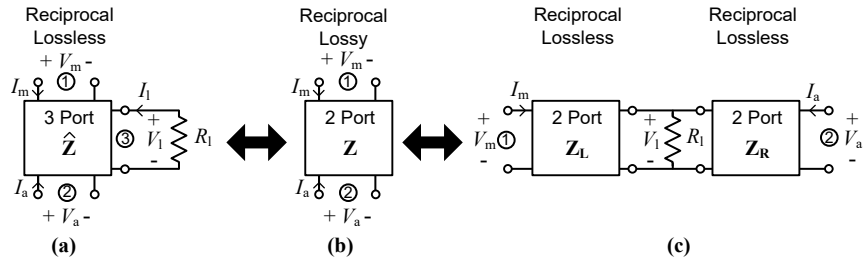


Figure 3.1: Black-box representation of a two-way combiner with (a) external load termination and (b) the load termination absorbed. (c) Representation of the black-box combiner for simple realization.

3.1 Black-Box Combiner Approach

The black-box method can easily be used for many different scenarios. In this section, the method is explained using a non-isolating two-way combiner for ALM PAs.

A two-way combiner can be represented in many different ways. It is reasonable to assume that the combing should be done passively without any losses. Therefore, a two-way combiner can be represented by a reciprocal and lossless three-port network $\hat{\mathbf{Z}}$ with the third port terminated, see Figure 3.1(a). It is convenient to absorb the load termination into the combiner since the dimension of the network is reduced. Thus, another representation of a two-way combiner is a reciprocal and lossy two-port network, see Figure 3.1(b). For simple network realization, a two-way combiner can also be represented by two lossless and reciprocal two-port networks with the load termination in-between, see Figure 3.1(c). These two-port networks ($\mathbf{Z_L}$ and $\mathbf{Z_R}$) can be synthesized using, for example, Π- and/or T-networks. This is described in detail in [58, 83] and is not covered in this thesis.

As discussed in Section 2.3, the loads presented to the different transistors in an ALM PA can be expressed in terms of both the combiner parameters and the transistor drain currents. Below, boundary conditions for a two-way ALM PA combiner are defined. For later analysis, the first transistor is denoted main (subscript m), and the second transistor is denoted auxiliary (subscript a). The boundary conditions are to present predetermined target fundamental load impedances at two distinct drive levels. These can be expressed in terms of the reciprocal and lossy two-port network $\mathbf{Z}$ [Figure 3.1(b)] as

$$Z_{\mathrm{l,m,max}} = Z_{11} + Z_{12}\alpha_{\max} \tag{3.1}$$

$$Z_{\mathrm{l,a,max}} = Z_{22} + Z_{12}/\alpha_{\max} \tag{3.2}$$

$$Z_{\mathrm{l,m,bo}} = Z_{11} + Z_{12}\alpha_{\mathrm{bo}} \tag{3.3}$$

$$Z_{\mathrm{l,a,bo}} = Z_{22} + Z_{12}/\alpha_{\mathrm{bo}} \tag{3.4}$$

where

$$\alpha_{\max} = I_{\mathrm{a,max}}/I_{\mathrm{m,max}} \qquad \text{and} \qquad \alpha_{\mathrm{bo}} = I_{\mathrm{a,bo}}/I_{\mathrm{m,bo}} \tag{3.5}$$

are fundamental drain current ratios and the maximum and backed-off drive levels, respectively. The subscript *max* refers to the maximum drive level, i.e. $\beta = 1$; *bo* refers to a predetermined backed-off drive level, i.e. $\beta = \beta_{\mathrm{bo}}$.

The different Z_l are predetermined "optimal" load terminations for the two transistors at the two drive levels. An additional equation originate from that it must be possible to convert the reciprocal and lossy two-port network $\mathbf{Z}$ to the reciprocal and lossless three-port network $\hat{\mathbf{Z}}$ with the third port terminated with the load termination [57]:

$$\Re\{Z_{12}\}^2 = \Re\{Z_{11}\}\Re\{Z_{22}\}. \tag{3.6}$$

In the Doherty PA, for example, this equation determines the static phase difference between the main and auxiliary transistor fundamental drain currents.

Once the reciprocal and lossy two-port network $\mathbf{Z}$ is solved in terms of target load impedances, it is interesting to analyze the voltage across the load termination, V_l. Expressing the three-port impedance parameters $\hat{\mathbf{Z}}$ in terms of the two-port impedance parameters $\mathbf{Z}$ results in an under-determined system of equations. For simplicity, $\hat{Z}_{33}$ can be set to zero, and the voltage across the load termination can be expressed as [Paper B]

$$V_\mathrm{l} = \pm j\sqrt{R_\mathrm{l}\Re\{Z_{11}\}}I_\mathrm{m} \pm j\sqrt{R_\mathrm{l}\Re\{Z_{22}\}}I_\mathrm{a}. \tag{3.7}$$

The four solutions arise from the periodic nature of the phase of the current ratio.

With the black-box combiner approach generally explained, the next section explores the new possibilities when it is applied to a two-way Doherty PA. The subsequent section presents the required modifications and new possibilities when applying the black-box approach to isolated two-way dividers.

3.2 Black-Box Combiner Doherty Amplifier

Although generalizations of circuits can lead to improved performance, many modifications of the Doherty PA in literature are unnecessarily constrained by the original topology and design equations. Nonetheless, some advances in the generalization of the Doherty PA have been presented in recent years. In order to solve practical limitations in the realization of the output network for a N-way Doherty PA, the Doherty PA theory was expanded by treating the output network as a black-box combiner in [102]. The network parameters of this combiner and the device periphery ratio were solved for maximum efficiency at maximum power and at back-off for any predetermined γ. In [102], the input phase delay θ is fixed to $\pm 90°$ when the circuit parameters are derived. In [57,58], on the other hand, Özen *et al.* showed that the input phase delay can adopt other values. The input phase delay θ and the output combiner parameters are solved for any predetermined γ for two fully utilized symmetrical transistors, i.e. for a unity device periphery ratio. For two fully utilized symmetrical transistors, the main and auxiliary transistor current relationship will deviate from the conventional [53, 54] Doherty PA case. More specifically, this true when $\gamma > 6$ dB for a class-B–class-B Doherty PA, or $\gamma > 4.8$ dB for a class-B–class-C Doherty PA. Thanks to the freedom of θ, it was shown that the presented solution still provides maximum efficiency at maximum power and at the predetermined back-off level γ, at the cost of some nonlinearity. It was further shown that, by using the proposed combiner synthesis approach,

impedance matching networks and offset lines [103], which are required in practice for parasitic compensation and impedance transformation, can be integrated into the same combiner network. However, some of the Doherty PA circuit design parameters in [57, 58] are solved analytically and some are found numerically. In [104], the parameters of a black-box three-port output combiner were derived analytically for an arbitrary power ratio between the outputs of the two transistors. However, neither the consequences of nonconventional current profiles resulting from the arbitrary power ratio, nor the limits of the range of power ratios were studied.

This section is divided into several parts. First, the Doherty PA operation for maximum efficiency is generalized beyond the symmetrical case. A summary of the analytical derivations and analysis from [g] is presented. Second, a modification of the black-box approach for improved linearity is presented. Here, the analytical derivations and analysis from [Paper B] are expanded. Third, the transmitter prototype from [Paper A] is presented. This prototype utilizes a dual-fed antenna as both the radiating element and the Doherty combiner. It is discussed how the black-box approach is beneficial in this integrated transmitter design, in terms of improved integration and reduced losses. Fourth, the linear Doherty PA prototype from [Paper B] is shown. Here, the conversion of the ideal design equations into a practical design methodology for realistic scenarios is summarized.

3.2.1 Generalized Solutions with Maximum Efficiency

A good starting point when applying the black-box method to the Doherty PA is to target load impedances that enable maximum efficiency. Below, this is done analytically for the ideal transistors. First, the ideal transistors are defined. Then, the design equations are derived. Finally, the ideal large signal behavior is analyzed.

Transistor models

Throughout this section, the transistors are modelled as ideal current sources. This allows for an analytical analysis of the fundamental behavior. Although the ideal analysis does not capture the full behavior of a Doherty PA in a realistic scenario, such analysis provides insights into the working principle and trends directly translatable to real transistors.

The fundamental main transistor drain current is modelled as a linear function, i.e.

$$I_{\mathrm{m}}(\beta) = \beta I_{\mathrm{MAX}}/2 \tag{3.8}$$

where I_{MAX} is the maximum DC current of the main transistor. The fundamental drain current of the auxiliary transistor is modelled as a piece-wise linear function, relating to the main transistor current according to

$$I_{\mathrm{a}}(\beta) = \begin{cases} 0, & \beta < \beta_{\mathrm{bo}} \\ r_{\mathrm{c}} I_{\mathrm{m,max}} \frac{\beta - \beta_{\mathrm{bo}}}{1 - \beta_{\mathrm{bo}}} e^{-j\theta}, & \beta \geq \beta_{\mathrm{bo}} \end{cases}. \tag{3.9}$$

Here, θ is the static phase difference between the two branches, $I_{\mathrm{m,max}}$ is the maximum fundamental drain current of the main transistor, and r_{c} is the

fundamental current magnitude ratio at maximum drive level. The current ratio can be expressed as

$$r_{\mathrm{c}} = \hat{r}_{\mathrm{c}}(1/\beta_{\mathrm{bo}} - 1). \tag{3.10}$$

The parameter $\hat{r}_{\mathrm{c}}$ is a novel current scaling parameter relating the generalized Doherty PA to the conventional [53, 54] Doherty PA. If $\hat{r}_c = 1$, a conventional ratio is obtained, and if $\hat{r}_c \neq 1$, the conventional current ratio is scaled. The auxiliary transistor starts to conduct when $\beta = \beta_{\mathrm{bo}}$. Note that β_{bo} also relate the maximum and backed-off power of the main transistor, see (2.9).

The main transistor current is actualized by class-B operation. The auxiliary current is actualized by class-C operation, but where the nonlinear fundamental drain current is simplified to the piece-wise linear current of (3.9). The DC current of the auxiliary transistor is simplified in the same way, see [i] for details.

Ideal design equations

The fundamental drain currents at the two drive levels for the main and auxiliary transistors are all dependent on $I_{\mathrm{m,max}}$. Therefore, if both transistors have the same supply voltage V_{DS}, the target impedances for both transistors at both drive levels can be expressed in terms of the conventional class-B optimal impedance of the main transistor: $R_{\mathrm{opt}} = V_{\mathrm{DS}}/(I_{\mathrm{MAX}}/2)$. The auxiliary transistor conducts no current at the backed-off drive level β_{bo}. The target fundamental load impedances, Z_{l}, can therefore be expressed as

$$Z_{\mathrm{l,m,max}} = R_{\mathrm{opt}} \tag{3.11}$$

$$Z_{\mathrm{l,a,max}} = R_{\mathrm{opt}}/r_{\mathrm{c}} \tag{3.12}$$

$$Z_{\mathrm{l,m,bo}} = R_{\mathrm{opt}}/\beta_{\mathrm{bo}} \tag{3.13}$$

and the current ratios can be expressed as

$$\alpha_{\mathrm{max}} = r_{\mathrm{c}} e^{-j\theta} \qquad \text{and} \qquad \alpha_{\mathrm{bo}} = 0. \tag{3.14}$$

Using (3.1)–(3.6) results in the following solution for the combiner network parameters:

$$Z_{11} = R_{\mathrm{opt}}/\beta_{\mathrm{bo}} \tag{3.15}$$

$$Z_{12} = -R_{\mathrm{opt}} e^{j\theta}/\hat{r}_{\mathrm{c}} \tag{3.16}$$

$$Z_{22} = R_{\mathrm{opt}} \frac{\beta_{\mathrm{bo}}(\hat{r}_{\mathrm{c}} + e^{j2\theta})}{\hat{r}_{\mathrm{c}}^2(1 - \beta_{\mathrm{bo}})} \tag{3.17}$$

where the phase delay θ has four solutions according to

$$\theta = \begin{cases} \pm\theta_{\mathrm{x}} \\ \pm(\pi - \theta_{\mathrm{x}}) \end{cases} \tag{3.18}$$

$$\theta_{\mathrm{x}} = \tan^{-1}\left(\sqrt{\frac{\beta_{\mathrm{bo}} + \hat{r}_{\mathrm{c}}}{1 - \hat{r}_{\mathrm{c}}}}\right). \tag{3.19}$$

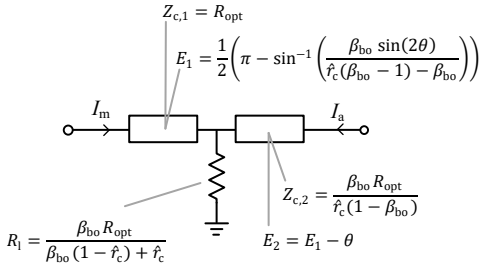


Figure 3.2: One combiner solution to the generalized Doherty PA architecture when $\theta = +\theta_x$.

From (3.19), it can be seen that $\hat{r}_c \leq 1$ for physical solutions. A lower limit of $\hat{r}_c$ is set by the condition that the fundamental drain voltage of the auxiliary transistor must always be larger than zero, which yields [g]

$$\beta_{bo} \leq \hat{r}_c \leq 1. \tag{3.20}$$

There are many ways to realize the output combiner of the generalized Doherty PA. One explicit example for $\theta = +\theta_x$ is presented in Figure 3.2. For more general approaches, see Figure 3.1(c) [58] or [104].

The relation between the back-off drive level β_{bo} and the dynamic range of efficiency enhancement γ is found by expanding (2.8). This results in

$$\gamma = \frac{\beta_{\mathrm{bo}}(1-\hat{r}_{\mathrm{c}}) + \hat{r}_{\mathrm{c}}}{\beta_{\mathrm{bo}}^2}. \tag{3.21}$$

It is interesting to compare the phase of the voltage across the load termination at the maximum and backed-off drive levels. Using (3.7), a ratio of the maximum and backed-off voltage across the load can be expanded to

$$\frac{V_{\mathrm{l,max}}}{V_{\mathrm{l,bo}}} = \frac{I_{\mathrm{m,max}}}{I_{\mathrm{m,bo}}}\left(1 \pm \sqrt{\frac{1-\hat{r}_{\mathrm{c}}}{1+\beta_{\mathrm{bo}}}}(1-\beta_{\mathrm{bo}})e^{-j\theta}\right). \tag{3.22}$$

From this ratio, it can be seen that the Doherty PA phase difference between the maximum and backed-off drive level is dependent on the inherent phase response of the main transistor, but not on the auxiliary transistor. This is reasonable since the phase of the auxiliary transistor current at maximum drive level is defined by θ. At the backed-off drive level, the auxiliary transistor current is zero. Ideal transistors have a static phase response versus drive level, but real transistors typically have a nonlinear response. It can also be seen that, for ideal transistors, current scaling ($\hat{r}_{\mathrm{c}} < 1$) causes a nonlinear phase response. Thus, it is possible to cancel out any inherent nonlinear phase response of a real transistor using current scaling.

Current scaling causes the gain to compress from drive levels between $\beta = \beta_{bo}$ to $\beta = 1$. By using (2.8) and (3.8)–(3.10), the gain compression between these two points can be expressed as

$$G_{\mathrm{comp}} = \frac{G_{\mathrm{max}}}{G_{\mathrm{bo}}} = \hat{r}_{\mathrm{c}}(1-\beta_{\mathrm{bo}}) + \beta_{\mathrm{bo}}. \tag{3.23}$$

Note that this expression is equal to one when $\hat{r}_{\mathrm{c}} = 1$, which means that the gain is linear. When $\hat{r}_{\mathrm{c}}$ decreases, the gain compression increases.

Table 3.1: Comparison of three different $\gamma = 6$ dB Doherty PAs. Case I is the conventional Doherty PA. Case II is the solution with equal transistor sizes. Case III is the solution with maximum possible current scaling. All impedances are normalized with R_{opt}. This table presents data for $\theta = +\theta_{\text{x}}$.

Case	$\hat{r}_{\text{c}}$	S_{aux}	$Z_{\text{l,m,max}}$	$Z_{\text{l,m,bo}}$=Z_{11}	Z_{12}	Z_{22}	θ
I	1	1.27	1.0+j0	2.0+j0	0–j1.0	0+j0	90°
II	0.68	1	1.0+j0	2.2+j0	–0.7–j1.3	0.2+j1.5	62°
III	0.40	0.71	1.0+j0	2.5+j0	–1.6–j1.9	1.1+j4.1	49°

A final interesting parameter is the relative size of the auxiliary transistor compared to the main transistor. It is defined by the relationship between auxiliary and main transistor maximum DC currents, i.e. $I_{\text{MAX,aux}} = S_{\text{aux}} I_{\text{MAX}}$. This relative size can be expressed as [g]

$$S_{\text{aux}} = \hat{r}_{\text{c}} \frac{\pi}{2\beta_{\text{bo}}} \frac{(\beta_{\text{bo}} - 1)^2}{\cos^{-1}(\beta_{\text{bo}}) - \beta_{\text{bo}}\sqrt{1 - \beta_{\text{bo}}^2}}. \tag{3.24}$$

It can be seen that $\hat{r}_{\text{c}}$ scales the relative size proportionally. Thus, it is possible to reduce the size of the auxiliary transistor for large values of γ compared to the conventional solution, thereby reducing the negative effects associated with a large auxiliary transistor.

Now, all necessary equations have been derived and the performance of the generalized Doherty PA operation can be studied.

Ideal performance evaluation

Below follows a comparison between three different solutions to the generalized Doherty PA for $\gamma = 6$ dB. Three cases from the minimum to the maximum value of $\hat{r}_c$ are considered. Case I is a conventional Doherty PA, i.e. no current scaling. Case II is the same solution as was described in [57, 58], i.e. some current scaling to reach symmetrical transistor sizes. Case III is the solution with maximum current scaling according to (3.20). The main transistors have the same size in all cases, i.e. they have the same maximum DC current. The cases are summarized in Table 3.1.

Figure 3.3 shows the magnitudes of the fundamental drain currents and voltages for both transistors versus drive level for the three cases defined above. It can be seen that Case I has the well-known conventional Doherty PA current and voltage profiles. Note that the maximum main and auxiliary currents are equal. Case II and III, where current scaling is applied, have nonconventional current and voltage profiles: the maximum auxiliary current is lower than the maximum main current, and the auxiliary drain voltage is nonlinear. Also, the auxiliary drain voltage increases at back-off as $\hat{r}_{\text{c}}$ becomes smaller.

The load modulation for the main and auxiliary transistors are plotted in Figure 3.4. The main transistor load modulation is always purely resistive and goes from R_{opt} at maximum power to $R_{\text{opt}}/\beta_{\text{bo}}$ at back-off. The auxiliary transistor load modulation is purely resistive for the conventional Doherty PA solution (Case I) but becomes complex for the current scaled solutions. The impedance changes from $R_{\text{opt}}/r_{\text{c}}$ at maximum power to infinity at back-off. The auxiliary transistor load modulation in Figure 3.4 (b) is valid for $\theta = +\theta_{\text{x}}$

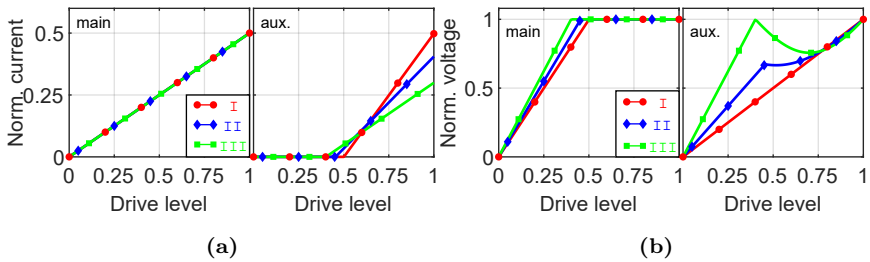


Figure 3.3: (a) Current and (b) voltage profiles of the generalized Doherty PA for Case I, II and III in Table 3.1. The current is normalized with I_{MAX}. The voltage is normalized with V_{DS}.

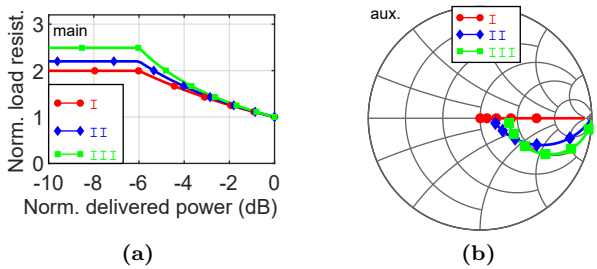


Figure 3.4: (a) Main and (b) auxiliary transistor load modulation versus delivered power for the generalized Doherty PA for Case I, II and III in Table 3.1. The load is normalized with the optimum class-B load in both plots. The load modulation of the main transistor is purely resistive and is therefore shown in a Cartesian plot. The load modulation in (b) is valid for $\theta = +\theta_{\mathrm{x}}$ and $\theta = -(\pi - \theta_{\mathrm{x}})$.

and $\theta = -(\pi - \theta_{\mathrm{x}})$. For the other set of phases, i.e. $\theta = -\theta_{\mathrm{x}}$ and $\theta = +(\pi - \theta_{\mathrm{x}})$, the auxiliary transistor load modulation is mirrored in the real axis.

The drain efficiency versus normalized delivered power is plotted in Figure 3.5(a). All cases present very similar efficiencies. The small variations come from different class-C biases and different load modulation of the auxiliary transistor.

Figure 3.5(b) shows normalized gain versus normalized delivered power. The gain is normalized to the conventional Doherty PA gain (Case I). It can be seen that the gain is significantly larger for the current scaled versions compared to the conventional Doherty PA solution, but at the cost of some nonlinearity.

The phase of the load termination voltage is plotted versus normalized delivered power in Figure 3.5(c). It can be seen that the conventional Doherty PA has zero phase distortion, while the current scaled Doherty PAs present phase distortion for ideal transistors. This phase distortion goes in different directions depending on the choice of θ.

So how do all these result translate to Doherty PAs with real transistors? For one thing, the gain of an ideal class-B transistor is proportional to the resistive load termination. Real transistors show a weaker relation. Therefore, the absolute values of the gains presented in this chapter do not translate directly to Doherty PAs with real transistors. However, current scaled Doherty PAs require less power to be split into the auxiliary transistor [g]. This translates well to Doherty PAs with real transistors since the gain degradation associated

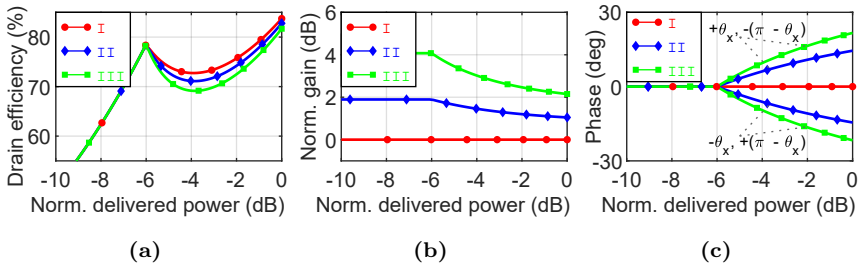


Figure 3.5: (a) Drain efficiency, (b) gain, and (c) phase versus normalized delivered power of the Doherty PA, for the generalized Doherty PA for Case I, II and III in Table 3.1. The gain is normalized with the conventional Doherty PA gain.

with a large auxiliary transistor is reduced. Thus, current scaled Doherty PAs with real transistors are expected to present higher gain, and therefore potentially higher power added efficiency (PAE). However, from (3.21), it can be seen that current scaled Doherty PAs require the backed-off power level of the main transistor alone to be further away from the maximum power level of the main transistor alone for a given γ. This results in lower efficiency at back-off for the Doherty PA due to parallel losses, see (2.6). The nonlinearities of the current scaled Doherty PA are not always a limitation since some applications allow linearization through DPD.

A good property of the black-box combiner is that the method itself translates very easily to real transistors. Equations (3.1)–(3.6) in Section 3.1 can easily be solved from simulated or measured transistor load-pull data rather than ideal target impedances. If the load-pull data is extracted in the transistor package plane, the black-box combiner will automatically include parasitic matching and offset line functionality, resulting in a very compact circuit. This section has demonstrated that the load pull data can be selected quite freely due to current scaling. The next section shows that reactive mismatching can also be added to the ideal target load impedances without sacrificing much efficiency or complicating the combiner. Thus, load-pull data from real transistors can be selected very freely when using the black-box method. Furthermore, since the combiner is equation-based, many different combinations of target impedances can be evaluated in full Doherty PA simulations very quickly.

3.2.2 Generalized Solutions with Improved Linearity

Even though the ideal conventional Doherty PA presents linear gain and phase responses, the responses when using real transistors are nonlinear. The gain is often compressed to reach higher efficiency levels. In a single-ended PA, the phase response is nonlinear due to, e.g., the nonlinear gate-source capacitance and the feedback gate-drain capacitance [105]. Load modulation of a PA causes severe phase distortion in the high power region. Due to the feedback capacitance, the phase response of a single transistor becomes dependent on the resistive load termination [66–68]. In the Doherty PA, in the high power region, where the load of the main transistor is modulated, the main transistor phase response is very nonlinear. This, in turn, means that the phase response of the conventional Doherty PA is very nonlinear, see (3.22). For modulated

signals, several other aspects affect PA linearity in addition to the amplitude and phase responses. For instance, the spectral regrowth is dependent on memory effects through the baseband terminations [106, 107] and thermal feedback [108]. Nevertheless, improving the static single frequency linearity in a Doherty PA can improve the linearity when using modulated signals as well, as demonstrated in [Paper B] [109].

Below, the mechanics of the method in [Paper B] is applied using ideal transistors. Then, the large signal performance is evaluated for these ideal transistors. The transistors are modelled according to (3.8) and (3.9).

Ideal design equations

For the generalized Doherty PA equations, linear gain can be obtained if the drain efficiency of the main transistor at back-off is relaxed. The gain of the Doherty PA will be equal at maximum output power and the backed-off power level if

$$\gamma = \frac{1}{\beta_{\mathrm{bo}}^2}.$$

This can be interpreted as the input power being backed-off equally to the output power. With this equation, (2.8) can now be solved for the main transistor fundamental voltage swing at back-off as

$$|V_{\mathrm{m,bo}}| = V_{\mathrm{DS}} \left(\beta_{\mathrm{bo}}(1-\hat{r}_{\mathrm{c}}) + \hat{r}_{\mathrm{c}}\right). \tag{3.25}$$

This can also be expressed as

$$R_{\mathrm{l,m,bo}} = (1+r_{\mathrm{c}})\, R_{\mathrm{l,m,max}}. \tag{3.26}$$

Note that the non-normalized r_{c} is used here. The resistances are calculated from the load impedance $Z(\beta) = V(\beta)/I(\beta)$, which in this case are purely resistive. It is interesting to note that (3.6) imposes the following constraint for physical solutions:

$$\Re\{Z_{\mathrm{l,m,bo}}\} \geq (1+r_{\mathrm{c}})\, \Re\{Z_{\mathrm{l,m,max}}\}. \tag{3.27}$$

Now, reactive mismatch can safely be added to the impedances. The following impedances are defined:

$$Z_{\mathrm{l,m,max}} = R_{\mathrm{l,m,max}} \pm jX_{\mathrm{l,m,max}} \tag{3.28}$$

$$Z_{\mathrm{m,bo}} = R_{\mathrm{l,m,bo}} \pm jX_{\mathrm{l,m,bo}}. \tag{3.29}$$

Adding a reactive component to $Z_{l,a}$ does not affect the phase response of the Doherty PA. The resistive and reactive parts of these impedances are defined such that the maximum possible voltage swing is always reached, i.e.

$$R_{\mathrm{l,m,max}} = U_{\mathrm{m}} R_{\mathrm{opt}} \tag{3.30}$$

$$X_{\mathrm{l,m,max}} = \sqrt{1-U_{\mathrm{m}}^2}\, R_{\mathrm{opt}} \tag{3.31}$$

$$R_{\mathrm{l,m,bo}} = U_{\mathrm{m}} \left(1+r_{\mathrm{c}}\right) R_{\mathrm{opt}} \tag{3.32}$$

$$X_{\mathrm{l,m,bo}} = \sqrt{1/\beta_{\mathrm{bo}}^2 - (1+r_{\mathrm{c}})^2 U_{\mathrm{m}}^2}\, R_{\mathrm{opt}}. \tag{3.33}$$

Table 3.2: Comparison of three different $\gamma = 6$ dB Doherty PAs. Case I is the conventional Doherty PA. Cases IV and V have been solved for linear gain and for a phase distortion of 30°. All impedances are normalized with R_{OPT}. This table presents data for positive $X_{\text{L,M,MAX}}$, negative $X_{\text{L,M,BO}}$, and $\theta = +\theta_{\text{X}}$

Case	$\hat{r}_{\text{c}}$	U_{m}	$Z_{\text{l,m,max}}$	$Z_{\text{l,m,bo}}$=Z_{11}	Z_{12}	Z_{22}	θ
I	1	1	1.0+j0	2.0+j0	0–j1.0	0+j0	90°
IV	1	0.97	0.97+j0.3	1.9–j0.5	–1.0–j0.7	0.5+j1.2	75°
V	0.85	1	1.0+j0	1.8–j0.8	–1.1–j0.7	0.7+j1.5	75°

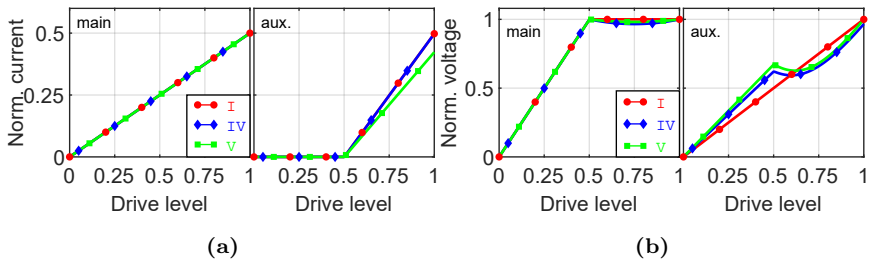


Figure 3.6: (a) Current and (b) voltage profiles of the generalized Doherty PA for Case I, IV and V in Table 3.2. The current is normalized with I_{MAX}. The voltage is normalized with V_{DS}.

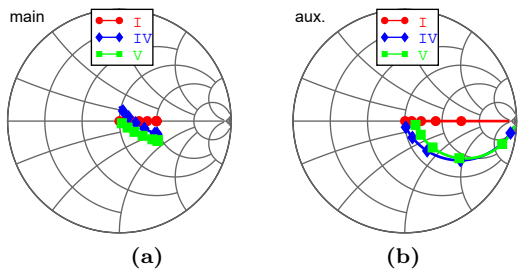


Figure 3.7: (a) Main and (b) auxiliary transistor load modulation versus delivered power for the generalized Doherty PA for Case I, IV and V in Table 3.2. The load is normalized with the optimum class-B load in both plots. The load modulation in (b) is valid for $\theta = +\theta_{\text{x}}$ and $\theta = -(\pi - \theta_{\text{x}})$.

Here U_{m} can be seen as a utilization parameter that can take any value from 0 to 1. For the conventional Doherty PA, i.e. $\hat{r}_{\text{c}} = 1$, U_{m} must be smaller than one if a reactive mismatch is added. This clearly lowers the drain efficiency at both the maximum and the backed-off drive level. From (3.33), it can be seen that U_{m} can be equal to 1 when reactive mismatch is added at back-off if $\hat{r}_{\text{c}} < 1$. This means that the efficiency of the current scaled Doherty PA only degrades at the backed-off drive level if reactive mismatch is added. It is also important to mention that the power utilization of the main transistor is proportional to U_{m}.

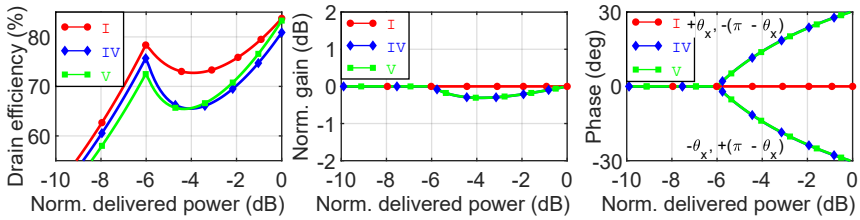


Figure 3.8: (a) Drain efficiency, (b) gain, and (c) phase versus normalized delivered power of the Doherty PA, for the generalized Doherty PA for Case I, IV and V in Table 3.2. The gain is normalized with itself.

Ideal performance evaluation

Below follows a comparison between three different solutions to the generalized Doherty PA for $\gamma = 6$ dB. The first case is the conventional Doherty PA. The other two cases have been solved for linear gain and for a phase distortion of 30°. The cases are summarized in Table 3.2. The performance is presented in Figures 3.6–3.8. The general behavior for these cases are similar to the cases for maximum efficiency. Therefore, the discussion below is kept short. All cases have the same current profiles and very similar voltage profiles for the main transistor. The auxiliary transistor voltage is increased at back-off for Case IV and V. The load modulation follows the expected behavior of current scaling and reactive mismatching. Note the complex load modulation of the auxiliary transistor and the 75° phase delay for Case IV. This indicates that Case IV is a nonconventional solution and that the combiner cannot be realized with the conventional quarter-wave transformer, despite a conventional current ratio. Figure 3.8 shows that reactive mismatching and current scaling introduce an insignificant gain nonlinearity.

The important aspect of this analysis is that two parameters for phase control in the high power region have been identified. These parameters can be tuned individually or combined to tune the phase of the Doherty PA in the high power region while maintaining high efficiency and linear gain.

3.2.3 Circuit Prototype - Antenna Combiner

This part presents one example of the integration improvements enabled by the black-box approach. In a transmitter, the PA and antenna are typically designed independently and are often matched to 50 Ω. It has been shown that it is possible to reduce the size of the PA OMN by utilizing a non-50-Ω input impedance of the antenna [110], i.e. having the antenna function both as the radiator and the matching network. The purpose of this closer integration between the PA and antenna is to reduce the overall size and losses. An antenna element utilizing air instead of a lossy substrate can be less lossy compared to matching elements such as lumped components, transmission lines and stubs. Nonetheless, few publications have studied improved integration in transmitters using high-efficiency PAs, e.g. Doherty PAs.

The black-box method provides the two-port network parameters for optimal

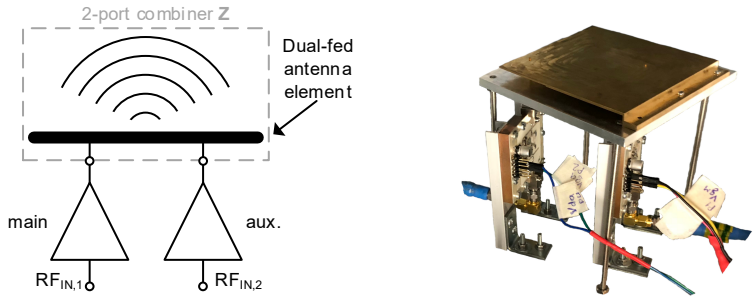


Figure 3.9: (a) Conceptual schematic of using a dual-fed antenna as the Doherty combiner. (b) Photograph of the Dohery antenna transmitter in [Paper A].

transistor loading conditions in a two-way Doherty PA. Thus, a dual-fed antenna presenting these parameters can be used both as the Doherty combiner and the radiator, see Figure 3.9(a). As mentioned, this allows for a more compact transmitter with reduced losses. Below, a brief literature review of different strategies for improving the integration between the Doherty PA and antenna(s) in a transmitter is presented. Then, the black-box enabled integration solution from [Paper A] is summarized. In particular, the prototype transmitter measurement results and challenges are discussed.

In [111, 112], Doherty combining is achieved by placing two identical monopole antennas close to each other. From a transistor perspective, the two antennas can be seen as a two-port network. This two-port replaces the resistor and quarter-wave transformer in a conventional Doherty PA. In this approach, the two-port antenna network is symmetrical. Thus, external matching is required since the optimal Doherty PA load impedance matrix is asymmetrical, see (3.15)-(3.17). External parasitic compensation and offset line functionality are also required. Therefore, this approach offers limited integration improvement. Furthermore, the two-patch antenna solution is unsuitable for beam-steering antenna arrays since the elements are too large to meet the requirement of no radiating grating lobes [113].

In [114], a dual-fed wire-loop antenna replaces only the resistor in a series Doherty combining network. This solution also offers limited improvement in integration and losses, but is, on the other hand, suitable for beam-steering antenna arrays.

One common challenge in integrated Doherty transmitters is the radiation pattern. The different nonlinear excitation of the two antenna ports, from the main and auxiliary transistors, respectively, results in a radiation pattern that may vary versus input power. This results in both amplitude and phase distortion of the radiated signal. The difference in on-axis antenna directivity at peak power and at 6 dB OPBO is reported to < 0.5 dB in [111], < 7 dB in [112], and < 0.1 dB in [114]. These numbers are estimated from reported figures. It is possible that pre-distorting the signal could compensate for this effect. The characterization required for such pre-distortion is, however, very challenging.

Another common challenge is accuracy in the characterization of the transmitter. In [111, 112], couplers where incorporated before the antenna feeds.

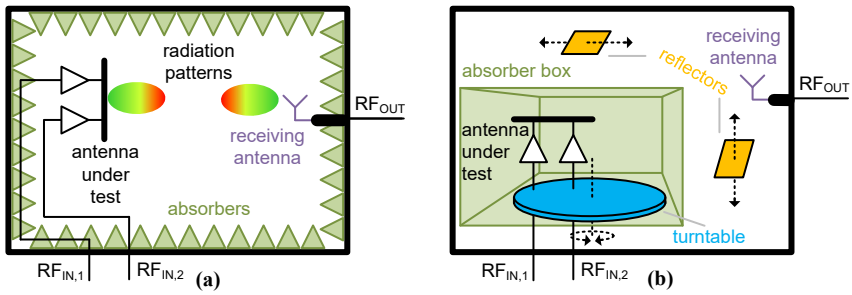


Figure 3.10: Illustration of (a) an anechoic chamber and (b) a reverberation chamber.

This provides simple and accurate PA characterization but it is not viable in a practical implementation, and it does not provide the delivered power after the antenna elements. In [114], an anechoic chamber was used to measure the radiated power. This method overcomes the problems of using couplers, but is relatively complex and has limited accuracy. The accuracy is discussed further below.

In [Paper A], an integrated Doherty antenna utilizing the black-box approach is presented. A dual-fed planar inverted F-antenna (PIFA) is designed to present the two-port parameters obtained from the black-box method. Among other things, the positions of the feeding pins and the grounding pins are used as optimization variables to have the antenna present the prescribed non-symmetrical two-port parameters. In this approach, the single dual-fed antenna element functions as radiator, Doherty combiner, parasitic compensation networks, and offset line network. As such, this approach provides the best reported integration improvement.

The prototype Doherty antenna transmitter in [Paper A] employs two 10-W GaN HEMTs (CGH40010F from Wolfspeed). The transmitter targets the frequency 2.14 GHz and $\gamma = 6$ dB. A photograph of the fabricated prototype is shown in Figure 3.9(b). The corresponding schematic can be found in [Paper A]. The PA boards comprise all network functionality except the fundamental output match, i.e. only bias, stabilization, input match and harmonic terminations are included. For test purposes, the PAs are mounted to the antenna using SMA connectors. These can be eliminated in real applications to reduce loss. Simulated load-pull data for the PA boards provide target impedances from which the black-box equations are solved. The equations for solving the two-port combiner parameters from load-pull data extracted at an extrinsic transistor plane is presented in [Paper B]. The dual-input PIFA antenna is then designed to present the computed two-port parameters.

In [Paper A], the transmitter is characterized in two ways: in an anechoic chamber and in a reverberation chamber, see Figure 3.10. In the anechoic chamber, the radiated signal is measured in a single direction. By rotating the transmitter (or antenna under test, AUT), the radiation pattern can be measured. Since the radiation pattern is power dependent, it has to be measured for a sweep of input powers. The transmitter can heat up significantly during the measurement method, since the radiation pattern should be measured for many spatial points. This may lead to inaccurate radiation pattern measurements. An alternative method is to extract the radiation pattern through simulations. Both alternatives introduce a significant uncertainty. Nonetheless, the on-axis

directivity of the AUT is required to extract the total transmitted power of the transmitter in anechoic chamber measurements, which in turn is needed for efficiency calculations. Several other factors, in addition to the radiation pattern, limit the accuracy of measured output power, such as uncertainties in the specified gain of the reference antenna used in calibration, misalignment between the AUT and receiving antenna, unwanted reflections in the chamber, and uncertainties in the calculation of the path loss between the AUT and receiving antenna. In [Paper A], the cumulative uncertainty for those particular anechoic chamber measurements is approximated to around ±1.3 dB. This number is based on observations, but is not statistically validated. It should also be mentioned that these uncertainties are in addition to any instrument uncertainties.

An alternative method for AUT characterization is to use a reverberation chamber, which is metal cavity where many cavity modes, originating from the AUT, are observed in a stochastic way [115]. The AUT is placed on a turntable and there are moving reflectors in the chamber. The power coupled to the receiving antenna is sampled for a large number of different positions of the turntable and reflectors. By first using a reference antenna (instead of the AUT), the average loss in the chamber can be obtained by averaging the sampled power. Then, when measuring the AUT, many samples of the output power from the receiving antenna are averaged. The total radiated power from the AUT is then obtained by subtracting the average chamber loss. Unfortunately, the metal cavity chamber affects the loading conditions of the transistors inside the active AUT. Figure 3.11(a) shows measured Z_{11} of the dual-fed antenna for 300 samples in the chamber. As a reference, the samples are related to the measured value of Z_{11} in free space ($\Delta Z_{11} = Z_{11,\text{rc}} - Z_{11,\text{f-space}}$). A large spread is observed. The parameters Z_{12} and Z_{22} show a similar spread. This spread affects the Doherty PA substantially. Figure 3.11(c) shows the simulated efficiency for each sampled value of the two-port matrix. Averaging the efficiency or two-port matrix will not give representative results. Furthermore, it can be seen that some samples result in severe compression at high power levels. Therefore, CW measurements in the chamber might break the transistors. These problems can be mitigated if the chamber is loaded with absorbers. In [Paper A], a box comprising absorbing material encapsulates the AUT and turntable. The resulting reduction in variance of Z_{11} is shown in Figure 3.11(b). The corresponding efficiency variation is shown in Figure 3.11(d). The mean value of Z_{11} is shifted compared to the free space value. This could be due to a close proximity to the reference antenna, which is present inside the absorber box for calibration purposes. Nonetheless, this shift has an insignificant effect on the efficiency, see [Paper A] for details. While the absorber box reduces the variation, it increases the uncertainty in the average chamber loss calculation [116]. In the measurements in [Paper A], the uncertainty is approximated to around ±0.35 dB. This number is based on observations, but is not statistically validated.

Figure 3.12 shows reverberation chamber measurements. The SMA connectors naturally degrade the efficiency. Therefore, the figure also shows simulations of the layout as manufactured where the output power is observed in the internal plane before any connectors. These simulations are perhaps more representative since the SMA connectors are only included in this design

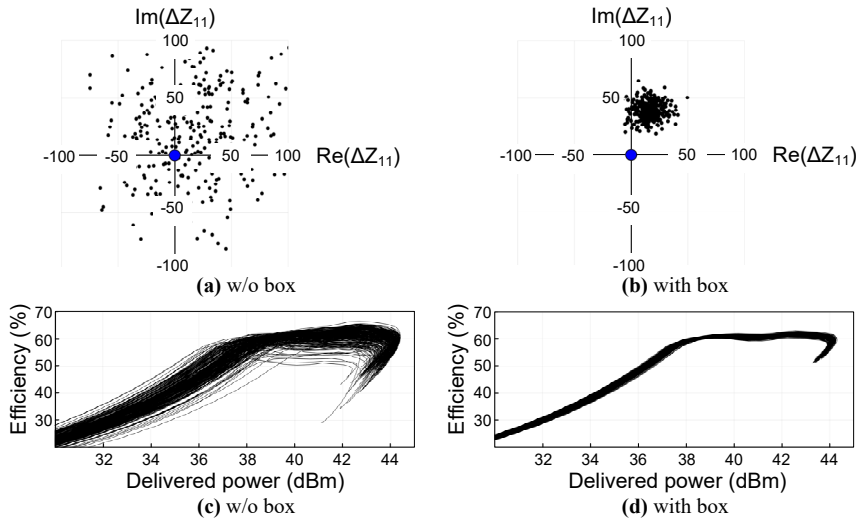


Figure 3.11: Reverberation chamber (RC) results. (a,b): measured ΔZ_{11} w/o and with the absorber box. ΔZ_{11} is the RC measurements minus the measured free space value. (c,d): Simulated efficiency for all measured two-port parameters in the RC w/o and with the absorber box.

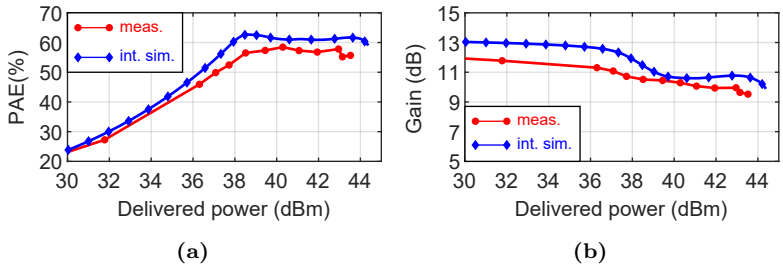


Figure 3.12: CW measurements (meas.) and simulations (int. sim.) at 2.14 GHz of the fabricated Doherty antenna transmitter from [Paper A]. In the simulations, the output power is observed at the internal plane before the connectors.

for test purposes. Despite the connectors, the prototype transmitter presents a PAE of 52% at 6 dB OPBO. The uncertainty in the chamber loss corresponds to a trust region of 58-68% for the drain efficiency at peak power. The simulated radiation pattern shows a difference of < 0.3 dB in the on-axis antenna directivity for all power levels.

There are many things yet to explore in the black-box Doherty antenna method. Perhaps there are multiple antenna solutions yielding the same two-port matrix, but with different radiation patterns. The method could also be modified for improved bandwidth. Incorporating harmonic matching into the antenna could be possible. Future work could also include empirical studies of the measurement uncertainties and how they can be improved upon. Furthermore, different approaches to the transistor-to-antenna transition can be explored.

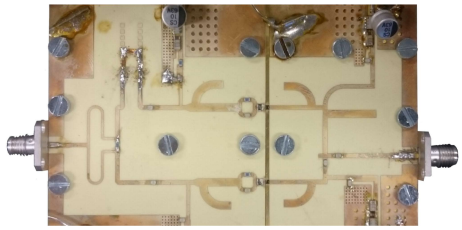


Figure 3.13: Photograph of the core area of the fabricated Doherty PA in [Paper B].

3.2.4 Circuit Prototype - Linear Design

This part presents one example of the Doherty PA linearity improvements enabled by the black-box approach. First, a brief literature review of different strategies for improving the linearity in the Doherty PA is presented. Then, the black-box enabled method from [Paper B] is summarized. In particular, an overview of the translation from the ideal design equations to a practical design methodology is presented.

One approach to improve the overall linearity of a Doherty PA was presented in [103,117,118], where it was improved by optimizing biases for intermodulation (IM) product cancellation at the load. The current profiles of a Doherty PA are functions of, among other things, bias levels. Therefore, optimizing bias levels for IM cancellation most likely changes the current profiles and thereby degrades the efficiency. In N-way Doherty PAs, the extra auxiliary transistors provide additional degrees of freedom, making it easier to find both efficiency and linearity optimized solutions [119,120], but at the cost of complexity. These strategies are in general strongly based on empirical methods.

In Section 3.2.2 [Paper B] it was showed that the generalized Doherty PA can be solved for linear gain simultaneously as applying current scaling. Furthermore, it was shown that current scaling can be combined with reactive mismatching to compensate the inherent nonlinear response of the Doherty PA. This combination hardly affects the drain efficiency performance, allowing for highly linear and efficient solutions for Doherty PAs with real transistors.

In a recent study [109], a Doherty PA prototype with high linearity was demonstrated. Current scaling for maximum efficiency from Section 3.2.1 [g,i] was used to introduce a phase compensating combiner, see Figure 3.5(c). Despite this method giving a non-linear gain, the fabricated PA in [109] was tuned to present linear gain and phase, and high efficiency.

The prototype PA in [Paper B] employs two 15-W GaN HEMTs (CGH60015D from Wolfspeed). The PA targets the frequency 2.14 GHz and $\gamma = 8$ dB. A photograph of the core area of the fabricated Doherty PA prototype is shown in Figure 3.13. A photograph of the whole circuit and the corresponding schematic can be found in [Paper B].

The design procedure was to first select a $Z_{\mathrm{l,m,bo}}$ that yields a good trade-off between gain compression and efficiency. Then different possible ratios of the maximum delivered power of the auxiliary and main transistors were evaluated. Each ratio provides different possible values of the load impedances $Z_{\mathrm{l,m,max}}$ and $Z_{\mathrm{l,a,max}}$. Each combination of $Z_{\mathrm{l,m,max}}$ and $Z_{\mathrm{l,a,max}}$ for each possible power ratio was evaluated in terms of efficiency and linearity. This corresponds to evaluating different current ratios and different reactive mismatching. Finally,

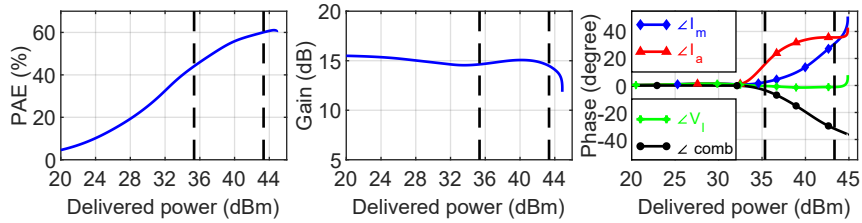


Figure 3.14: CW simulations at 2.14 GHz using input and output networks with ideal circuit elements of the Doherty PA in [Paper B].

the best combination of impedances in terms of efficiency and linearity was selected, which provided the basis for the black-box combiner design, see [Paper B] for details.

Simulations using ideal input networks and an ideal black-box combiner are shown in Figure 3.14. Two dashed vertical lines demonstrates the target maximum power and the intended back-off level. As intended, the Doherty PA presents high efficiency, linear gain and linear phase. The phase compensating effect of current scaling and reactive mismatching is demonstrated in Figure 3.14(c), where the phase is plotted in different planes, including the phase response of the main transistor current, the auxiliary transistor current, and the voltage across the load. The figure also includes the phase response the circuit would have had if the main and auxiliary transistors had inherently flat phase responses ($\angle$ comb). To clarify, the phase response of the voltage across the load termination is studied with the combiner being excited with modified transistor currents. The magnitudes stay the same as in the full simulations, but the inherent phase responses and the phase difference are set to constant. The constant phase difference is set to a value extracted at peak output power in the full simulation. Observing $\angle$ comb gives an approximation of the phase compensating effect of the combiner. In Figure 3.14(c), it can be seen that the main transistor presents severe phase distortion and that it is cancelled by current scaling and reactive mismatching.

The measured performance is presented in Figure 3.15. The offset in gain between simulations with ideal networks and measurements is believed to be a consequence of inaccurate modelling of the transistors, for more details, see [Paper B]. Despite this difference, the prototype PA presents nearly flat gain and phase responses with a PAE of 39% at 8 dB OPBO.

Measurements for a 5, 10 and 20 MHz LTE signal with 8.6 dB PAPR are presented in [Paper B]. The PA presents an average PAE of 40% for all signals with an average delivered power of 35.4 dBm. Without DPD, the PA presents an adjacent channel power ratio (ACPR) lower than –40.5 dBc for all signals - a state-of-the-art raw linearity and efficiency performance.

Several aspects of the method are interesting to explore further. In a way, the auxiliary transistor compensates for deep compression of the main transistor in the high power region. At back-off, however, the auxiliary transistor is not conducting and cannot compensate for compression. Thus, there is a trade-off between gain linearity and efficiency for low powers up until the back-off level for the Doherty PA. Different strategies for improving upon this trade-off can be

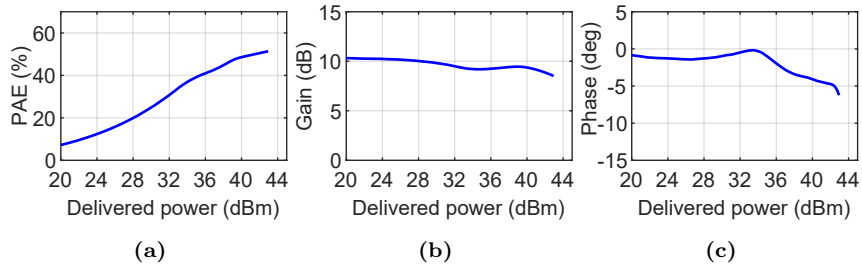


Figure 3.15: CW measurements at 2.14 GHz of the fabricated Doherty PA in [Paper B].

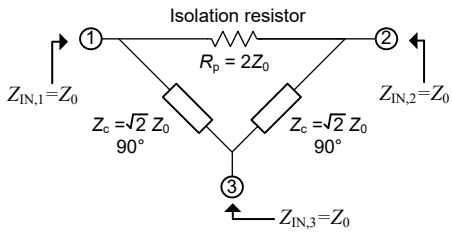


Figure 3.16: Conventional Wilkinson power divider. The two transmission lines are 90° at the design frequency. Ports 1 and 2 are electrically isolated at the design frequency. The input impedances of all ports are Z_0.

studied. Furthermore, the method could be modified for improved bandwidth, and the method could be studied in conjunction with IMD3 cancellation and baseband terminations.

3.3 Black-Box Power Divider

The black-box method is not only suitable for non-isolating combiners for ALM PAs. This section shows that it is also applicable for generalization of two-way isolating power dividers/combiners. The two-way Wilkinson power divider [121] is a common topology that appears as a subset in the generalized design space. This sections starts with a brief summary of the Wilkinson divider. Thereafter, the design equations of the generalized deigns space and a design example are presented.

The two-way Wilkinson divider, in its simplest form, comprises two quarter-wave transmission lines and an isolation resistor, see Figure 3.16. Starting off from this topology, many modifications have been presented for two-way dividers, which, for example, are: asymmetrical power splitting [122], improved bandwidth [123], multiband [124, 125], and smaller size [126]. One particular modification is to introduce physical isolation (physical separation) between the two electrically isolated ports [127–130]. Conventionally, these two ports are only separated by a resistor. Thus, the two electrically isolated ports are very closely spaced together. Physical isolation introduces improved layout flexibility, which can, for example, be helpful in designing a more compact divider. In [127], short transmission lines were added to either side of the isolating resistor for physical isolation. These transmission lines can also be used for modelling the mounting pads and physical length of a real resistor.

If the mounting pads and length are not accounted for, the divider design becomes suboptimal. This problem typically increases with frequency. Physical isolation can facilitate using physically large inductors in the two splitting branches in integrated designs, it can reduce thermal problems in amplifier designs, and it can reduce undesirable electromagnetic coupling between the two splitting branches.

Modifications of the Wilkinson divider to directly match to complex impedances have not been studied extensively [131–133], despite many antennas and active devices presenting complex input impedances. This is done through optimization in [131] and analytically in [132]. More specifically, in [132], the conventional Wilkinson topology is modified to include a reactive element in series with the isolation resistor. This allows for an equal complex termination at all ports. The reactive element is either capacitive or inductive depending on the sign of the port termination reactance. One drawback is that the required value of the inductor or capacitor, in the isolation network, might be difficult to realize in practice. Furthermore, if the input port impedance is 50 Ω and the two electrically isolated ports are terminated with equal complex impedances, external matching is required at the input port. This can severely limit the bandwidth in some cases [Paper C]. Many modifications of Wilkinson power divers comprise extra transmission lines at the two electrically isolated ports, after the isolation resistor, to match to arbitrary impedances at those ports, e.g. [133]. This can be seen as external matching, rather than direct matching. External matching can, of course, be added to any type of Wilkinson divider.

A new design space opens up when applying the black-box method to an isolated two-way power divider [Paper C]. Not restricting the topology to comprise two quarter-wave transmission lines as the splitting network, rather to replace them with arbitrary networks, unlocks new degrees of freedom. Replacing the isolation resistor with an arbitrary network opens up additional degrees of freedom. This freedom can be used, e.g., to match directly the input port to 50 Ω, and directly match to equal complex port impedances at the two other ports. Furthermore, physical isolation can be added if desired. It is also shown that many known modifications to the Wilkinson divider appear as subsets of the more generalized black-box divider.

3.3.1 Generalized Solutions

Like ALM PA combiner analysis in Section 3.1, the initial divider analysis is based on a single symmetrical, reciprocal and lossy two-port network, where the third port-termination and the isolation resistance are absorbed. This allows for a low-complexity analysis and a better understanding of the fundamental operation, which in turn makes it possible to identify an expanded design space. This two-port network $\mathbf{Y}_\mathrm{C}$ is shown in Figure 3.17(a). For the power divider case, it is convenient to work with admittance parameters when using the black-box approach. To make it easy to synthesize the network $\mathbf{Y}_\mathrm{C}$, it is split into one symmetrical, reciprocal and lossy two-port network with isolation functionality ($\mathbf{Y}_\mathrm{B}$) and one symmetrical, reciprocal and lossy two-port network ($\mathbf{Y}_\mathrm{A}$) coupling to the third port-termination (Y_{03}), see Figure 3.17(b). Thereafter, the third port-termination Y_{03} is de-embedded from $\mathbf{Y}_\mathrm{A}$, resulting in two loss-less and reciprocal networks $\mathbf{Y}_\mathrm{AL}$ and $\mathbf{Y}_\mathrm{AR}$, see Figure 3.17(c). Note

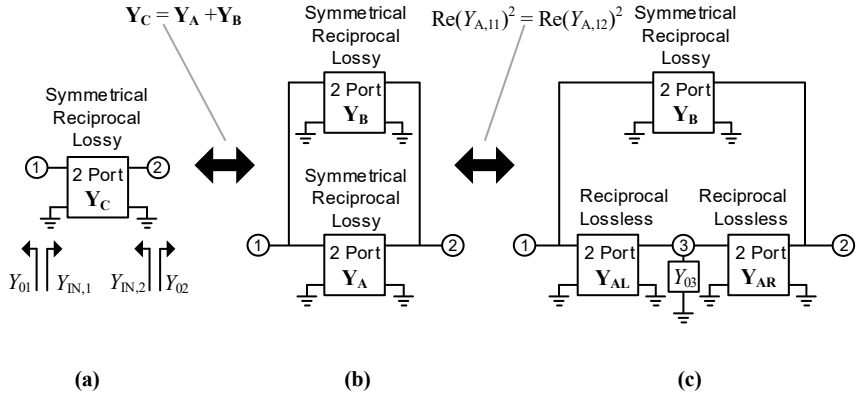


Figure 3.17: A generalized representation of a two-way isolated power divider. (a) The simplest representation ($\mathbf{Y_C}$). (b) $\mathbf{Y_C}$ can be de-composed to a network with isolation functionality ($\mathbf{Y_B}$) and a network with the splitting functionality ($\mathbf{Y_A}$). (c) The splitting network ($\mathbf{Y_A}$) can be decomposed into two networks ($\mathbf{Y_{AL}}$ and $\mathbf{Y_{AR}}$) with the third port termination (Y_{03}) in-between.

that this final schematic now looks like a Wilkinson divider where all circuit elements have been replaced with more general two-port networks. Below, it is shown that the topology of $\mathbf{Y}_\mathrm{B}$ must be predetermined. The topology of $\mathbf{Y}_\mathrm{AL}$ and $\mathbf{Y}_\mathrm{AR}$ can, for example, be realized with Π- and/or T-networks, using lumped elements and/or transmission lines. The decomposition of $\mathbf{Y}_\mathrm{A}$ and synthetization of $\mathbf{Y}_\mathrm{AL}$ and $\mathbf{Y}_\mathrm{AR}$ follow the method in [58,83] and is not covered in this thesis. Ultimately, in the generalized divider, all circuit element values are functions of the predetermined port impedances $Y_{01} = Y_{02}$ and Y_{03} (or correspondingly $Y_{\mathrm{IN},1} = Y_{\mathrm{IN},2}$ and $Y_{\mathrm{IN},3}$) and the predetermined topology of $\mathbf{Y}_\mathrm{B}$.

Now, going back to the simple representation of the divider, i.e. $\mathbf{Y}_\mathrm{C}$ in Figure 3.17(a), it is easy to set up the design goals of presenting predetermined complex input admittances $Y_{\mathrm{IN},1} = Y_{\mathrm{IN},2}$ at port 1 and 2, respectively, and to have port 1 and 2 electrically isolated. The arbitrary termination of the third port, Y_{03}, influences later design decisions. With these design goals, the modified black-box equations become

$$Y_{\mathrm{C},11} = Y_{\mathrm{IN},1} \tag{3.34}$$

$$Y_{\mathrm{C},12} = 0. \tag{3.35}$$

The conversion from Figure 3.17(a) to (b) imposes

$$\mathbf{Y_C} = \mathbf{Y_A} + \mathbf{Y_B} \tag{3.36}$$

and going from Figure 3.17(b) to (c) imposes

$$\Re\{Y_{\mathrm{A},11}\}^2 = \Re\{Y_{\mathrm{A},12}\}^2. \tag{3.37}$$

The solution to the network $\mathbf{Y}_\mathrm{A}$ can simplified to

$$Y_{\mathrm{A},11} = Y_{\mathrm{IN},1} - Y_{\mathrm{B},11} \tag{3.38}$$

$$Y_{\mathrm{A},12} = -Y_{\mathrm{B},12}. \tag{3.39}$$

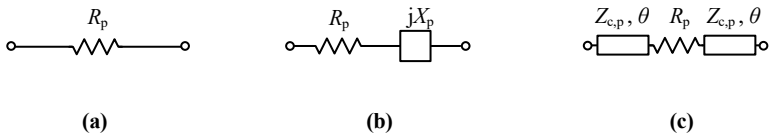


Figure 3.18: Three examples of the topology of the isolation network $\mathbf{Y_B}$.

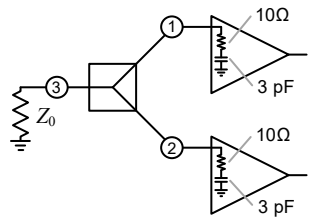


Figure 3.19: Example scenario where a divider with matching is useful.

Here $Y_{\mathrm{B},11}$ and $Y_{\mathrm{B},12}$ are design parameters that must satisfy

$$G_{\mathrm{IN},1}^2 - 2G_{\mathrm{IN},1}G_{\mathrm{B},11} + G_{\mathrm{B},11}^2 - G_{\mathrm{B},12}^2 = 0 \tag{3.40}$$

where $G_{\mathrm{IN},1}$, $G_{\mathrm{B},11}$ and $G_{\mathrm{B},12}$ are the conductive parts of $Y_{\mathrm{IN},1}$, $Y_{\mathrm{B},11}$ and $Y_{\mathrm{B},12}$, respectively. All in all, the solutions to the network parameters of $\mathbf{Y_{AL}}$, $\mathbf{Y_{AR}}$, and $\mathbf{Y_B}$ are functions of both the target impedances $Y_{\mathrm{IN},1} = Y_{\mathrm{IN},2}$, Y_{03}, and the choice of the topology of the isolation network $\mathbf{Y_B}$.

Figure 3.18 shows three examples of the topology of the isolation network $\mathbf{Y_B}$. The different solutions to the network $\mathbf{Y}_\mathrm{A}$ for the three cases are presented in [Paper D]. The conventional Wilkinson divider and the dividers in [132] and [127] are subsets of the generalized solutions of Figure 3.18(a), (b), and (c), respectively. For the three isolation topologies, the generalized design space offers more degrees of freedom since both the input admittances $Y_{\mathrm{IN},1} = Y_{\mathrm{IN},2}$ and $Y_{\mathrm{IN},3}$ are independent and can be complex.

3.3.2 Circuit Prototype - Integrated Matching

Below, the generalized divider is evaluated for a realistic scenario: an input power splitter directly matching to two PAs with complex input impedances at 2 GHz, see Figure 3.19(a). To demonstrate the flexibility of the method, a first generalized divider example (G.D. 1) with physical isolation is selected for evaluation. In particular, G.D. 1 has an isolation network comprising two 30° transmission lines and a resistor. To demonstrate the bandwidth trade-offs when having physical isolation, a second generalized divider example (G.D. 2) with only a resistor as the isolation network is also evaluated. Furthermore, a conventional Wilkinson divider with external matching at port 1 and 2 is added for comparison.

For practical and performance reasons at the design frequency of 2 GHz, both example dividers are realized with transmission lines. For a fair comparison, both example dividers (G.D. 1 and 2) are based on the "positive" $\Pi - \Pi$ realization of $\mathbf{Y_{AL}}$ and $\mathbf{Y_{AR}}$. A detailed description of the realizations is presented in [Paper C]. Schematics of G.D. 1, G.D. 2, and the conventional Wilkinson divider with single stub external matching at port 1 and 2 are

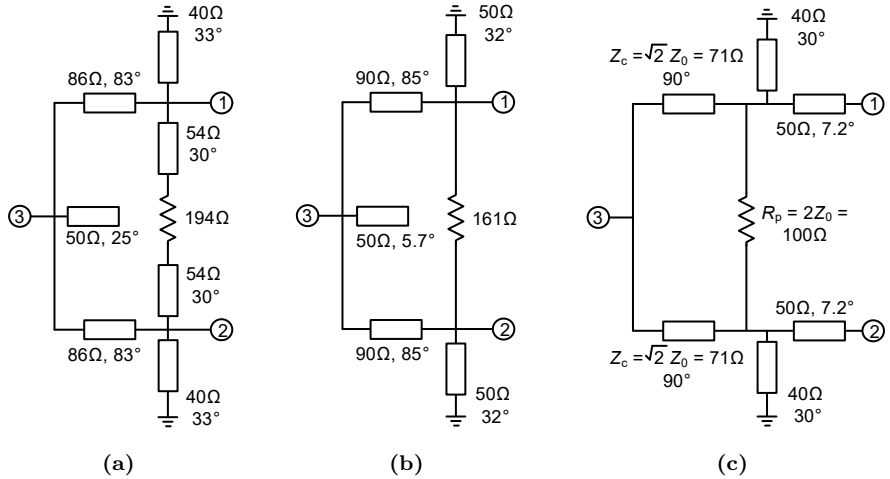


Figure 3.20: Schematics for three dividers. (a) The first example of the generalized divider (G.D. 1), where the isolation network comprises a resistor and two 30° transmission lines. (b) The second example of the generalized divider (G.D. 2), where the isolation network comprises a single resistor. (c) A conventional Wilkinson divider where port 1 and 2 have external single stub matching.

shown in Figure 3.20. It should be mentioned that the external matching can be implemented in a multitude of various manners, resulting in different performance. In this case, the simplest way is selected.

Figure 3.22(a) shows simulated $|S_{13}| = |S_{23}|$ for the ideal dividers. It can be seen that the divider G.D. 2 presents the close to the same bandwidth as the conventional Wilkinson divider with external matching. G.D. 1 demonstrates the bandwidth trade-off when including physical isolation. G.D. 1 and the Wilkinson divider were fabricated, see the photographs in Figure 3.21. The measured performance is shown in Figure 3.22(b).

Two example dividers in the generalized design space of two-way isolated dividers have been shown for an example amplifier scenario. The generalized divider presents a unique flexibility with direct integrated matching that does not sacrifice any bandwidth compared to a conventional Wilkinson divider with single stub external matching at port 1 and 2. Furthermore, the bandwidth trade-off when adding physical isolation was shown. Beyond the example scenario, the black-box method broadens the design space and provides new fundamental understanding of two-way isolated dividers.

Many other benefits and flexibilities could present themselves if the method is studied beyond the three examples of the topology of the isolation network. Furthermore, the method could be modified for asymmetrical splitting and phase asymmetry.

3.4 Chapter Summary

This chapter has demonstrated the potential of the black-box method. Unlocking all variables in a circuit/architecture, including the topology itself, broadens the design space and provides new understanding of the fundamental operation.

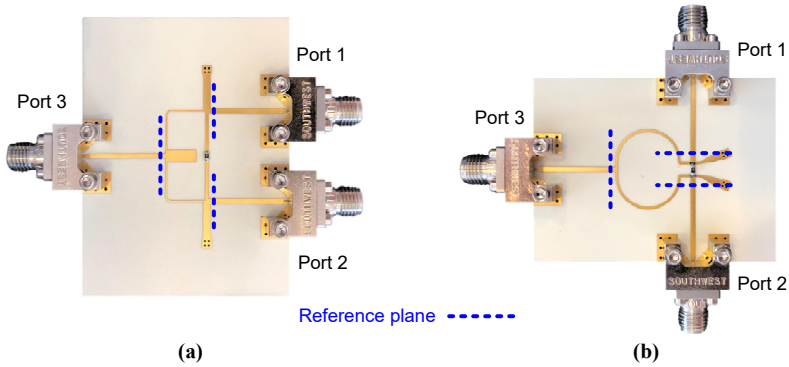


Figure 3.21: Photographs of the fabricated dividers (a) the generalized divider (G.D. 1) and (b) the conventional Wilkinson divider with external matching.

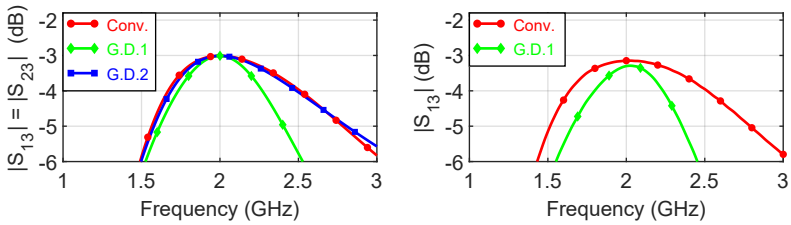


Figure 3.22: (a) Simulations of the ideal dividers in Figure 3.20. (b) Measurements of the fabricated dividers in Figure 3.21.

Applying the black-box method to the Doherty PA gives the insight that the conventional magnitude ratio of the maximum fundamental currents of the main and auxiliary transistors is an unnecessary constraint. Unlocking this ratio, i.e. applying current scaling, broadens the design space. This is particularly useful in real Doherty PA design where device periphery sizes might be limited. Furthermore, scaling down the relative size of the auxiliary transistor provides an overall higher gain. Current scaling and reactive mismatching enable new solutions that are simultaneously linear and efficient, which can reduce system complexity by omitting the DPD or lower its complexity. In practical designs, the black-box method facilitates the design procedure since many different solutions can be evaluated quickly. Finally, the method provides a combiner that is a single circuit block with integrated functionality, a block that simultaneously acts as the Doherty combiner, provides fundamental matching, and provides offset line functionality. An application exploiting this is a single dual-fed antenna element presenting the two-port parameters calculated from the black-box method. Such antenna improves integration, which can help reduce size and costs, and reduces losses.

Applying the black-box method to a two-way isolated divider broadens the design space. Not basing the divider on the topology of the conventional Wilkinson divider enables new functionality, such as direct integrated matching, physical isolation, and flexibility in the isolation network.

Chapter 4

Load Modulated Balanced Amplifier (LMBA)

The black-box combiner approach has expanded the design space of the well-established Doherty PA. Since the load modulated balanced amplifier (LMBA) is a relatively unexplored ALM PA architecture, this chapter focuses on its design equations when using a predefined combiner. The architecture comprises a quadrature balanced amplifier as a main branch and a control signal is injected through an auxiliary branch into the isolation port of the output coupler. The driving force behind the interest in the LMBA is the quadrature coupler, which can be made very broadband [134]. In contrast to the Doherty PA, where improved bandwidth is based on modifications to an inherently narrowband output combiner, the LMBA starts with an inherently broadband output combiner. This could potentially lead to improved performance across a wide bandwidth.

This chapter starts with a review of the brief history of the LMBA and the different variants. Then, one particular embodiment: the Doherty-like RF-input LMBA [Paper D] is presented.

4.1 Principle of Operation

The LMBA is a version of a three-way ALM PA. A generic three-way ALM PA is shown in Figure 4.1. For simplicity, the load termination is absorbed into the output combiner. For later analysis, two transistors are denoted main 1 and main 2, respectively, and the third transistor is denoted auxiliary. Note that the auxiliary transistor is sometimes called *control* transistor. The phase of all transistor inputs are related to one transistor, in this case main 1. For this circuit, the impedances presented to all three transistors, at any drive level, can be expressed as

$$Z_{\mathrm{l,m1}} = Z_{11} + Z_{12}\alpha_3 + Z_{13}\alpha_1 \tag{4.1}$$

$$Z_{\mathrm{l,m2}} = Z_{22} + Z_{12}/\alpha_3 + Z_{23}\alpha_2 \tag{4.2}$$

$$Z_{\mathrm{l,a}} = Z_{33} + Z_{13}/\alpha_1 + Z_{23}/\alpha_2 \tag{4.3}$$

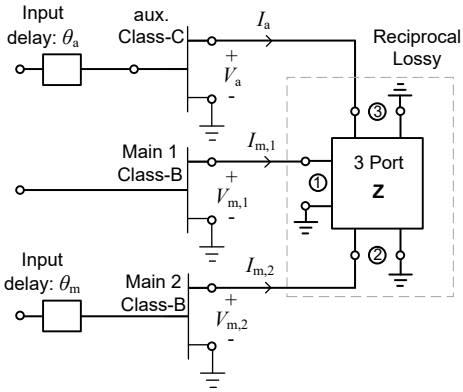


Figure 4.1: Shemetic of a generic three-way active load modulation power amplifier. The resistive load termination is absorbed into the output combiner.

where

$$\alpha_1 = I_{\mathrm{a}}/I_{\mathrm{m1}} \quad , \quad \alpha_2 = I_{\mathrm{a}}/I_{\mathrm{m2}} \quad \text{, and} \quad \alpha_3 = I_{\mathrm{m2}}/I_{\mathrm{m1}}. \tag{4.4}$$

It can be seen that are many different ways of introducing asymmetries in the currents versus the drive level for load modulation.

These equations are simplified significantly if the two main transistors are configured as a balanced amplifier with quadrature couplers at the input and output, see the main branch in Figure 4.2. In this balanced configuration, both main transistors provide equal fundamental drain currents in magnitude but the second transistor current is delayed 90° relative to the first transistor current, i.e. $I_{\mathrm{m2}} = I_{\mathrm{m1}} e^{-j\pi/2}$. If the load termination is equal to the system impedance of the output coupler, i.e. $R_{\mathrm{L}} = Z_{\mathrm{c2}}$, and is absorbed into the combiner, the resulting three-port parameters of the output combiner are

$$\mathbf{Z} = Z_{\mathrm{c2}} \begin{bmatrix} 0 & +j & -j\sqrt{2} \\ +j & 2 & -\sqrt{2} \\ -j\sqrt{2} & -\sqrt{2} & 1 \end{bmatrix}. \tag{4.5}$$

Using the currents of the two main transistors and the combiner impedance parameters, the loads presented to the two main transistors and to the auxiliary transistors are calculated to

$$Z_{\mathrm{l,m1}} = Z_{\mathrm{l,m2}} = Z_{\mathrm{c2}} \left(1 - j\sqrt{2}\alpha_1\right) \tag{4.6}$$

$$Z_{\mathrm{l,a}} = Z_{\mathrm{c2}}. \tag{4.7}$$

The load presented to the two main transistors can be changed around the characteristic impedance of the output coupler Z_{c2} depending on the current ratio α_1. Thus, any phase and/or magnitude asymmetry versus drive level results in load modulation for the main transistors. The auxiliary transistor, however, always sees a fixed load of Z_{c2}, independent of the current ratio α_1 and thereby independent of the drive level.

The LMBA architecture was first presented in [22], which utilizes both phase and magnitude asymmetry in the current ratio α_1 versus drive level. This makes

it possible to move the load modulation very freely in any direction. Thus, OMNs compensating transistor parasitics can be possibly be omitted, making it possible to directly utilize the benefits of a broadband quadrature coupler. Supply networks are, however, still required. The LMBA in [22] comprises broadband off-the-shelf couplers, and has no OMNs for the BA transistors. The control signal is injected separately with a fixed power roughly 6 dB lower than the maximum power of one main transistor. The main transistors are class-B biased. In a more practical implementation, an auxiliary transistor would amplify the control signal. The fixed output power and fixed load presented to an auxiliary transistor would result in a constant DC power consumption. This does not lower the system efficiency significantly due its relative low power.

The same embodiment as [22] was demonstrated in [135], but with a reconfigurable supply voltage versus frequency. Despite the extra degrees of freedom from the reconfigurable supply, the limited load modulation with fixed control signal power could not overcome resonances introduced by the supply networks. This resulted in reduced efficiency for some frequencies. In [136], a similar embodiment was demonstrated, where an auxiliary transistor is utilized for the control signal amplification and different discrete output power levels from this branch were studied.

The first single RF-input LMBA was demonstrated in [137, 138]. The load modulation is achieved through only magnitude asymmetry in the current ratio α_1. More specifically, both the BA and auxiliary transistors are operated in class-B mode, but the auxiliary transistor compresses earlier than the BA transistors. Since only magnitude asymmetry is utilized, it is challenging to achieve the best possible load modulation without OMNs for the BA transistors. In [138], however, the target load modulation trajectories for different frequencies are relaxed somewhat – in a way that the OMNs can be omitted completely. This facilitates wideband PA design significantly. Each frequency requires a different static phase in the current ratio α_1 (versus input power). This is achieved by a Butterworth filter at the input to the BA. The approach in [137, 138] is largely empirical since it relies on different compression characteristics of the BA and auxiliary transistors. Furthermore, the compression approach for achieving magnitude asymmetry in the current ratio α_1 limits the possible dynamic range of load modulation.

In [139], a dual RF-input LMBA with driving profiles resembling the ones in the Doherty PA was presented. Magnitude only asymmetry in the current ratio α_1 is achieved by having the BA transistors operate in class-B mode and to have the auxiliary transistor operate in class-C mode. In this embodiment, OMNs for the BA transistors are required for an appropriate load modulation. It was shown that the required OMNs of the BA transistors do not affect the dynamic range of load modulation. The prototype PA utilizes a nonlinear digital input power splitting function between the BA and the auxiliary transistor. This splitting function is found empirically together with the class-C bias of the auxiliary transistor. The phase difference between the two inputs is static versus drive level but varies versus frequency. Further measurements [140, 141] were later reported for the prototype LMBA in [139]. In [140], it was demonstrated that a nonlinear input splitting function yields somewhat better performance compared to using a linear splitting function emulating a passive splitter for that particular prototype. In [141], it was shown that a real passive input

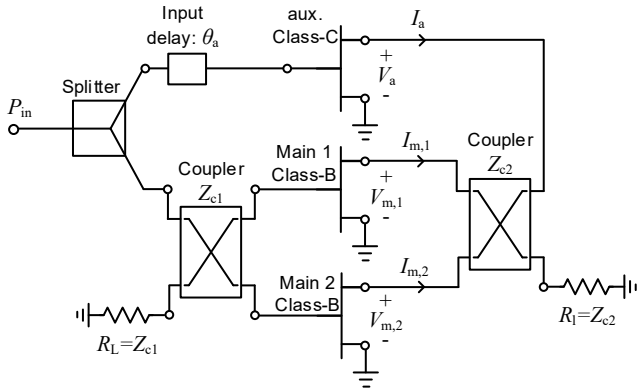


Figure 4.2: Schematic of a RF-input Doherty-like load modulated balanced amplifier.

splitter results in the same performance as an emulated passive splitter at a single frequency.

In [Paper D], a single RF-input Doherty-like LMBA was presented, where the theoretical analysis goes beyond the analysis in [139]. The derived design equations allow a direct comparison to other ALM architectures. The analysis and experimental verification are summarized in the next section.

4.2 Doherty-Like RF-Input LMBA

First in this section, the theoretical analysis using ideal transistor from [Paper D] is summarized. Then, the large signal performance for ideal transistors is presented. Finally, a fabricated prototype PA based on the design equations is shown.

4.2.1 Ideal Design Equations

Figure 4.2 shows a RF-input Doherty-like LMBA. In the following analysis, no OMNs are included for the BA or auxiliary transistors. It will be shown that this results in a constraint in the auxiliary transistor supply voltage. The analysis could be done with an OMN for the auxiliary transistor with different results. It will be shown that the constraint is not necessarily a limitation. Generally, when studying the fundamental operation of different ALM architectures, many required networks are omitted, such as harmonic terminations and parasitic matching. Thus, analyzing the RF-input Doherty-like LMBA without OMNs allows for a direct comparison with other architectures, as was done in Section 2.4. Furthermore, since OMNs can be implemented in many different ways, including them in the analysis makes it more difficult to assess fundamental bandwidth constraints.

The two main transistors are modelled as linear class-B mode and the auxiliary transistor is modelled as a class-C mode, where the fundamental and DC drain currents are simplified to piece-wise linear functions, like in the Doherty PA analysis in Section 3.2.1.

The target fundamental load impedances for the two main transistors at the maximum and backed-off drive level can be expressed in terms of the optimal class-B impedance R_{opt} as

$$Z_{\mathrm{l,m1,max}} = Z_{\mathrm{l,m2,max}} = R_{\mathrm{opt}} \tag{4.8}$$

$$Z_{\mathrm{l,m1,bo}} = Z_{\mathrm{l,m2,bo}} = R_{\mathrm{opt}}/\beta_{\mathrm{bo}}. \tag{4.9}$$

If the supply voltage of the auxiliary transistor is related to the supply voltage of the main transistors as: $V_{DS,a} = xV_{\mathrm{DS}}$, the target impedance of the auxiliary transistor can be expressed as

$$Z_{\mathrm{l,a,max}} = \frac{xR_{\mathrm{opt}}}{|\alpha_{1,\mathrm{max}}|} \tag{4.10}$$

where $\alpha_{1,\mathrm{max}}$ is the current ratio at maximum drive level, i.e. $\alpha_{1,\mathrm{max}} = I_{\mathrm{a,max}}/I_{\mathrm{m1,max}}$. With these target impedances, the unknown design parameters are solved from (4.6) and (4.7) to

$$Z_{\mathrm{c2}} = R_{\mathrm{opt}}/\beta_{\mathrm{bo}} \tag{4.11}$$

$$\alpha_{1,\mathrm{max}} = \frac{1-\beta_{\mathrm{bo}}}{\sqrt{2}} e^{-j\pi/2} \tag{4.12}$$

$$x = \frac{1-\beta_{\mathrm{bo}}}{\sqrt{2}\beta_{\mathrm{bo}}}. \tag{4.13}$$

The relation between the back-off drive level β_{bo} and the dynamic range of efficiency enhancement γ is found by expanding (2.8). This results in

$$\gamma = \left(\frac{1+\beta_{\mathrm{bo}}}{2\beta_{\mathrm{bo}}}\right)^2. \tag{4.14}$$

The RF-input Doherty-like LMBA presents a linear phase of the voltage across the load termination but a nonlinear gain characteristic in the load modulation region. The gain compression can be expressed as

$$G_{\mathrm{comp}} = \frac{G_{\mathrm{max}}}{G_{\mathrm{bo}}} = \left(\frac{1+\beta_{\mathrm{bo}}}{2}\right)^2. \tag{4.15}$$

The relative size of the auxiliary transistor can be expressed as [Paper D]

$$S_{\mathrm{aux}} = \frac{\pi}{2\sqrt{2}} \frac{(\beta_{\mathrm{bo}}-1)^2}{\cos^{-1}(\beta_{\mathrm{bo}}) - \beta_{\mathrm{bo}}\sqrt{1-\beta_{\mathrm{bo}}^2}}. \tag{4.16}$$

These parameters were studied versus γ in Section 2.4 and are compared to other ALM PA architectures. One of the drawbacks of the RF-input Doherty-like LMBA is that the auxiliary transistor supply voltage becomes unrealistically large for large values of γ, see Figure 2.8(d). As mentioned before, it is possible to include an OMN for the auxiliary transistor. However, if the output combiner in an ALM PA is directly presenting the theoretical optimal resistive impedances (when conventional PA classes are used), the OMNs required for real transistors only need to compensate for transistor parasitics. Nevertheless, in this approach, a range around 5 to 7 dB for γ is realistic.

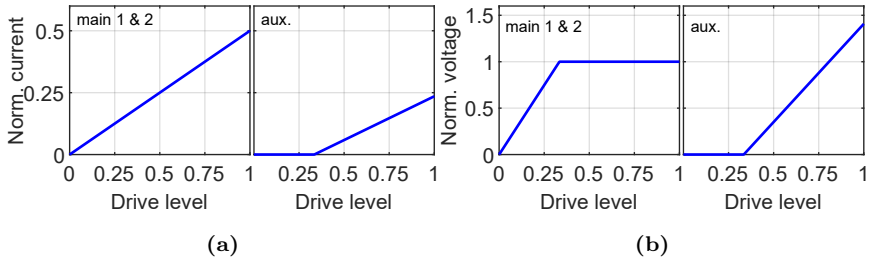


Figure 4.3: (a) Current and (b) voltage profiles of the RF-input LMBA. The current is normalized with I_{MAX}. The voltage is normalized with the main transistor supply V_{DS}.

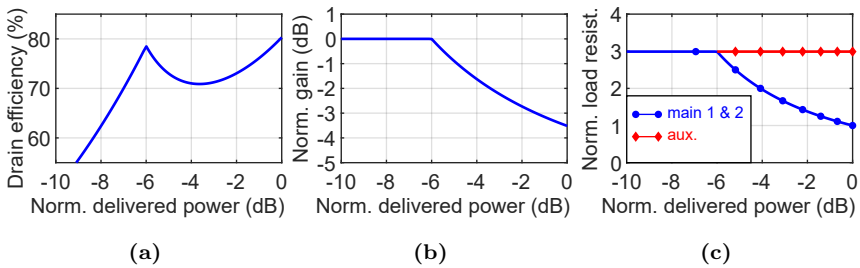


Figure 4.4: (a) Drain efficiency, (b) gain, and (c) load modulation versus normalized delivered power of the RF-input LMBA. The gain is normalized with itself at back-off. The load is normalized with R_{opt}.

Now, all necessary equations have been derived and the ideal performance can be studied. In particular, an RF-input Doherty-like LMBA designed for an efficiency range $\gamma = 6$ dB is studied.

In Figure 4.3, the magnitudes of the fundamental drain currents and voltages for all transistors are plotted versus drive level. It can be seen that the current profiles of all transistors and the voltage profiles of the main transistors resemble the Doherty PA profiles. Unlike the Doherty PA, the fundamental voltage of the auxiliary transistor is zero at the backed-off drive level. For an ideal transistor, the backed-off off-state output impedance in class-C mode is open circuit. A real transistor presents a lossy capacitive off-state impedance. In a Doherty PA, this complex off-state impedance must be accounted for in practice for proper load modulation, usually done with an offset line [103]. The zero voltage and current at the backed-off drive level in the Doherty-like LMBA indicates two things: there is no need to compensate for any complex off-state impedance in a real transistor and there will be no power dissipation at the output of the auxiliary transistor at the backed-off drive level. The omission of an offset line results in a more compact circuit and potentially better bandwidth, as observed in [139]. No power dissipation results in improved efficiency at the backed-off drive level for real transistors.

The drain efficiency, gain, and load modulation are plotted in Figure 4.4. The efficiency profile is very similar to the profile of the Doherty PA. The small differences come from different relative sizes of the auxiliary transistor, different class-C bias, and different loads presented to the auxiliary transistor.

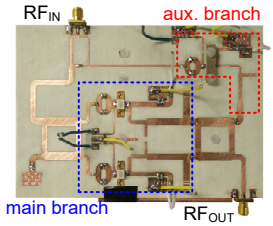


Figure 4.5: Photograph of the fabricated RF-input LMBA in [Paper D].

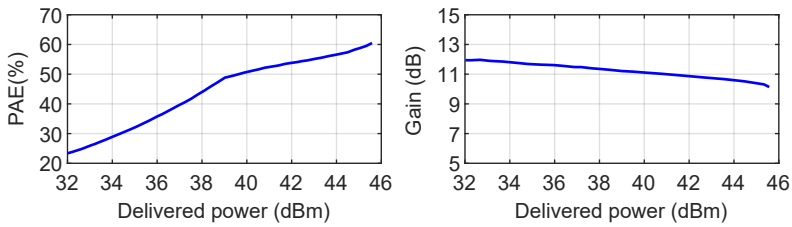


Figure 4.6: CW measurements at 2.4 GHz of the fabricated PA in [Paper D].

The gain presents the compression predicted by (4.15). The load modulation of the main transistors resemble the Doherty PA load modulation but the load presented to the auxiliary transistor is constant.

4.2.2 Circuit Prototype

The design equations were experimentally verified with a prototype PA in [Paper D], designed for $\gamma = 6$ dB and for 2.4 GHz. The prototype PA employs two 10-W GaN HEMTs (CGH40010F from Wolfspeed) for the main transistors and a 6-W GaN HEMT (CGH40006P from Wolfspeed) for the auxiliary transistor. Targeting $\gamma = 6$ dB results in $S_{\text{aux}} = 0.54$, see (4.16). Thus, the transistor size selection fits well. The main transistors are supplied with 24 V and the auxiliary transistor is supplied with 34 V. A photograph of the fabricated RF-input LMBA prototype is shown in Figure 4.5. A schematic can be found in [Paper D].

Measured CW performance is presented in Figure 4.6. The measured results agree reasonably well with simulations of the prototype PA, for more details, see [Paper D]. The prototype PA presents a PAE of 50% at 6 dB OPBO. Modulated measurements for the prototype PA are presented for a 10 MHz LTE signal with 7.5 dB PAPR in [Paper D]. The PA presents an average drain efficiency of 47% with an average delivered power of 38.0 dBm. Without DPD, the PA presents an adjacent channel power ratio of -27 dBc. The fabricated prototype demonstrates the potential of the architecture. However, future studies should include the interaction with OMNs and focus on increasing the bandwidth. Nevertheless, [Paper D] contributes with a useful initial study.

4.3 Chapter Summary

This chapter has reviewed the brief history of the LMBA architecture and has summarized the embodiment RF-input Doherty-like LMBA from [Paper D]. The utilization of a broadband quadrature coupler has shown great broadband capabilities for dual RF-input designs [22, 135] and for single RF-input designs [138]. Initial studies of the Doherty-like LMBA have been presented for dual-RF inputs in [139] and for single RF-input in [Paper D]. Clever designs of the LMBA has allowed omission or reduced OMNs for the BA transistors, as shown in [22,135,138], making it possible to fully exploit broadband quadrature couplers as the output combiner. The Doherty-like driving makes it possible to realize a simple and effective analog input power splitter.

There are many things yet to study for the LMBA architecture. For the dual RF-input implementation, theoretical input driving profiles (in magnitude and phase) can be studied when including the required supply network and transistor parasitics. The effect of harmonic terminations can also be included. Theoretical analysis can also be done for the RF-input Doherty-like LMBA with frequency dependent OMNs, supply networks, transistor parasitics, and harmonic terminations.

Chapter 5

Load-Pull Based Active Load Modulation PA Emulation

In the PA design stage, it is crucial to predict the performance before fabrication. This chapter presents a new measurement-based design methodology for ALM PAs. This methodology can predict the full ALM behavior and gives measurement-based insight into the internal working principle before the full circuit is manufactured.

5.1 PA Performance Prediction

The most challenging circuit element to predict is the transistor. Transistor performance prediction can be simulation and/or measurement based. For a single-ended PA, load-pull measurements can predict the PA performance for CW and modulated signals very accurately, see [142] for an overview. Simulations of PA performance requires an accurate transistor model. The development of transistor models can in some cases be very time consuming [143]. However, with the model obtained, evaluating PA performance for many different design considerations (terminations, biasing etc.) can be done very quickly. Research is concurrently enhancing transistor model accuracy, for example by improved modelling of dynamic effects due to transistor trapping [144].

Measurement- and simulation-based performance prediction becomes more challenging for ALM PAs, where multiple transistors are interacting with each other. The following example demonstrates one challenge when using measurement-based load-pull data, extracted for individual transistors, in Doherty PA design. At the backed-off drive level in a class-B/C Doherty PA, the auxiliary transistor should be off. However, the output current of the main transistor will be coupled to the gate of the auxiliary transistor. This effectively changes the drive level where the auxiliary transistor turns on. This can be accounted for by post-tuning the auxiliary bias. This, in turn, can change the optimal impedance that should be presented to the auxiliary transistor

and the inherent phase delay of the auxiliary transistor. Thus, the combiner might not be optimal any longer and should be re-optimized, which in turn changes the coupling to the auxiliary transistor gate. Furthermore, harmonic and intermodulation load-modulation is not captured in this design approach. Transistor models are not necessarily optimized to be the most accurate for ALM PA operation. After all, several reported ALM PA prototypes present some degree of disagreements between simulations and measurements, e.g. see [58, 61, 82, 138, 145, 146]. Post-tuning can restore the performance of a fabricated ALM PA, such as tuning the input phase delays, input power splitting, bias, and physical modifications of the matching networks. This is often time consuming and might not yield satisfactory results.

The performance of an ALM PA can be understood by observing the voltage waves at the transistor outputs. This is easily done in simulations. They can also be measured if couplers are incorporated at the transistors outputs [147]. This is impractical and modifications to the OMNs are required. The voltage waves can also be measured with near-field probing [148]. Both of these methods, however, only provide insight after the prototype is manufactured.

Measured-based emulation is another approach in predicting ALM PA performance in the design stage [Paper E]. The idea is to capture the full ALM PA behavior by using active load-pull measurements. A single transistor (or device under test, DUT) is exited in turns as different states, corresponding to the different transistors in an ALM PA. The load impedance in one state is determined by the knowledge about the behavior of the other transistors and the combiner parameters. Emulation captures the full ALM PA behavior and it provides measurement-based insights into the interaction between the transistors in an early design stage.

The first version of active load-pull emulation was demonstrated in [149–151], where the coupling between PAs in an antenna array is studied. The initial work in [149] demonstrated that this approach simplifies studies of how the PAs are affected by coupling in an antenna array, compared to over-the-air measurements. In [150, 151], the effects of the antenna coupling is studied in more detail by removing the inherent individual PA distortion through DPD. Different input phase delays are studied for different antenna array applications, e.g. beam forming and massive MIMO.

ALM PA emulation is more challenging than antenna array emulation. The coupling is significantly larger. Furthermore, the dynamic loading conditions of the transistors are not necessarily centered on 50 Ω, which puts more stringent requirements on accuracy of the load-pull setup. Phase differences between branches have to be treated more carefully. For example, if an analog input phase delay should be emulated, the phase delay cannot simply be added to the output waves. This is explained in more detail in the next section. Furthermore, the different transistors are operating under very different conditions. For these reasons, more consideration has to be put into the emulation method, higher accuracy of the active load-pull setup is required, and convergence can be more challenging.

In [Paper E], an initial study of ALM PA emulation is demonstrated on a two-way Doherty PA. These first experiments aim to be as simple as possible in order to demonstrate that the method works: only CW signals are studied, two off-the-shelf PAs matched to 50 Ω are used for the two branches, and low-pass

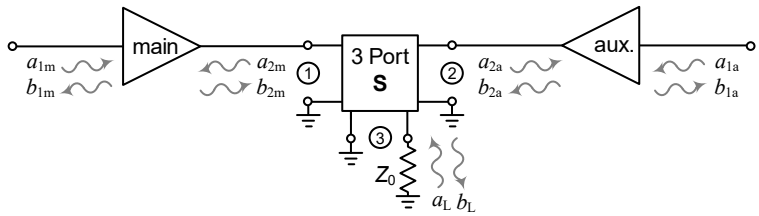


Figure 5.1: The voltage waves in a two-way Doherty PA.

filters are added to the outputs of the branch PAs for harmonic suppression. Although the initial study is simplified, the ultimate goal of the emulation method is to use it in the design stage to identify the optimal combiner and operation conditions of the transistors.

5.2 Two-Way Doherty PA Emulation

This section presents the ALM PA emulation method, applied to a two-way Doherty PA, from [Paper E]. In this implementation, a single active load-pull setup is used, where a single DUT is acting as the main and auxiliary transistors, respectively, in turn. It is assumed that the main and auxiliary branches include all necessary amplifier blocks, such as bias networks. Therefore, hereinafter, these branches are referred to as the main and auxiliary branch PAs. First in this section, the emulation method is fully explained. Thereafter, the experimental results are presented.

5.2.1 Method

The different voltage waves in a two-way Doherty PA are defined in Figure 5.1. The combiner is represented by a generic passive three-port network. The third port of this three-port network is terminated with the system impedance Z_0. Thus, the two-port S-parameters of an equivalent combiner, with the load termination inside, has equal S_{11}, S_{12} and S_{22} as the three-port representation.

The emulation method is described by the following. For one set of emulations, the input power is fixed. This means that $|a_{1m}|$ and $|a_{1a}|$ are fixed for one set. The magnitude ratio $|a_{1m}|/|a_{1a}|$ can be selected arbitrarily. For example, to emulate a 3-dB analog splitter, the relation $|a_{1m}| = |a_{1a}|$ should be fulfilled for all input powers (all emulation sets). In each emulation set, the procedure is done in iterations until convergence is obtained. Each iteration consists of two measurements: one measurement when the DUT is excited as the main branch PA and one measurement where the DUT is excited as the auxiliary branch PA, see Figure 5.2.

The active load-pull setup has two input signals: X_{TX1} and X_{TX2}. These two signals are amplified by a respective driver amplifier, with the respective complex voltage gains G_{TX1} and G_{TX2}. The input signal X_{TX1} is fixed for one emulation set. The output from the TX2 driver amplifier should produce the a_2 wave that appears in a Doherty PA. This desired wave a_2 is denoted $a_{2,\mathrm{want}}$. The second input signal X_{TX2} can be determined from

$$a_{2,\mathrm{want}} = X_{\mathrm{TX2}} G_{\mathrm{TX2}} \tag{5.1}$$

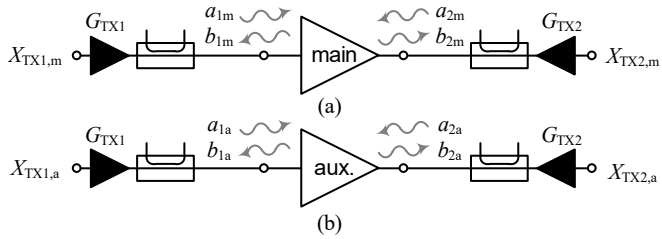


Figure 5.2: The emulation procedure in an active load-pull setup. In each iteration, there are two measurements: (a) one for the main PA and (b) one for the auxiliary PA. In the active load-pull setup, there are two input signals: X_{TX1} and X_{TX2}, which are amplified by individual driver amplifiers with the complex voltage gains G_{TX1} and G_{TX2}, respectively.

As mentioned, the desired wave $a_{2,\mathrm{want}}$ should be the a_2 wave that appears in a Doherty PA. In a Doherty PA, the a_2 waves of the main and auxiliary branch PAs are dependent on both the respective output waves of the main and auxiliary PAs, e.g. $a_{2\mathrm{m}} = S_{11}b_{2\mathrm{m}} + S_{12}b_{2\mathrm{a}}$ for the main PA. The b_2 waves are in turn dependent on the a_2 waves. Thus, the desired wave $a_{2,\mathrm{want}}$, that is to be injected at the DUT output, has to be based on previous measurements. For this reason, the procedure has to be done in iterations. For each iteration n, there are two measurements where the desired waves $a_{2,\mathrm{want}}$ are determined by

$$\text{Measurement 1}: \quad a_{2\mathrm{m,want}}(n) = S_{11}b_{2\mathrm{m}}(n-1) + S_{12}b_{2\mathrm{a}}(n-1) \tag{5.2}$$

$$\text{Measurement 2}: \quad a_{2\mathrm{a,want}}(n) = S_{22}b_{2\mathrm{a}}(n-1) + S_{21}b_{2\mathrm{m}}(n-1) \tag{5.3}$$

The iteration procedure is summarized in Table 5.1. Initially, the measured waves a_{2m} and a_{2a} will not be equal to the desired waves $a_{2,\mathrm{want,m}}$ and $a_{2,\mathrm{want,a}}$, respectively. If the iterations converge, they will be equal. An error metric is defined as

$$\mathrm{error}(n) = |a_2(n) - a_{2,\mathrm{want}}(n)|/|a_{2,\mathrm{want}}(n)|. \tag{5.4}$$

When this error is close to zero, the iterations can stop and the emulation set is presumed converged. A small enough error means that (5.2) and (5.3) are fulfilled independent of the iteration n, which means that the true Doherty PA behavior is emulated.

The initial value of $a_{2,\mathrm{want}}$ for the main and auxiliary branch PAs can be any value. A practical approach is to set them to zero, which corresponds to no injection from TX2 in the first iteration (denoted iteration 0).

In a Doherty PA, the phase difference between $b_{2\mathrm{m}}$ and $b_{2\mathrm{a}}$ is important. In practice, however, a phase difference is introduced at the input, i.e. between $a_{1\mathrm{m}}$ and $a_{1\mathrm{a}}$. The input phase difference ($-\theta_{\mathrm{in}} = \angle(a_{1\mathrm{a}}/a_{1\mathrm{m}})$) is not equal to the output phase difference ($-\theta_{\mathrm{out}} = \angle(b_{2\mathrm{a}}/b_{2\mathrm{m}})$) since the two branch PAs have different inherent phase delays ($-\phi_{\mathrm{m}} = \angle(b_{2\mathrm{m}}/a_{1\mathrm{m}})$ and $-\phi_{\mathrm{a}} = \angle(b_{2\mathrm{a}}/a_{1\mathrm{a}})$). Since a single active load-pull setup is used, the phases of all waves in a single measurement are normalized to a_1. Therefore, the input phase difference is introduced by modifying the desired waves to

$$a_{2\mathrm{m,want}} = S_{11}|b_{2\mathrm{m}}|e^{-j\phi_{\mathrm{m}}} + S_{12}|b_{2\mathrm{a}}|e^{-j\phi_{\mathrm{a}}-j\theta_{\mathrm{in}}} \tag{5.5}$$

$$a_{2\mathrm{a,want}} = S_{22}|b_{2\mathrm{a}}|e^{-j\phi_{\mathrm{a}}} + S_{21}|b_{2\mathrm{m}}|e^{-j\phi_{\mathrm{m}}+j\theta_{\mathrm{in}}} \tag{5.6}$$

Table 5.1: The iteration procedure for a two-way Doherty PA. The active load-pull setup has two inputs (X_{TX1} and X_{TX2}), see Figure 5.2. For one emulation set, X_{TX1} is fixed for each iteration. Each iteration has two measurements: one for the main branch PA operation and one for the auxiliary branch PA operation. In each iteration, X_{TX2} is determined by measurements from the previous iteration.

		Input	Outputs		
Iteration, n	Measurement	$\frac{X_{\mathrm{TX2}}}{G_{\mathrm{TX2}}}(n) = a_{2,\mathrm{want}}(n)$	$b_2(n)$	$a_2(n)$	error(n)
0	1	0	$b_{2\mathrm{m}}(0)$	$a_{2\mathrm{m}}(0)$	
	2	0	$b_{2\mathrm{a}}(0)$	$a_{2\mathrm{a}}(0)$	
1	1	$S_{11}b_{2\mathrm{m}}(0) + S_{12}b_{2\mathrm{a}}(0)$	$b_{2\mathrm{m}}(1)$	$a_{2\mathrm{m}}(1)$	$\mathrm{error_m}(1)$
	2	$S_{22}b_{2\mathrm{a}}(0) + S_{21}b_{2\mathrm{m}}(0)$	$b_{2\mathrm{a}}(1)$	$a_{2\mathrm{a}}(1)$	$\mathrm{error_a}(1)$
2	1	$S_{11}b_{2\mathrm{m}}(1) + S_{12}b_{2\mathrm{a}}(1)$	$b_{2\mathrm{m}}(2)$	$a_{2\mathrm{m}}(2)$	$\mathrm{error_m}(2)$
	2	$S_{22}b_{2\mathrm{a}}(1) + S_{21}b_{2\mathrm{m}}(1)$	$b_{2\mathrm{a}}(2)$	$a_{2\mathrm{a}}(2)$	$\mathrm{error_a}(2)$
⋮		⋮		⋮	
n	1	$S_{11}b_{2\mathrm{m}}(n\text{-}1)+S_{12}b_{2\mathrm{a}}(n\text{-}1)$	$b_{2\mathrm{m}}(n)$	$a_{2\mathrm{m}}(n)$	$\mathrm{error_m}(n)$
	2	$S_{22}b_{2\mathrm{a}}(n\text{-}1)+S_{21}b_{2\mathrm{m}}(n\text{-}1)$	$b_{2\mathrm{a}}(n)$	$a_{2\mathrm{a}}(n)$	$\mathrm{error_a}(n)$

For simplicity, the iteration dependencies are not written out explicitly in the equations above. Finally, the performance at the load of the combiner needs to be calculated. The output wave from the third port of the combiner, b_{L}, is calculated from

$$b_{\mathrm{L}} = S_{31}|b_{2\mathrm{m}}|e^{-j\phi_{\mathrm{m}}} + S_{32}|b_{2\mathrm{a}}|e^{-j\phi_{\mathrm{a}}-j\theta_{\mathrm{in}}} \tag{5.7}$$

Since the third port of the combiner is terminated with the system impedance Z_0, the reflected wave in this node is zero ($a_{\mathrm{L}} = 0$). Now, all necessary details of the method have been explained.

5.2.2 Preliminary Experimental Results

Initial experimental results were done in [Paper E]. Two off-the-shelf 6-W PAs operated at 2.14 GHz are used (Wolfspeed CGH40006P-TB). The initial experiment emulates the system, containing two PAs and a combiner, shown in Figure 5.3. The combiner is based on the conventional quarterwave topology, see [Paper E] for a schematic. The measured S-parameters of this combiner are used in the emulations. The active load-pull setup is based on the WebLab measurement system [151, 152]. This setup does not have harmonic injection capabilities. Therefore, a low pass filter is added to the outputs of the main and auxiliary branch PAs, respectively. The emulation is compared to verification measurements, in which a power meter is connected to the output of the combiner. The single PA used in the emulation is used as the main branch PA in the verification measurements. The input signals in the emulation represent a static analog power splitter and a static analog phase delay, see [Paper E] for details.

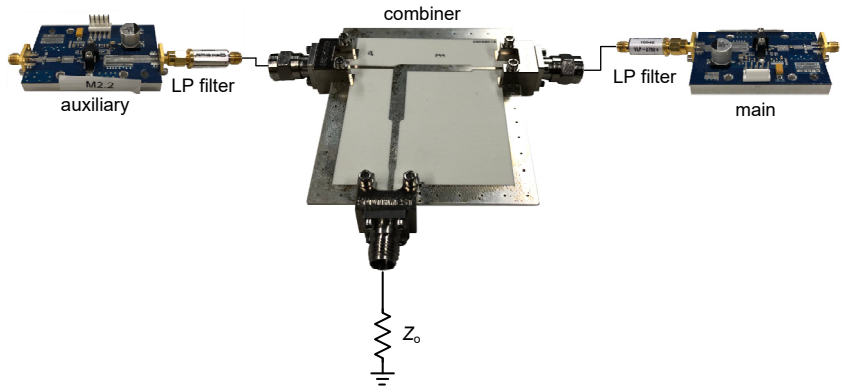
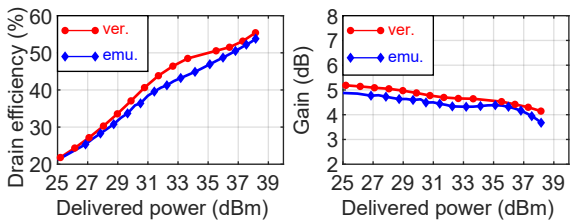


Figure 5.3: Photograph of the Doherty PA. The measured S-parameters of the combiner are used for the emulation. The two PAs are connected to the combiner in the verification measurements.



(a) **(b)**

Figure 5.4: Comparison of verification measurements and emulation at 2.14 GHz.

Figure 5.4 compares the Doherty PA drain efficiency and gain of the emulation and verification measurements. The difference in verification measurements relative to emulations in the figure are as follows. For the efficiency, there is a maximum difference of +4.5 percentage points at 33.6 dBm of delivered power. The average difference is +1.6 percentage points from 18.2 to 38.2 dBm. For the gain, the there is a maximum difference of +0.46 dB at 38.2 dBm. The average difference is +0.31 dB from 18.2 to 38.2 dBm. The authors of [Paper E] believe that the disagreement between verification measurements and emulations are due to a non-perfect calibration of the active load-pull system. This will be improved upon in future work. Nevertheless, the new type of measurement based insights coming from the method can still be observed.

Figure 5.5 and 5.6 demonstrate the measurement-based insights into the internal Doherty operation. Figure 5.5 shows the emulated behavior in the plane before the combiner, i.e. just at the outputs of the filters. The figure shows the Doherty PA performance and the individual main and auxiliary branch PA performance. Figure 5.5(a) and (b) show the drain efficiency and gain versus the power available from source (i.e. the power before the input power splitter that is imitated). Figure 5.5(c) shows different phases versus power available from source. The nonlinear nature of the output phase delay θ_{out} is clearly demonstrated. Figure 5.6 shows the load modulation of the main and auxiliary branch PAs in the plane before the combiner. The information

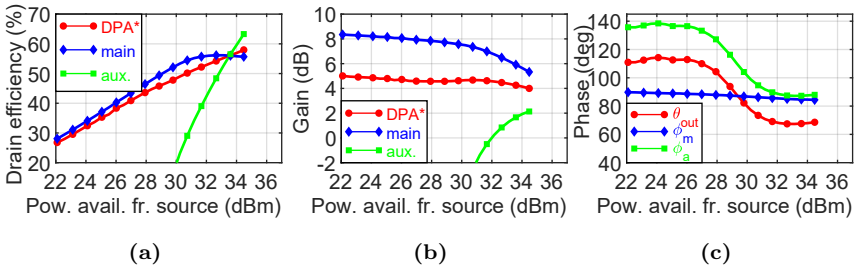


Figure 5.5: Emulated behavior in the plane before the combiner, i.e. just at the outputs of the filters. Different performance metrics for the Doherty PA, and the main and auxiliary PAs. The performance is plotted versus the power available from source (i.e. the power before the input power splitter that is imitated).

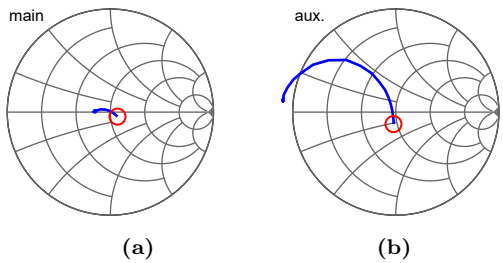


Figure 5.6: Emulated dynamic load of the (a) main PA and (b) auxiliary PA. The red circles mark maximum input power.

from this internal operation, which is difficult to obtain with other methods, could facilitate identifying optimal Doherty PA performance in future designs, by investigating different combiners and ways to operate the transistors (bias, phase delays, etc.)

5.3 Chapter Summary

This chapter has briefly reviewed conventional ALM PA design methods. It was shown that the active load-pull emulation method has great potential for ALM PAs. This method can predict the intricate behavior in ALM PAs and it gives measurement-based insights into the internal operation of the circuit in the design stage.

In future work, the method should be demonstrated for ALM PAs using modulated signals. Different combiners, biases, input power split ratios, and phase delays can be studied in emulation before fabrication, to find a solution with the best possible performance. Using this method, the design of an ALM PA could also be done in conjunction with DPD capabilities.

Chapter 6

Conclusions

A profound understanding of the fundamental operation in PA architectures is required to design for future demands. This thesis has presented several promising techniques to meet this goal.

An analytical combiner approach has been applied to a two-way Doherty PA. The principle of operation was generalized by treating the output combiner as a black-box and solving its parameters for a novel continuum of current profiles. Solving for maximum efficiency and scaling the conventional maximum current magnitude ratio results in new solutions with significantly higher gain. Solving for linear gain and high efficiency, combined with current scaling and reactive mismatching, results in the possibility of controlling the phase response in the high power region. This control can be used to compensate the severe inherent phase distortion in the high power region – coming from the load modulation of real transistors – in Doherty PAs. Treating the output combiner as a black-box is a robust and flexible method that has enabled a whole new direction of Doherty PA research. One particularly interesting flexibility, demonstrated in this thesis, is the possibility of improved integration by using a dual-fed antenna as the Doherty combiner. It was also shown that the black-box approach is equally suitable for expanding the design space of isolated dividers, where new solutions with improved integration were identified.

The LMBA is an emerging efficiency enhanced PA. This thesis has focused one particular embodiment: the RF-input Doherty-like LMBA. This version allows for a simpler and more effective realization compared to dual-input LMBAs. It also demonstrates some interesting advantages over the Doherty PA: the constant impedance presented to the auxiliary transistor results in more flexibility and potentially improved performance, and the smaller relative size of the auxiliary transistor leads to higher gain.

A measurement-based design method for ALM PAs using active load-pull techniques has been presented. This method can predict the intricate behavior in ALM PAs and it gives measurement-based insights into the internal operation of the circuit in the design stage. This facilitates the design of ALM PAs for the overall optimal performance.

The thesis has presented different promising techniques for improved performance in high-efficiency PAs, such as improved linearity, higher gain, improved integration, lower losses, and improved design methodology. The results will

therefore contribute to the development of more energy efficient and high capacity wireless services in the future. Improved PA properties facilitate the realization of multi-antenna transmitters. Such transmitters, which will be a key ingredient in future wireless systems, can lower system energy consumption significantly. Altogether, the techniques presented in this thesis can facilitate the development of sustainable future wireless systems.

6.1 Future Work

Based on the requirements in future wireless systems, the author believes the seven following PA research topics to be highly relevant and interesting:

- **Wideband black-box Doherty PA**. In this thesis, all Doherty PA derivations assume single frequency operation. Solving the black-box equations for the continuous class-B/J mode of operation, and synthesizing a combiner with the appropriate frequency response, could lead to high efficiency across a large bandwidth.
- **Improved linearity of the black-box Doherty PA**. Current scaling and reactive mismatching enable improved linearity in the high power region without sacrificing much efficiency. Improvements of the gain compression versus efficiency in the low power region can lead to an even better efficiency-linearity trade-off.
- **Improved integrated Doherty antenna transmitter**. The radiation pattern, measurement uncertainties and transistor-to-antenna transition can be improved upon for an overall better transmitter. Adding receiver functionality to the same antenna would also be highly interesting.
- **Expanded functionality of the black-box divider**. Modifications for asymmetrical power splitting and for an asymmetrical phase difference between the branches can be studied. These properties, together with complex port terminations, are useful for input power dividers in ALM PAs.
- **N-way black-box combiner/divider**. Although it is straightforward to find solutions to the N-port network parameters, the circuit synthetization is not. Successful realization would be highly interesting for both ALM PAs and power dividers.
- **Wideband RF-input Doherty-like LMBA**. Theoretical analysis can be done when incorporating frequency dependent OMNs, harmonic terminations, and supply networks to explore wideband possibilities.
- **ALM emulation using modulated signals**. The next step in the emulation method is to use modulated signals. Furthermore, the ALM combiner design can be based on both the intended signal and the available DPD complexity. The emulation method can also be explored for Chireix outphasing and the Doherty-outphasing continuum.

Acknowledgments

Finally, you, the reader, have reached the end of this thesis – or, perhaps more likely, this chapter is among the first (or only) parts you have read and will read. Nevertheless, this chapter has been the most fun for me to write and I consider it to be of great importance. Even though it has been tough and challenging being a Ph.D. student these past five years, it has also been very enjoyable. Therefore, in these final pages, I would like to express my deepest gratitude to the people who have supported me throughout my studies, making this work possible.

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