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Test structures for evaluating Al$_2$O$_3$ dielectrics for graphene field effect transistors on flexible substrates

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Abstract — **We have developed a test structure for evaluating the quality of Al$_2$O$_3$ gate dielectrics grown on graphene for graphene field effect transistors on flexible substrates. The test structure consists of a metal/dielectric/graphene stack on a PET substrate and requires only one lithography step for the patterning of the topside metal electrodes. Results from measurements of leakage current, capacitance and loss tangent are presented.**

Keywords—test structures, graphene, field effect transistors, leakage current, capacitance, loss tangents, hysteresis

I. INTRODUCTION

Graphene is a two-dimensional material consisting of a single layer of carbon atoms arranged in a hexagonal lattice. Based on its unique electrical properties in combination with its chemical stability and mechanical flexibility, graphene has emerged as a promising material for flexible electronics in a wide range of applications. One such example is the flexible graphene terahertz detector previously reported in [1]. An important component in this context is the graphene-based field effect transistor (GFET), the properties of which when based on rigid SiO$_2$/Si substrates have developed rapidly in recent years. However, fabrication of high-performance GFETs on flexible substrates like polyethylene terephthalate (PET) substrates is a different story not yet well documented.

One crucial step in making high performance GFETs on flexible substrates is finding reproducible methods for fabricating dielectric films of high quality. In this paper, the design and fabrication of a test structure for evaluating the electrical properties of the gate dielectric will be described, and results from its use for evaluating the quality of flexible GFET Al$_2$O$_3$ dielectrics will be presented.

II. TEST STRUCTURE DESIGN AND FABRICATION

For evaluating the quality of the gate dielectric, a simple test structure was designed according to the principle shown in Fig. 1. The test structure is a metal-Al$_2$O$_3$-graphene capacitor placed on a flexible PET substrate. This type of test structure has been previously used with good results on solid substrates [2-3], but not before for evaluating the dielectric properties of

aluminum oxide (Al$_2$O$_3$) when the bottom electrode is a thin layer of graphene on a flexible PET substrate.

Also shown in Fig. 1 is the equivalent electrical circuit of the test structure. Since the dielectric was not patterned, there is no external contact to the graphene bottom plate. Instead, its dc potential is set through resistive voltage division. Since $R_P >> R_S + R_O$, most of the applied dc voltage occurs across the circular capacitor with capacitance C under test. Therefore, both the leakage current and the capacitance of the circular capacitor can be measured as a function of voltage. Similarly, during capacitance measurements the ac signal occurs across the circular capacitor under test since $C_O >> C$ because of the large area of the outer surrounding capacitor compared to the area of the inner capacitor. The only requirement for evaluating the dissipation losses is that the sheet resistance of the bottom graphene electrode must be known and uniform.

A. Test structure design

Test structures with three different diameters of the circular top electrode, 30, 40 and 50 μm, were designed for the purpose of evaluating the quality of the dielectric. The diameter of the outer circle defining the metal ground was 220 μm. The top Ti/Au electrode consists of a 100 nm layer of gold on top of a 5 nm adhesion layer of titanium, and was patterned by use of standard lift-off technology. With only the top metal layer being patterned, only one photolithographic process step is needed. As described above, probing during measurements is made from the topside of the test structure, with the potential of the bottom electrode being determined by resistive and capacitive voltage division. In the micro photo of the test structure shown in Fig. 2, the dark area surrounding the center top electrode is where the top metal was removed. For comparison, two types of structures are shown in Fig. 2. At the top of the photograph some complete test structures are shown with graphene as the bottom electrode, while at the bottom some open test structure are shown without the graphene electrode. The ripples below the outer electrode on the top structures are associated with the delamination of graphene from the PET substrate due to strain caused by the large area of the surrounding metal electrode. However, no ripples are to be seen below the center top electrode. Previous investigations indicate that there is usually no delamination of graphene under metal electrodes smaller than 100×100 μm^2.
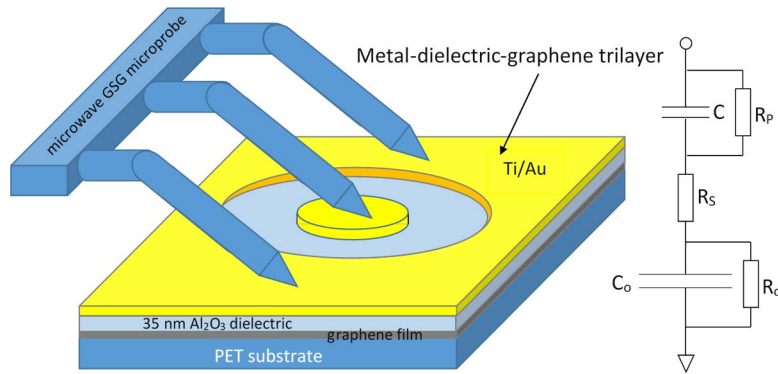
Fig. 1. Metal-dielectric-graphene trilayer test structure and equivalent circuit.

B. Test structure fabrication

Initially, the graphene for the bottom electrode was grown by chemical vapor deposition (CVD) on copper foil. The graphene was separated from the copper foil using electro-chemical bubbling and transferred to the PET substrate using a supporting polymer PMMA frame that was dissolved after transfer. However, due to low yield, measurement results to be reported in this paper are from CVD graphene films on PET substrates acquired from Graphenea. In this case, the graphene film was separated from the copper foil and transferred to the PET substrate using a wet process indicating that the copper foil was removed by wet etching. When separated from the copper foil, the graphene film was placed on the target PET substrate to which it adheres by van der Waals forces. One of the main problems of any transfer method, and the disadvantage of not being able to deposit the graphene film directly on the target substrate, is that the graphene after transfer often shows some tears, wrinkles, and holes [4]. The dielectric film was formed by natural oxidation of a 3 nm thick aluminum film followed by e-beam evaporation of a 30 nm layer of Al_2O_3. The final thickness of the dielectric film was around 35 nm.
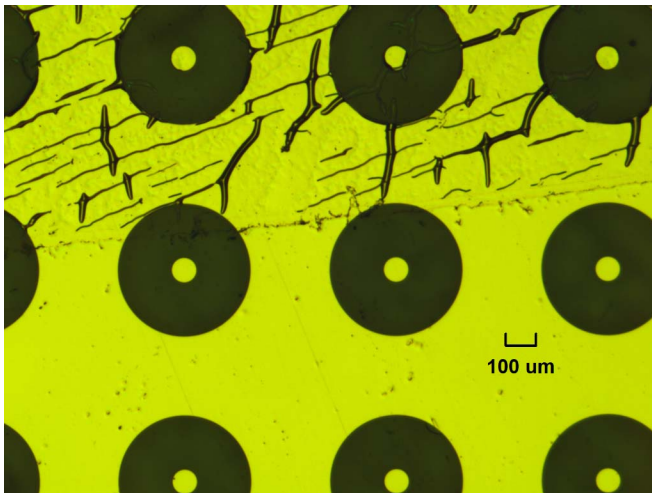

Fig. 2. Photo of the test structures. The test structures at the top are placed on the graphene film, while the structures below are placed directly on the PET substrate. Graphene wrinkles are clearly visible below the large outer metal contact area.

III. EXPERIMENTS

In this section the evaluation of the test structures concerning leakage and capacitance will be evaluated and discussed. The leakage current was measured versus the applied voltage using a Keithley 2604B SourceMeter. During measurements the voltage was increased in steps of 20 – 50 mV with 100 ms delay times. The capacitance of the test structures was measured using a HP 4285A LCR meter and a semiconductor parameter analyzer at 1 MHz (Agilent B1500A).

A. Leakage measurements

Test structures with different diameters of the inner circular electrode were first characterized with respect to leakage current. Because of the large ratio between the area of the outer ground electrode and the area of the inner circular electrode, the resistance R_P between the inner electrode and the graphene film is much larger than resistance R_O between the graphene film and the outer electrode. Therefore, most of the applied dc voltage appears across the dielectric between the inner electrode and the graphene film. As previously reported in [5], leakage currents were found to be less than 1 $\mu A/cm^2$ for most non-defect capacitors in a voltage range from -2 to 2 V. In the voltage range from -5 to 5V the leakage current density was found to be less than 100 $\mu A/cm^2$ - a level considered negligible compared to drain and photo currents typical for terahertz detectors based on GFETs [6].

Furthermore, a pronounced hysteresis effect was observed in some samples except for low voltages where the leakage current is determined by thermal noise. The hysteresis effect is clearly visible in the graph shown in Fig. 3 where experimental data from [5] has been replotted on a semi-logarithmic scale. GFET hysteresis effects are well known, and are generally believed to be due to the charging and discharging of dielectric interface states [7-10].

Another observation based on the experimental data in Fig. 3 is the exponential dependence of the leakage current on the applied voltage. The most probable mechanisms controlling the nonlinear dc current through the dielectric film are Schottky emission, Poole-Frenkel emission, and space-charge limited currents (SCLC) - all showing a linear dependence on a semi-logarithmic scale as discussed in [11]. In this case we believe that Poole-Frenkel emission will dominate due to charge hopping between oxygen vacancies in the dielectric.
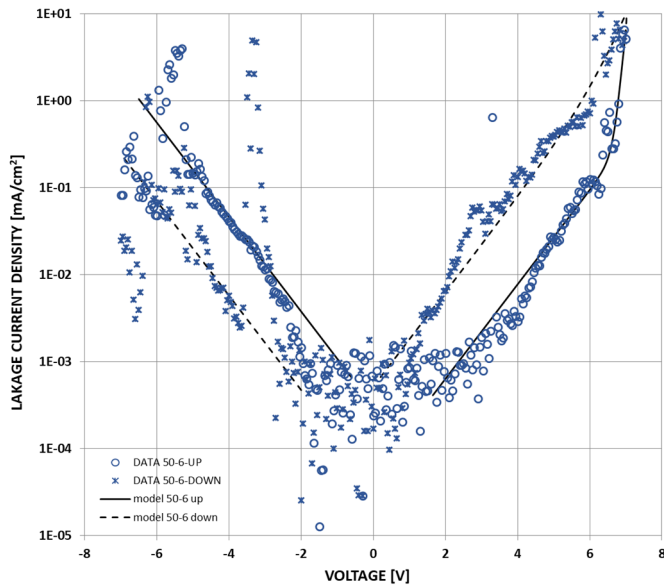
Fig. 3.   Leakage current density vs. voltage for sample 50-6 with a top electrode diameter of 50 μm. Experimental data (symbols) and exponential models (lines). Characteristics obtained for increasing voltages are shown with circles (model: solid lines), while those obtained for the downwards voltage sweep are shown with crosses (model: dashed lines). Data replotted from [5].

However, not all samples exhibited such hysteresis effects while sweeping the voltage upwards and downwards as shown in Fig. 4. Here two samples, 30-5 and 30-6 with inner electrode diameters of 30 μm, show similar I/V characteristics without hysteresis. This is also true for sample 50-5 with a diameter of 50 μm. This sample shows very low leakage, less than 100 μA/cm², for voltages up to 7 V. Measurements were then repeated with different sweep rates. Some results from
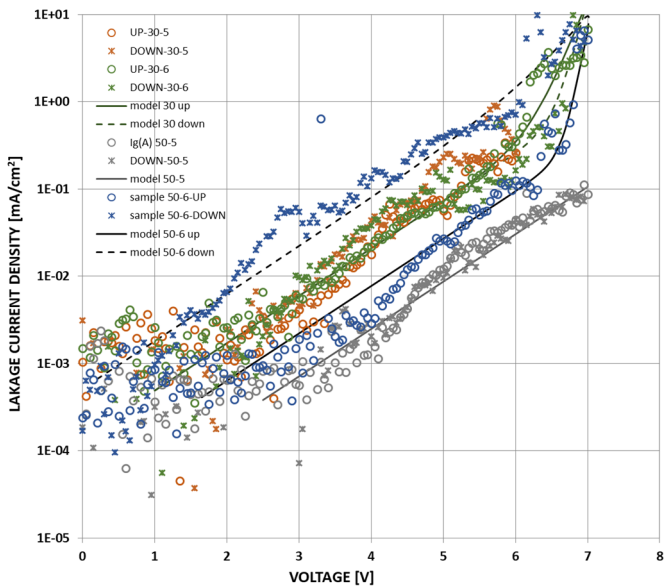

Fig. 4.   Leakage current density vs. voltage. Experimental data (symbols) and exponential models (lines). While a considerable hysteresis effect is observed for sample 50-6, no hysteresis is observed for the two samples 30-5 and 30-6 with a diameter of 30 μm, or for sample 50-5 with a diameter of 50 μm.
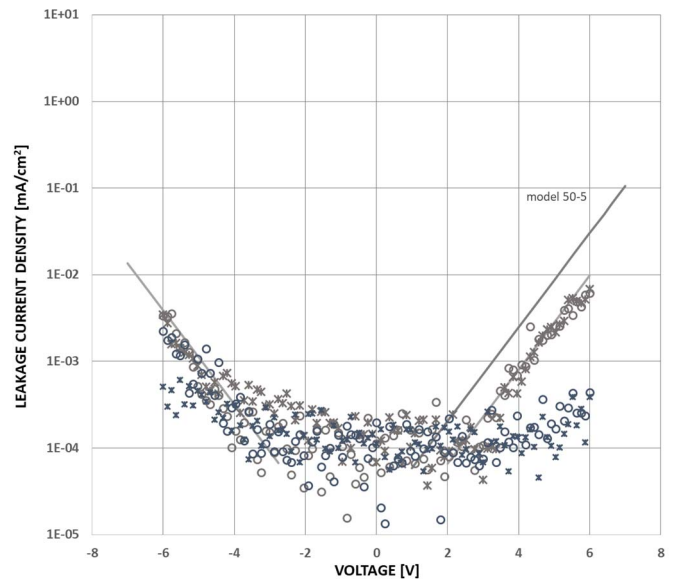

Fig. 5.   Leakage current density vs. voltage. Experimental data (symbols) and exponential models (lines).

measurements with two different sweep rates are shown above in Fig. 5 for a sample with a top electrode with a diameter of 30 μm. The initial measurements done with a delay time of 100 ms showed the same type of leakage currents exponentially dependent on the voltage as already discussed. No hysteresis effects were observed. However, by increasing the delay time to 1 s, the leakage current was reduced about one order of magnitude for positive voltages around 6 V, while not much difference was observed for negative voltages.

B. Capacitance measurements

Capacitance measurements were first performed at zero bias for determining the relative permittivity of the dielectric. These measurements were done at 1 MHz on test structures with three different diameters (30, 40 and 50 μm) using an HP 4285A LCR meter. An average capacitance per unit area of slightly less than 200 nF/cm² was obtained, indicating a relative permittivity of 7.6 assuming an insulator thickness of 35 nm. This value is slightly below the value for bulk Al_2O_3 which is typically 9 [12].

A set of capacitance versus voltage (CV) measurements was then performed on test structures with a top electrode diameter of 30 μm using an Agilent B1500A semiconductor parameter analyzer. As shown in Fig. 6, the applied bias was swept forward from -6 V to 6 V and backwards from 6 V to -6 V with four different sweep rates (delay times) to track the hysteresis effects. The CV curves obtained for the four different forward sweep rates coincide with each other within ±0.5% as indicated by the error bars. This means that the Dirac point stays almost constant independent of the sweep rate, indicating that there is no accumulation of holes in the charge traps. However, for the four backward sweeps a significant hysteresis effect was observed, and the slower the sweep rate, the larger the hysteresis. This means that injected charges shift the Dirac point to values that are more negative.
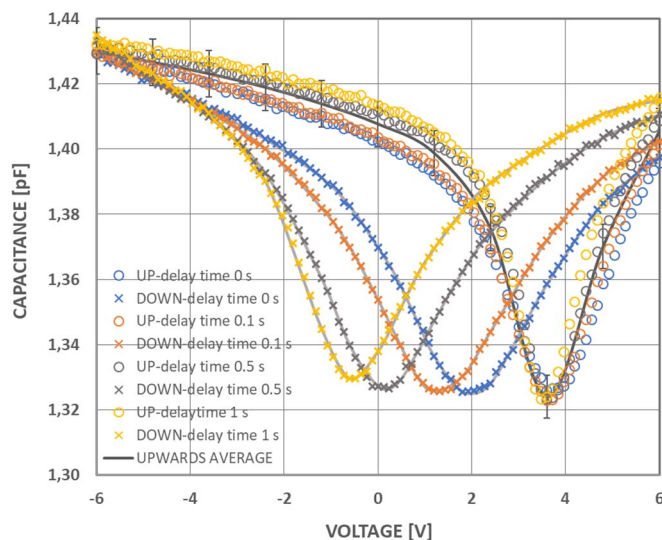
Fig. 6. Capacitance vs. voltage for four different voltage sweep rates. A voltage step of 0.12 V was used during measurements at 1 MHz.

C. Measurements of dielectric losses

The carrier mobility in graphene FETs has previously been shown to be strongly correlated to the loss tangent of the dielectric; the smaller the loss tangent, the larger the charge carrier mobility [13]. Therefore, the factors determining the losses of the test structure was investigated. Measurements of the total loss tangent are shown in Fig. 7 together with theoretically calculated series and parallel loss tangents using the equivalent electrical circuit model from Fig. 1. In the model, a capacitance per unit area of 200 nF/cm^2 was used. An area dependent series resistance on the order of 1000 Ω was estimated from measurements forcing the probes in direct contact with the graphene as described in [5] for structures 30 µm in diameter. While the loss tangents of both the parallel resistance R_P and the PET substrate were found negligible, the loss tangent of the series resistance was found to dominate. The differences between experimental data and losses derived from the circuit model are due to dielectric losses caused by defects in the Al$_2$O$_3$ dielectric. Obviously, there is room for improvement of the dielectric. For comparison, the loss tangent of bulk alumina is as low as 10^{-5} [14].

IV. Conclusions

A test structure, originally proposed and evaluated for investigating dielectric properties of capacitors on solid-state substrates, has been shown to be useful for evaluating the properties of the dielectric of GFETs on flexible polymer substrates. The test structure has topside contacts only, and its fabrication does not require any patterning of the dielectric. Low level leakage was observed for most non-defect samples at low voltages. As the voltage was increased beyond ±2 V, currents exponentially dependent on the applied voltage were observed and believed to be due to Poole-Frenkel emission. Confusing hysteresis effects were observed during leakage current and capacitance measurements in some samples under test - probably due to the charging and discharging of interface traps located at the many interfaces of the test structure.
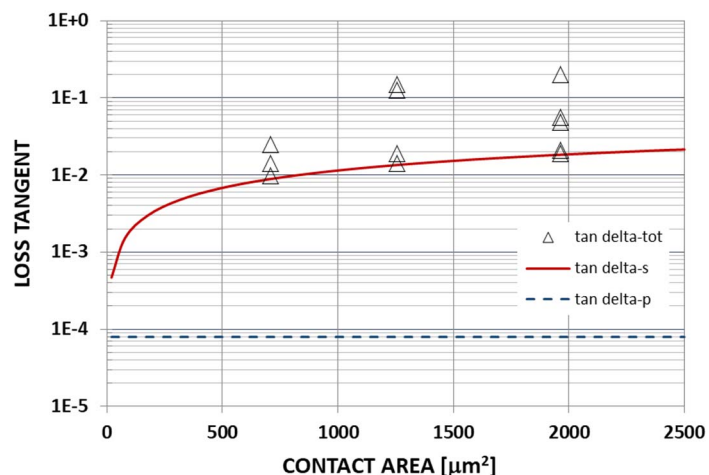

Fig. 7. The measured total loss tangent (symbols) together with the calculated series dissipation factor (solid line) and parallel loss tangents (dashed line) derived from the equivalent circuit in Fig. 1 vs. circular contact area.

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