

THESIS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

Cross-Correlator Implementations Enabling Aperture Synthesis for Geostationary-Based Remote Sensing

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for Geostationary-Based Remote Sensing**

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A 64-channel cross-correlator unit, including chip photos of digital correlator and analog-to-digital converter.

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ABSTRACT

An ever-increasing demand for weather prediction and high climate modelling accuracy drives the need for better atmospheric data collection. These demands include better spatial and temporal coverage of mainly humidity and temperature distributions in the atmosphere. A new type of remote sensing satellite technology is emerging, originating in the field of radio astronomy where telescope aperture upscaling could not keep up with the increasing demand for higher resolution. Aperture synthesis imaging takes an array of receivers and emulates apertures extending way beyond what is possible with any single antenna. In the field of Earth remote sensing, the same idea could be used to construct satellites observing in the microwave region at a high resolution with foldable antenna arrays. If placed in a geostationary orbit, these could produce images with high temporal resolution, however, such altitudes make the resolution requirement and, hence, signal processing very demanding. The relentless development in miniaturization of integrated circuits has in recent years made the concept of high resolution aperture synthesis imaging aboard a satellite platform viable.

The work presented in this thesis addresses the challenge of performing the vital signal processing required aboard an aperture synthesis imager; namely the cross-correlation. A number of factors make the application challenging; the very restrictive power budgets of satellites, the immense amount of signal processing required for larger arrays, and the environmental aspects of in-space operation. The design, fabrication and evaluation of two cross-correlator application-specific integrated circuits (ASICs), one analog-to-digital converter (ADC) ASIC and one complete cross-correlator back-end is presented. Design concepts such as clocking schemes, data routing and reconfigurable accuracy for the cross-correlators and offset compensation and interfacing of the ADCs are explained. The underlying reasons for design choices as well as ASIC design and testing methodologies are described. The ASICs are put into their proper context as part of an interferometer system, and some different cross-correlator back-end architectures are explored.

The result from this work is a very power-efficient, high-performance way of constructing cross-correlators which clearly demonstrates the viability of space-borne microwave imaging interferometer back-ends.

Keywords: Cross-correlation, synthetic aperture, interferometric imaging, remote sensing, signal processing, full-custom, ASIC.

Preface

Parts of the contributions presented in this thesis have previously been published at conferences or in journals. References to the papers will be made using the roman numerals associated with the papers.

- I **Erik Ryman**, Stefan Back Andersson, Johan Riesbeck, Slavko Dejanovic, Anders Emrich and Per Larsson-Edefors, “A SiGe 8-Channel Comparator for Application in a Synthetic Aperture Radiometer,” in *IEEE International Symposium on Circuits and Systems (ISCAS)*, Beijing, China, May 19-23, 2013
- II **Erik Ryman**, Anders Emrich, Stefan Back Andersson, Lars Svensson and Per Larsson-Edefors, “1.6 GHz Low-Power Cross-Correlator System Enabling Geostationary Earth Orbit Aperture Synthesis,” in *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 49, no. 11, pp. 2720-2729, November 2014
- III **Erik Ryman**, Anders Emrich, Lars Svensson and Per Larsson-Edefors, “A 3-GHz Reconfigurable 2/3-Level 96/48-Channel Cross-Correlator for Synthetic Aperture Radiometry,” in *43rd IEEE European Solid State Circuits Conference (ESSCIRC)*, Leuven, Belgium, September 11-14, 2017

Other publications by the author, not included in this thesis, are listed below.

- ▷ **Erik Ryman**, Anders Emrich, Johan Embretsén, Johan Riesbeck, Stefan Back Andersson, Per Larsson-Edefors and Lars Svensson, “Digital Cross-Correlators: Two Approaches,” in *GigaHertz Symposium*, Lund, Sweden, March 9-10, 2010
- ▷ **Erik Ryman**, Per Larsson-Edefors, Lars Svensson, Anders Emrich and Stefan Back Andersson, “A Single-chip 64 Input Low Power High Speed Cross-Correlator for Space Application,” in *Microwave Technologies and Techniques Workshop (MTTW)*, Noordwijk, The Netherlands, May 10-12, 2010
- ▷ **Erik Ryman**, Anders Emrich, Stefan Back Andersson, Johan Riesbeck, Lars Svensson and Per Larsson-Edefors, “3.6-GHz 0.2-mW/ch/GHz 65-nm Cross-Correlator for Synthetic Aperture Radiometry,” in *IEEE Custom Integrated*

Circuits Conference (CICC), San Jose, California, USA, September 18-21, 2011

- ▷ **Erik Ryman**, Anders Emrich, Stefan Back Andersson, Johan Riesbeck and Per Larsson-Edefors, “Application of an Eight-Channel Comparator in a Cross-Correlator for Synthetic Aperture Radiometry,” in *International Workshop on Analogue and Mixed-Signal Integrated Circuits for Space Applications (AM-ICSA)*, Noordwijk, The Netherlands, August 26-28, 2012
- ▷ **Erik Ryman**, Anders Emrich, Stefan Back Andersson, Johan Riesbeck and Per Larsson-Edefors, “Development of a Cross-Correlator System for Space-Borne Earth Observation Interferometric Imaging,” in *International Symposium on Space Terahertz Technology (ISSTT)*, Groningen, The Netherlands, April 10, 2013
- ▷ **Erik Ryman**, Anders Emrich, Alan Tanner and Isaac Ramos, “A Highly Efficient and Compact Cross-Correlator for Synthetic Aperture Radiometry from GEO,” in *13th Specialist Meeting on Microwave Radiometry and Remote Sensing of the Environment (MicroRad)*, Pasadena, California, USA, March 24-27, 2014
- ▷ Anders Emrich, Urban Frisk, Peter Sobis, Arvid Hammar, **Erik Ryman** and Karl-Erik Kempe, “Radiometer instruments for space applications,” in *39th International Conference on Infrared, Millimeter, and Terahertz waves (IRMMW-THz)*, Tucson, Arizona, USA, September 14-19, 2014
- ▷ Anders Emrich, Johan Embretsén, Karl-Erik Kempe, **Erik Ryman** and Peter de Maagt “54 and 183 GHz Interferometer in Geosynchronous Orbit,” in *5th Workshop on Advanced RF Sensors and Remote Sensing Instruments (ARSI)*, Noordwijk, The Netherlands, September 12-14, 2017

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Acronyms

ADC analog-to-digital converter

ASIC application-specific integrated circuit

BGA ball grid array

BiCMOS Bipolar+CMOS

BJT bipolar junction transistor

CAD computer aided design

CML current-mode logic

CMOS complementary metal-oxide-semiconductor

DAC digital-to-analog converter

DICE dual interlocked storage cell

ENEPIG electroless nickel electroless palladium immersion gold

FC flip-chip

FE front-end

FOV field of view

FPGA field-programmable gate array

GEO geostationary Earth orbit

HDL hardware description language

IF intermediate frequency

IO input/output

LEO low Earth orbit

LET linear energy transfer

LO local oscillator

MOSFET metal-oxide-semiconductor field-effect transistor

PCB printed circuit board

QFN quad-flat no-leads

RF radio frequency

RMS root mean square

SEE single-event effect

SEL single-event latchup

SEU single-event upset

SNR signal-to-noise ratio

TID total ionizing dose

VLBI very long baseline interferometry

e-VLBI electronic VLBI

V_{th} threshold voltage

Part I

INTRODUCTION

Chapter 1

Introduction

Climate and weather concerns have become increasingly relevant in recent years, especially as climate change has risen to the top of current environmental concerns. Increasing demands on weather forecasts and climatology drive the need for better models providing better predictions in the short term and a more thorough understanding of the behavior of our atmosphere in the long term. Together with the advancement of climate models, the requirement for more precise and better temporal and spatial coverage of measurements is rising.

Atmospheric measurements have traditionally been largely done from ground-based weather stations. With the introduction of remote sensing of atmospheric data from satellites in orbit, a much wider coverage has been achieved. Atmospheric observations from satellites are performed in the visible spectrum as well as in infrared and radio wavelengths. One advantage of performing observations in the radio part of the electromagnetic spectrum is the possibility to penetrate cloud formations, otherwise obstructing the visibility from orbit.

Absorption and emission of radiation is a continuously ongoing process in the atmosphere. Molecules from different gasses within the atmosphere all have different spectral properties since atoms and molecules can only exist in certain levels of energy, or states, specific to each substance. This means that the absorption and emission occur only at energies related to the difference in energy between these states. Each energy level translates to a specific frequency of radiation, and each substance, hence, has a very specific set of frequencies (or spectral lines) where light is absorbed or emitted. Observations of these lines do not only give information about the concentrations of different substances making up the atmosphere, but can also give information on atmospheric properties such as temperature and pressure.

A number of spectral lines have been identified, by the EUMETSAT in 2001, as especially interesting [1]. Observations of the 50-60-GHz lines and the 118-GHz

line of atmospheric O_2 can be studied to measure temperature of the atmosphere. The 183-GHz H_2O line gives information on humidity [2], while the 380-GHz H_2O line can be used for observation of humidity at high altitude [3].

A number of satellites are performing observation from low Earth orbit (LEO) today in the 50-60-GHz band and 183-GHz band, with good sensitivity and resolutions in the order of 15-25 km. For highly dynamic weather patterns, however, a time resolution in the order of 4-6 hours for full-coverage images, is not nearly enough. High humidity may very quickly turn into rainfall and an instrument that is able to discern this difference with temporal resolutions in fractions of hours is very desirable. Temporal resolution requirements may differ around the world, mainly due to differing weather patterns. In Europe, an update time in the order of half an hour may suffice while tropical storms forming over the North Atlantic, Pacific Ocean or the Indian Ocean, heavily afflicting coastal regions, may require 5-10 minute update times.

There is an inverse relationship between the required antenna aperture and both the imaging resolution and observed frequency used for radiometry. This means that for the lower frequencies (for example, 54 GHz) and a requirement of about 35-km resolution, an instrument placed in geostationary Earth orbit (GEO) would require a parabolic dish antenna of close to 8 meter aperture. The current generation of launchers cannot accommodate such large payloads. The Ariane 5, currently European Space Agency's (ESA) most powerful rocket, for example, has a diameter of 5.4 meters and can only accommodate payloads with a diameter of up to 4.57 meters [4].

A concept of a new type of weather satellite, borrowing the aperture synthesis technology developed for astronomical radio observatories, has been progressing in recent years. The aperture synthesis approach takes an array of small antennas arranged in a two-dimensional pattern to emulate a single parabolic dish with an aperture equivalent to the longest baseline¹. An array of antennas can be folded during launch which makes this solution viable for deployment in space. The most common design concept is to place receivers on three foldable arms, which are extended after reaching orbit, a concept which was successfully demonstrated with the launch of the Soil Moisture and Ocean Salinity (SMOS) satellite in 2009 [5]. The aperture synthesis approach to remote sensing does, however, require large amounts of signal processing. The immense amount of raw data generated from the array exceed any possible downlink rate by orders of magnitude, which means part of the signal processing and data reduction has to be performed on satellite. In aperture synthesis imaging, complex visibility samples of the UV -plane are taken, where the UV -plane is the Fourier transform of the brightness temperature image. Typically visibility samples are obtained by performing cross-correlation between

¹A baseline in this context is the distance extended by any two antennas in the array.

signal pairs in the array. The cross-correlation function is in principle a multiplication and integration of two signals performed at different time delay steps applied to one of the signals. The integration part of this is the key to the data reduction required. This means that only the cross-correlation has to be performed on the satellite, while remaining signal processing can be performed on ground, where computing resources are considerably less restricted.

1.1 Problem Statement

In a satellite, power generation and dissipation of the heat generated by the electronics are two of the major design concerns. Using as little power as possible is thus of great importance for the cross-correlator systems considered. With decades of ongoing miniaturization of electronics, we have reached a threshold where the quite computationally intensive task of aperture synthesis can be accommodated within the power/heat budget of a satellite. This is, however, only true when considering an application-specific integrated circuit (ASIC) for the task. In contrast, processor-based solutions are not suited to the task of performing massively parallel multiplications with very limited bit-depth (1-2 bits). A field-programmable gate array (FPGA)-based approach would be better than a processor-based solution, but would have difficulties handling the desired bandwidth. In addition, the power dissipation of the FPGA would still be an order of magnitude higher than for the ASIC. Our approach is a full-custom ASIC solution, which will bring us to well within the restrictive power budgets of on-satellite implementation.

1.2 Thesis Outline

This thesis will cover the implementation of two cross-correlator ASIC designs an analog-to-digital converter (ADC) and one complete correlator system. Chapter 2 will delve deeper into the technical aspects of aperture synthesis instruments, ASICs, printed circuit board (PCB) design and radiation environment considerations. Chapter 3 will give an overview of other work in the general field of aperture synthesis interferometry and, specifically, cross-correlators. Chapter 4 will describe the contributions of this work. Part 2 of this thesis contains publications.

Chapter 2

Technical Background

This chapter will explain some of the technical aspects of the work. It will briefly describe the radiometer function and aperture synthesis as well as the work flow of circuit and printed circuit board (PCB) design. It will also describe some aspects of designing electronics for space application, particularly radiation tolerance.

2.1 Radiometry

In the field of remote sensing, the radiometer is, as the name suggests, an instrument for measuring emission in the radio band (frequencies below infrared) of the electromagnetic spectrum. There are a number of different radiometer types. One of the simplest is the total power radiometer which simply detects the time-average power of a band-limited radio frequency (RF) noise signal and converts it to a voltage. In a heterodyne radiometer, a mixer converts a band-pass filtered RF signal down to baseband using a local oscillator (LO) source. The resulting baseband is the difference between the RF and LO frequencies. At baseband, the signal is easier to digitize to perform more detailed signal analysis.

For reasonably short averaging times, known as integration times, the root mean square (RMS) receiver output fluctuation σ_T , follows the ideal radiometer equation:

$$\sigma_T = \frac{T_{SYS}}{\sqrt{\tau B}} \quad (2.1)$$

T_{SYS} is the system temperature, B is signal bandwidth, and τ is integration time. From this the signal-to-noise ratio (SNR) can be calculated:

$$\text{SNR} = \frac{T_{SRC}}{\sigma_T} = \frac{T_{SRC}}{T_{SYS}} \sqrt{\tau B} \quad (2.2)$$

Here, T_{SRC} is the source signal temperature. A long integration time and large bandwidth, thus, is of interest to increase SNR. In reality, however, gain fluctuations, ΔG , from the RF-chain will limit for how long integration times this equation is valid. If we insert this term into the radiometer equation we get a more realistic RMS output fluctuation:

$$\sigma_T = T_{SYS} \sqrt{\frac{1}{\tau B} + \left(\frac{\Delta G}{G}\right)^2} \quad (2.3)$$

Frequent instrument calibration to mitigate this fluctuation may limit the length of any single integration.

Some other system and user-level aspects may also limit the length of integration time; in the aperture synthesis imaging applications, an update rate requirement in the order of minutes would mean that potentially integration times of the same order can be applied. However, most instrument concepts sample only parts of an image at a time, meaning snapshots have to be taken much more frequently.

The other approach to increasing SNR is to process a wider frequency band. There are, however, also limits to how wide the band of interest is. When studying the slope of a spectrum line, for example, one has to be able to resolve a frequency-limited region of the spectrum. Digital back-end processing of a very large bandwidth also comes at a cost in power dissipation.

2.2 Aperture Synthesis

Consider a single pair of antennas, a baseline as shown in Figure 2.1, receiving at a single radio frequency ω . For a distant radio point-source, the emission comes in approximately as a planar wave front. If we consider the amplitude, V , to be the same for both receivers, the difference in detected signal is only that one of them will experience a geometric delay, τ_g , due to the longer path from the source to antenna, for non-zero angles of incidence, θ . Hence, we obtain the two detector voltages V_A and V_B as:

$$V_A = V \cos(\omega t), \quad V_B = V \cos(\omega(t - \tau_g)) \quad (2.4)$$

If we multiply the voltages from the two receivers and average over a long enough time (many waves) we get a function dependent only on angle of incidence and signal amplitude, assuming a fixed frequency:

$$\langle V_A V_B \rangle = \langle V^2 \cos(\omega t) \cos(\omega(t - \tau_g)) \rangle = \frac{V^2}{2} \cos(\omega \tau_g) \quad (2.5)$$

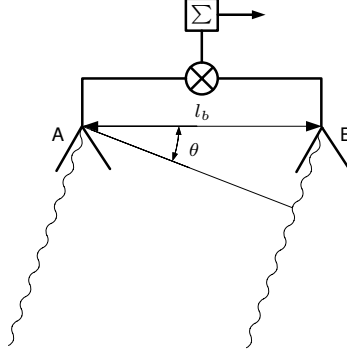


Figure 2.1: An interferometer baseline.

The geometric delay, τ_g , is dependent on both angle of incidence, θ , and baseline length, l_b :

$$\tau_g = \frac{l_b}{c} \sin(\theta) \quad (2.6)$$

Here, c is the speed of light.

The sensitivity of the instrument varies as a cosine of the angle across the field of view (FOV), while the frequency of this cosine is inversely proportional to baseline length. If an extended radio source is observed, the output of our detector is this cosine multiplied in each point by the source's brightness temperature I (and gain) averaged over the entire FOV, Ω :

$$C_C = \int_{\Omega} I \cos(\omega \tau_g) d\Omega \quad (2.7)$$

In effect this could be considered one sample of the spatial frequency spectrum of the source's brightness temperature distribution. By sampling with many different baseline lengths, different parts of this spectrum are sampled. Adding phase information to these samples makes it possible to reconstruct the source brightness temperature distribution, by means of the inverse Fourier transform. If we add a sinusoidal sampling, Eq. 2.8, we obtain the complex visibility, Eq. 2.9, which makes this reconstruction possible. In practice the sinusoidal sampling is attained by adding a phase shift of a quarter of a wavelength to one of the receivers.

$$C_S = \int_{\Omega} I \sin(\omega \tau_g) d\Omega \quad (2.8)$$

$$V_V = C_c - jC_S \quad (2.9)$$

The implementation of the interferometer, shown in Figure 2.2, includes band-pass filtering of the RF signal, amplification stages, down-mixing to intermediate frequency (IF) in both in-phase I and quadrature Q components using an LO source whereafter the IF signal is low-pass filtered and fed to a correlator, which performs the pair-wise multiplication and integration.

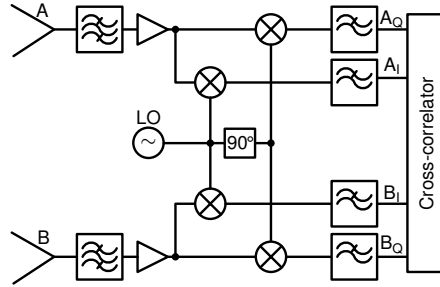


Figure 2.2: Example of an interferometer baseline with in-phase (I) and quadrature phase (Q) mixing of channels A and B.

The smallest baseline, the *unit spacing*, defines the non-ambiguous FOV. To cover the entire visibility plane, all multiples of unit spacings up to the longest baseline have to be sampled. Placing antenna elements on a row with unit distance all the way up to the required maximum baseline length will naturally incur an unnecessary overhead since the unit distance then is repeated $n - 1$ times for n antennas. Antenna placement patterns with minimum redundancy are therefore advisable.

For the remote sensing example, the Earth extends about 17 degrees as seen from geostationary Earth orbit (GEO). The smallest baseline thus has to be in the order of a few millimeters for 183-GHz observations. With an angular resolution requirement of 0.1° , baselines up to 1 meter have to be covered. If a unit spacing of 5 mm is chosen, a minimum of 200 baseline lengths have to be covered. In the ideal case this could be done by about 20 antennas. However, for any number of antennas greater than four, the antenna array will by necessity have either some redundancy or some gaps in the visibility sampling [6]. Minimizing the redundancy while avoiding gaps is a non-trivial problem.

In some cases, there are restrictions to antenna placement. For satellite implementations for example, a foldable structure may be required, limiting the placement options. A 3-armed Y-shaped array has been suggested for many of the missions. Even in cases where the entire array can be fitted in the launch vehicle as is, there may be restrictions caused by structure weight limitations and the need for rotation of the array. A rotating array will add the benefit of sampling additional baseline directions without the need for additional receivers. Since these

instruments operate in an environment where repairs are not feasible, there is also the requirement of enough redundancy for allowing failure of one or more receiver chains, hence additional receivers and cross-correlator channels may be required.

2.3 Cross-Correlation

The multiplication and averaging previously described in Eq. 2.5 is also known as cross-correlation. The cross-correlation of two signals, f and g , is a simple multiplication and integration of two signals with a time shift, τ , applied to one of the signals:

$$(f \star g)(\tau) \stackrel{\text{def}}{=} \int_{-\infty}^{\infty} f^*(t) g(t + \tau) dt \quad (2.10)$$

Here, $f^*(t)$ is the complex conjugate of the signal $f(t)$. In the radiometer the complex signal is formed by the two separate signals from the in-phase (f_I) and quadrature phase (f_Q) mixers such that $f(t) = f_I(t) + j f_Q(t)$:

$$(f \star g)(\tau) = \int_{-\infty}^{\infty} (f_I(t) - j f_Q(t)) (g_I(t + \tau) + j g_Q(t + \tau)) dt \quad (2.11)$$

which after multiplication can be split into separate integrations:

$$\begin{aligned} (f \star g)(\tau) = & \int_{-\infty}^{\infty} f_I(t) g_I(t + \tau) dt - j \int_{-\infty}^{\infty} f_Q(t) g_I(t + \tau) dt \\ & + j \int_{-\infty}^{\infty} f_I(t) g_Q(t + \tau) dt - j^2 \int_{-\infty}^{\infty} f_Q(t) g_Q(t + \tau) dt \end{aligned} \quad (2.12)$$

This is actually the combination of four real-valued cross-correlation products which may be calculated separately:

$$f \star g = f_I \star g_I + f_Q \star g_Q + j(f_I \star g_Q - f_Q \star g_I) \quad (2.13)$$

2.3.1 Digital Implementation Considerations

When implementing the cross-correlation function as a digital signal processing unit, we have to perform quantization and sampling. The corresponding digital cross-correlation operates on digitized signals:

$$(f \star g)[n] \stackrel{\text{def}}{=} \sum_{m=-\infty}^{\infty} f^*[m] g[m + n] \quad (2.14)$$

Table 2.1: SNR degradation [7]

	Nyquist	2×Nyquist	3×Nyquist	$\lim_{f_s \rightarrow \infty}$
2-level	1.57	1.35	1.29	1.25
3-level	1.23	1.13	1.10	1.08
4-level	1.13	1.07	1.06	1.03

The time shift is divided into discrete lags, n . For interferometers used in remote sensing, the integration time has to be limited and usually only the 0:th lag ($n = 0$) is used, hence the cross-correlation here can be simplified further:

$$(f \star g) = \sum_{m=0}^M f^*[m] g[m] \quad (2.15)$$

Digitizing the cross-correlation infers quantization and sampling errors which degrade SNR. A degradation factor, D , can be defined as [7]:

$$D = \frac{\text{SNR}_{\text{analog}}}{\text{SNR}_{\text{digitized}}} \quad (2.16)$$

The degradation depends on quantization levels and sample rate. As shown in Table 2.1 the decrease in degradation from increasing quantization levels or sampling frequency, f_s , quickly levels off, and approaches 1 as both numbers are increased.

A system-level trade-off analysis between quantization levels, sample rate, system complexity and power dissipation has to be made. For analog-to-digital converters (ADCs), power dissipation will scale fairly linearly with number of sampling levels, assuming one extra comparator is added for each added level. On the cross-correlator side the trade-off between sampling levels and power dissipation becomes a bit more complex and will depend on architecture. However, with a simple assumption of linear scaling for sample rate and sampling levels with power dissipation, it becomes clear that with a restrictive power budget, going beyond four quantization levels or 2× oversampling will not be beneficial.

For N signals there are $N \cdot (N - 1)/2$ possible pairs. For a complex cross-correlator, in principle only the $f_I \star g_I, f_I \star g_Q, f_Q \star g_I$ and $f_Q \star g_Q$ products are required; however, the additional $f_I \star f_Q$ and $g_I \star g_Q$ products are still important when performing compensation for IQ-mixer phase imbalances. Since cross-correlation products then have to be calculated for all pair-wise I and Q signals, there is no need to distinguish between I and Q channels from a cross-correlator hardware perspective. The same cross-correlator unit, thus, may operate as an N -channel real valued correlator or as an $N/2$ -channel complex correlator as needed without any hardware changes.

The integrating part of the cross-correlation means that data compression is achieved. Consider a single correlation product operating at a sample rate of 1 Gs/s with 1-bit sampling. If an integration time of only one second is used, the data rate will be reduced from 1 Gb/s to $\log_2(10^9) = 30$ b/s, a compression factor of $\sim 3 \cdot 10^7$. For an array of only 48 antennas, the raw data rate would reach 96 Gb/s in continuous operation with I/Q sampling. Considering realistic downlink data rates may reach just 1 Gb/s [8], and that pushing downlink rate further will be very costly in power dissipation, it is clear that at least the cross-correlation part of the signal processing involved in aperture synthesis has to be performed on the satellite.

2.3.2 Correlator System Configurations

For many of the instruments considered, the channel count of one individual cross-correlator application-specific integrated circuit (ASIC) may not be enough for the full cross-correlation unit. Larger correlators can however be assembled from smaller units. One way to do this is to split the analog signals and connect these to additional cross-correlator units. Figure 2.3a shows an example where 144 signals are connected to three 96-channel units. Another approach, only available with separate ADCs, is to split signals after digitization, as shown in Figure 2.3b. Advantages of splitting on the digital side include reduced signal power requirement from the front-end (FE), reduced power dissipation for analog to digital conversion since it only is performed once for each channel, and that identical samples are used for each channel throughout the correlator system. This approach will however require additional digital signal splitters and may increase routing complexity.

For both of these approaches, efficiency will be lower than for a one-to-one mapping of input channels to cross-correlator ASIC channels. Besides the cost of extra splitters, two cross-correlators will calculate the same products for all signal pairs within each 48-channel bus, which is a redundant operation.

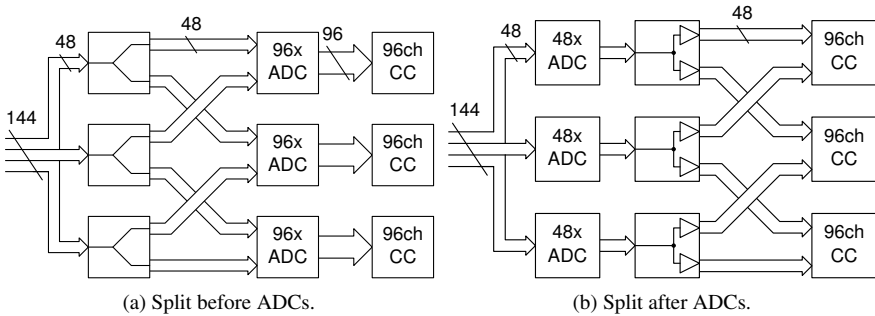


Figure 2.3: Configuration options for a 144-input correlator system.

The number of cross-correlator ASICs required follows the same $N \cdot (N - 1)/2$ pattern as the number of two input cross-correlators inside the ASIC. The only difference is that here $N = \lceil N_{tot}/(N_{ASIC}/2) \rceil$, where N_{ASIC} is the input channel count of the ASIC and N_{tot} is the total number of channels to be correlated. The number of ASICs required is shown in Figure 2.4. Note that the number of channels is double the number of receivers due to the IQ-mixers.

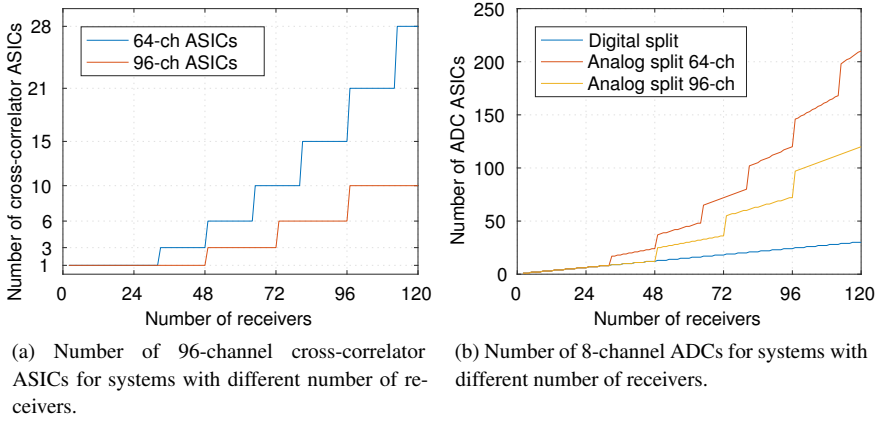


Figure 2.4: Resource requirements for larger correlator systems.

Adding extra frequency bands can be done by simply adding an extra cross-correlator system for each required band. Alternatively if resources are limited, cross-correlator systems can be run in time-division mode, switching between imaging of different bands. The latter approach will, however, degrade imaging sensitivity or update time of the instrument.

2.4 CMOS and Bipolar Circuits

The silicon complementary metal-oxide-semiconductor (CMOS) integrated circuit has, since its invention in 1963 [9], revolutionized the field of computing. With its relatively simple structure it has been continually scaled down at a relentless pace, resulting in an ever-increasing number of transistors available per unit area of silicon. Today transistors have feature sizes in the order of a few nanometers.

The metal-oxide-semiconductor field-effect transistor (MOSFET) consists of bulk silicon with three interleaved regions of either P- or N-type doping. Either P-channel (PMOS) or N-channel MOSFETs (NMOS) can be formed on the same silicon substrate by changing doping order. The combining of PMOS and NMOS on the same die forms the complementary function of the CMOS circuit. While a

PMOS transistor will turn on when a negative source-gate voltage is applied, the NMOS will turn on with a positive voltage. On top of the middle region, an oxide layer acts as a thin isolation between the gate, and the underlying channel, forming a capacitive coupling attracting charge carriers when the gate potential is raised (NMOS). At a high enough voltage, corresponding to the threshold voltage, the transistor is considered to be in its on-state and charges can flow from the source to the drain, the two surrounding regions, assuming that a voltage is also applied across these. From these two basic kinds of transistors all sorts of logic operations are implemented in today's electronics. Variations in drive strength, threshold voltage, leakage current, etc. can be achieved by different doping concentrations, oxide thicknesses, and gate dimensions, and today it is common for ASIC-manufacturers to supply a range of transistor options for the designer to choose from. In addition to the as-designed transistor varieties, there is a natural, unwanted, variation in transistor properties caused by inaccuracy in manufacturing. These variations lead to across-circuit differences in propagation speed which have to be accounted for by including timing margins during design and by performing simulations of the different transistor variations, or corners.

The bipolar junction transistor (BJT) was developed in 1947 [10], and the technology of integrating them into circuits was first developed during the 1950s. Much like the MOSFET's source, drain and gate, the BJT has three terminals, emitter, collector and base, with similar functions. The BJT differs from the MOSFET in that it does not have an insulation for the base terminal, rather a current flows through this terminal and the current amplification factor β determines the current flowing between emitter and collector. BJTs come in two versions, NPN and PNP. In an NPN transistor, a current flowing from the base to the emitter allows an amplified current from collector to emitter to flow. The PNP reverses these current directions.

Since BJTs need current to flow constantly for their on-state, they are usually not used for complex digital circuits, but are more common in analog designs.

Some fabrication processes allow adding MOSFETs on the same silicon die as BJTs. These are known as Bipolar+CMOS (BiCMOS).

2.5 The Full-Custom ASIC Design Flow

Designing full-custom digital ASICs is a higher-risk and a more labor-intensive endeavor than the more common approach of synthesizing hardware description language (HDL) designs using standard-cell libraries. In the full-custom work flow, it is up to the designer to perform timing, functional, and power analysis by circuit simulation rather than let the tools perform these analyses automatically. This increases the risk of failure to meet requirements. Some of the advantages of full-custom can include smaller chip area, better performance and lower power dissipa-

tion when done carefully. In spite of the risks involved, some cases exist where the full-custom approach is advantageous. The correlator, mainly thanks to the very repetitive layout, is just such an application.

In a typical full-custom design flow, after desired behavior of the circuit is decided, the circuit schematic phase is initiated. Schematics are drawn in a computer aided design (CAD) software, building cells from transistor-level hierarchically up to full ASIC-level. Circuit simulation of cells is performed simultaneously to verify functionality. For large designs, circuit simulations of higher hierarchical levels can quickly become insurmountable, but this depends on different factors such as available computing power and the size of the circuit. For every cell to be simulated, test benches are created, emulating the environment in which the cell is to operate. To account for variability between devices in fabrication, simulations are performed in different corner cases, varying transistor properties throughout the schematic.

The layout phase of the ASIC design includes drawing the physical representation of the circuit in silicon and metal layers. Computer tools are used to aid in comparing the physical design with the schematic to verify component types, scaling and connectivity. During this phase, parasitics (wire resistances, capacitances and in some case inductances) are extracted from the layout to allow for more accurate simulations. Again, to account for fabrication variability, parasitic extraction is performed in different corner cases and co-simulated with the corner cases for the components. Compliance to a large number of design rules is checked by automated tools to verify the manufacturability of the circuit throughout the entire layout phase. Naturally, these two phases of ASIC design are not entirely separated, but results from the parasitic extracted netlist simulations will feed back to update requirements of the schematic components, usually by modifying drive strength and adding buffers.

2.6 PCB Work Flow

The work flow for creating PCBs is similar to the full-custom ASIC design flow in the sense that it consists mainly of a schematic phase and a layout phase. For the cross-correlator application which is heavy in signal count, routability of the PCB should be considered already at ASIC design stage. For example, placing pads in a configuration so as not to complicate the PCB design may be important. For high-speed PCB layouts, such as the test boards and correlator board presented in Chapter 4, special considerations have to be taken for the critical high-speed (frequency of a few GHz) traces. Path-length matching, impedance matching, and bend radius limitations have been applied for high-speed traces. In addition to this, dielectric material selection has to be considered as the commonly used FR-4 materials may not be suitable for high frequencies. Finally, surface finish of the

PCB has to be considered, for PCBs where wire bonding of naked dies is considered (such as many of the boards presented in this work). Electroless nickel electroless palladium immersion gold (ENEPIG) may be used for good bond-wire adhesion. If only packaged ASICs are to be used, low-cost alternatives may suffice.

2.7 Considerations for Hardware in Space

Not shielded by the Earth's atmosphere and magnetic field, higher levels of radiation are to be expected operating in a space environment. In fact, for GEO, the radiation levels are even higher than in interplanetary space, because of charged particles being trapped in regions by the Earth's magnetic field, as discovered in 1958 by Pioneer 3 and Explorer IV [11], now named the Van Allen radiation belts. GEO is located within the outer radiation belt where mainly high energy electrons are captured. In addition to electrons, other high and low energy particles are common, such as protons, neutrons and heavy ions.

When designing ASICs for the space environment, special considerations have to be taken into account. Such considerations include how critical the component is for the system, what error modes are acceptable, and how costly radiation hardening¹ is going to be. For mission-critical circuits such as mission control computers, hardening may be vital and even so, spares may have to be designed into the system. In the field of signal processors for scientific data acquisition, tolerance for soft errors (non destructive errors) may be more relaxed. While circuit failure is unacceptable, some single-event effects (SEEs) may be tolerated. To mitigate the risk of experiencing SEEs, radiation-tolerant process technologies can be used; the design can also be made tolerant by means of circuit design techniques. In addition, shielding will reduce the amount of radiation experienced. Usually electronic circuits are encapsulated in aluminum and the satellite structure itself will also act as a radiation shield.

Radiation testing is common practice for ASICs that are to be used in space. Mainly two different kinds of tests are performed depending on the circuit application. A total ionizing dose (TID) test is done to verify that the circuit can handle a certain amount of radiation during its expected operating life, without failure or severe degradation. Here, the ASIC in question can be subjected to radiation from a radioactive material; most commonly, a CO-60 source is used. Dose rate can easily be varied by distance between test object and radiation source. The TID tolerance of any circuit varies with design, manufacturing, operating environment etc. and can be very hard to predict without actual testing.

For finding out the soft error rate when in operation, much higher particle ener-

¹ Radiation hardening involves circuit design and fabrication techniques for minimizing the risk of faults caused by ionizing radiation.

gies are required than what is available from a CO-60 source, to correctly test for what the circuit will experience in the space environment. SEE tests are performed, usually at a particle acceleration facility, where particle beams are accelerated to very high speeds before bombarding the ASIC. A host of different particles are used in a number of inclination angles and speeds to test for different linear energy transfer (LET) levels. LET is the amount of energy deposited in the circuit per unit distance traveled and it varies throughout the traversal of the material as the particle slows down. A higher LET translates to a higher probability of an error occurring. To reduce testing time, much higher dose rates per cross-section area of the beam, called fluence, than what is experienced during the mission is used. Data on error rate of the circuit along with the corresponding fluence, circuit measurements and LET levels are used in special software to calculate expected error rate for the particular orbit and shielding of the envisioned mission.

Since SEEs will likely occur, it is important to handle these. For the cross-correlator application, where the majority of the ASIC area consists of integrators, the most common error will be a change of the value of one of these integration counters. Errors occurring in bits of lower significance will be difficult to detect but will luckily not severely affect the final imaging results. Errors in more significant bits will be easier to detect and data can be discarded assuming these errors occur infrequently enough that it does not severely degrade the instrument performance. SEEs can also occur in the input data and clock routing parts of the ASIC. In this case, a single event could affect many correlation products, which may seem severe, however, only a single count of the integrators would be erroneous and thus it would give very little impact on final results. The most severe SEE would be one occurring in control or readout logic with the potential of destroying an entire data set (all correlation products). However, considering that most instrument concepts employ phase switch, array rotation or frequent calibrations, a single integration will usually be in the order of up to a few seconds. Thus, even discarding one data set is not that severe of an operation.

Another risk of CMOS in a radiation environment is the occurrence of a single-event latchup (SEL). A SEL happens when parasitic NPN and PNP transistors, in the CMOS structure, go into a forward biased mode, keeping each other in saturation. This means a low impedance path between power and ground is formed, which is kept until power is cycled or the circuit is destroyed. These events are usually handled by external monitoring of supply current. In recent times, however, the supply voltage scaling has made modern CMOS processes inherently SEL-immune. A minimum voltage is required for the parasitic transistors to hold their forward-biased mode, and in many CMOS-processes the standard core supply voltage is lower than this latchup-holding voltage [12, 13].

In addition to radiation tests, other stress tests are often performed. These include temperature cycling, and vacuum, vibration, and shock tests.

Chapter 3

Related Work

This chapter will present the history of interferometry and aperture synthesis within the field of radio astronomy from the earliest work up till the currently ongoing developments. It will also describe the first applications of these techniques in the field of remote sensing and present the ongoing initiatives where the work presented in this thesis would be relevant.

3.1 Aperture Synthesis for Radio Astronomy

Astronomical observation using interferometers was first developed for optical instruments such as the Michelson stellar interferometer, which was used to perform the first measurements of the diameters of large astronomical bodies, among others Betelgeuse in 1920 [14]. It was later determined that the same principles could be used for radio astronomy; and development of interferometers for radio astronomy began at the Cavendish Laboratory in Cambridge and simultaneously at the Division of Radiophysics, Commonwealth Scientific and Industrial Research Organisation (CSIRO) in Sydney. Two-dimensional measurement of radio brightness of the sun was performed in Cambridge at 1.4-m wavelengths as early as 1953 [15] followed by observations at 21 cm in 1955 [16]. The same year observations at 60 cm were reported from Sydney [17]. Additional arrays were built in Cambridge; a radio-star array in 1957 [18] and the One-Mile Telescope in 1962 [19] both consisted of a fixed part and a movable part mounted on railway tracks, covering additional baselines by successively moving along the track as new measurements were taken. Signals for these arrays were digitally recorded on punched paper tapes and computations were performed by the Electronic Delay Storage Automatic Calculator (EDSAC). Today, there are numerous observatories and networks of observatories employing aperture synthesis for increasing angular resolution of radio

astronomical observations giving us images of the universe in the radio spectrum with an unprecedented sharpness. In the following, a few important examples will be reviewed:

One of the early large radio observatories still in operation applying aperture synthesis is the Very Large Array (VLA), completed in 1980 in New Mexico [20]. The observatory consists of 27 telescopes, each with an aperture of 25 meters. The telescopes are arranged in reconfigurable Y-shaped pattern, where each arm is extending up to 21 km. The reconfigurability is achieved by the telescopes being mounted on railway tracks. The original correlator system for the VLA consisted of 39,500 ASICs. VLA applies 3-level quantization and a sample rate of 100 MS/s for an analog bandwidth of 50 MHz. Up to 16 spectral channels could be resolved over the full bandwidth and up to 251 channels for lower bandwidths, requiring a total of 11,232 complex cross-correlators.

The correlator, along with other electronics, for the VLA underwent major updates in the Expanded VLA (EVLA) program completed in 2012 [21]. The EVLA correlator can perform cross-correlation of 496 baselines, for support of up to 32 antennas. Bandwidth of up to 16 GHz per antenna is available with 16,384 spectral channels, expandable up to four million channels if bandwidth is reduced.

Even radio observatories not initially intended for this application are sometimes linked together to perform very long baseline interferometry (VLBI) measurements. This practice has been used for extending the aperture to sizes close to the Earth diameter since 1976 [22]. At this time, observations were done by four telescopes with bandwidth of 2 MHz recorded on video tapes for processing at U. S. National Radio Astronomy Observatory (NRAO). Today, uses for these networks include not only astronomy but also tracking spacecrafts and geodesy [23].

Due to the very long distances between telescopes and the very high data rates, VLBI has traditionally been performed by recording the individual telescope's data streams at their respective location whereafter data have been transported to a central processing facility. In recent years the ever-increasing demand for data bandwidth over intercontinental interconnections has enabled the emergence of real-time VLBI with direct data streaming, known as electronic VLBI (e-VLBI), a technique now implemented in the European VLBI Network (EVN) [24].

Another initiative, the LOw Frequency ARray (LOFAR) uses local small antenna clusters distributed across Europe centered on the Netherlands where the highest density of clusters, the central hub, is placed [25]. The LOFAR array uses two types of antennas for an operating frequency range covering 10-250 MHz. The maximum baseline extends to roughly 180 km. In spite of the rather modest bandwidth of up to 96 MHz, the amount of data being processed is still immense due to the number of receivers. Instead of traditional telescopes, LOFAR uses an array of simple antennas at each station to perform beam-forming, that is, it will steer the pointing direction not by physically moving one large antenna, but rather by using

the local cluster as a phased array. The signal processing for this array phasing is performed locally at each cluster using field-programmable gate arrays (FPGAs). The combined signal is then transferred to a central processing facility located in the Netherlands.

Aside from the direct scientific results generated, LOFAR is also an important pathfinder to an even more ambitious project for radio astronomy, the Square Kilometre Array (SKA). SKA is an ongoing initiative of building the world's most sensitive radio observatory in South Africa and Australia with a combined collecting area of one square kilometer. The first phase, SKA1, of the 2-phase construction will constitute about 10% of the final observatory. SKA1 will consist of two arrays; one with 133 15-m mid-frequency antennas (SKA1-mid) placed in South Africa, and one with ~131,000 log-periodic low-frequency antennas forming 512 clusters (SKA1-low) in Australia [26]. The SKA1-mid correlator will have a combined input data bandwidth of ~57 Tb/s performing ~10 peta-operations per second. For the SKA1-low, beamforming will be applied within each cluster (much like LOFAR) to reduce the amount of data required at the central correlator. The SKA1-low correlator will handle correlations between clusters at a combined input data bandwidth of ~10 Tb/s performing ~1 peta-operations per second.

3.2 Microwave Remote Sensing

For Earth remote sensing, requirements naturally differ significantly compared to ground-based radio astronomy observatories. Size and power constraints are orders of magnitude more challenging for on-satellite application, however, for measurements of temperature and water vapor concentrations, requirements on sensitivity and spectral and angular resolution are significantly less demanding. The field of remote sensing by aperture synthesis is relatively new and only a few instruments have so far been assembled. The early generation of instruments are all operating within the 1400-1427 MHz band for a few reasons: this range is protected for radio astronomy and Earth observation usages, it did strike a good balance between required ground resolution and available receiver technology for the time, and finally it can be used for detection of mainly soil moisture and sea surface salinity. As receiver technology has evolved, higher frequencies have in later years become feasible for other observations and for achieving higher resolution for the same array size.

3.2.1 ESTAR and 2D-STAR, Airborne Aperture Synthesis

The Electronically Scanning Thinned-Array Radiometer (ESTAR) was the first instrument using aperture synthesis for remote sensing applications. The ESTAR

was built by Goddard Space Flight Center and the University of Massachusetts at Amherst in 1989 to function as a demonstrator of aperture synthesis for remote sensing while measuring soil moisture and, later, ocean salinity using the 1400 to 1427-MHz band. As an airborne instrument the ESTAR achieved high resolution images using a hybrid approach employing aperture synthesis in the across-flight-path dimension and by real aperture scanning while travelling along the flight path [27]. The ESTAR's five antennas were stick antennas oriented in a direction parallel to the flight path. The original ESTAR correlator performed completely analog complex cross-correlation on all ten baselines from the five antennas with a power dissipation of around 100 W [28]. The instrument down-mixed each RF signal to two IF signals at slightly different intermediate frequencies. The correlators combined the higher IF from one FE with the lower IF of another and used a square-law detector diode on the combined signal. This signal was then I/Q-demodulated and low-pass filtered to give the final analog complex visibility. The correlator was later rebuilt, updating the mechanical mounting of the components to a PCB and swapping out a diode, but was otherwise identical [29].

In 2002 the ESTAR was superseded by the construction of another airborne radiometer, the 2D-STAR [30]. In 2D-STAR aperture synthesis is performed in two dimensions as opposed to the hybrid approach used by ESTAR. The 2D-STAR instrument performed soil-moisture measurements by observations of a 24-MHz wide band centered around 1.413 GHz. Patch antennas were used instead of dipoles, placed in a square array of 11 by 11 patches spaced at 0.5 wavelengths. This design also allowed for using both horizontal and vertical polarization as opposed to the single polarization of ESTAR. From the array of antennas only 21 were populated with receivers in a cross, "+", pattern with 11 antennas in each arm. The full antenna array was constructed as to make tests of other configurations possible. The correlator was also upgraded to a digital, FPGA-based version, performing 8-bit I and IQ products and averaging over 10 samples, each measurement taken over a duration of 10 ms.

3.2.2 HydroSTAR and SMOS, First Employment in Space

Following the successful results from the ESTAR, a similar instrument for deployment in low Earth orbit (LEO) was proposed, the HYDROSTAR [31]. The HYDROSTAR would have had 16 rectangular stick antennas placed along the orbit trajectory. The antenna array proposed would be folded during launch and in the fully extended state would span 9.5 by 5.8 meters. The HYDROSTAR never got funded and another satellite, the Soil Moisture and Ocean Salinity (SMOS), claimed the title of carrying the first aperture-synthesis instrument in orbit.

The Microwave Imaging Radiometer with Aperture Synthesis (MIRAS), carried as the sole instrument on board the SMOS satellite, was launched on Novem-

ber 2, 2009 [5]. SMOS was funded by European Space Agency (ESA), and is still in operation. It has proved very successful, retrieving long-term data sets of ocean surface salinity and soil moisture which are of high interest for improving climate models and weather forecasts [32]. Resolution on the Earth surface is 50 km and a complete sweep of the Earth is done every 3 days with the satellite orbiting in LEO. SMOS has also been demonstrated to possess capabilities not initially intended such as measuring hurricane wind speeds and sea ice thicknesses up to 50 cm [33, 34]. The array consists of 72 receivers, also operating in the 1400 to 1427-MHz range, mounted on three triple-hinged arms deployed after launch into a Y-shape. Fully extended the array reaches a diameter of 8 m. Cross-correlation is performed by the MIRAS Correlator and Control Unit (MIRAS-CCU), consisting of nine ASICs implemented in a radiation hardened 0.35- μ m CMOS process [35]. The MIRAS-CCU performs complex 1-bit cross-correlations between all 72 receiver pairs. Operating at a clock frequency of 55.84 MHz it has a power dissipation of 34 W.

3.2.3 GeoSTAR, GAS and GIMS, Aperture Synthesis in GEO

Microwave imaging from GEO is a highly desired goal for achieving imaging update times in the order of minutes, which is not possible with a single instrument placed in LEO. When considering microwave imaging from GEO, the angular resolution of the instrument becomes even more critical to achieving adequate on-ground resolution, which further motivates the use of aperture synthesis. There are still no aperture synthesis microwave imagers in GEO, but a few initiatives aim to change this.

One of the ongoing initiatives is the Geostationary Synthetic Thinned Aperture Radiometer (GeoSTAR) which is being developed by NASA's Jet Propulsion Laboratory (JPL) [36]. GeoSTAR would perform temperature and humidity sounding using 4-6 channels around 50 GHz and 4-5 channels around 183 GHz respectively. Receiver elements would be placed in a foldable Y-shaped array extending out to baselines of up to 4 meters. Reaching a spatial resolution of 45 km for full hemisphere coverage from GEO would require up to 300 receiver elements for the 50-GHz band.

GeoSTAR has undergone three prototyping rounds, GeoSTAR-I through III. The GeoSTAR-I demonstrator, constructed in 2005, was a 24-element 50-60-GHz interferometer [37]. The correlator used was implemented using FPGAs, but was based on earlier correlator ASIC development for the Global Precipitation Measurement interferometer initiative [38]. 8-bit ADCs and the FPGA-based correlator were chosen based on availability and low cost rather than efficiency [39].

The GeoSTAR-II demonstrator, built in 2011, used 48 receiver elements operating from 165 to 183 GHz with a bandwidth of up to 500 MHz [40]. The antennas

were organized into three sub-arrays with 16 antennas each. The correlator for GeoSTAR-II was implemented using custom 90-nm ASICs performing 2-bit cross-correlation between 19×19 inputs with a power dissipation of $250 \mu\text{W}/\text{correlation}$ at 500 MHz bandwidth. An ADC was also designed in the same 90-nm CMOS process dissipating 30 mW while sampling at 750 MS/s.

The GeoSTAR-III demonstrator, presented in 2016 as an extended version of GeoSTAR-II, uses a new correlator back-end and comprises 9 sub-arrays for a total of 144 receivers [41]. A correlator ASIC, developed at the University of Michigan, performs 2-bit correlations between two sets of 64 inputs for a total of 4096 correlation products, or 6,144T multiplications per cycle at 1.5 GHz [42]. To reduce interconnect power dissipation and system complexity, the correlator also performs on-chip AD-conversion. Power dissipation of the chip is reported to be 3.735 W, equivalent to $0.61 \text{ pJ}/\text{correlation}/\text{cycle}$ when operating at 1.5 GHz. This is reduced to 1.443 W or $0.35 \text{ pJ}/\text{correlation}/\text{cycle}$ when operating at the minimum targeted frequency of 1 GHz. The chip is fabricated in a 65-nm CMOS process and measures 18 mm^2 with a digital correlator core of 6 mm^2 . The correlator subsystem for GeoSTAR-III uses three correlator PCBs covering all inter-arm products.

The Geostationary Atmospheric Sounder (GAS) is an ESA-funded initiative developed by RUAG Space and Omnisys Instruments [43]. The envisioned instrument would use an array of elements placed in a Y-shaped array on foldable booms just like SMOS and GeoSTAR and would perform observations in four different bands simultaneously, 53, 118, 183 and 380 GHz for measuring atmospheric temperature and humidity distributions. To reach a desired on-ground resolution when observing from GEO of 30 km for the 53-GHz band, the array would span baselines exceeding 1200 wavelengths, corresponding to 6.8 m. 136 elements would be used for the 53-GHz band and 107 elements each for the 118, 183 and 380-GHz bands. The GAS array would be rotating, sampling baselines in different directions without a need for additional antenna elements, trading off image update rate for a reduced total element count and lower system complexity.

A prototype for the 53 GHz band was demonstrated in 2009 [44]. The demonstrator implemented a rotating array of 21 elements with baselines of up to 75 cm, which would be equivalent to a 300-km resolution as seen from GEO. The cross-correlator unit for the demonstrator was capable of sampling 48 signals (24 FEs I and Q) at 220 MHz and 3-level quantization. The digital correlator core was based on a Xilinx Virtex-5 FPGA and performed cross-correlation between all inputs with a 7-lag depth.

The Geostationary Interferometric Microwave Sounder (GIMS) is an initiative by National Space Science Center (NSSC) within Chinese Academy of Sciences (CAS) of constructing a radiometer for remote sensing of atmospheric temperature profiles from GEO [45, 46]. The instrument will perform observation of the oxygen band in the 50-56 GHz range at 6-8 different bands. A spatial resolution of 50 km

for a full hemisphere coverage, 0.6 K radiometric sensitivity and a 5 minute update time are targeted. The instrument will carry 70 receivers on a rotating circular array with a diameter of at least 2.8 m. A first demonstrator was developed and tested in the 2009-2012 time frame [46, 47]. The demonstrator was equipped with a circular, rotating, array with a diameter of 2.8 m carrying 28 antennas including one in the array center. The instrument was operating between 50 and 56 GHz with a bandwidth of around 300 MHz. Angular resolution of 0.08° corresponding to 50 km resolution from GEO, a FOV of 5° corresponding to 3000×3000 km from GEO, and a sensitivity of 1K were achieved with a 5 minute integration time.

A second demonstrator (GIMS-II) was reported in 2017 [48]. One of the main goals was to increase the FOV to accommodate the full hemisphere as seen from GEO. The number of receivers was increased to 70 in an array of ≥ 3.6 m diameter. The FEs have a bandwidth of 160 MHz operating within a range of 50-56 GHz. The digitization for GIMS-II is performed by 14 10-channel ADCs sampling at 500 MS/s with 3-level quantization. An FPGA-based correlator performs pair-wise cross-correlation on the 140 signals (70 receivers with I and Q sampling).

The work presented in this thesis is not aimed at radio-astronomy applications, but it is particularly relevant for the future implementation of aperture-synthesis based radiometers placed in GEO.

3.3 Synthetic Aperture in Security Screening

In addition to the usages of cross-correlators in radio astronomy and remote sensing, mm-wave security screening is emerging as a new field where aperture synthesis can be used. Performance targets for these applications is in many ways similar to those of the remote sensing application. In one such system reported in [49], an FPGA-based 32-channel complex cross-correlator developed at Omnisys Instruments is used. When performing these scans, the interferometer operates in near-field and even 3D-imaging can be performed by adopting a 3D Fourier transform on the cross-correlation products [50]. The cross-correlator performs 2-level sampling of 300 MHz band at a power dissipation of 130 W [51].

Another security scanning initiative is being presented in [52]. Here, an 8 lane parallel cross-correlator is being developed. Working at a core clock of 250 MHz, a sample rate of 2 Gs/s for each channel channel is handled. The cross-correlator performs correlation of 64 channels (32 I and 32 Q) at an estimated power dissipation of 7.5 W, not including ADCs.

3.4 Preceding ASIC Development

Parts of the work presented in this thesis builds on earlier experience at Omnisys Instruments, mainly on autocorrelator ASICs used for spectrometry. A range of autocorrelators has been developed at Omnisys Instruments with the latest, fifth generation, being the Highly Integrated Full-custom Autocorrelation Spectrometer (HIFAS) [53]. HIFAS is still being integrated in new instruments such as the Sub-millimetre Wave Instrument (SWI) on the JUpiter ICy moons Explorer (JUICE) mission [54], while earlier autocorrelators have been used in, among others, the Odin satellite launched in 2001 [55].

While autocorrelation is by definition only a cross-correlation of a signal with itself, the usages and hence implementations may differ significantly. Since previous autocorrelators are targeted for spectrometry, spectral resolution has been the main driver for these ASIC architectures, while the cross-correlators presented here targets imaging resolution. This means the autocorrelator implements a large number of lags while the cross-correlator implements a large number of input channels.

On an architecture level, this means a more straightforward approach to signal routing can be implemented in the autocorrelator, with lags placed along a signal bus. The cross-correlator, however, may not be as well suited for this strategy and the implementations presented in this thesis uses a cross-coupling network. However, similarities still exist, a row-wise synchronous architecture with data and clock flowing together through the chip is used in the cross-correlator, inherited from HIFAS. Also, pipeline stages for data synchronization are used in a similar fashion in both architectures. While the architectures differ on clock and data distribution level, at a lower level there are naturally similarities. The autocorrelator lags are basically multiply-and-accumulate blocks which is also true for the cross-correlator products.

Chapter 4

This Work

The work presented in this thesis includes two digital cross-correlator ASICs and one ADC ASIC. Paper I describes the ADC. Paper II describes a complete correlator unit integrating eight of these ADCs together with a 64-channel digital cross-correlator ASIC on one PCB. Finally, Paper III describes an updated cross-correlator ASIC that has an improved readout speed and power efficiency as well as an option for configuring the correlator as either a 96-channel 2-level correlator or as a 48-channel 3-level correlator. This chapter will expand on the underlying work and results of Papers I-III.

4.1 Cross-Correlator ASICs

One of the major concerns going into this project was the data routing, making pair-wise connections between all inputs to each 2-input cross-correlator cell, and to keep these inputs synchronous throughout the ASIC. The topology that solves these issues, used and presented in Papers II and III, is basically the same for both.

The readout scheme presented in Paper III proved to be very area efficient even though data buffering was implemented. The main reason behind this is that the storage of previous integrator data could be done in very simple latches, shown in Figure 4.1a, while still working as a shift register during readout. The shifting is done one row at a time through an 8-bit wide bus with one controller for each block of eight bits handling the special clocking required, shown in Figure 4.1b. An enable bit is propagated through the row to control when the shifting starts for each 8-bit block.

One experience gained from the radiation tests done for the 64-channel correlator, presented in Paper II, was that while radiation tolerance was at an acceptable level, the most gain would be made from radiation hardening of the readout logic

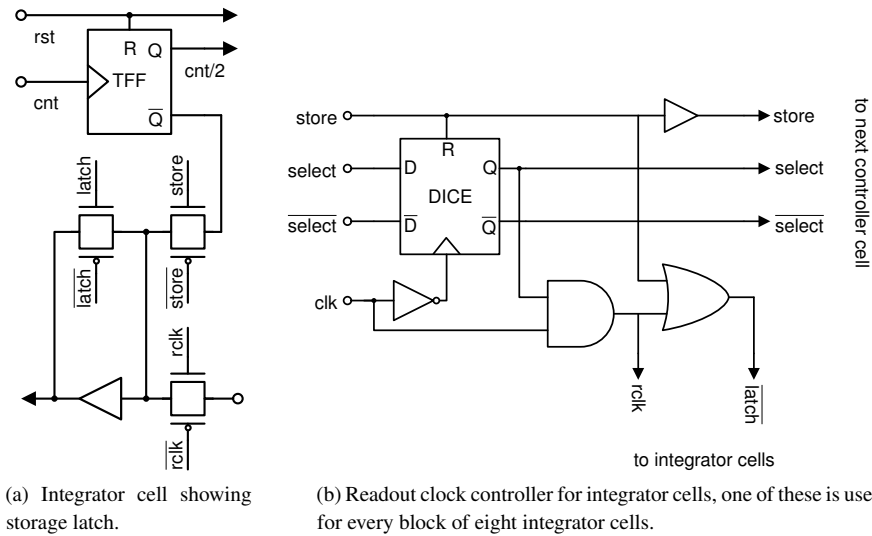


Figure 4.1: Integration readout schematics for the 96-channel cross-correlator presented in Paper III.

since any error occurring here would invalidate a complete frame of data. Additionally, radiation hardening of the readout logic would come at a relatively low cost since it constitutes a minor part of the chip area and operates at relatively low speed. Readout control counters, for controlling loading a new word into the serializer and controlling when to shift row, are implemented using clocked dual interlocked storage cells (DICE latches), [56]. The DICE latch, shown Figure 4.2a, will retain its value even with a single-event upset (SEU) occurring in any one of its internal nodes. Since the ASIC is implemented in 65-nm CMOS, different net nodes may have small enough separation that there is a considerable risk of a single ion causing upsets on several nodes simultaneously. With this in mind, separation of sensitive node-pairs of the DICE latches significantly reduces the risk of an upset [57]. Such separation is employed for the DICE latches in the cross-correlator.

For controlling the readout logic's enable bit propagation, shown in Figure 4.1b, only a high bit needs to be propagated. The latch is reset low before next readout simultaneously with the storage of data into the storage latch. This means buffering of the data inputs of the DICE latch, as shown in Figure 4.2a, can be avoided and a smaller version can be implemented by simply using different transistor types—high threshold voltage (V_{th}), low power or low V_{th} , general purpose transistors—giving a weaker or stronger drive, as shown in Figure 4.2b. The stronger drive NMOS transistors can easily overpower the weaker PMOS resulting in a new state being written into the latch.

For future radiation tests, in addition to readout logic, one entire column of correlator cells was also implemented using DICE latches for the integration counters. This would be useful for finding out the level of radiation tolerance introduced by using DICE compared to the ordinary latches, which is an important piece of information for cost vs benefit analysis of radiation hardening for future cross-correlator designs.

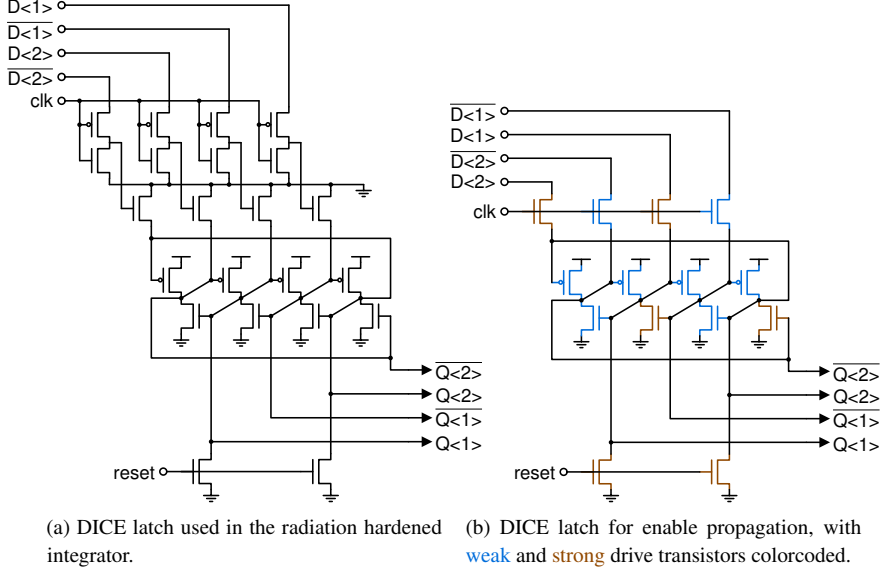
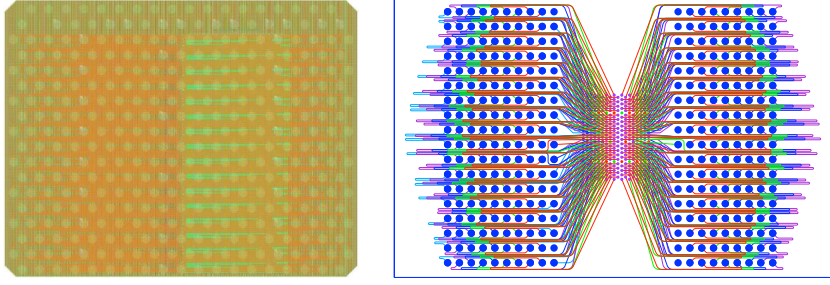


Figure 4.2: Two versions of the DICE-latches used.

A 128-channel cross-correlator design in 40-nm CMOS was also designed, see Figure 4.3a. This design featured fully differential inputs, requiring a total of 312 input/output (IO) signal pads, for a total of 348 pads including supply. The design featured flip-chip (FC) technology to achieve this number of IOs. Still, with a minimum pad pitch requirement of $150\mu\text{m}$, the 1.9-mm^2 active logic area makes up only a fourth of the 7-mm^2 total chip area. An 8-layer silicon ball grid array (BGA) substrate was developed for the packaging, see Figure 4.3b, featuring length-matched data paths to minimize input skew. Neither the chip nor the substrate were fabricated; however, many of the design ideas, such as the buffered readout and the use of DICE latches, were introduced in the 128-channel cross-correlator design.

A statistical analysis, mentioned in Paper II, was performed to verify the routing topology's ability to handle clock synchronization throughout the chip [58]. The analysis was based on circuit simulation results of a single path from one buffer block to the next, performed a few hundred times with statistical, randomized circuit corners to find the timing variation of the path. Added to this is the min and



(a) Cross-correlator layout, the FC pads can be discerned as octagons distributed across the surface. (b) FC BGA substrate design, the smaller FC pads can be seen in the center and the length-matched paths are seen sticking out to the sides.

Figure 4.3: The 40-nm 128-channel cross-correlator.

max corner spread from RC-extraction of metal wires. With all results of the circuit simulations reduced to a single number, the timing variation, a MATLAB model of the entire routing structure can be constructed. This model makes it easy to simulate thousands of ASICs, a feat not possible with circuit-level simulation. Full circuit simulation of even a single chip cannot be done within reasonable time. The same analysis was also performed for the 96-channel correlator presented in Paper III. Simulation results of 100,000 chips for each design are presented in Figure 4.4. As shown, the 96-channel correlator has lower worst-case skew even though it is a larger design in terms of number of nodes. A big part in this improvement is the considerably denser design, which is a result of experiences gained between the works presented in Papers II and III.

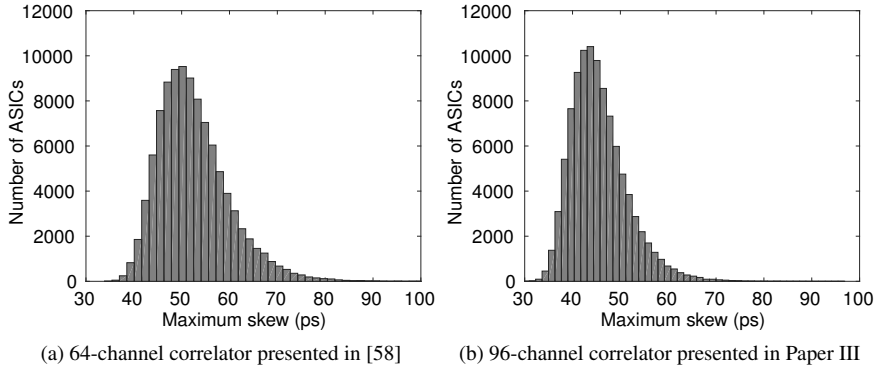


Figure 4.4: Statistical simulation results.

The statistical model also makes it possible to predict performance of other designs when increasing the number of input channels. A simulation of channel counts from 64 up to 256 was also performed, Figure 4.5. Note that, according to circuit simulations, for a performance target of 3 GHz a skew of at least 120 ps can be tolerated before on-chip synchronizers start failing.

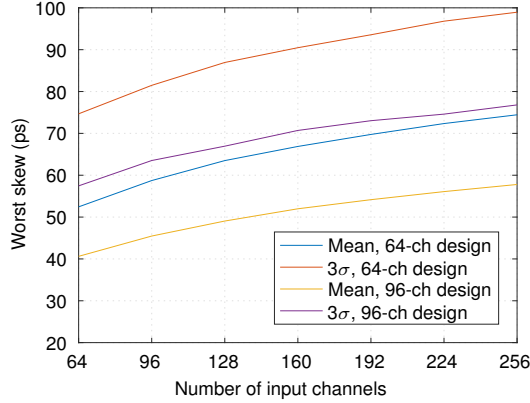


Figure 4.5: Statistical skew analysis of extended correlator designs.

For both cross-correlators ASICs, custom test bench PCBs were developed, see Figure 4.6. This enabled tests to be PC-controlled with automated handling of parameter sweeps, data recording and monitoring. Both boards were connected to PC through an additional commercially available controller for handling of commands over USB. The 64-channel test bench used an Arduino board [59] for this task while the 96-channel test bench was connected through a Pipistrello FPGA-board [60]. Using an FPGA as controller gave the advantage of cycle-accurate integration timing and the Pipistrello also gave the option of using a relatively high-speed serial interface for readout of correlation data through the available HDMI-connector. Special care was taken to make a good signal path for the high-speed input signals and clocks. This includes impedance matching, using high-speed dielectric materials, avoiding solder-mask on high-speed paths as well as avoiding sharp bends on these paths.

Packaging of the cross-correlators becomes important when operating at up to a few GHz, when aspects such as cross-talk or signal degradation come into play. For the 64-channel correlator two packaging versions were produced, one mounted in a standard quad-flat no-leads (QFN) package and one custom-made substrate. The substrate shown in Figure 4.7a featured patterned termination resistors along the edge as signal termination was not included in the 64-channel ASIC. In addition to this, decoupling was included on the substrate, which was manufactured in an aluminum nitride material with bondable gold coating. The substrate was mounted

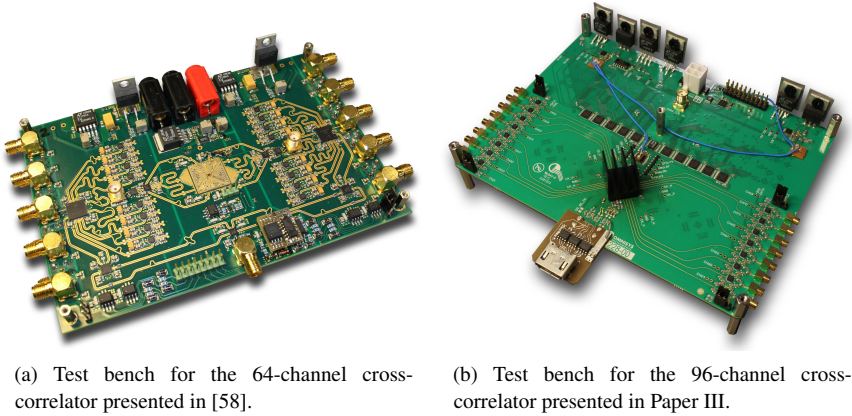


Figure 4.6: Test bench PCBs for cross-correlator ASICs

on the test board and connected by wire bonding. An additional version of the test board for the QFN package was also made, showing similar performance.

For the 96-channel cross-correlator the number of IOs had increased significantly, hence a BGA-package was found to be a more suitable match. Going for BGA meant a custom-made substrate had to be designed, shown in Figure 4.7b. The package design was handled by a contractor who performed electromagnetic, thermal, thermomechanical and mold flow simulations to verify the package. Length match was not done internally on the substrate, but for exact timing the length matching instead has to be performed on PCB.

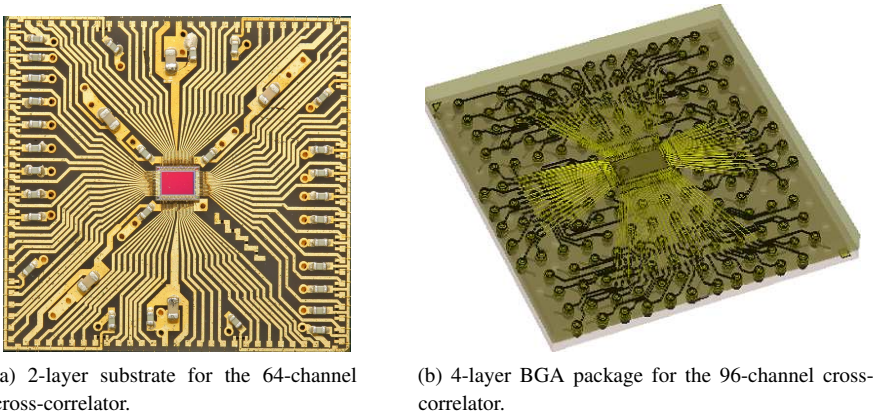


Figure 4.7: Packaging of cross-correlators.

A study into making a synthesized 96-channel cross-correlator as a comparison to the full-custom approach shows that, in simulations, the synthesized version, achieves about half the top speed and moderately higher power dissipation than measured results from the full-custom ASIC. This is due to the usage of a clock tree and input registers for handling clocking and synchronization instead of the much more costly clock and data routing approach in the full-custom ASIC. The delay spread in the synthesized version is handled by the tools, optimizing all timing paths for handling setup and hold times for best and worst case corners. Where the real advantage of this full-custom approach lies is in logic density, here a factor of three lower logic area was achieved with full-custom as compared to the synthesized version. The higher density may prove important for future upscaling of the correlator as more receivers are required for achieving desired resolution from GEO. With a denser layout, speed penalties of upscaling will likely also be lower.

4.2 Sampler ASIC

The 8-channel ADC presented in Paper I was designed specifically for the cross-correlator, where inputs are divided into banks of eight. Features include clock return path, per channel offset calibration and current-mode logic (CML) outputs.

For tests of the ADC two versions of a simple carrier board were designed, one for mounting a naked die, wirebonded directly to the PCB, shown in Figure 6.7, and one for a QFN package. No significant differences were detected between the two and the full test campaign was done only for the naked die version. Additionally, two boards, shown in Figure 4.8, were designed for handling programmable supply voltages, signal levels and common-mode input levels. All tests of the ADC were performed in a temperature-controlled chamber, as temperature variations can have an impact on internal offsets. This also made it possible to measure the temperature-dependent offset drift as reported in Paper II.

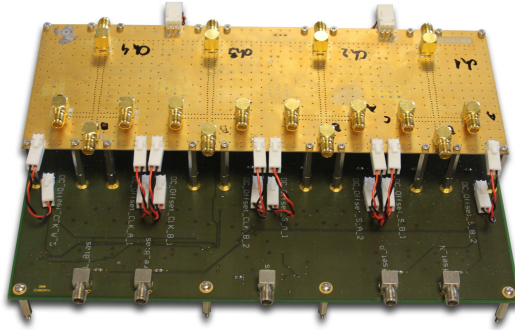


Figure 4.8: The ADC bias (bottom) and IF (top) test boards.

4.3 Assembling a Cross-Correlator System

While the assembled correlator unit in Paper II was limited in bandwidth by mainly the choice of input transformers and a clock splitter, due to the relatively low sample rate requirements for the GeoSTAR proposal work for which it was originally constructed, the correlator and ADCs ASICs both support significantly higher bandwidth. The motivation behind the relatively high bandwidth is the increased sensitivity that can be achieved both from taking in a wider IF band and from performing oversampling. Running at higher sampling speed does however come at a cost in terms of power dissipation.

In the work performed for the GeoSTAR proposal, temperature cycling tests in a vacuum environment were performed on the cross-correlator board. The PCB was mounted on a temperature-controlled metal plate inside a vacuum chamber. Cross-correlation measurements were performed continually for a subset of 10 of the 64 input channels while cycling plate temperatures between -13°C and 90°C , which translated to about a 50°C span measured on the active components (ADCs and cross-correlator), as shown in Figure 4.9. The test was designed both to verify stability and to stress the unit. Two uncorrelated noise sources were used, one distributed to eight inputs and the other to two inputs, both at a power level of -20 dBm at the correlator port. Calibration of the cross-correlator was performed only before cycling started. Correlation values varied with temperature, mainly for the same-source inputs with the most variable correlation product reaching 0.7 percentage points, while different-source correlation stayed below 0.08 % as shown in Figure 4.10. In total the correlator was subjected to 17 complete temperature cycles without any noticeable degradation. Electronics, such as the cross-correlator, which does not have to be mounted on the outside of the satellite, would in a real mission be kept within a much narrower temperature span, controlled by the satellite platform. This reduces the stresses and minimizes the need for frequent calibration.

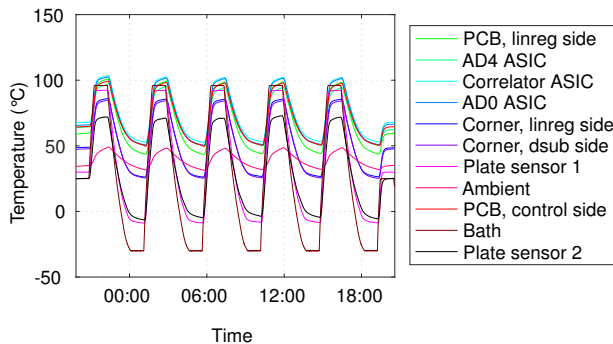


Figure 4.9: Temperature measured at different locations during thermal cycling.

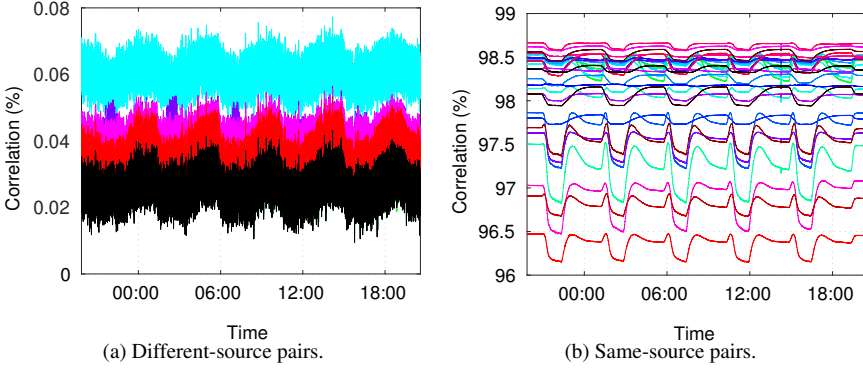


Figure 4.10: Correlation values from thermal cycling test of the 64-channel cross-correlator unit.

Power budgets of satellites are strict, not only due to available power but maybe even more so due to the issue of heat management. With the power dissipation figures presented for the ADC in Paper I and the cross-correlator in Paper III, system-level power dissipation can be estimated. Power dissipation estimation for 96-channel cross-correlator systems employing 2-, 3- and 4-level quantization, as discussed in Section 2.3.1, operating at 1.5, 2.5 and 3 GHz, is illustrated in Figure 4.11. Figures for cross-correlator ASIC, ADC and CML-interface power dissipation are distinguished.

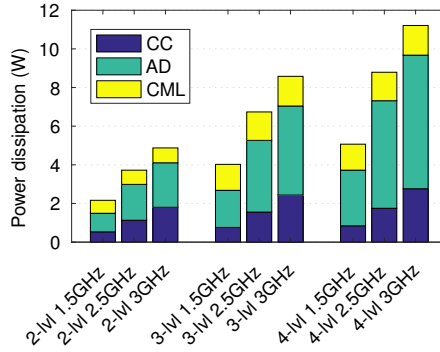


Figure 4.11: 96-channel cross-correlator system power dissipation.

We can see that with the current ASICs, the analog to digital conversion makes up the major part of the power dissipation. It should be noted that the CML numbers for 2.5 and 3 GHz are based on linear interpolation between LP and HP corners operating at 1.5 and 4.5 GHz (as described in Paper I). Figures for additional quan-

tization levels are estimated based on architecture assumptions combined with the partial power figures resolved for clocking, data path and multipliers+counters as described in Paper III.

Power dissipation estimation can also be done for the expanded, 144-channel systems suggested in Section 2.3.2. Four cases based on the 96-channel cross-correlator ASIC are examined; running at 1.5 or 3 GHz for both the system with analog splitters and when splitting the digital signal after ADCs. Power dissipation for splitting the digital signals and clock distribution is taken into account using the power dissipation figures from the CML drivers used in the ADCs. An estimation of power dissipation for the added analog amplification required to retain signal levels when doing analog splitting is also included, even though close to negligible in comparison.

The results in Figure 4.12 clearly show the advantage in terms of system power that can be gained from distributing the signals digitally, at least when using the current ADCs. With the already relatively conservative choice of 65-nm CMOS process together with the 130-nm BiCMOS process for ADCs the total power dissipation of a complete correlator system is well within manageable limits. With a choice of even more advanced fabrication processes the power figure can be reduced even further, which could prove vital for instruments adding extra frequency bands through usage of parallel cross-correlator systems.

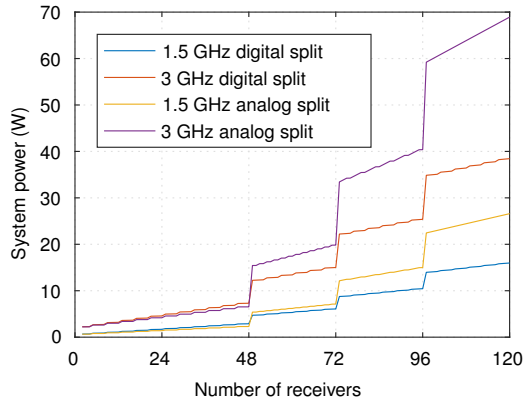


Figure 4.12: Estimated cross-correlator system power, including signal and clock splitters, ADCs and cross-correlators, for four cases.

When building cross-correlator systems, it may be important to verify proper functionality of the ASICs. In Paper III functionality tests were performed using programmable static input patterns. Here, inputs were driven in groups connected to an 8-bit driver, hence, only 256 input patterns could be tested, and many of the products were not exercised. To perform a full coverage test, due to the xor multi-

plication scheme used in the 2-level mode, all input channels of the cross-correlator have to be programmed individually. For a 96-channel cross-correlator this would translate to a total of 2^{96} available patterns. Exercising all integration counter bits individually also means sweeping through 2^D different integration times, where D is the integrator depth. Sweeping through all available patterns would take many orders of magnitude more time than the age of the Universe, luckily all possible input patterns do not need testing for full coverage of all correlation products. One could easily devise a test pattern where the integration time sweep is performed with only one input channel set to high at a time. For full coverage, then, only $N_{channels} - 1$ time sweeps have to be performed, and number of frames to be tested is $(N_{channels} - 1) \cdot 2^D$. For the 96-channel cross-correlator with 4-bit prescaler and 24-bit integrator, a full coverage test can be performed in less than a minute at 1 GHz. More clever input pattern choices can further reduce this to less than 6 seconds of testing time.

4.4 Integration in the GAIS Demonstrator

Since publication, the cross-correlator PCB presented in Paper II has been used in a demonstrator for the Geostationary Atmospheric Interferometric Sounder (GAIS) project [61]. An enclosure shown in Figure 4.13 was designed for the board and the unit was integrated in the GAIS demonstrator in Figure 4.14a. The GAIS demonstrator was developed at Omnisys Instruments and performs observations at the 183-GHz H_2O line. The 24 antennas of the array are placed within an arc of approximately 1-dm width across a half-circle with a diameter (longest baseline) of 1.4 m, with the shortest baseline extending a mere 6 mm. Receiver placements were determined in simulation by starting with an initial placement and then iteratively relocating each receiver to find a better position. In this context better placement of receivers means as even a distribution of baseline lengths as possible. The complete structure is also rotated, similar to GAS and GIMS, to sample multiple angles of baselines.

Imaging of the Sun, shown in Figure 4.15a, as well as other tests were performed in the summer of 2017. The demonstrator was also integrated in the center of the circular 53-GHz GIMS-II demonstrator, Figure 4.14b¹, showing the viability of combining the two on a single satellite platform. Imaging demonstrations performed at the NSSC facility are shown in Figure 4.15b.

Imaging at 183-GHz proved to be a significant step up in complexity from earlier experiences during demonstrations at 53 GHz performed within the GAS campaign. The up to 1.4 m baselines of the GAIS demonstrator constitutes a more than 6-fold increase in resolution compared to imaging at 53 GHz with baselines of up

¹Image by Johan Embretsén.

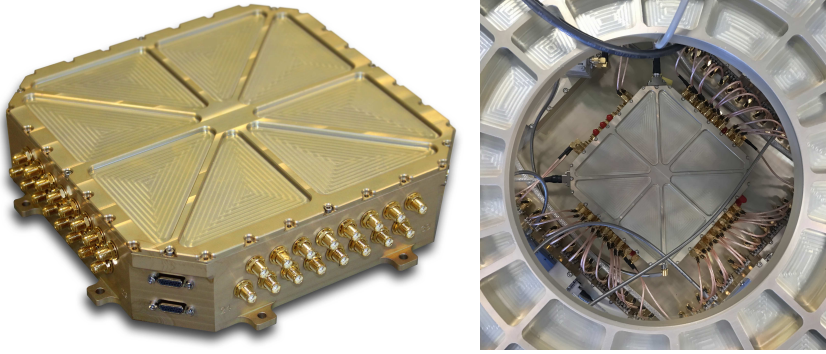


Figure 4.13: The GAIS cross-correlator unit.

to 75 cm. This also means a more than 6-fold increase in requirements of phase control within the system, hence extensive work on phase alignment, electrical as well as structural, was performed and procedures for phase calibration were developed for this demonstrator. The success of this demonstrator work has paved the way for a future aperture synthesis instrument in GEO.

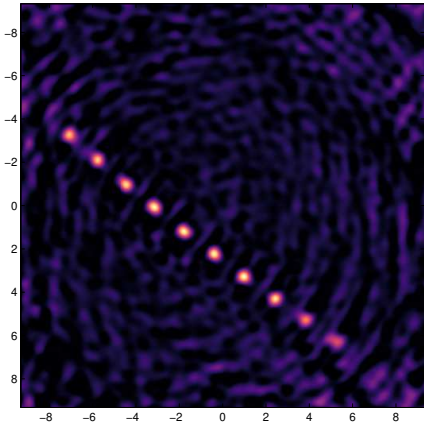


(a) GAIS standalone demonstrator performing Sun measurements.

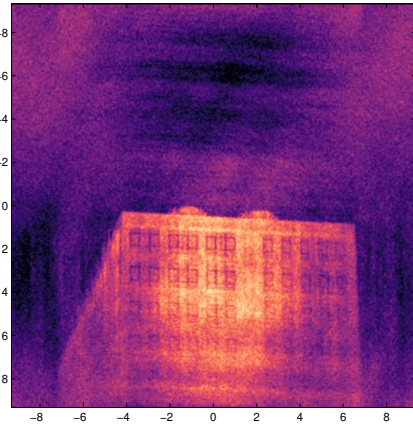


(b) GAIS demonstrator integrated in GIMS-II performing imaging at NSSC.

Figure 4.14: The GAIS demonstrator.



(a) Sun passage.



(b) The NSSC building.

Figure 4.15: GAIS demonstrator imaging results.

Chapter 5

Summary and Future Work

This thesis presents efforts to implement power-efficient cross-correlators. While other usage scenarios may be found, the cross-correlator work presented mainly targets usages in satellites performing microwave remote sensing from GEO by means of aperture synthesis. With this in mind, Chapter 2 introduces the ideas of radiometry, aperture synthesis and discusses the GEO environment while Chapter 3 focuses on the history of radio astronomy, and the current and future applications in remote sensing. In Papers I-III, my work on cross-correlator systems and ASICs is presented. Chapter 4 expands the results from the papers by describing test methodologies, introducing more in-depth system-level analyses, and demonstrating the successful implementation in the GAIS demonstrator.

For full-size instruments, it is likely that more than 96 channels are of interest, or especially more than 48 3-level channels. With the work demonstrated in this thesis, much of the foundation has been laid, and larger cross-correlators may be designed using the existing building blocks. There is also room for future improvements other than expanding input count. Such work may include further power dissipation reduction and design ideas to simplify and improve the system.

Reduction of power dissipation may be achieved in a number of ways besides additional circuit optimization. Analog-to-digital conversion is a major contributor to the overall power budget of the cross-correlator system, hence, migrating the ADC to newer technology nodes may be advantageous. The ADC to cross-correlator interconnect power dissipation is also far from insignificant and could potentially be reduced. One way of reducing interconnect power dissipation would be to include the ADC on the cross-correlator ASIC, however, considerations such as channel isolation have to be taken into account. Making all IOs (and not only clocks) differential would mean a more robust signal interface between ADCs and cross-correlator, and signal swing could then potentially be reduced further, saving power. The significant increase in IOs will, however, likely require implementing

flip-chip techniques for minimizing chip area, which usually leads to a higher packaging cost.

For system complexity reduction, a few improvements can be done at the ASIC-level. On the 64-channel cross-correlator presented in Paper II, the offset calibration was handled by 16 eight-channel programmable potentiometers. A major reduction in board-level routing complexity could be achieved by integrating the offset calibration digital-to-analog converters (DACs) in the ADC. Adding a built-in clock splitter in the cross-correlator for distributing sample clock to the ADCs may also be done for reducing the number of components in the system. This would, however, incur an overhead if constructing correlator systems implementing split-after-ADC architecture as discussed in Section 2.3.2. Since operating in 2-level mode does not give information on signal magnitude, adding a total-power channel on chip could be useful for calibrating the brightness temperature of the image.

Constructing a complete cross-correlator based on the newer 96-channel ASIC is, of course, a natural next step, improving on the design presented in Paper II, not only by increased channel count. Significant improvements in power dissipation could be achieved by replacing linear regulators with more efficient power conditioning circuits. In addition, higher bandwidths could quite easily be reached by replacing the clock splitter circuit and by substituting input transformers with higher bandwidth alternatives. With the ongoing initiatives such as GAIS driving the correlator system requirements, it is likely that a cross-correlator of this type will integrate more than one cross-correlator ASIC on a single PCB. A system with at least three cross-correlator ASICs on one PCB remains to be built, and even larger systems using several such boards connected by a central distribution card can be conceived in the future.

In conclusion, the work presented in this thesis demonstrates a way of constructing cross-correlators that are well within performance target for aperture synthesis based remote sensing from GEO while simultaneously meeting power dissipation requirements for application on a satellite platform.

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