Thesis for the degree of Doctor of Philosophy

Buffer Related Dispersive Effects in Microwave GaN HEMTs

Johan Bergsten

CHALMERS

Department of Microtechnology and Nanoscience - MC2

Chalmers University of Technology

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Department of Microtechnology and Nanoscience - MC2
Chalmers University of Technology
SE-412 96 Göteborg
Sweden
Telephone + 46 (0)31-772 1000

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Chalmers University of Technology

Abstract

In applications such as mobile communication and radar, microwave power generation at high frequency is of utmost importance. The GaN HEMT offers a unique set of properties that makes it suitable for high power amplification at high frequencies. However, their performance is limited by trap states, leading to reduced output power and time variant effects. Furthermore, for good high frequency performance a high efficiency it is essential to limit the access resistances in the transistor. The GaN HEMT technology has long lacked a good ohmic contact with good reproducibility.

In this thesis, three buffer designs are considered; C-doped GaN, AlGaN back barriers and a thin GaN structure. The three designs are evaluated in terms of trapping effects using the drain current transient technique. For the C-doped GaN buffer, trapping at dislocations covered with C-clusters is believed to be the main factor limiting output power. Dislocations are presumed to play a major role for the trapping behavior of AlGaN back barriers and the thin structure as well. The maximum output powers for C-doped GaN, AlGaN back barriers and the thin structure are 3.3, 2.7, and 3.9 W/mm at 30 GHz. The output power is found to be limited by trapping effects for all buffer designs.

Moreover, a Ta-based, recessed ohmic contact enables a contact resistance of down to 0.14 Ωmm. The results also indicate that a highly reproducible process might be possible for deeply recessed contacts. An optimized AlGaN/GaN interface shows high mobility >2000 cm^2/Vs without the use of an AlN-exclusion layer. The improved interface also decreases trapping effects and the gate-source capacitance at large electric fields compared to an unoptimized interface.

KEYWORDS: GaN HEMT, buffer design, C-doping, trapping effects, recessed ohmic contacts, AlGaN/GaN interface quality.

List of appended papers

This thesis is based on the work contained in the following papers:

A. **J. Bergsten**, A. Malmros, M. Tordjman, P. Gamarra, C. Lacam, M.-A. di Forte-Poisson, and N. Rorsman, "Low resistive Au-free, Ta-based, recessed ohmic contacts to InAlN/AlN/GaN heterostructures," *Semiconductor Science and Technology*, vol. 30, iss. 10, pp. 105034, 2015.

B. **J. Bergsten**, J.-T. Chen, S. Gustafsson, A. Malmros, U. Forsberg, M. Thorsell, E. Janzén, and N. Rorsman, "Performance Enhancement of Microwave GaN HEMTs Without an AlN-Exclusion Layer Using an Optimized AlGaN/GaN Interface Growth Process," *IEEE Transactions on Electron Devices*, vol. 63, iss. 1, pp. 333-338, 2015.

C. S. Gustafsson, J.-T. Chen, **J. Bergsten**, U. Forsberg, M. Thorsell, E. Janzén, and N. Rorsman, "Dispersive Effects in Microwave AlGaN/AlN/GaN HEMTs With Carbon-Doped Buffer," *IEEE Transactions on Electron Devices*, vol. 62, iss. 7, pp. 2162-2169, 2015.

D. **J. Bergsten**, X. Li, D. Nilsson, Ö. Danielsson, H. Pedersen, E. Janzén, U. Forsberg, and N. Rorsman, "AlGaN/GaN high electron mobility transistors with intentionally doped GaN buffer using propane as carbon precursor," *Japanese Journal of Applied Physics*, vol. 55, pp. 05FK02, 2016.

E. **J. Bergsten**, M. Thorsell, J.-T. Chen, D. Adolph, O. Kordina, E. Ö. Sveinbjörnsson, and N. Rorsman, "Electron Trapping in Extended Defects in Microwave AlGaN/GaN HEMTs with Carbon Doped Buffers," *Submitted to IEEE Transactions on Electron Devices.*

Other publications

The following papers have been published but are not included in the thesis. Their content partially overlap with the appended papers or are out of the scope of this thesis.

a. X. Li, **J. Bergsten**, D. Nilsson, Ö. Danielsson, H. Pedersen, N. Rorsman, E. Janzén, and U. Forsberg, "Carbon doped GaN buffer layer using propane for high electron mobility transistor applications: Growth and device results," *Applied Physics Letters*, vol. 107, iss. 26, pp. 262105, 2015.

b. T. Huang, A. Malmros, **J. Bergsten**, S. Gustafsson, O. Axelsson, M. Thorsell, and N. Rorsman, "Suppression of Dispersive Effects in AlGaN / GaN High-Electron-Mobility Transistors Using Bilayer SiN_x Grown by Low Pressure Chemical Vapor Deposition," *IEEE Electron Device Letters*, vol. 36, iss. 6, pp. 537-539, 2015.

c. T. Huang, O. Axelsson, A. Malmros, **J. Bergsten**, S. Gustafsson, M. Thorsell, and N. Rorsman, "Low-Pressure-Chemical-Vapor-Deposition SiN_x passivated AlGaN/GaN HEMTs for power amplifier application," *Asia-Pacific Microwave Conference Proceedings, APMC*, vol. 3, 2016.

d. T. Huang, C. Liu, **J. Bergsten**, H. Jiang, K. M. Lau, and N. Rorsman "Fabrication and Improved Performance of AlGaN/GaN HEMTs with Regrown Ohmic Contacts and Passivation-First Process," *Compound Semiconductor Week*, 2016.

e. A. Pooth, **J. Bergsten**, N. Rorsman, H. Hirshy, R. Perks, P. Tasker, T. Martin, R. F. Webster, D. Cherns, M. J. Uren, and M. Kuball, "Morphological and electrical comparison of Ti and Ta based ohmic contacts for AlGaN/GaN-on-SiC HFETs," *Microelectronics Reliability*, vol. 68, pp. 2-4, 2017.

f. T. Huang, O. Axelsson, **J. Bergsten**, M. Thorsell, and N. Rorsman, "Achieving Low-Recovery Time in AlGaN/GaN HEMTs with AlN Interlayer under Low-Noise Amplifiers Operation," *IEEE Electron Device Letters*, vol. 38, iss. 7, pp. 926-928, 2017.

g. T. Huang, **J. Bergsten**, M. Thorsell, and N. Rorsman, "Small- and Large-Signal Analyses of Different Low-Pressure-Chemical-Vapor-Deposition SiN_x Passivations for Microwave GaN HEMTs," *IEEE Transactions on Electron Devices*, vol. 65, iss. 3, pp. 908-914, 2018.

h. **J. Bergsten**, "Advanced Heterostructure Designs and Recessed Ohmic Contacts for III-Nitride-Based HEMTs," Thesis for the degree of Licentiate of Engineering, Department of Microtechnology and Nanoscience, Chalmers University of Technology, Gothenburg, Sweden, 2015.

Contents

Chapter 1

Introduction

GaN high electron mobility transistors (HEMTs) are of great interest for microwave power generation at high frequency. At the early stages, the advancements of GaN HEMTs were mainly driven by radar applications in the defense industry. In these, high output power, efficiency, and robustness are of great importance. The last couple of years, radar systems based on GaN HEMT monolithic microwave integrated circuits (MMICs) have started entered the market. Currently, mm-wave scanners for security applications are also among possible applications for GaN HEMTs. Furthermore, as the demand for higher data rates in mobile communication is increasing, higher operating frequencies are required in order to increase bandwidths and escape the congested bands in the sub 6 GHz range. In the 5th generation of wireless systems (5G), operating frequencies up to 60 GHz are expected. Moreover, wireless links in the backhaul of the 5G network (requiring very high data rates) are expected to operate at frequencies up to 170 GHz. These demands are a good fit for the large bandwidths achievable through the GaN HEMT technology. Aside from these applications, GaN HEMTs are readily employed in high power switching applications. In these, the low on-resistance, high switching frequencies and high operating voltages offer exceptional performance [1]. Even though GaN HEMTs for power applications share many of the issues of GaN HEMTs for microwave applications, power devices will not be considered in this thesis.

The excellent performance of the GaN HEMT is enabled by the large band gap of GaN (3.4 eV), its large electron velocity ($2 \cdot 10^7$ cm/s), together with the ability to form HEMT epi-structures with

high electron mobility (> 2000 cm^2/Vs) and large electron sheet density ($> 1 \cdot 10^{13}$ cm^{-2}). The large band gap leads to robust devices that can operate at high voltages. The high electron mobility and large sheet density decreases the losses in the transistors and, together with the large electron velocity, enables excellent high frequency performance with f_T and f_{max} reaching over 400 GHz [2]. In total, the exceptional material qualities leads to high achievable output power ($Pout = 3$ W/mm) even at operating frequencies around 100 GHz [3]. Furthermore, due to the large operating voltages superior linearity and lower matching losses compared to competing technologies are expected [4]. The HEMT structure also facilitates great noise performance, making GaN HEMTs ideal for low noise amplifiers.

However, even though GaN HEMT technology has matured exceedingly over the past years, several problems still remain. For example, a highly repeatable ohmic contact with low contact resistance is not yet available. This leads to reduced yield, reduced efficiency and reduced high frequency performance. Furthermore, DC-AC dispersion is a major concern, leading to reduced output power and efficiency. In some applications, such as low noise amplifiers, linearity can also be heavily affected by dispersive effects. The dispersive effects are due to traps located mainly on the surface or in the bulk of the semiconductor. The effects of the surface traps can be almost completely mitigated using passivation layers and field plates while the bulk traps require extensive epi-structure optimization to be minimized. Since the HEMTs operate at high power levels, large demands are put on thermal management. The epi-structure is commonly grown on SiC substrates, enabling an effective removal of excess heat. However, layers of poor crystalline quality or ternary alloys (e.g. AlGaN or InAlN) in the epi-structure can severely increase the total thermal impedance between the transistor and the substrate [5, 6]. From a commercial standpoint the GaN HEMT technology lacks standardized processes, leading to reduced reliability, uniformity, and repeatability, which are associated with large associated costs.

The main part of the thesis is attributed to buffer design and its effect on dispersive effects and output power. The goal has been to summarize the three appended papers dealing with this topic, trying to give a combined interpretation of the results. In the case when the appended papers does not cover the topic that is discussed, previously unpublished results are used to facilitate the discussion. Other aspects

on GaN HEMT technology are also investigated with focus on areas where problems still remain. Furthermore, this thesis aims to give the reader a brief introduction to the basic ideas and problems of the GaN HEMT.

The thesis is organized as follows. A brief introduction to the GaN HEMT, its operation, and the epi-structure design is given in Chapter 2. In Chapter 3 crucial technological aspects of the GaN HEMT is discussed, including ohmic contacts and surface passivations. The main contribution of this thesis, regarding buffer design and characterization, is presented in Chapter 4. Finally, Chapter 5 presents conclusions that can be drawn from this thesis and a future outlook of the field. Parts of the research work in this thesis have already been published in the Licentiate thesis [h]. Therefore, text and figures from [h] may be fully or partially reproduced in this thesis.

Chapter 2

GaN HEMT fundamentals

The aim of this chapter is to give a brief introduction to the basic design and function of a GaN HEMT. This is used as a basis for discussion of different issues and design choices, parts of which are considered more extensively later in the thesis. Section 2.1 deals with the transistor layout and its operation. In section 2.2 a brief introduction to a standard GaN HEMT epi-structure on a SiC substrate, similar to what has mostly been used in this thesis, is presented.

2.1 The GaN HEMT and its operation

A schematic cross section of an AlGaN/GaN HEMT, with its essential parts indicated, can be seen in Fig. 2.1. The 2-dimensional electron gas (2DEG) in the AlGaN/GaN interface forms the channel of the transistor. The electrons in the 2DEG should have a high electron mobility (μ) to decrease the resistance of the access regions. Furthermore, the electron sheet concentration (n_s) should be appropriately large for the intended application. Standard values for μ and n_s in an AlGaN/GaN heterostructure are 2000 $\mathrm{cm}^2/\mathrm{Vs}$ and 10^{13} cm^{-2} respectively.

2DEG formation The mechanisms responsible for the formation of the 2DEG is well described in [7]. In short, the III-N materials are all polarized due to the strong ionicity of their covalent atomic bonds. In the standard Ga-polar case, the polarization fields are pointing down into the structure, as indicated in Fig. 2.2a. The polarization field strength is larger in AlGaN compared to GaN, giving a net positive

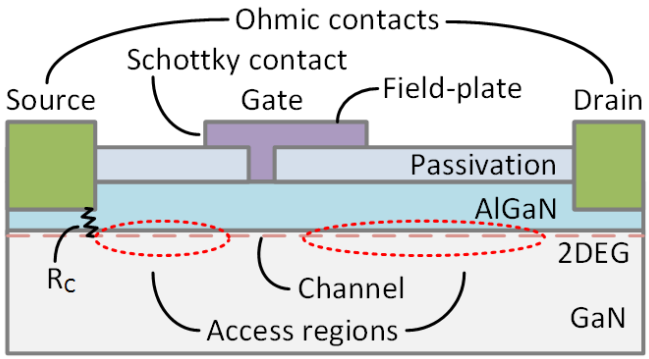
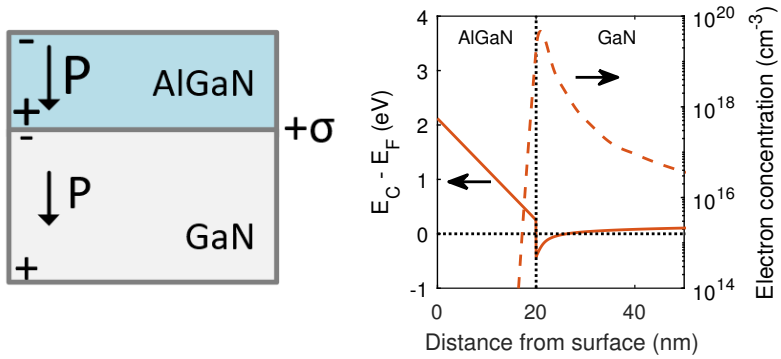


Figure 2.1: Schematic illustration of an AlGaN/GaN HEMT. Image not to scale.

polarization charge at the AlGaN/GaN interface. This charge attracts electrons originating from the AlGaN surface, forming the 2DEG. The number of electrons in the 2DEG will be the same as the polarization charge which depends on the Al content and thickness of the AlGaN layer, where increasing Al-concentration and thickness leads to larger n_s. For an AlGaN barrier layer the Al-concentration usually range from 15 to 30%, and the thickness from 10 to 25 nm. The band structure of an $Al_{0.30}Ga_{0.70}N$/GaN structure can be seen in Fig. 2.2b. Compared to the AlGaAs/GaAs structure an important difference is that no n-doping in the AlGaN barrier layer is required to generate the electrons in the 2DEG. However, since the 2DEG is formed of electrons from the surface it is exceedingly sensitive to changes in the surface potential.

Ohmic and Schottky contacts The ohmic drain and source contacts should supply a connection to the 2DEG with low contact resistance (R_C). Due to the large band gaps of the III-N:s, ohmic contact formation is hard to achieve. The topic of ohmic contacts have been a long standing issue in the GaN HEMT community and is explored in more detail in Chapter 3.

The purpose of the gate Schottky contact is to control the current flowing between the two ohmic contacts. This is done by utilizing the field effect where a change in V_{GS} will result in band bending under the gate contact. For a sufficiently negative V_{GS}, a depletion of the 2DEG under the gate contact is achieved, as illustrated in Fig. 2.3. Ni is the most commonly used gate metal for GaN HEMTs and is also used in



(a) (b)

Figure 2.2: (a) Polarization fields in an AlGaN/GaN epi-structure, resulting in a net positive charge σ at the interface. (b) Conduction band and electron concentration of the heterostructure in (a).

this thesis. Other large work function metals can also be employed, such as Pt, Pd, Ir or Au [8]. The gate metal should also offer a low resistivity, to decrease the gate resistance, and good adhesion to the surface. The maximum output current is set by when the forward biased Schottky diode starts conducting. When it does, any change in applied gate voltage will modulate the gate leakage current instead of the band bending. A metal-insulator-semiconductor (MIS) structure can be used to limit gate leakage [9].

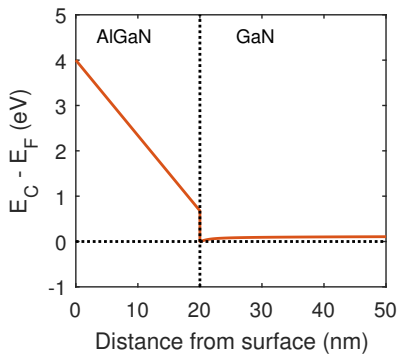


Figure 2.3: Schematic illustration of flat band condition.

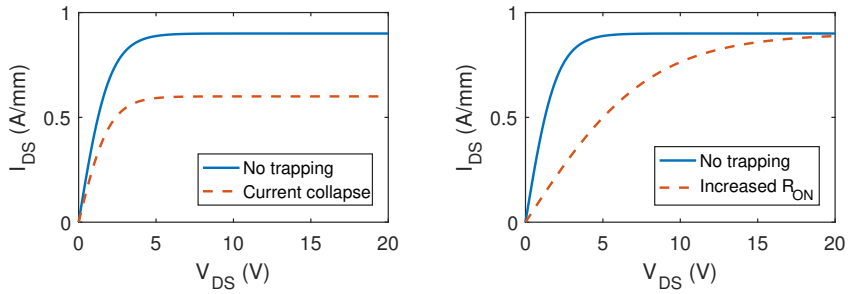


Figure 2.4: A schematic illustration of (a) current collapse and (b) dynamic R_{ON}.

Surface effects Since the electrons in the 2DEG originates from the barrier surface it is very sensitive to changes in the surface potential [10]. Electrons can interact with trap states at the surface, reducing the number of electrons in the 2DEG. During transistor operation, this can have a large negative impact on performance. In fact, trapped electrons on the surface acts like a virtual gate, depleting the 2DEG [11]. If the trapping occur around the gate a decrease in I_{DS} will be measured, an effect known as current collapse, see Fig 2.4a. If the trapping occur in the drain access region, an increase in R_{ON} will be measured, Fig 2.4b. The trapped electrons usually originate from the gate metal and can get trapped during e.g. off-state biasing conditions or for large drain voltages. To mitigate these effects a surface passivation is usually deposited with the aim to passivate trap states or effectively blocking electrons from getting trapped.

Surface passivation The most investigated passivation layer for GaN HEMTs is silicon nitride, SiN_x [12, 13, 14, 15]. In this case, nitrogen is believed to play a crucial part in filling nitrogen vacancies on the surface, reducing the number of interface traps [16]. Other commonly used passivations are SiO_2 and Al_2O_3 [17, 18]. Several studies have compared different passivation layer's ability to reduce current collapse with various results [19, 20, 21]. Generally, SiN_x is found to give best performance. However, only comparing the passivation material is problematic since both pre- and post-treatments have shown to have large impact on trapping effects. For example, both N and O plasma based

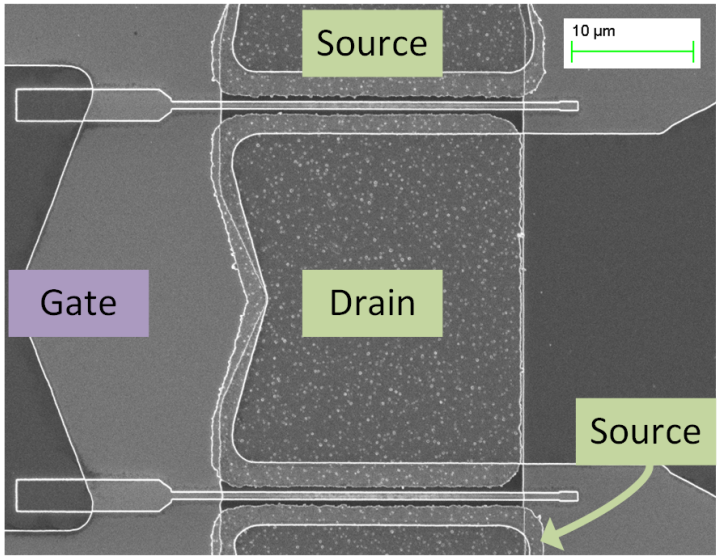


Figure 2.5: SEM micrograph of a HEMT fabricated in this work. The gate, drain, and source contacts are indicated in the figure.

pre-treatments have shown to increase the effectiveness of the passivation layer [22, 23]. The topic of surface passivations and surface effects on III-N heterostructures is complex and many effects are not yet fully understood. Consequently, it is a popular research topic with many publications each year. For a more in depth look in to surface effects and passivations on GaN and AlGaN see [24].

Device layout A scanning electron microscope (SEM) micrograph of a GaN HEMT fabricated in this work can be seen in Fig. 2.5. The source, drain and gate contacts are indicated in the figure. As seen, two gate contacts are present. This design is made up of two transistors in parallel, with a shared drain contact. This is a common method to reduce the total area of the transistor for a certain gate width. In this thesis most, most measurements have been performed on 2x50 μm devices. Typical transistor dimensions are as follows; L_{DS} = 2-3 μm, L_{GD} = 1-2 μm, L_{GS} = 1 μm, L_G = 50-200 nm.

High frequency operation Two standard figures of merit of a transistors ability to operate at high frequencies are f_T and f_{max}. f_T (f_{max}) is defined as the maximum frequency at which the transistor can supply

small signal current (power) gain. f_T is proportional to $v_e/\mathrm{L_G}$, where v_e is the electron velocity, whereas f_{max} is given by;

$$f_{max} = \frac{1}{2}\frac{f_T}{\sqrt{2\pi \cdot f_T \cdot C_{gd}(R_g + R_s) \cdot \frac{R_g+R_s}{R_{ds}}}}. \tag{2.1}$$

Here, C_{gd} is the gate-drain capacitance, R_g and R_s are the gate and source access resistances, and R_{ds} is the output resistance. The main method of increasing the high frequency performance is down-scaling of $\mathrm{L_G}$. However, as $\mathrm{L_G}$ is decreased, short channel effects start emerging, weakening the gate control. The short channel effects can be reduced by making the barrier layer thinner, decreasing the distance between the gate and the 2DEG. It has been reported that the aspect ratio between the gate length and AlGaN barrier thickness should be at least 15 in order to limit short channel effects [25]. However, as the barrier thickness is decreased n_s will also decrease, creating a complex optimization problem. Other than gate length scaling, decreasing the resistance in the access regions and the ohmic contacts are also vitally important for high frequency performance.

Electric fields in the structure One of the advantages of GaN HEMTs are the large breakdown voltages. During operation, large drain biases are regularly applied, leading to large electric fields. In Fig. 2.6 the electric potential distribution in a GaN HEMT held in off-state with a large drain bias are visualized. As seen, the change in electric potential (electric field) is largest at the gate edge on the drain side but also extends deeper into the GaN layer. Therefore, the large fields can have a considerable impact on the electron occupation of trap states in these areas. Gate or source connected field plates can help reduce the electric field strength and in so the number of occupied traps [26, 27]. In this work, a gate integrated field plate, as indicated in Fig. 2.1, is commonly used.

2.2 The GaN HEMT epi-structure

This section will give a brief overview of a standard GaN HEMT epi-structure, commonly used for RF power amplifier applications, see Fig. 2.7. The purpose of each layer will be shortly explained and alternative material selections will be outlined. Currently, more exotic epi-structures are frequently reported. These will be covered more

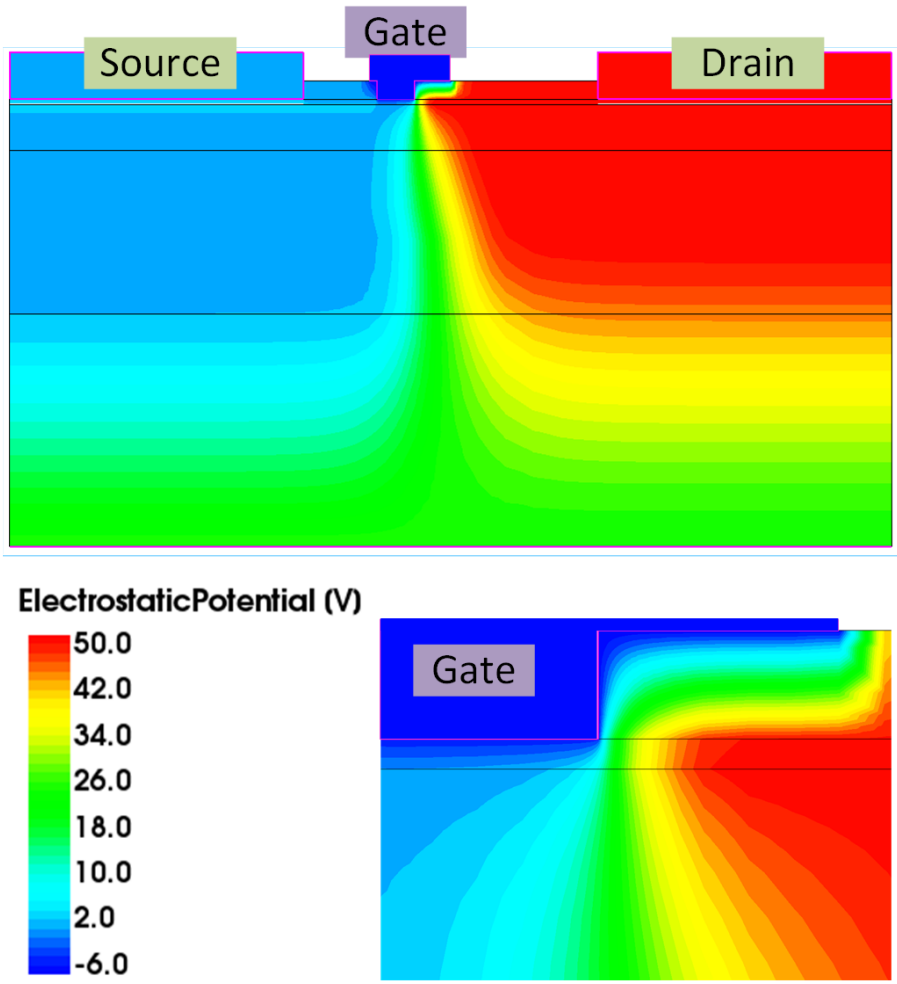


Figure 2.6: Electric potential distribution in a GaN HEMT biased in an off-state with a drain voltage of 50 V. Sentaurus simulations courtesy of Hans Hjelmgren.

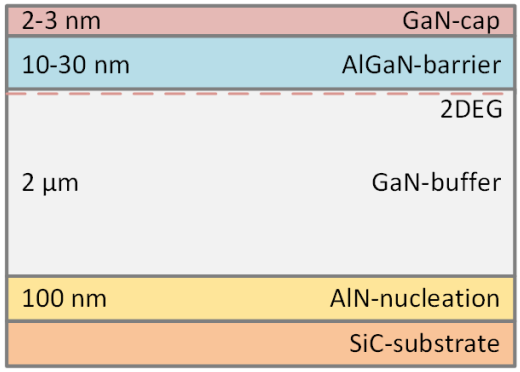


Figure 2.7: A schematic figure of an GaN epi-structure on a SiC substrate with approximate layer thicknesses indicated. Image not to scale.

extensively later in the thesis. Several different techniques are available to grow the epi-structure, the most commonly used are metal organic chemical vapor deposition (MOCVD) and molecular beam epitaxy (MBE). In this work, the main material suppliers (and collaborators) has been Linköping University and SweGaN AB, both of which use the same hot-wall MOCVD system [28]. However, materials have also been supplied by Cree Inc., IQE, and III-V lab, using the more common cold-wall MOCVD technique. As indicated by the name, in the hot-wall system the temperature of the growth target is controlled by heating the walls of the growth chamber, whereas only the target is heated in the cold-wall system. The lower temperature gradients in the hot-wall case generally results in better wafer uniformity but the technique is less suited for large scale fabrication compared to cold-wall systems. Since all the materials in this work have been grown using MOCVD, this will be the main growth method considered in this thesis.

Substrate A good substrate material should have a lattice constant close to the material that is to be grown on it. Under operation the HEMTs will generate a lot of heat so a large thermal conductivity of the substrate is desired. Furthermore, for high frequency applications the substrate should preferably be highly resistive in order to minimize parasitical capacitance. For commercial applications the substrate price is also of large concern. Table 2.1 summarizes the most common substrate alternatives for GaN-based epi-structures and their performance with respect to the parameters discussed above.

Material	Lattice mismatch with GaN (|%|)	Thermal conductivity (W/mm K)	Price
4H-SiC	3.4	490	Moderate
Si	17	150	Low
GaN	0	260	High
AlN	2.5	285	High
Diamond	12	600-2000	High

Table 2.1: Available substrates for III-N growth.

The high thermal conductivity and low lattice mismatch of SiC has made it the most common substrate for RF power amplifier applications. Meanwhile, the low price of Si substrates has made it the standard substrate for high power applications. GaN and AlN are both very attractive substrates but are only beginning to become commercially available in very small sizes. On these, very high quality GaN can be grown with low dislocation densities. Diamond is interesting due to its extremely high thermal conductivity. However, the large lattice mismatch and large difference in thermal expansion coefficient makes growth difficult. In this work SiC substrates have mainly been used.

Nucleation layer The function of the nucleation layer is mainly to facilitate two-dimensional growth of the subsequent GaN buffer, but also to mitigate the lattice mismatch between GaN and the substrate. Due to the lattice mismatch the crystal quality is inherently low for the nucleation layer, making it a poor thermal conductor. Since much of the benefits of using substrates with large thermal conductivity is negated by putting a thermal barrier in between the substrate and the devices, effort has been put in to optimizing the quality of the nucleation layer [5]. For SiC substrates AlN is most commonly used as nucleation layer. The larger lattice mismatch between GaN and Si sets larger requirements on the nucleation layer. Therefore, it is not uncommon to use strained AlN/GaN superlattices [29]. An advantage with GaN substrates is that no nucleation layer is required which will aid the overall heat transport through the structure.

GaN buffer The purpose of the GaN buffer layer is to decrease the number of defects in the channel region and enable a flat surface for

the barrier layer to be grown upon. Usually, the GaN buffer needs to be grown to a thickness of more than 1μm before these conditions are met. The buffer also needs to supply a good bottom confinement in order to limit short channel effects. This can be achieved in a number of ways, unfortunately all of them are associated with increased trapping in the buffer region. Minimizing trapping effects while maintaining good confinement is therefore a common research topic for GaN HEMTs. This is also a large part of the thesis work and is further investigated in Chapter 4.

Barrier As explained above, using an AlGaN barrier as example, the 2DEG is formed due to the polarization charge in the barrier/GaN interface. However, other barrier materials than AlGaN are commonly employed. $In_{0.17}Al_{0.83}N$ has the advantage of being lattice matched to GaN. This gives less strain in the structure which is beneficial from a reliability perspective. Furthermore, the high Al-concentration of $In_{0.17}Al_{0.83}N$ results in a large polarization field, meaning a large n_s can be achieved for thinner barrier thicknesses. This is advantageous for high frequency applications since good gate control can be obtained even for short gate lengths. Even thinner barriers are possible when using pure AlN as barrier material. In this case, a barrier thickness of 3-4 nm is enough to generate a high n_s. Therefore, HEMTs with high values of f_T and f_{max} commonly utilize InAlN [30] or AlN [2] barriers.

GaN cap On top of the (usually Al rich) barrier layer it is common to include a thin (2-3 nm) GaN cap layer. This layer is intended to protect the surface of the barrier from oxidizing once it is removed from the growth chamber. The GaN cap layer reduces the maximum drain current as well as the gate leakage [31].

Chapter 3

GaN HEMT technology

Standardized processes with high yield are of great importance for any semiconductor technology. Many emerging technologies struggle to compete with more mature technologies, such as Si or GaAs, due to higher associated costs. Over the last 20 years GaN HEMT technology has matured immensely. However, areas still remain where no standardized solutions exists. Most notably are the ohmic contacts which have been a long standing problem. The large band gap complicates the contact formation and although low resistive ohmic contacts are frequently reported, a standardized contact is not yet available. Another area of large interest is surface passivation. However, compared to ohmic contacts, surface passivation techniques are rather mature. A proper passivation layer in combination with field plates have shown to almost completely remove surface trapping [32]. A large part of the advances for GaN HEMTs can also be attributed to advances in material growth. Over the years, crystal quality have gradually increased and epi-structure designs that were previously only theoretically conceivable are now routinely grown. Nevertheless, dislocations and other growth defects can still have a limiting effect on device reliability and performance [33].

This chapter will give an overview of some important and challenging areas of GaN HEMT technology. First, the process flow for HEMT fabrication used in this thesis is presented in section 3.1. Second, ohmic contacts to GaN-based heterostructures are considered. A recess etched Ta-based contact is reported in paper [A] and the general state of ohmic contacts to GaN-based heterostructures is treated in section 3.2. Third,

achieving low device-to-device leakage has been investigated in section 3.3. Lastly, section 3.4 deals with material growth, specifically the quality of the GaN to AlGaN transition. Paper [B] reports on the effect of the AlGaN/GaN interface quality on electron penetration into the barrier layer. Buffer design is also of vital importance for the GaN HEMT large-signal and high frequency performance. This topic is considered in Chapter 4.

3.1 HEMT fabrication process

The process flow for HEMT devices used in this thesis is presented in Fig. 3.1. The processing steps are as follows:

1. A Si-rich SiN passivation layer (50-70 nm) is deposited using low pressure chemical vapor deposition (LP-CVD). This passivation has shown to give a good protection from surface trapping [34].
2. Mesa isolation is achieved using photolithography and an Oxford ICP-RIE dry etching system (used for all dry etching processes). The SiN is etched in a NF_3-based plasma, whereas the heterostructure is etched in a Cl/Ar-based plasma.
3. Recessed ohmic contacts are formed. This is a self-aligned process in which the same resist mask is used for both etching and metal lift-off. A low power Cl-based plasma is used for the recess etching, followed by surface cleaning in diluted HCl and HF. Metal deposition is performed in an e-beam evaporator system using a metal stack of Ta/Al/Ta. The contacts are annealed in a rapid thermal anneal system in N ambient at 550-600 °C. The ohmic contact process is explained in further detail in paper [A].
4. The gate footprint is defined using e-beam lithography and plasma etching. Most of the SiN is etched in a anisotropic etching process, based on CF_4/Ar. This allows the correct gate length to be maintained since the gate length is set by the etched trench in the SiN. The last part of the SiN is etched using the standard NF_3 plasma in order to remove any polymer residues created by the CF_4.
5. Another e-beam lithographic step is used to define the gate metal, which is deposited using e-beam evaporation. A Ni/Pt/Au metal stack is used, forming a gate with an integrated field plate.
6. Metal contact pads (Ti/Au/Ti) are formed using optical lithography and e-beam evaporation.

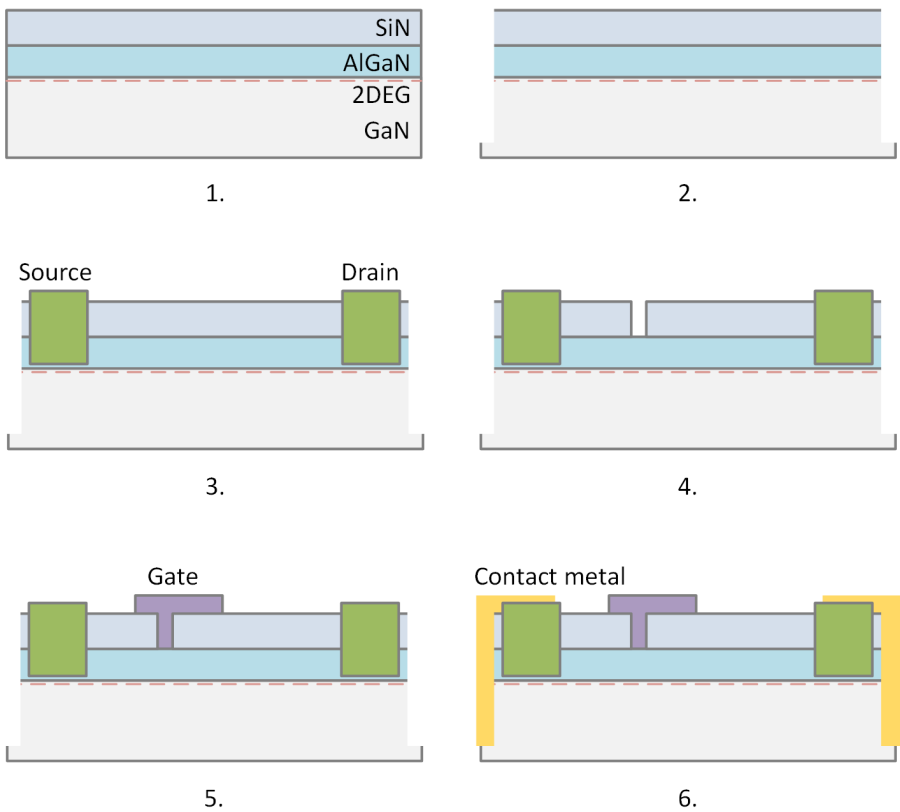


Figure 3.1: Illustration of the GaN HEMT process flow used in this thesis. Images not to scale.

3.2 Ohmic contacts

A reliable ohmic contact process with low contact resistance (R_C) is essential in all semiconductor technologies. For HEMTs, low R_C is especially vital for the high frequency performance of extremely scaled devices [35]. Noise performance, efficiency, and reliability are also enhanced for devices with low R_C-contacts. Furthermore, for devices with short drain and source access regions, the line edge acuity of the contacts is of great importance in order to prevent short circuits with the gate metal.

Planar contacts The standard way to achieve ohmic contacts with low R_C in GaN HEMT epi-structures is a Ti/Al/Ni/Au metal stack deposited directly on top of the barrier layer [36, 37, 38, 39, 40]. This planar contact method can give low R_C ($\sim 0.15\ \Omega mm$) but requires a high anneal temperature (800-900 °C) which may cause increased sheet resistance in the 2DEG [41]. Furthermore, poor line edge definition may be obtained due to the low melting point of Al (~ 660 °C), causing reactions with the Au layer [42, 43]. Many explanations for the low R_C obtained with Ti/Al-based contacts have been suggested. The formation of TiN through extraction of N from the semiconductor is the most common one. Here, N-vacancies in the barrier layer is thought to act as n-dopants which will effectively decrease the energy barrier seen by the electrons, increasing the tunneling probability and reducing the contact resistance [44, 45, 46, 47]. However, the violent reaction occurring when forming TiN have shown to lead to protrusions in to the semiconductor [48]. In paper [e] these protrusions have been connected to increased vertical and lateral leakage currents, limiting high voltage operation.

To get a sense of typical R_C values for planar contacts, Table 3.1 compares literature values of contacts formed to various GaN heterostructures where the metal stack has been deposited on top of the barrier. Both Ti/Al/Ni/Au and other metallization schemes are included. As seen, typically an anneal temperature of over 800 °C is required, with the exception of an Mo-based contact annealed at 650 °C. Another observation that can be made is that for Ti/Al-based contacts a higher R_C is generally obtained for AlGaN barriers with high Al-content. This is probably related to the larger energy barrier present in these cases.

Ref.	Barrier	Metal stack	Anneal temp. (°C)	R_C (Ωmm)
[36]	GaN/$Al_{0.28}Ga_{0.72}N$/ AlN (2/27/1 nm)	Ti/Al/Ni/Au	820	0.45
[38]	$Al_{0.24}Ga_{0.76}N$ (18 nm)	Ti/Al/Ni/Au	830	0.2
[40]	$Al_{0.30}Ga_{0.70}N$ (24 nm)	Ti/Al/Mo/Au	750	0.35
[49]	$Al_{0.26}Ga_{0.74}N$/AlN (-/- nm)	Ta/Ti/Al/ Mo/Au	825	0.4
[50]	GaN/$Al_{0.20}Ga_{0.80}N$/ AlN (2/20/2 nm)	Ti/TiN	850	0.13
[50]	GaN/$Al_{0.35}Ga_{0.65}N$/ (2/20 nm)	Ti/TiN	850	0.6
[51]	$In_{0.17}Al_{0.83}N$/AlN (6/1 nm)	Mo/Al/Mo/Au	650	0.15
[52]	$In_{0.17}Al_{0.83}N$/AlN (7/1 nm)	Si/Ge/Ti/ Al/Ni/Au	820	0.35
[53]	$In_{0.18}Al_{0.82}N$/AlN (10/1 nm)	Ti/Al/Ni/Au	900	0.15
[54]	$In_{0.18}Al_{0.82}N$/AlN (9/1 nm)	Ta/Si/Ti/ Al/Ni/Au	825	0.36

Table 3.1: Literature values of R_C for planar contacts on different heterostructures.

Ref.	Barrier	R_C (Ωmm)
[57]	$In_{0.17}Al_{0.83}N$/AlN (3/2 nm)	0.16
[55]	$In_{0.18}Al_{0.82}N$/AlN (8/1 nm)	0.10
[58]	GaN/AlN (3/4 nm)	0.10
[56]	GaN/$Al_{0.26}Ga_{0.74}N$/ (3/18 nm)	0.31
[d]	GaN/$Al_{0.30}Ga_{0.70}N$/ (2/11 nm)	0.24

Table 3.2: Literature values of R_C for regrown contacts on different heterostructures.

Regrown n^+-GaN contacts Extremely low values of R_C ($\sim 0.1\ \Omega mm$) have been achieved using regrown n^+-GaN contacts [2, 55]. These contacts are made by etching past the barrier, in to the buffer layer, and then growing lattice matched, highly doped n-GaN in the recess. This allows for the formation of a direct contact between the 2DEG and the n^+-GaN with low resistance. The n^+-GaN is then easily contacted using standard metallization. This technique offers very low R_C but the processing is complex and costly which could make it unsuitable for large scale fabrication. Furthermore, a large 2DEG density is required to obtain extremely low values of R_C for regrown contacts [56]. Since a large n_s is not always an option other contact processes are sometimes more reasonable options. Due to their nature, regrown contacts are mostly used on extremely down-scaled devices for high frequency operation. As explained in section 2.2, in these cases an AlN or InAlN barrier is usually employed for which a large n_s is easily attained. Table 3.2 shows achieved contact resistances on different heterostructures using regrown contacts. As expected, for barriers sustaining a large n_s an extremely low R_C can be achieved. However, for structures with a more moderate n_s ($\sim 1 \cdot 10^{13}$ cm^{-2}), R_C is comparable to metal-based contacts. This was also the case for the regrown contacts in paper [d].

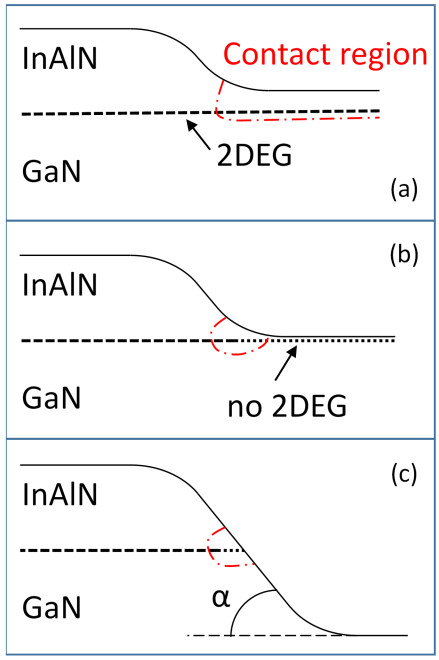


Figure 3.2: Illustration of three different cases of the formation of recessed ohmic contacts; (a) one where the barrier is still present, (b) one where the barrier is present but it is so thin that no 2DEG is formed under it and (c) one where the barrier has been entirely etched.

Recess etched contacts Recess etched metal based contacts can be seen as a compromise between planar metal contacts and regrown contacts. In this case, a recess etch is performed prior to metal deposition which has shown to decrease the required anneal temperature [59]. However, recess etching introduces additional parameters, such as recess depth and slope of the recess sidewall. Generally, the formation of recessed ohmic contacts can be divided in to three different cases; one where the barrier is still present, one where the barrier is present but it is so thin that no 2DEG is formed under it, and one where the barrier has been entirely etched away, Fig. 3.2. In the first case the contact mechanisms should be similar to planar metal based contacts. However, in the two later cases current transport have to rely on a sidewall contact [60]. For these, the sidewall angle (α) should be of great importance as it will determine the 2DEG-to-metal distance [56].

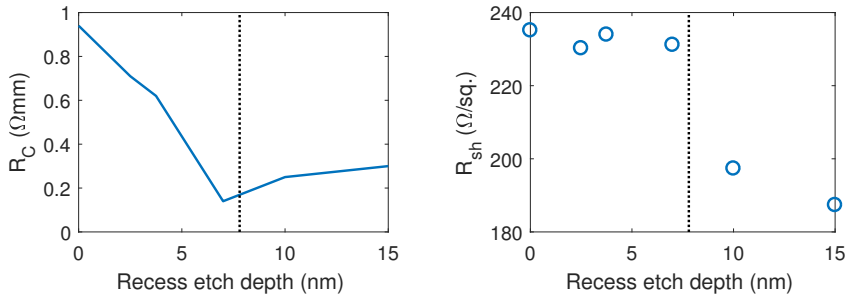
The effect of recess depth on R_C has been studied a number of times

Ref.	Barrier	Metal stack	Anneal temp. (°C)	R_C (Ωmm)
[A]	$In_{0.17}Al_{0.83}N$/AlN (6/2 nm)	Ta/Al/Ta	550	0.14
[51]	$In_{0.17}Al_{0.83}N$/AlN (6/1 nm)	Mo/Al/Mo/Au	650	0.15
[64]	$In_{0.18}Al_{0.82}N$/AlN (9/1 nm)	Ti/Al/Ni/Au	600	0.70
[59]	$In_{0.18}Al_{0.82}N$ (15 nm)	Ti/Al/Ni/Au	700	0.39
[60]	GaN/$Al_{0.30}Ga_{0.70}N$/ AlN (10/22/1 nm)	Ti/Al/Mo/Au	850	0.26
[65]	AlGaN (22 nm)	Ti/Al/Ni/Au	820	0.15
[66]	GaN/$Al_{0.26}Ga_{0.74}N$ (2/18 nm)	Ti/Al/W	800	0.5

Table 3.3: Literature values of R_C for recessed contacts on different heterostructures.

with various results. A minimum in R_C has been found for recess depths around the 2DEG [51, 61, 62], when a large portion of the barrier was left [59, 63], and when the barrier was completely removed [60]. All in all, no clear conclusions regarding the optimum recess depth are easily drawn from the literature, perhaps because recess depth is not the only critical parameter. In paper [A] a parameter study was performed, varying the recess etch depth and anneal temperature using a Ta/Al/Ta metal stack with different thicknesses of the bottom Ta layer. This was done on an InAlN/AlN/GaN heterostructure with the lowest R_C (0.14 Ωmm) achieved for a recess etch which almost removed the whole barrier. Table 3.3 contains values of R_C achieved using recessed contacts. Generally, the anneal temperatures are lower for recessed contacts compared to the planar contacts. Not only do the contacts presented in paper [A] have a comparably low anneal temperature, the R_C is also close to state of the art, even compared to regrown contacts.

From a reproducibility perspective it is interesting to note that in paper [A] a low R_C was achieved also for deeper etches, as seen in Fig. 3.3a. For recess depths close to the barrier thickness, a very stable etch-



(a) (b)

Figure 3.3: A plot of (a) R_C and (b) R_{sh} versus etching depth using a bottom Ta thickness of 5 nm in paper [A]. The plot is constructed from the optimum anneal condition for each recess etch depth. The 2DEG position is indicated with a dotted line.

ing process is required to get reproducible contacts. Furthermore, even for small changes in the barrier design re-optimization of the etching time is necessary. A method to increase the reproducibility of recessed contacts could be to make a deep recess, well past the barrier layer. Ideally, this would remove the etching depth as a critical parameter and changes in the barrier layer would not affect R_C. This concept was further investigated in a Master's thesis [67]. In this work, the idea was to investigate the dependence of R_C on recess sidewall slope (α in Fig. 3.2) for deeply etched contacts. This was achieved through a new plasma etching process and control of the resist profile. Using a simple model, it was calculated that a near vertical etch would be ideal, although no experimental data supporting this was found. Further studies in this area are ongoing.

Another interesting property of the deeply etched contacts in paper [A] was the decrease in R_{sh} seen in Fig. 3.3b. A possible explanation is that the removal of the barrier under the contacts decreased a compressive strain in the heterostructure between the contacts. This would give a larger total polarization in this section which would increase n_s in the 2DEG [7].

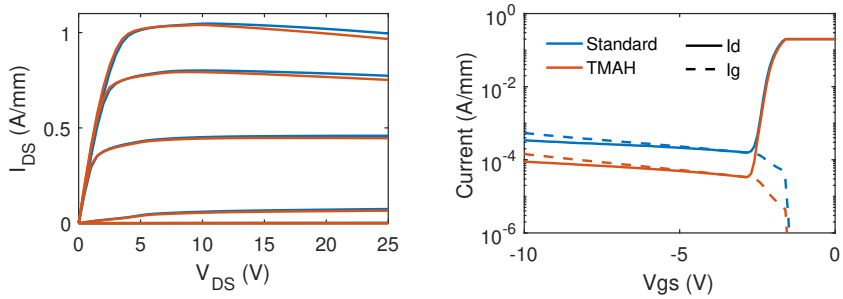
3.3 Device isolation

For MMIC applications electrically isolating devices from each other is of high importance. Generally, two different approaches to achieve de-

vice isolation on GaN heterostructures are available. By etching mesas to define the active regions the only device-to-device current path available is through the highly resistive buffer or surface states along the way. Alternatively, high energy ion implantation can be used to damage the crystal and in so increase the resistivity. Both mesa etching and ion implantation has shown low device-to-device leakage [60, 68, 69]. However, lower gate-leakage is expected for ion implantation since there is no risk of the gate metal directly contacting the 2DEG [70]. Furthermore, a flat surface may simplify further processing as the mesas might cause varying resist thicknesses or interference effects during lithography exposure. Nevertheless, mesa etching might be preferable since ion implantation may degrade at high temperatures [71, 72]. In this thesis, reasonable device-to-device isolation levels ($> 10^6$ Ωmm at 100 V for a separation of 5 μm) are achieved using mesa etching. However, this value can be significantly larger depending on the buffer resistivity.

Decreased gate leakage using TMAH An experiment was designed with the intention of decreasing the gate leakage currents for the mesa etched devices. The chemical tetramethylammonium hydroxide (TMAH) has previously been used to decrease leakage currents in various GaN-based devices [73, 74, 75, 76]. Generally, TMAH works as an weak etchant on GaN, although it mostly etches areas with crystal defects. It has been shown to remove plasma etching damages and making etched sidewalls more vertical [77], as well as removing the native Ga-oxide and dangling bonds on the GaN surface [76]. Therefore, TMAH could decrease the gate leakage by producing a more vertical mesa sidewall, minimizing the gate metal-to-2DEG contact.

TMAH was applied on the dry etched surface after mesa etching (step 2 in Fig 3.1). The etching was performed for 10 min in a TMAH solution of 25%, kept at 80 °C. Two identical chips were used from the Fe-doped wafer in paper [E]. The first chip was processed using the standard HEMT process described in section 3.1 (denoted Standard), the other chip was processed in tandem but was also etched in TMAH after the mesa etch (denoted TMAH). The output characteristics remained unchanged by the TMAH treatment, Fig. 3.4a. However, a decrease in the gate leakage current by a factor of 5 was measured in the transfer characteristics, Fig. 3.4b. Most probably, this was due to a more vertical mesa sidewall, but could also be related to removal of current conducting surface states. In any case, TMAH treatment shows de-



(a) (b)

Figure 3.4: (a) output and (b) transfer characteristics for samples with and without TMAH treatment. In (a) V_{GS} = -4:1:1 V and in (b) V_{DS} = 10 V. Note that a current compliance corresponding to 0.2 A/mm has been used in (b).

creased gate leakage with no obvious side-effects. The approach should be easy to include in any mesa isolation process.

3.4 2DEG mobility enhancement

Electron mobility is intrinsically high in the 2DEG due to the separation of the electrons and the ionized donor atoms. At room temperature (RT) several scattering processes contribute to the total mobility, although optical and acoustic phonons usually have the largest impact [78]. The phonon scattering is highly temperature dependent and their importance can be decreased by lowering the temperature. Other important processes are scattering due to interface roughness, alloy disorder scattering, and scattering at dislocations [79], which are all temperature independent processes. The relative importance of each process can be studied by varying the temperature or n_s and fit the resulting mobility changes to theoretical models for the scattering mechanisms [78, 79].

AlN exclusion layer A common method to increase the mobility of the 2DEG in GaN heterostructures is to include a thin (1-2 nm) AlN exclusion layer at the bottom of the barrier stack, see Fig. 3.5a. The large band gap of AlN is believed to limit the number of electrons penetrating into the barrier layer. The mobility in the 2DEG is then increased since a large prevalence of alloy disorder scattering is present

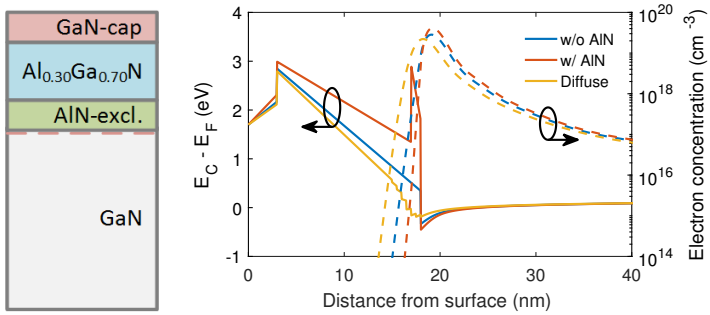


Figure 3.5: (a) Schematic illustration of barrier layer including an AlN-exclusion layer. (b) Simulated conduction band energies and electron densities for three AlGaN/GaN heterostructure with different AlGaN/GaN interfaces. The AlN layer is 1 nm thick and the diffuse interface changes Al-content from 0 % to 30 % over a distance of 3 nm.

in the barrier layer. Fig. 3.5b shows Poisson-Schrödinger simulations of AlGaN/GaN epi-structures with and without an AlN exclusion layer. As seen, the electron concentration extends further in to the barrier layer without the AlN exclusion layer. However, the inclusion of a high band gap AlN layer may inhibit the formation of ohmic contacts [80, 81, 82]. Furthermore, controlling the exact thickness of the thin AlN layer is problematic and even small variations in thickness can have large implications on e.g. n_s and ohmic contact resistance (which is another reason for using deeply recessed ohmic contacts). Table 3.4 lists literature values of achieved electron mobility for AlGaN/GaN systems with and without AlN exclusion layers, to show typical values for both cases.

Optimized AlGaN/GaN interface Using an optimized growth process, a sharp transition from GaN to AlGaN has been achieved, increasing electron mobility without including an AlN exclusion layer [83]. This can enable lower R_C while maintaining a low R_{sh} in epi-structures without AlN exclusion layers. In paper [B] such a structure was compared to an unoptimized AlGaN/GaN structure. The band diagram of the unoptimized structure is visualized in Fig. 3.5a as a diffuse interface that changes Al-content from 0 % to 30 % over a distance of 3 nm. It was found that the increased electron mobility was due to a lower alloy

Ref.	Growth method	Barrier	AlN-excl.	Mobility (cm^2/Vs)	$n_s \cdot 10^{-13}$ (cm^{-2})
[28]	MOCVD	$Al_{0.22}Ga_{0.78}N$ 23 nm	2 nm	2300	1.0
[28]	MOCVD	$Al_{0.22}Ga_{0.78}N$ 23 nm	-	1600	-
[85]	MOCVD	$Al_{0.25}Ga_{0.75}N$ 29 nm	- nm	2200	1.1
[85]	MOCVD	$Al_{0.25}Ga_{0.75}N$ 29 nm	-	1300	0.9
[86]	MBE	$Al_{0.24}Ga_{0.76}N$ 30 nm	2 nm	1700	1.8
[86]	MBE	$Al_{0.24}Ga_{0.76}N$ 30 nm	-	1300	1.2
[83]	MOCVD	$Al_{0.17}Ga_{0.83}N$ 28 nm	2 nm	2200	0.8
[83]	MOCVD	$Al_{0.17}Ga_{0.83}N$ 28 nm	-	1700	0.6

Table 3.4: Literature values of room temperature 2DEG mobility and carrier concentration together with barrier design. All epi-structures have been grown on SiC substrates.

disorder scattering at the sharp interface. Furthermore, it is shown that in the unoptimized structure the electrons penetrate in to the barrier layer in a larger degree, leading to increased C_{gs} (extracted using the model in [84]) and increased dispersion at large drain bias. It is possible that the increased mobility seen in samples with an AlN exclusion layer is not only due to the large band gap of AlN increasing confinement. It could also be related to an improved interface quality created by the large difference in growth settings between GaN and AlN growth. It is worth noting that the mobility achieved in the optimized structure in paper [B] was lower than expected. This was due to the growth process being optimized for a different substrate size than what was used in paper [B]. In an optimized growth process, the sharp interface can yield a mobility greater than 2200 cm^2/Vs [83].

Chapter 4

Buffer design and characterization

For their intended applications GaN HEMTs are required to be able to operate at high frequency and deliver a high output power. Furthermore, a high reliability is of large importance. The buffer design can have a large effect on these properties. For a leaky buffer the reliability is expected to decrease [87], and high operating frequencies cannot be achieved if the buffer does not confine the electrons, limiting short channel effects [88]. Lastly, dispersion due to traps in the buffer can severely limit the output power, and time-variant effects, such as charging and discharging phenomena, is a major concern for large-signal applications.

Unintentionally doped GaN in usually n-type due to the large incorporation impurities during growth. Therefore, compensation doping is required in order to increase the resistivity of the GaN buffer and fulfill the requirements listed above. In these structures a trade off between low leakage and low dispersion has to be made since the compensating dopants are a large source of trapping centers. Field plates can reduce the effect of buffer traps by reducing the peak electric field [27]. However, the trapping cannot be completely removed since the compensating atoms are required in order to reduce the buffer leakage. A possible alternative to compensation doped GaN buffers is the use of back barriers. In this case the bottom confinement is achieved by the means of an energy barrier. Ideally, this would remove the need for compensation doping and a device free of buffer dispersion could

be achieved. However, due to limitations in achievable material quality this is not the case in practice.

This chapter deals with the two main approaches of buffer design described above; compensation doped GaN and back barriers. First, a brief introduction to trap characterization through drain current transient measurements is given in section 4.1. In section 4.2 compensation doping of GaN buffers is discussed. Of particular interest are C-doped buffers and therefore a more detailed analysis of these is given, based on the results presented in the appended papers [C], [D], and [E]. Fe-doping is also considered since this is the current industry standard for microwave HEMTs. Section 4.3 describes the use of back barriers, their associated advantages and disadvantages. Also included is previously unpublished work on epi-structures utilizing back barriers. The results are used as a basis for discussion regarding design choices associated with back barriers. Following this, a new type of epi-structure, utilizing a thin buffer, is briefly discussed in section 4.4. This structure does not require compensation doping and is using the AlN-exclusion layer as a type of back barrier. Lastly, the different buffer designs are evaluated in terms of achievable output power in section 4.5.

4.1 Trap characterization

Trap characterization is an important tool for understanding and improving GaN HEMT devices. The characterization can have two goals; understanding what is causing the trapping or understanding the traps' effects on device performance. Commonly, pulsed-IV is used for trap characterization in GaN HEMTs. In this method, both V_{GS} and V_{DS} are pulsed from a quiescent, trap filling bias point to an active bias point where the current is measured. This method can quantify the effects of trapping to a certain degree but gives less information of the actual trapping mechanisms. Other methods that are commonly used are deep-level transient spectroscopy (DLTS) and photoluminescence, both of which mostly focus on understanding what are causing the trapping effects. The drain current transient (DCT) technique, which is explained below, can capture both aspects but is in this case mostly used for understanding the underlying defects creating the traps.

Surface reactions with atmospheric moisture The surface passivation should not only prevent electron trapping on the surface, it should also preserve the surface when exposed to different atmospheres

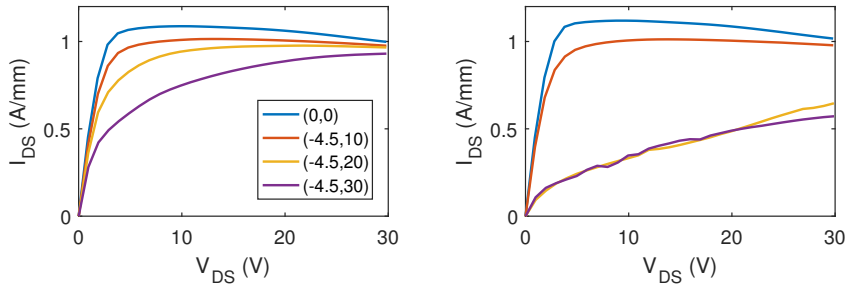


Figure 4.1: Pulsed-IV measurements performed on the same device in (a) nitrogen atmosphere, and (b) air atmosphere. Four different quiescent bias points are used (V_{GSQ},V_{DSQ})

and protect from other contaminants. For example, atmospheric moisture might oxidize the surface with the aid of large electrical fields [89, 90]. In this thesis, similar effects have been observed for devices with SiN passivation. In Fig. 4.1 results from pulsed-IV measurements on the same device in different atmospheres are shown. In N_2 atmosphere the current decreases in an expected way with increasing quiescent drain bias. However, in air ambient almost total current collapse is measured for the two highest quiescent drain biases. In these cases it is believed that the large electric field enables moisture from the atmosphere to penetrate at the metal-SiN interface on the gate and drain edges. The moisture reacts with the surface of the barrier, changing the local electrical potential and in so the number of carriers in the 2DEG. This process seems to be reversible since the behavior in Fig. 4.1a is recovered after re-introducing a N_2 ambient. Therefore, the buffer trap characterizations have been performed in a N_2 ambient to prevent these effects from interfering with the measurements.

DCT-analysis The main trap characterization method used in this thesis is the drain current transient (DCT) technique. In this, the transistor is kept at a high stress bias point for a period of time, allowing traps to be filled. Following this, the bias is quickly switched to a low stress point, where the drain current is monitored for an extended time. When electrons are emitted from the traps, an increase in the drain current is observed. Depending on which high stress bias point is

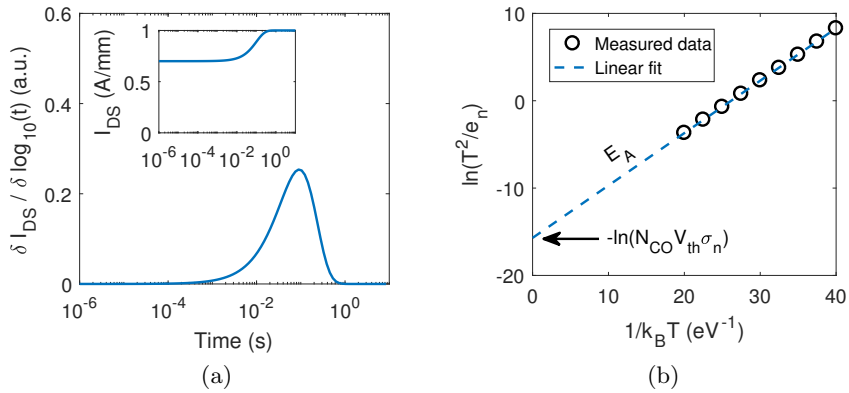


Figure 4.2: (a) An example of a DCT measurement showing a single trap level with a time constant of 0.1 s. (b) Depiction of the extraction of the activation energy (E_A) and the capture cross section (σ_n) from an Arrhenius plot.

chosen, traps in different regions of the transistor can be filled. Using a large drain bias with the gate pinched is believed to mostly fill traps in the buffer region [91]. An example of a DCT measurement with a single trap level can be seen in Fig. 4.2a. From the measurement data the trap time constant can be extracted by fitting the following equation;

$$\frac{I_{DS}}{I_{DS,q}} = 1 - \sum_{i=1}^{N} \alpha_i \cdot \exp\left(-\frac{t}{\tau_i}\right)^{\beta_i}. \tag{4.1}$$

This model has been found to give the most accurate results for extraction of time constants [92]. Here, $I_{DS}/I_{DS,q}$ is the drain current normalized by the quiescent drain current, α_i is the amplitude of the trapping effect, τ_i is the trapping/de-trapping time constant, β_i is the stretching term and N is the number of traps. The stretching term can give additional information regarding the defect responsible for the trap level. For a point defect $\beta = 1$ and a standard exponential behavior is measured. However, for more complex emission processes β can be less than 1. For example, a small β has been related to the trapping/de-trapping kinetics being governed by hopping [93], or tunneling [94]. A small β has also been connected to the trapping centers forming a continuous distribution of energy levels rather than a discrete level [95].

Arrhenius behavior To characterize traps it is useful to extract their activation energy (E_A) and capture cross sections (σ_n). For a trapped electron being emitted to the conduction band through a thermally activated process the emission rate is given by;

$$e_n = \sigma_n v_{th} N_C \cdot \exp(-E_A/k_B T). \tag{4.2}$$

Here, v_{th} is the thermal velocity, N_C is the effective density of states in the conduction band, k_B is Boltzmann's constant, and T is the absolute temperature. E_A and σ_n can be extracted by performing DCT measurements at different temperatures and extracting e_n to construct an Arrhenius plot, as seen in Fig. 4.2b. In the Arrhenius plot $ln(T^2/e_n)$ is plotted versus $1/k_B T$. Using Eq. (4.2), $\ln(T^2/e_n)$ can be re-written as;

$$\ln\left(\frac{T^2 exp(E_A/k_B T)}{(T^2 N_{C0})\sigma_n v_{th}}\right) = E_A/k_B T - \ln(N_{C0}\sigma_n v_{th}), \tag{4.3}$$

where N_{C0} is the temperature independent part of N_C. When plotted versus $1/k_B T$ a line ($y = kx+m$) with $k = E_A$ and $m = -\ln(N_{C0}\sigma_n v_{th})$ will be obtained. σ_n can then be calculated since N_{C0} and v_{th} are known for GaN. Specific defects can be identified using E_A and σ_n since these should be unique. A compilation of E_A and σ_n for several traps found in GaN and their assumed origin can be found in [92].

Characterization of extended defects Point defects in semiconductors do not interact with each other, making each filled trap's emission time well described by Eq. (4.2) using a single E_A and σ_n. For extended defects the behaviour is more complex. Firstly, trapped electrons at an extended defect may change the local potential and in so change to effective capture cross section of the trap center [96]. Secondly, trap states along extended defects may have capture cross sections varying over several orders of magnitude [97]. These effects can be investigated through DCT measurements by varying the time spent in the trap filling bias condition (filling time variation). For longer filling times, traps with smaller σ_n may be trapped, leading to a large variation in the DCT signature for different filling times. In a sense, these measurements are similar to DLTS, although the DCT measurements is more versatile since both the gate and drain voltages can be changed in order to stress different areas of the device. The theory described above is the basis for the DCT analysis performed in paper [E]. For

further reading on the DCT technique [92] and [98] are highly recommended.

4.2 Compensation doped GaN

Due to the large band gap of GaN the intrinsic carrier concentration is very low ($\sim 10^{-10}$ cm^{-3}). However, as a result of the high growth temperatures, unwanted material from e.g. the growth chamber or substrate give large concentrations of impurities in the crystals. Two common impurities are Si and O, both of which are shallow donors in GaN [99]. Consequently, unintentionally doped (uid) GaN is often n-type. As explained in chapter 2.2 this is an issue for HEMT devices since the electrons in the 2DEG needs to be confined to minimize short channel effects and buffer leakage [88]. Hence, the excess electrons needs to be decreased in order to increase the resistivity of the buffer.

GaN buffers were initially rendered highly resistive by introducing a high density of defects in the buffer, but this also reduced the crystal quality in the 2DEG region, leading to decreased mobility [86, 100]. Currently, compensation doping using deep acceptors is the standard method to achieve high resistive buffers. In this method the compensation atoms can be minimized close to the barrier, maximizing n_s and μ in the 2DEG. The two most commonly used acceptors are Fe and C, which will be described more in detail in the following paragraphs. Other dopants forming deep acceptors in GaN are for example magnesium [101] or beryllium [102], but these are rarely used in HEMT devices.

Fe-doped GaN buffers

Fe-doped buffers are the current industry standard for microwave GaN HEMTs due to their high resistivity and high associated output power. To grow Fe-doped GaN using MOCVD, the Fe atoms need to be introduced in the growth chamber using a precursor. From a growth perspective, an advantage of Fe-doping is the large process window, giving a stable, reproducible growth process [103]. A disadvantage is the growth related memory effect which makes rapid transitions from high to low Fe-concentrations difficult to achieve. This is due to Fe segregating on the GaN surface during growth. Once the Fe-precursor has been turned off the remaining Fe on the surface will be incorporated with an exponential tail in the subsequently grown GaN [104].

Fe-doped GaN commonly shows a Fermi level pinning of around 0.6 eV below the conduction band [105, 106]. However, this level is not believed to be related to Fe in itself, but rather that the presence of this level is enhanced by the Fe-incorporation [107]. The actual Fe-level is believed to be located deeper in the energy band [108]. The 0.6 eV level is regularly seen in devices with Fe-doped buffers, leading to increased on-resistance and reduced drain current. Furthermore, this level has a room temperature emission time in the millisecond range. Therefore, it can have a large performance impact in applications that are sensitive to transient effects [109].

Microwave HEMTs with Fe-doped buffers Compared to unintentionally doped buffers, Fe-doping has been found to limit the achievable output power [110]. However, a low Fe-concentration has been found to decrease short-channel effects while maintaining a high output power [111]. The highest reported output power for GaN HEMTs have been achieved using an Fe-doped buffer (40 W/mm at 4 GHz under pulsed conditions) [26]. However, the exceptional result is mostly attributed to field plate optimization and no mention of reliability is made for these extreme operating conditions. An interesting approach to the growth related memory effects is presented in [112]. Here, a thin uid GaN channel is grown on a free standing Fe-doped GaN substrate, ensuring a rapid transition from high to low Fe-concentration. This results in 9.7 W/mm output power at 10 GHz, although in this case the excellent results should probably rather be attributed to the improved crystal quality and heat transport enabled by the GaN substrate rather than the Fe-doping profile.

Overall, Fe-doped GaN buffers are not as frequently investigated as C-doped buffers. This is probably due to Fe-doping suffering from fewer issues compared to C-doped buffers but also since C-doping is common in the commercially larger field of power electronics. As a result, the behavior of Fe-doped buffers in microwave applications can be predicted rather well whereas the underlying mechanisms are not as well understood. In this thesis, only one Fe-doped epi-structure has been reported (in paper [E]), grown by Cree Inc.. The purpose of this sample was to benchmark the HEMT process on an industry standard epi-structure. Generally, it offered a good trade off between dispersive effects and leakage. However, it also suffered from the characteristic 0.6 eV level which introduced knee-walkout effects and current collapse, and in so

reducing the achievable output power. Clearly, even though Fe-doped buffers generally give the best performance in microwave applications, problems still remain.

C-doped GaN buffers

Highly C-doped GaN generally offers a higher resistivity compared to Fe-doped GaN [113]. Therefore, C-doped buffers are most commonly used in power applications in which a highly resisitve buffer is crucial in order to enhance the breakdown voltage [114]. In this thesis, C-doped buffers have been investigated for microwave applications, where a lower C-concentration is generally required due to the lower operating voltages. One of the advantages of C-doping is that it does not suffer from the same memory effects as explained for Fe incorporation. Instead, rapid changes from high to low C-concentration are readily achievable. For GaN films grown with MOCVD, the C-concentration may be controlled by managing the incorporation of residual C in the chamber. The residual C mainly originates from the Ga precursor (trimethyl gallium) and the incorporation rate is most commonly controlled by varying the growth pressure or temperature. Generally, at low pressure and at low temperature the C incorporation increases [115]. However, the same growth conditions can also lead to a degraded crystal quality, with increased presence of dislocations [116, 117]. This gives a trade off between high C-concentration and high crystalline quality. It is possible to avoid these issues by incorporating C using a C-carrying gas. For example, this was done in paper [a] using propane. In this case the growth settings can be optimized for high quality GaN and the C-concentration can be controlled by changing the flow rate of the C-precursor.

Incorporation of C in the GaN crystal Depending on growth conditions, C may be incorporated in a number of different places in the GaN crystal [118]. From physical simulations it has been found that when C is substituted with a Ga atom (C_{Ga}), a shallow donor in the conduction band is formed [119]. When C is substituted for an N atom (C_N), a deep acceptor state $\sim$0.9 eV above the valence band maximum is formed [120]. C may also be incorporated in an interstitial position. Although, among these configurations C_N is the most energetically favourable for most growth conditions [120]. It is also the C_N configuration that is believed to be responsible for the increased resistivity observed for C-doped GaN layers, where the deep

acceptor level works as a compensation dopant [108]. However, the exact mechanisms are still not fully understood.

The ideal conditions examined in physical simulations generally do not account for defects, which are always present in real samples. These defects can form separate energy levels [121], or even change the incorporation of C in the crystal. For example, dislocations commonly functions as attractors of defects in semiconductor materials [122]. This means that other impurities are accumulated at the dislocation. The process is called gettering and can be used to "clean" semiconductors of unwanted dopants. Gettering of impurity atoms to dislocations has also been reported for GaN [33, 123]. In these cases the impurity atoms are decorating the dislocations, forming states and changing the charge of the dislocation cores [123]. As proposed in paper [E], to fully control the incorporation of C in the GaN crystal, residual C-doping is probably not a feasible option since many variables are changed when changing C-concentration. From this perspective extrinsic C-doping is more promising since the general growth conditions and the C-incorporation are easier to separate.

Highly C-doped GaN buffers For power applications, high C-concentrations ($\sim 10^{19}$ cm^{-3}) are required in order to limit breakdown [114]. At these C-concentrations GaN has been shown to become p-type [124]. This can have large implications on dispersion in HEMT structures [125, 126]. The problem arises due to a pn-diode formed between the p-type GaN and the 2DEG channel region. For fast switching from large to small drain biases, electrons can get trapped in the p-type region, effectively forming a back-biased pn-diode. In this case, the trapped electrons have no obvious way of returning to the 2DEG due to the electrostatic barrier. It has been argued that dislocations could form a leakage path through the pn-diode barrier for the trapped electrons [127]. This has been partially verified in experiments with devices of different surface area [128]. Here, smaller devices display larger dispersive effects and a larger device-to-device spread compared to larger devices. This is attributed to a lateral charge transport mechanism that is highly localized and distributed with a ~ 100 μm scale of separation. The large distance excludes dislocation as a possible candidate for these vertical leakage paths since these are much more abundant. However, as discussed in [33], dislocations can getter C from the surrounding GaN, forming a C-depleted region around itself. When two disloca-

tions are close to each other a "deep carbon depletion"-region may be formed, drastically decreasing vertical breakdown. Possibly, the same mechanism could be responsible for the behavior found in [128] since the separation of the "deep depletion"-regions were found to be around 10 μm.

Moderately C-doped GaN buffers The theories on trapping mechanisms in HEMTs using highly C-doped, p-type, GaN are indeed interesting. However, for microwave HEMTs (the topic of this thesis) vertical breakdown is rarely an issue so lower C-concentrations are generally used. In [113] it was found that GaN shifted from n-type to p-type at a C-concentration of $1.6 - 2.9 \cdot 10^{18}$ cm^{-3}. In a general GaN sample the shift from n-type to p-type should not only depend on the C-concentration but also on the background impurity levels. For lower Si and O impurity levels a lower C-concentration is required in order to render GaN p-type.

Fermi level position in moderately C-doped GaN Kelvin probe force microscope (KPFM) measurements (similar to those in [113]) have been used to estimate the Fermi level's position in a typical C-doped buffer used in this thesis. The GaN layer has been doped using a residual process to a C-concentration of $1 \cdot 10^{18}$ cm^{-3}. An Fe-doped sample was also measured for comparison. The Fe-concentration is in this case unknown due to the proprietary doping process. However, the Fe-doped sample is still interesting as a reference considering the Fermi level in Fe-doped GaN is usually pinned at 0.6 eV below the conduction band. The samples were cleaned using diluted (1:10) HCl and HF solutions to remove potential surface oxides. A Ti/Au-stack (5/100 nm) was deposited directly on the surface. This metal stack has been shown to have a work function of 4.95 eV [129], thus providing a reference potential value. KPFM scans were performed across the edge of the deposited metal, including both the GaN and metal surfaces in a single scan, Fig. 4.3. This way the potential difference between the metal and the GaN layer can be measured. The Fermi level position is calculated using the following equation;

$$\Delta E_F = \phi_{Ti/Au} + e\Delta V - \chi_{GaN} - \Delta\phi. \tag{4.4}$$

Here, ΔE_F is the Fermi level to conduction band distance, $\phi_{Ti/Au}$ is the work function of the metal stack (4.95 eV), e is the electron charge,

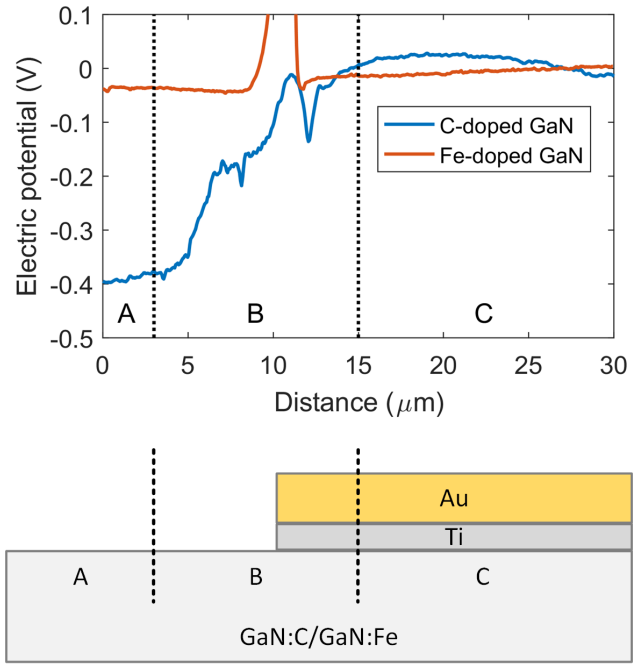


Figure 4.3: Kelvin probe force microscopy scans on C- and Fe-doped GaN.

ΔV is the measured potential difference between the GaN surface and the Ti/Au metal stack, χ_{GaN} is the electron affinity of GaN, and $\Delta\phi$ is the net band bending caused by surface or dipole charges. From [113]; $\chi_{GaN} = 3.5$ eV for a cleaned surface and $\Delta\phi = 0.4$ eV for semi-insulating GaN. Fig. 4.3 gives a ΔV of roughly -0.4 V for the C-doped sample and -0.05 V for the Fe-doped. This results in a Fermi level position 0.65 eV and 1 eV below the conduction band for the C-doped and Fe-doped GaN respectively. In a hand waving argument, 0.4 eV can be taken a rough uncertainty in the measurement since a value of 0.6 eV is expected for the Fe-doped sample. Regardless, it is clear that the C-doped GaN is more n-type than the Fe-doped GaN in this case. This was also confirmed in mesa isolation measurements where the Fe-doped buffer offered 20 times lower leakage currents at 200 V.

C-doped buffers for microwave applications In the literature only a handful of studies have investigated the use of C-doped buffers for microwave applications [130, 131, 132, 133]. In these it is not verified

whether the GaN buffer is p-type or n-type. For C-concentrations low enough to form n-type GaN (moderately C-doped GaN) no pn-diode should exist between the GaN buffer and the 2DEG. Consequently, a different trapping behavior than described for highly C-doped GaN buffers could be expected. Using the results from the KPFM measurements and what was found in [113], a reasonable assumption is that C-concentrations $\leq 1 \cdot 10^{18}$ cm^{-3} should give n-type GaN. From the references this leaves [130] and [132]. In both of these cases a clear reduction in output power is measured for increasing C-concentration in the buffer. However, no deeper analysis on the origin of the trapping effects have been performed.

One of the advantages with C-doped buffers is the possibility to tailor the doping profile with a high precision. In paper [C] this was used to develop a stepped C-profile, with low C-concentration in vicinity of the 2DEG and a high concentration deep in the buffer. The stepped profile (Stepped:C) was compared to an unintentionally doped sample (Low:C) and a sample with a constant, high C-concentration (High:C). The exact doping profiles are shown in Fig.4.4. The C-concentrations in the three samples are expected to give n-type GaN. The three epi-structures were evaluated with respect to leakage and dispersion. Figures of merit such as drain induced barrier lowering (DIBL) and dynamic R_{ON} were extracted. DIBL is a measure of how much the pinch-off voltage shifts with increasing V_{DS} and give a measure of confinement. Pulsed-IV measurements were used to extract the dynamic R_{ON} as the increase (in %) between the quiescent bias points (V_{GSQ},V_{DSQ}) = (0,0) and (-6,15) V. It was found that the stepped C-profile gave a good trade off between short channel effects, leakage, and dispersion, as indicated by a low value of DIBL (1.2 mV/V) and dynamic R_{ON} (35 %). Corresponding values for High:C and Low:C were 0.1 mV/V and 750 %, and 22.4 mV/V and 10 % respectively. Even though an extensive trapping analysis was performed, no clear results regarding the origin of the C-induced trapping was found.

Buffer traps in n-type, C-doped GaN The work in paper [C] was continued in paper [E]. A more thorough trap characterization was performed in order to understand which trapping centers are important in n-type, C-doped buffers. Here, two C-doped epi-structures were investigated, Stepped:C and Exp:C (see Fig. 4.4 for exact profiles). Low:C from paper [C] was also used to facilitate further discussion. Tem-

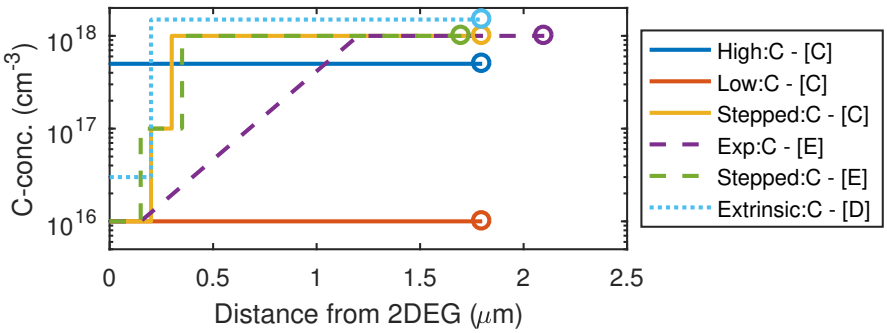
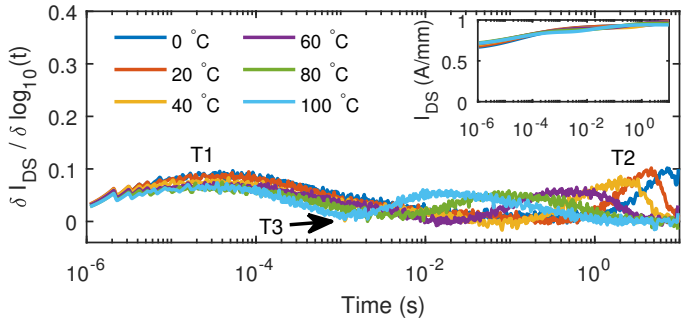


Figure 4.4: Doping profiles for the C-doped epi-structures presented in this thesis.

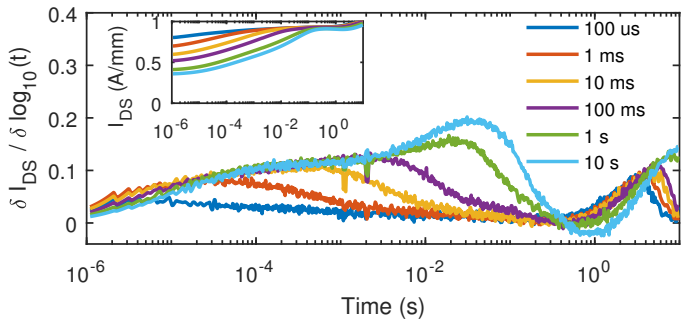
perature and filling time dependent DCT measurements were used to extract three traps, denoted T1, T2 and T3. The DCT measurements for Exp:C are presented in Fig. 4.5, where the three traps have been indicated at their respective peak. T1 had a room temperature (RT) emission time of ~ 50 μs, for T2 the RT emission time was ~ 5 s, and for T3 ~ 500 ms.

The processes responsible for the three traps are summarized in Fig. 4.6. T1 is associated with the largest current decrease and seems to be related to trapping at C-clustering around dislocations. This is supported by an increasing amplitude as well as a widening of the peak of T1 for longer filling times, indicating that the trap is due to extended defects. Furthermore, by comparing the amplitude of T1 between the three samples it is found to correlate with a high C-concentration. Additionally, gettering of C to dislocations is a well known effect in GaN [33]. The main current transport mechanism for T1 is believed to be hopping or tunneling as indicated by an activation energy close to 0 eV. In paper [E] it is proposed that a reduction of the dislocation density might be a way to reduce the impact of T1.

T2 and T3 only account for a few percent of the total current decrease but the mechanisms behind them are interesting. In a sense, the process is similar to the problems associated with the pn-diode present for high C-concentrations. The amplitude of T3 is negative and is believed to be related to hole emission from the C_N level. As indicated in Fig. 4.6, band bending will occur at the GaN/AlN-nucleation interface due to the polarization gradient present there. The band bending will create vacant C_N levels which can be filled by electrical stimulation, as



(a)



(b)

Figure 4.5: (a) Temperature and (b) filling time dependent DCT measurements for Exp:C from paper [E]. The high stress voltage was (V_{GS},V_{DS}) = (V_P-2,50) V and the low stress voltage was (1,7) V. A filling time of 1 ms was used in (a) and the measurements in (b) were performed at 20 °C.

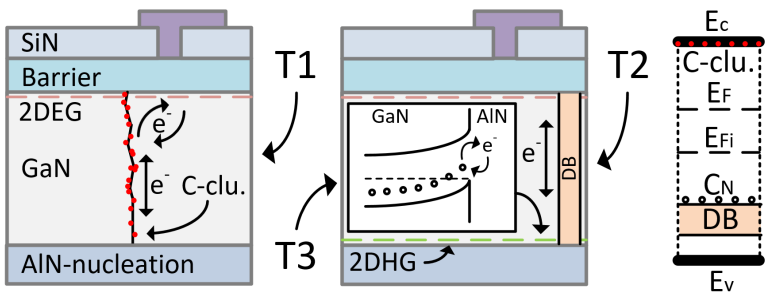


Figure 4.6: Schematic figure depicting the trapping processes of T1, T2, and T3. The band diagram shows the different trap levels (C-clusters (•), C_N (○), and defect band (DB)), as well as the intrinsic and approximate Fermi levels in our C-doped samples.

explained in [126]. The trapped electrons at the GaN/AlN interface are transported through the GaN buffer by means of the recently discovered defect band [121]. The leakage process is registered as trap T2 which has the same non-Arrhenius behavior as found in [121].

Extrinsic C-doping for a reduced dislocation density By controlling the C-concentration using a C-carrying gas, a lower dislocation density could be achieved for the same C-concentration. In this way, the importance of the T1 trap might be reduced. It is also possible that the different growth conditions could alter the gettering rate of the C atoms. An initial experiment using extrinsic C-doping is presented in paper [D]. In this paper, propane is used as C-carrying gas and the C-profile in Fig. 4.4 is achieved. The buffer supplied an excellent confinement resulting in a DIBL of 0.13 mV/V at $V_{DS} = 30$ V. However, large dispersive effects leading to knee-walkout, and thus limited output power, were also present. The C-concentration of Extrinsic:C was slightly larger compared to what was used in the residually doped samples in paper [E]. Probably, the larger C-concentration counteracted the lower dislocation density in this case. Another possibility is that the larger C-concentration rendered the GaN p-type, giving rise to the pn-diode related issues described for the highly C-doped buffers. Without further extrinsically doped samples to compare with it is difficult to draw any clear conclusions given the different growth conditions and C-profiles used in the two cases.

4.3 Back-barrier

A different way to increase the confinement is to introduce a back-barrier. The back-barrier is a high energy barrier that prevents the electrons from extending down into the heterostructure at larger drain biases. In this case the 2DEG has large energy barriers on both sides, sometimes called double heterostructure- (DH-) HEMT. To exemplify, the band diagram of an AlGaN/GaN/AlGaN structure, compared to a regular AlGaN/GaN structure, is shown in Fig. 4.7. In this particular case, the electron concentration decreases by $\sim 20\%$ by including the back-barrier. However, the confinement is increased, making it ideal for high frequency operation. This is also what the back-barrier is mostly used for in the literature. For example, the highest reported f_T and f_{max} for a GaN based HEMT has been achieved using an AlN/GaN/AlGaN heterostructure [2]. Several other devices showing impressive high fre-

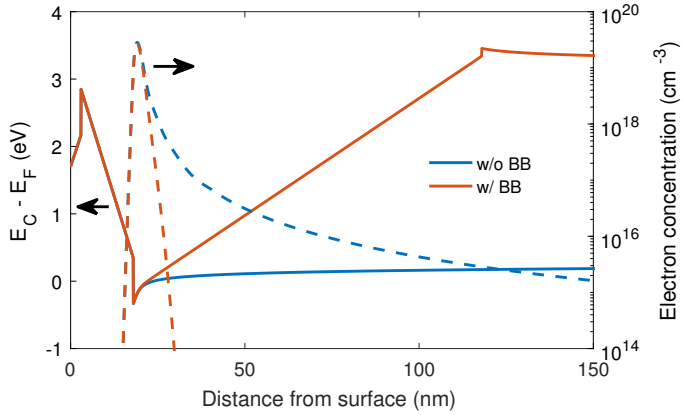


Figure 4.7: Simulated conduction band energies and electron densities for an AlGaN/GaN heterostructure with and without an $Al_{0.05}Ga_{0.95}N$ back-barrier.

quency performance using AlGaN or InGaN back-barriers have also been reported [52, 134, 135].

However, some drawbacks are also associated with the use of back-barriers. For example, $Al_xGa_{1-x}N$ has a significantly lower thermal conductance compared to GaN and AlN. This is attributed to an increase in phonon scattering caused by the increased disorder in the crystal [6]. Therefore, devices with $Al_xGa_{1-x}N$ back-barriers often show an obvious decrease in drain currents at large dissipated power [134, 136, 137]. The effective thermal conductance can be increased by thinning down the back-barrier layer and growing a GaN buffer underneath (as explained in Chapter 2 the whole epi-structure still needs to be roughly 2 μm thick in order to get a good crystal quality). However, this can introduce a parasitic channel in the interface between the AlGaN back-barrier and the GaN buffer. If this design is chosen the parasitic channel is usually removed by introducing deep acceptors in the GaN buffer [131, 138].

In theory, the back-barrier structure should be able to minimize trapping effects since no deep acceptors are required to get a good confinement. However, the $Al_xGa_{1-x}N$ ternary alloy is intrinsically more difficult to grow with a high crystal quality [139]. As described above, crystal defects can also contribute extensively to trapping effects. Furthermore, even though dopants are not required, the background doping for AlGaN is usually higher compared to GaN growth [140]. Generally,

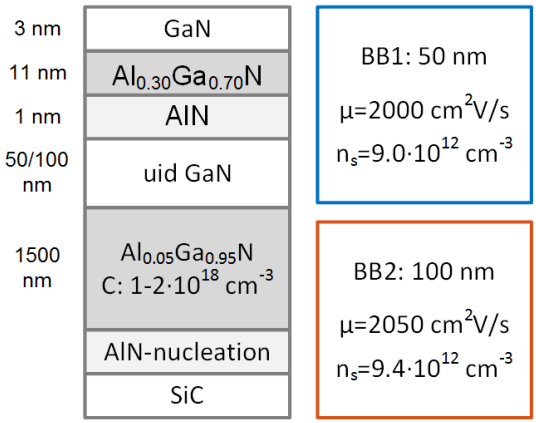


Figure 4.8: The epi-structure designs and measured electron concentration and mobility of the two back barrier materials.

trapping in devices utilizing back barriers has not been as extensively investigated as for compensation doped GaN buffers. Therefore, important trapping centers in back barriers are difficult to find in the literature.

Back barrier materials in this thesis HEMTs on epi-structures with AlGaN back-barriers were processed in order to gain further knowledge of important trapping effects. The devices were the first try on back barrier structures with the main idea to investigate the effect of the uid GaN channel thickness on different performance figures. Two epi-structures with designs described in Fig. 4.8 were used. BB1 had a uid GaN thickness of 50 nm and BB2 100 nm. A large C-concentration in the AlGaN back-barrier was included to suppress leakage through this layer. Although, in hindsight, these values are probably too large. Regardless, the GaN channel thickness did not affect the 2DEG significantly and both structures showed reasonable values of sheet carrier density and a high electron mobility, Fig. 4.8.

DC-characteristics DC-characteristics were measured on devices with $L_G = 100$ nm in order to verify the functionality of the HEMTs. The saturated drain current (I_{DSS}, I_{DS} at $V_{GS} = 1$ V) was 0.6 A/mm and 0.8 A/mm for BB1 and BB2 respectively. Comparing to a regular AlGaN/GaN structure with similar 2DEG properties this current

is lower than expected. This could be due to the back-barrier limiting the band bending in the uid GaN region. This would also explain the lower current in BB1 since this sample has a thinner GaN channel. The maximum transconductance (g_m) was around 350 mS/mm in both samples even though BB2 had a larger current. This was a result of the lower pinch-off voltage in BB2 (-2.0 and -2.5 V for BB1 and BB2 respectively). Overall, BB1 and BB2 were found to function properly although their performance were worse compared to a regular AlGaN/GaN epi-structure without back barrier.

Trapping evaluation Filling time dependent DCT measurements were performed to investigate trapping effects, see Fig. 4.9. An off-state voltage of (V_P-2,30) V was used in order facilitate complete current recovery after 10 s. The DCT signatures of both BB1 and BB2 shared similarities with the C-doped samples discussed above. A fast time constant, similar to T1, with a large dependence on filling time was present in both samples. A slow time constant was also registered. However, for the slow time constant no dependence on filling time was found. With the discussion regarding the C-doped buffers in mind, it seems likely that the fast time constant is related to trapping at dislocations. The origin of the slow trap is more difficult to explain, although it is less important in terms of associated current decrease. Comparing BB1 to BB2 the current decrease is obviously much larger in BB1. This most likely means that the dislocations responsible for the trapping is located in the back barrier since this is closer to the 2DEG in BB1. Since the back barrier is C-doped it is possible that the same C-clustering as discussed for C-doped GaN buffers is present also in these structures.

4.4 Thin buffer

Many of the problems associated with both compensation doped GaN buffers and back barriers are due to the fact that the buffer needs to be grown to a thickness of around 2 μm. If a high quality GaN layer could be achieved for a much lower thickness, the AlN-nucleation layer would function as a back-barrier and no compensation doping would be required. Furthermore, growth times would be decreased leading to reduced epi-wafer costs. However, worse thermal behavior could be expected due to the smaller separation between the device and the high thermal boundary resistance of the AlN-nucleation layer [141]. Using

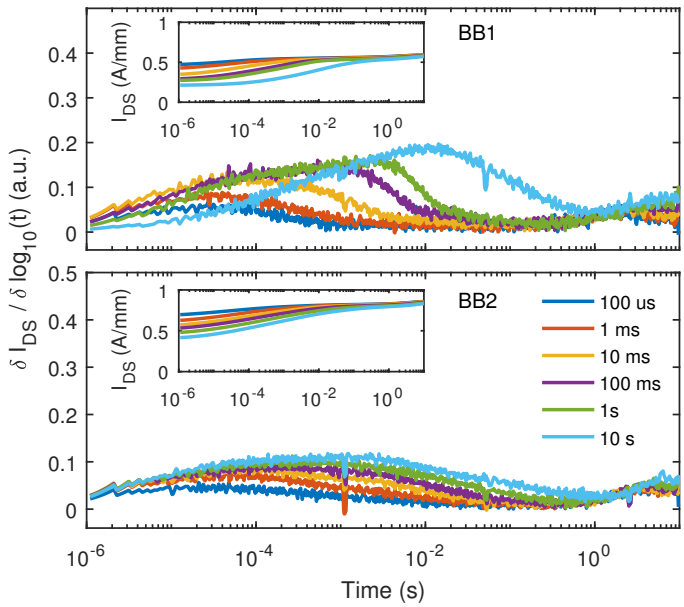


Figure 4.9: Filling time dependent DCT measurements for devices with back barriers. The off-state voltage was (V_{GS},V_{DS}) = (-4.5,30) V and the on-state voltage was (1,7) V.

a thin GaN buffer has previously been investigated with poor results [142, 143, 144]. In these cases the low crystalline quality impede the HEMT performance significantly. However, using an optimized AlN-nucleation process [5], thin HEMT structures of high quality have been achieved in this thesis. The epi-structure design is presented in Fig. 4.10. For an epi-structure with a 200 nm thick GaN layer excellent values of μ and n_s were measured (2050 cm^2/Vs, $1.1 \cdot 10^{13}$ cm^{-2}) using van der Pauw structures, showing no indication of low crystalline quality around the 2DEG. HEMT devices were fabricated in order to evaluate the performance also for larger electric fields.

DC-characteristics The output characteristics are presented in Fig. 4.11a. The low on-resistance was achieved through a combination of low R_{sh} and low R_C (0.3 Ωmm). No short channel effects are present, as indicated by an extracted DIBL of 1.0 mV/V at 27 V. This value can be compared to 1.2 mV/V for a C-doped buffer with ~ 2 μm thick buffer (paper [C]). Furthermore, the thermal performance does not

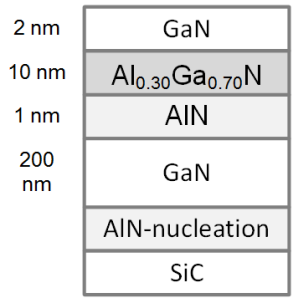


Figure 4.10: Design of the thin HEMT epi-structure.

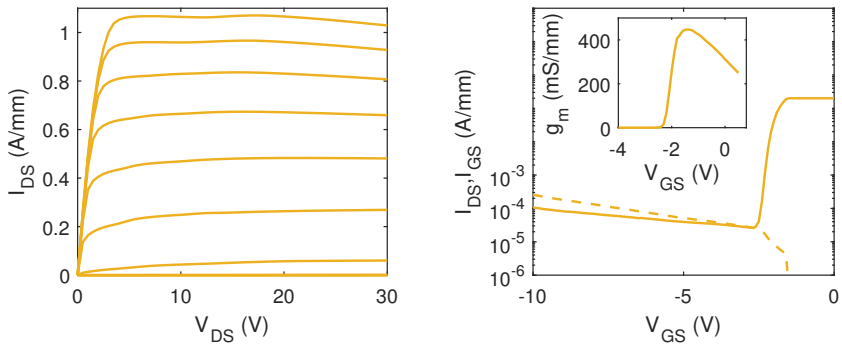
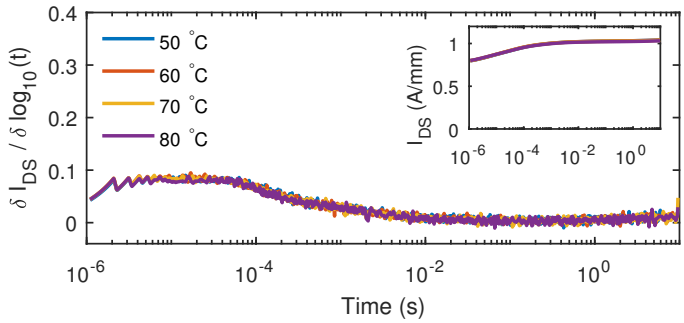


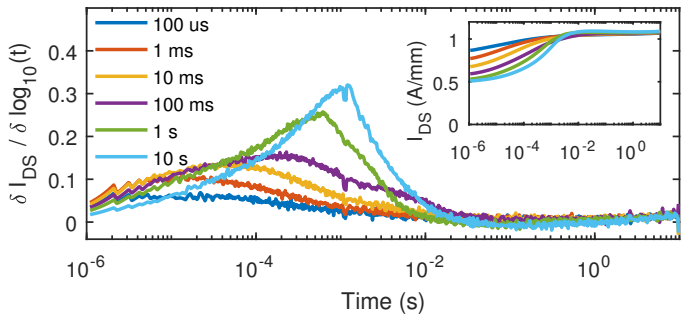
Figure 4.11: Output (a) and transfer (b) characteristics measured for devices with $L_g = 200$ nm. In (a) $\Delta V_{GS} = 0.5$ V and the largest current is measured for $V_{GS} = 1$ V. In (b) the solid line is I_{DS} and the dashed line is I_{GS}, the measurements are performed at $V_{DS} = 10$ V.

seem to be severely degraded by the thin GaN buffer. In the transfer characteristics a clear pinch-off behavior and a large transconductance (450 mS/mm) are found, Fig. 4.11b. For compensation doped buffers using the same barrier design the transconductance is usually closer to 400 mS/mm (paper [E]).

DCT evaluation An extensive DCT evaluation was performed in order to identify important trapping processes. Temperature dependent DCT measurements are presented in Fig. 4.12a. One trap, with and emission time of around 10 μs were identified. However, no temperature dependence was seen. This most likely implies that the trap mechanism



(a)



(b)

Figure 4.12: (a) Temperature and (b) filling time dependent DCT measurements for the thin buffer sample. The high stress voltage was (V_{GS},V_{DS}) = (V_P-2,50) V and the low stress voltage was (1,7) V. A filling time of 1 ms was used in (a) and the measurements in (b) were performed at 20 °C.

is governed by tunneling [145].

Filling time dependent measurements are performed at room temperature to gain further insight in to the trap's origin, Fig. 4.12b. A large dependence on filling time is found for the amplitude of the trap, indicating that it is due to extended defects. Probably, the trap is due to dislocations in the AlN-nucleation layer which are accessed through a tunneling process.

4.5 The impact of buffer design on output power

Load-pull measurements were performed as an application relevant comparison between the various buffer designs that have been investigated in this thesis, Table 4.1. The measurements were performed at 30 GHz

with a quiescent V_{DS} of 10 and 30 V, and a quiescent drain current of around 10 % of I_{DSS}. The load and source impedance were optimized for maximum output power. For comparison, Table 4.2 contains literature values of achievable output power at similar frequencies for the different buffer designs.

Low:C does not suffer from buffer related dispersive effects and therefore deliver the largest output power of all samples in this thesis. This was somewhat unexpected given the similar performance to Stepped:C in paper [C]. However, the load-pull measurements in paper [C] were performed at $V_{DSQ} = 15$ V, for which the trapping effects in Stepped:C were limited. This clearly exemplifies the importance of evaluating buffer trapping effects at relevant operating voltages. Comparing to literature values of uid GaN buffers the Low:C sample offers exceptional performance. However, for all of these devices the efficiency is fairly limited, most likely due to difficulties in reaching pinch-off. Therefore, uid GaN buffers are not desirable in real applications since this will decrease their reliability [87].

The C-doped devices in this thesis performed similarly (except for High:C which is also limited by a small gain at this frequency). For the low V_{DSQ} all of them supplied output powers in line of what is expected from the DC-data. However, for the large V_{DSQ} they all suffered from trapping effects, limiting the maximum output power and decreasing the efficiency. Compared to the literature values in [133], the C-doped devices in this thesis perform significantly worse. This should partially be related to the larger n_s ($1.8 \cdot 10^{13}$ cm^{-2}) and thinner barrier layer (giving less short channel effects) in [133], but could also be related to a different doping profile which unfortunately is not disclosed. The Fe-doped device showed both increased output power and efficiency when increasing V_{DSQ} from 10 to 30 V. However, compared to Low:C the output power is obviously lower, indicating that the Fe-induced trapping limits the output power in this case. Similar results have been found in [110, 111].

BB2 offered performance in line with the C-doped GaN buffers while the output power of BB1 was very limited. This was expected from the lower current of BB1 and the extensive trapping found in Fig. 4.9. Comparing to the literature, the output power of BB2 is similar to that reported in [149] but significantly lower than in [150]. In [149] the AlGaN back barrier was grown directly on the nucleation layer (similar to this work) but in [150] the AlGaN back barrier was combined with a

C-doped GaN buffer. Possibly, the lower output power for the devices in this thesis (and in [149]) can be explained by thermal issues or increased trapping due to worse crystalline quality.

Devices on the thin HEMT structure showed excellent performance, similar to the Exp:Fe sample. However, comparing to the Low:C sample it is clear that the trap identified in the DCT measurements limit performance. This is further indicated by the decrease in efficiency when increasing V_{DSQ} from 10 V to 30 V. To improve the output power further, structural improvements of the AlN-nucleation layer should be prioritized. Nevertheless, the thin HEMT structure offers competitive performance already at this stage.

In conclusion, the results in this thesis indicate that Fe-doped buffers remain the benchmark which other buffer designs should be compared to. The uid GaN buffers supply the highest output power but is limited in efficiency and reliability. The extensive trapping effects in C-doped buffers needs to be addressed in order establish this as a viable option for microwave applications. Back barrier designs also requires further optimization to minimize trapping and thermal effects. The thin buffer structure is an interesting option that showed performance in line with the Fe-doped buffer. However, also in this case the trapping effects reduced the achievable output power. For C-doped GaN, AlGaN back barrier, and thin buffer designs, improving the crystalline quality is believed to be a possible route for enhanced performance.

	V_{DSQ} = 10 V		V_{DSQ} = 30 V	
Device [Ref.]	P_{out} (W/mm)	PAE (%)	P_{out} (W/mm)	PAE (%)
Low:C [C]	1.8	20	5.7	20
High:C [C]	0.3	3	0.1	1
Stepped:C [C]	1.5	30	3.3	23
Extrinsic:C [D]	1.0	30	2.0	15
Exp:C [E]	1.8	26	2.6	15
Stepped:C [E]	1.6	30	2.5	15
Exp:Fe [E]	1.3	20	3.9	25
BB1	0.7	30	0.5	5
BB2	1.1	30	2.7	20
Thin buffer	1.8	35	3.9	25

Table 4.1: Load-pull measurements for devices with various buffer designs. Listed are the maximum output power and associated power added efficiency at two quiescent bias points. The devices have a gate length of 100 nm and source drain distance of ∼2.8 μm.

Ref.	Barrier	V_{DSQ} (V)	freq. (GHz)	P_{out} (W/mm)	PAE (%)
uid GaN buffers					
[146]	$GaN/Al_{0.31}Ga_{0.69}N$ (1/25 nm)	35	18	5.1	20
[147]	$In_{0.15}Al_{0.85}N/AlN$ (8/1 nm)	15	18	2.9	28
[148]	$GaN/Al_{0.25}Ga_{0.75}N$ (2/25 nm)	30	30	4.0	15
C-doped GaN buffers					
[133]	AlN (4 nm)	30	18	6.3	40
[133]	AlN (4 nm)	20	40	4.7	30
Back barrier					
[149]	$In_{0.17}Al_{0.83}N/AlN$ (7/1 nm)	20	29	2.1	22
[150]	InAlGaN/AlN (6/1 nm)	20	30	6.0	36

Table 4.2: Literature values of achievable output power for devices with different buffer designs.

Chapter 5

Conclusions and future outlook

The aim of this thesis has been to optimize the buffer design to improve the performance in terms of output power and time variant effects in GaN HEMTs for microwave applications. The thesis has also presented work done to reduce losses in GaN HEMT technology, in the form of low resisitve ohmic contacts and improved barrier quality.

A Ta-based recessed ohmic contact have been presented which show close to state of the art performance with an R_C of 0.14 Ωmm. Compared to the most commonly used, Ti/Al/Ni/Au contact, the contact presented in this thesis requires lower anneal temperature (550-600 °C) leading to better edge acuity and no degradation of the 2DEG sheet resistance. The lowest contact resistance was found for a recess depth close to the barrier thickness. A general problem for recess etched contacts is the optimization of the etching depth and the repeatability of the etching process. Future work should focus on increasing the repeatability of the ohmic process rather than just aiming for low R_C's. The results presented in this thesis also hint that a more repeatable process might be possible by etching deeper, well past the barrier layer. Investigations into these areas are currently ongoing, showing promising results.

The higher mobility associated with the inclusion of an AlN-exclusion layer (>2000 cm^2/Vs) can also be achieved by a more well defined AlGaN/GaN interface. The sharper interface leads to less dispersion and lower C_{gs} at large drain bias compared to a diffuse AlGaN/GaN in-

terface. Furthermore, the sharp AlGaN/GaN interface enables a low access resistance while simultaneously allowing for easier formation of ohmic contacts, which can be hindered by the large band gap of AlN. Possibly, the high mobility achieved with an AlN-exclusion layer is not only related to the large band gap of AlN but also due to a good interface quality, inherently achieved by the large growth difference between GaN and AlN growth.

The trapping behavior of C-doped buffers for microwave applications have been thoroughly investigated in this thesis. The lower C-concentrations required for microwave applications compared to power applications is showed to result in n-type GaN. Consequently, the trapping behavior of such buffers is not limited by the formation of a pn-diode between the GaN buffer and the 2DEG. Instead, it is suggested that trapping at dislocations covered with C-clusters is the main source of dispersion. The trapping effects severely limited the output power to 2.5 W/mm at 30 GHz. Future work should target C-doped buffers with reduced dislocation densities. This could verify the ideas presented in this thesis and possibly reduce the dispersive effects in C-doped buffers. Freestanding GaN substrates could be used to decrease the dislocation density by at least two orders of magnitude [151]. The C-incorporation would have to be controlled using an external C-source, as not to degrade the crystal quality.

AlGaN Back back barriers with a large C-concentration is shown to suffer from extensive trapping effects. However, a epi-structure with a 100 nm uid GaN channel showed performance in line with C-doped GaN buffers. Similarly to the C-doped buffers, the trapping in the back barrier devices also seemed to be enabled by extended defects. Therefore, improved crystal quality is of large interest also in this case. Furthermore, the C-concentration should be minimized in the back barrier to assess its contribution to the total trapping behavior. In the literature, the best results seems to be enabled when the back barrier is grown on a GaN buffer layer. Future works should adopt this method and investigate how this affects trapping.

The thin HEMT structure showed excellent DC characteristics and RF output power (3.9 W/mm at 30 GHz). However, the performance is limited by trapping at dislocations, most probably originating from the AlN-nucleation layer. Therefore, future work should focus on further optimizing the nucleation layer. Furthermore, an extensive thermal evaluation should be undertaken, to verify that the thin GaN buffer

does not degrade the thermal performance of the epi-structure.

Looking in to the future of epi-design for GaN HEMTs, N-polar structures offer interesting opportunities for high frequency operation. The N-polar case intrinsically offers a good electron confinement due to the high energy barrier below the 2DEG and the polarization fields "pushing" the electrons upwards [152]. Furthermore, both surface and buffer trapping effects can be mitigated in interesting ways [153]. For a highly optimized N-polar material an extremely impressive output power density of 6.5 W/mm at 94 GHz has been reported [152].

Chapter 6

Summary of appended papers

This chapter summarizes the publications which are included in this thesis. An abstract and my contributions are presented for each publication.

Paper A

J. Bergsten, A. Malmros, M. Tordjman, P. Gamarra, C. Lacam, M.-A. di Forte-Poisson, and N. Rorsman, "Low resistive Au-free, Ta-based, recessed ohmic contacts to InAlN/AlN/GaN heterostructures," *Semiconductor Science and Technology*, vol. 30, iss. 10, pp. 105034, 2015.

The paper investigates the formation of recessed, Ta/Al/Ta, ohmic contacts to an InAlN/AlN/GaN heterostructures. A contact resistance (R_C) as low as 0.14 Ωmm is found for contacts where the recess etch has stopped just above the 2D electron gas channel. At this depth the contacts are also found to be less sensitive to other process parameters, such as anneal duration and temperature. For deeper recesses R_C remains low but requires annealing at higher temperatures for contact formation. An optimum bottom Ta layer thickness of 5–10 nm is found. Two reliability experiments preliminary confirm the stability of the recessed contacts.

My contribution: I designed the experiments, fabricated the test-structures, performed the measurements, and wrote the paper with feedback from the co-authors.

Paper B

J. Bergsten, J.-T. Chen, S. Gustafsson, A. Malmros, U. Forsberg, M. Thorsell, E. Janzén, and N. Rorsman, "Performance Enhancement of Microwave GaN HEMTs Without an AlN-Exclusion Layer Using an Optimized AlGaN/GaN Interface Growth Process," *IEEE Transactions on Electron Devices*, vol. 63, iss. 1, pp. 333-338, 2015.

High-electron mobility transistors (HEMTs) with different sharpness of the AlGaN/GaN interface are investigated. Two structures, one with an optimized AlGaN/GaN interface and another with an unoptimized, are grown using hot-wall metal-organic chemical vapor deposition. The electron mobility of the optimized structure is 1760 cm^2/Vs as compared with 1660 cm^2/Vs for the unoptimized structure. The higher mobility manifests as lower parasitic resistance yielding a better dc and high-frequency performance. A small-signal equivalent model is extracted, which indicate a lower electron penetration into the buffer in the optimized sample. Pulsed-IV measurements imply that the sharper interface provides less dispersive effects at large drain biases.
My contribution: I fabricated the HEMTs, performed the measurements as well as the physical and compact modelling, and wrote the paper with feedback from the co-authors.

Paper C

S. Gustafsson, J.-T. Chen, **J. Bergsten**, U. Forsberg, M. Thorsell, E. Janzén, and N. Rorsman, "Dispersive Effects in Microwave AlGaN/AlN/GaN HEMTs With Carbon-Doped Buffer," *IEEE Transactions on Electron Devices*, vol. 62, iss. 7, pp. 2162-2169, 2015.

HEMTs have been fabricated on three epitaxial structures: two with uniform C doping profile but different concentration and one with a stepped doping profile. The leakage currents in OFF-state at 10 V drain voltage were in the same order of magnitude (10^{-4} A/mm) for the high-doped and stepped-doped buffer. The highly doped material had a current collapse (CC) of 79 % compared with 16 % for the stepped-doped material under dynamic I–V conditions. The low-doped material had low CC (5 %) but poor buffer isolation. Trap characterization revealed that the high-doped material had two trap levels at 0.15 and 0.59 eV, while the lowly doped material had only one trap level at

0.59 eV. This paper indicates that carbon is a potential substitute to iron as a deep level acceptor.
My contribution: JB and NR fabricated the HEMTs, SG and JB performed the measurements and wrote the paper with feedback from the co-authors.

Paper D

J. Bergsten, X. Li, D. Nilsson, Ö. Danielsson, H. Pedersen, E. Janzén, U. Forsberg, and N. Rorsman, "AlGaN/GaN high electron mobility transistors with intentionally doped GaN buffer using propane as carbon precursor," *Japanese Journal of Applied Physics*, vol. 55, pp. 05FK02, 2016.

AlGaN/GaN epi-structures are grown by metalorganic chemical vapor deposition using propane as precursor to achieve a C-doped GaN buffer. This approach allows for optimization of the GaN growth conditions without compromising material quality to achieve semi-insulating properties. HEMTs are fabricated and evaluated in terms of isolation and dispersion. Good isolation with OFF-state currents of $2 \cdot 10^{-6}$ A/mm, breakdown fields of 70 V/μm, and low drain induced barrier lowering of 0.13 mV/V are found. However, severe dispersive effects are identified using pulsed-IV measurements. Current collapse and knee walkout effects limit the maximum output power to 1.3 W/mm.
My contribution: I fabricated the HEMTs, performed the measurements, and wrote the paper with feedback from the co-authors.

Paper E

J. Bergsten, M. Thorsell, J.-T. Chen, D. Adolph, O. Kordina, E. Ö. Sveinbjörnsson, and N. Rorsman, "Electron Trapping in Extended Defects in Microwave AlGaN/GaN HEMTs with Carbon Doped Buffers," *Submitted to IEEE Transactions on Electron Devices.*

AlGaN/GaN high electron mobility transistors (HEMTs) fabricated on epi-structures with C-doped buffers are investigated. Changes in growth parameters are used to control the C-concentration in metalorganic chemical vapor deposition. The C-concentration is low enough to result in n-type GaN. Reference devices are also fabricated on a structure us-

ing Fe as dopant, to exclude any process related variations and provide a relevant benchmark. Pulsed-IV measurements show extensive dispersion in the C-doped devices, with values of dynamic R_{ON} 3-4 times larger than in the DC-case. In drain current transient measurements the trap filling time is varied, finding large prevalence of trapping at dislocations for the C-doped samples. The measurements indicate that clusters of C around the dislocations are the main cause for the increased dispersion.
My contribution: I designed the experiments, fabricated the HEMTs, performed the measurements, analyzed the results, and wrote the paper with feedback from the co-authors.

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Paper A

Low resistive Au-free, Ta-based, recessed ohmic contacts to InAlN/AlN/GaN heterostructures

J. Bergsten, A. Malmros, M. Tordjman, P. Gamarra, C. Lacam, M.-A. di Forte-Poisson and N. Rorsman

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Paper B

Performance Enhancement of Microwave GaN HEMTs Without an AlN-exclusion Layer Using an Optimized AlGaN/GaN Interface Growth Process

J. Bergsten, J.-T. Chen, S. Gustafsson, A. Malmros, U. Forsberg, M. Thorsell, E. Janzén, and N. Rorsman

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Paper C

Dispersive Effects in Microwave AlGaN/AlN/GaN HEMTs With Carbon-Doped Buffer

S. Gustafsson, J.-T. Chen, J. Bergsten, U. Forsberg, M. Thorsell, E. Janzén, and N. Rorsman

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Paper D

AlGaN/GaN high electron mobility transistors with intentionally doped GaN buffer using propane as carbon precursor

J. Bergsten, X. Li, D. Nilsson, Ö. Danielsson, H. Pedersen, E. Janzén, U. Forsberg, and N. Rorsman

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Paper E

Electron Trapping in Extended Defects in Microwave AlGaN/GaN HEMTs with Carbon Doped Buffers

J. Bergsten, M. Thorsell, J.-T. Chen, D. Adolph, O. Kordina, E. Ö. Sveinbjörnsson, and N. Rorsman

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