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# High-mobility solution-processed copper phthalocyanine-based organic field-effect transistors

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**Abstract**
Solution-processed films of 1,4,8,11,15,18,22,25-octakis(hexyl) copper phthalocyanine ($CuPc_6$) were utilized as an active semiconducting layer in the fabrication of organic field-effect transistors (OFETs) in the bottom-gate configurations using chemical vapour deposited silicon dioxide ($SiO_2$) as gate dielectrics. The surface treatment of the gate dielectric with a self-assembled monolayer of octadecyltrichlorosilane (OTS) resulted in values of $4 \times 10^{-2}$ cm$^2$ V$^{-1}$ s$^{-1}$ and $10^6$ for saturation mobility and on/off current ratio, respectively. This improvement was accompanied by a shift in the threshold voltage from 3 V for untreated devices to −2 V for OTS treated devices. The trap density at the interface between the gate dielectric and semiconductor decreased by about one order of magnitude after the surface treatment. The transistors with the OTS treated gate dielectrics were more stable over a 30-day period in air than untreated ones.

Keywords: substituted copper phthalocyanine, organic thin film transistor, surface treatment, AFM, topology, field effect mobility

## 1. Introduction

Over the last three decades extensive research has been undertaken to develop organic field-effect transistors (OFETs). This has been driven by scientific interest [1, 2] and the potential applications of OFETs in new technologies such as flexible displays [3, 4], logic circuits [5–7], radio frequency identification (RFID) tags [8, 9], electronic paper [10,11] and sensing [12–14]. Organic compound-based devices offer interesting advantages over their inorganic counterparts in terms of their cost-effective deposition using low-energy vapour and solution phase methods that are suitable for large-area coverage on both solid and flexible substrates [15–17]. Furthermore, molecular tailoring of organic compounds via chemical modification can achieve high field-effect performance of the active semiconducting layers. For example, fused acene [18], oligothiophene [19], tetrathiafulvalene derivatives [20] and conjugated polymers [21] exhibit field-effect mobilities much larger than 0.1 cm$^2$ V$^{-1}$ s$^{-1}$. However, the chemical and electrical stabilities of these OFETs, and consequent degradation in on-current, threshold voltage and field-effect mobility under air exposure remain a problem. The passivation of the organic semiconductor has therefore attracted much attention recently [22, 23].

Metal phthalocyanines are 18 $\pi$-electron macrocyclic conjugated compounds and their derivatives are generally non-toxic and well known for their intrinsic thermal and chemical stability. Examples of phthalocyanine-based OFETs reportedly have good field-effect properties with

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field-effect mobilities ranging from $10^{-3}$ to 1.0 $cm^2 V^{-1} s^{-1}$, the values depending upon the central metal atom, gate dielectric and the deposition techniques and parameters [24]. Electrical performance was satisfactorily stable for more than half a year even when the devices were stored in open air [25]. However, phthalocyanine compounds that carry no substituents on the ring system are essentially insoluble in organic solvents and are therefore not amenable to solution processing for deposition as thin films. To overcome this difficulty, p-channels were formed by depositing well-ordered Langmuir–Blodgett films on $SiO_2$ layers of amphiphilic 2,9,16-tri(tert-butyl)-23-(10-hydroxydecyloxy) metal-free and copper phthalocyanine derivatives [26] and heteroleptic bis(phthalocyaninato) terbium and lutetium complexes [27]. Metallophthalocyanine-based OFETs performed better than those with metal-free compounds and their mobility varied between $4.0 \times 10^{-4}$ and $1.7 \times 10^{-3}$ $cm^2 V^{-1} s^{-1}$, depending upon the film crystallinity, substituent types and central metal ions. An all-organic transistor was fabricated using Langmuir–Blodgett films of metal-free amino-tri-tert-butyl-phthalocyanine on a 200 nm thick polymethylmethacrylate gate dielectric, but the device was much slower, giving values of $5.2 \times 10^{-6}$ $cm^2 V^{-1} s^{-1}$ and 100 for the mobility and on/off current ratio, respectively [28]. Liquid-crystal zinc (II) phthalocyanine and lutetium (III) bisphthalocyanine derivatives, both substituted with peripheral individual functional groups, were spin-coated at room temperature on $SiO_2/Si$ substrates as active layers of organic thin-film transistors because of easy solution-based formulation of supramolecular structures with the ability to design desired mesomorphic properties [29, 30]. The post-deposition annealing of these compounds was found to be critical for controlling charge transport along a preferential direction. Spun films of a thermotropic liquid-crystal lutetium bisphthalocyanine sandwich complexes substituted with 16 octyl chains were employed as active organic semiconducting layers. An increase from $1.5 \times 10^{-3}$ $cm^2 V^{-1} s^{-1}$ for as-deposited films to $8.0 \times 10^{-3}$ $cm^2 V^{-1} s^{-1}$ for the films annealed at 70 °C was achieved for the field-effect mobility in the saturated regime. At the same time, the threshold voltage was reduced from −25 to −12.5 V and the sub-threshold voltage swing decreased from 3.8 to 1.6 V $decade^{-1}$ for the corresponding devices [31].

This paper reports the electrical characteristics of bottom-gate transistors in which the active semiconductor layer is the spin-coated film of a copper phthalocyanine derivative were substituted with hexyl ($C_6H_{13}$) chains at the eight non-peripheral (1,4,8,11,15,18,22,25-) sites as shown in figure 1(a). This molecule is hereafter referred to as $CuPc_6$. Our previous work has demonstrated that this type of substituted compound has satisfactory solubility in most common solvents and forms well-ordered spin-coated films as judged by low-angle x-ray reflectivity measurements [32, 33]. These investigations also indicate that during the evaporation process the molecules assemble into layers of columns whose axes are parallel to the surface of the substrate [34]. The control of the interface between

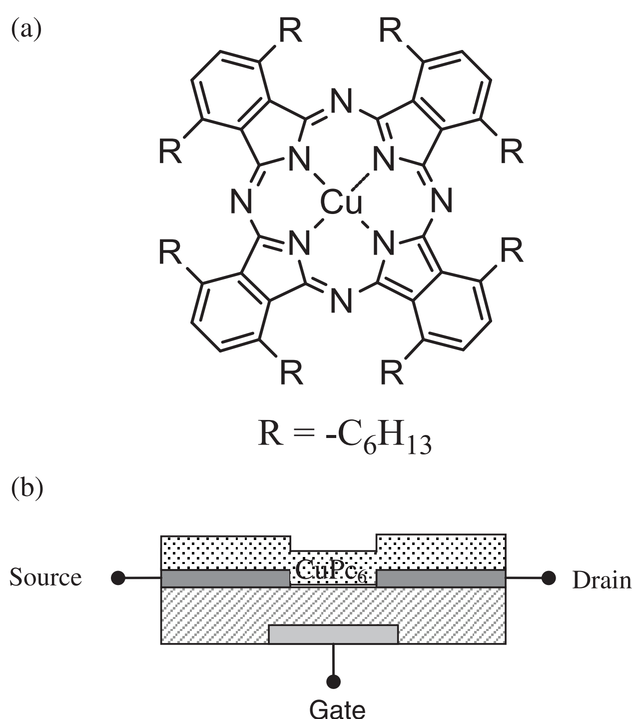


**Figure 1.** (a) Molecular structure of 1,4,8,11,15,18,22,25-octakis(hexyl)phthalocyaninato copper(II) derivatives and (b) bottom-gated bottom-contact structure (cross sectional view) used for fabrication of organic field-effect transistor.

the organic active layer and the gate dielectric layer is important for realization of faster transistors with low threshold voltages. Attempts have been made to coat the gate surface with self-assembled monolayers (SAMs) of $\beta$-phenethyltrichlorosilane, octadecyltrichlorosilane (OTS) or hexamethyldisilane [35, 36] for passivation of dangling bonds and interfacial traps. In the present work, the silicon dioxide ($SiO_2$) gate dielectric surface was modified with the OTS monolayer. The effect of the gate surface treatment on the transistor performance was examined and correlated with the atomic force microscopy (AFM) studies of the morphology of the $CuPc_6$ layer.

## 2. Experimental details

1,4,8,11,15,18,22,25-octakis(hexyl) phthalocyaninato copper(II), $CuPc_6$, was synthesized as described in [37]. The bottom gated OFET structure in figure 1(b) was formed by depositing a thin $CuPc_6$ film as an active layer on a highly n-doped silicon (Si) wafer substrate of resistivity $1 \times 10^{-3}$ Ω m. The deposition was conducted at room temperature by spinning a small volume of the spreading solution of $CuPc_6$ in highly pure chloroform (concentration 5 g $l^{-1}$) at 2000 rpm for 30 s, allowing the complete evaporation of organic solvent. The film thickness $d$ was estimated as 70 nm using the Dektak 6M stylus profilometer. Prior to the device fabrication, the substrates were cleaned thoroughly in acetone, isopropanol and finally in deionized water. The pre-patterned interdigitated electrode system consisted of the sputtered gold film (50 nm thick) with

an adhesive underlayer of 20 nm thick titanium, providing the channel of length $L = 5\,\mu$m and width $W = 1$ mm between the source and drain. The capacitance per unit area $C_{ox}$ was estimated as $1 \times 10^{-4}\,\mathrm{F\,m^{-2}}$ for the 250 nm thick chemical vapour deposited silicon dioxide ($SiO_2$) layer acting as the gate dielectric. The ohmic contact for the gate terminal was prepared by depositing an indium/gallium (In/Ga) eutectic layer on the uncoated side of the Si substrate, which was carefully etched using hydrofluoric acid to remove the native oxide. In order to study the effect of the surface treatment of the gate layer on the transistor performance, a selection of OFET substrates were immersed for 10 min in a solution of OTS in anhydrous toluene kept at a temperature above 50 °C prior to the deposition of the $CuPc_6$ active layer. A single layer of tightly packed and highly ordered molecules was self-assembled on the gate surface. The electrical measurements were performed on both OTS-treated and untreated devices under ambient conditions using a Keithley 4200 semiconductor parameter analyser. The surface morphology of the films was investigated in the tapping mode using a Park PSIA XE-100 atomic force microscope. The images were recorded over an area of $5 \times 5\,\mu\mathrm{m}^2$ for both as-deposited and annealed devices. To study the stability, $CuPc_6$ OFETs were stored in open laboratory atmosphere for 30 days and then the morphological and electrical measurements were repeated for these devices under the same conditions as before.

## 3. Results and discussion

Figure 2 shows the AFM images of the $CuPc_6$ films on the $SiO_2$ gate oxides. The morphology containing long twisted fibres is clearly seen for the $CuPc_6$ film deposited on unmodified gate oxide (figure 2(a)); the fibres were not uniformly covering the surface, and formed large random clusters. However, a granular, uniform and void-free morphology was observed for the $CuPc_6$ film deposited on the OTS treated gate oxide, with a grain size of approximately 200 nm (figure 2(b)). The adhesion of $CuPc_6$ was improved remarkably and the average surface roughness was reduced for the OTS treated samples (2.02 nm) compared to untreated devices (3.24 nm). It is evident from figure 2(c) that the morphology of the $CuPc_6$ film on the modified gate oxide layer was unchanged by storage in air for 30 days.

The transfer characteristic of drain-source current $I_{DS}$ versus gate voltage $V_G$ for drain-source voltage $V_{DS} = -40$ V (figure 3) exhibits a two orders of magnitude increase in the on/off current ratio of the OTS treated field-effect transistors compared with the devices with untreated gate oxide. Irrespective of the OTS treatment, the drain-source current $I_{DS}$ was larger for off-to-on trace than on-to-off trace for all negative values of $V_G$. This behaviour is similar to one observed for the pentacene-based OFETs [38]. It has been argued that the $I_{DS}$ rise in the off-to-on trace is due to the supply of additional holes compensating immobile trapped electrons in the semiconductor whereas the on-to-off $I_{DS}$ is due to the accumulation of holes in the channel in the absence of trapped electrons. The difference in $V_G$ corresponding to the off-to-on and on-to-off traces for $I_{DS} = 10^{-9}$ A was estimated as 13 V and 7.6 V for untreated and OTS treated devices, respectively, as a measure of the hysteresis. This substantial reduction of hysteresis indicates the effect

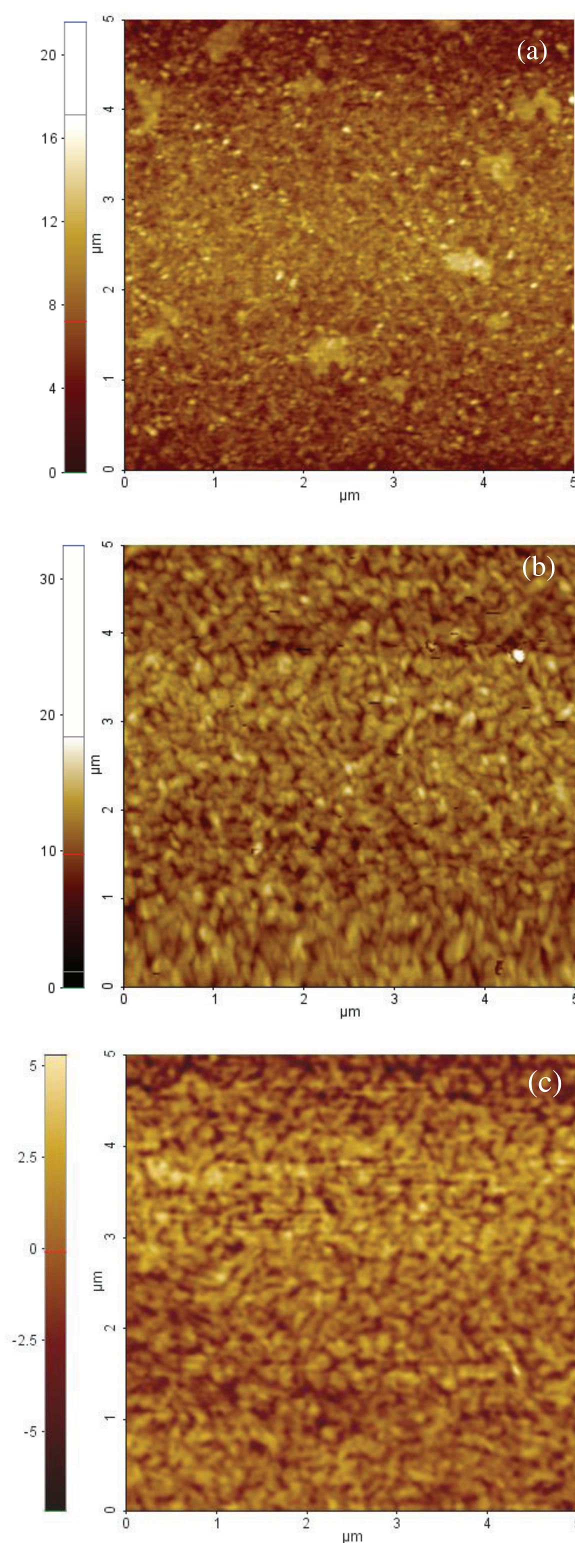


**Figure 2.** AFM images of $CuPc_6$ films on $SiO_2$ (a) without OTS treatment (b) with OTS treatment and (c) with OTS treatment after 30 days. The colour scale bar at the left side shows the height in nm for the $z$-axis.

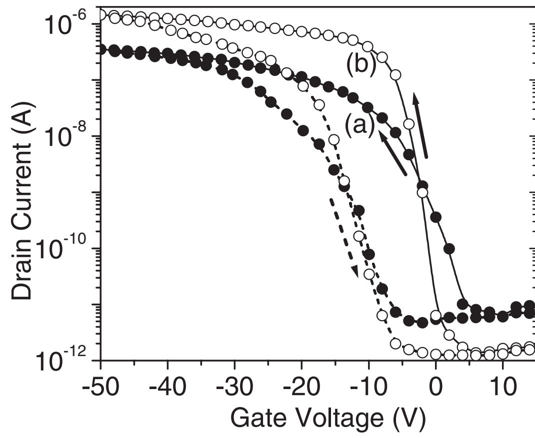


**Figure 3.** Transfer curves for $CuPc_6$ field-effect transistor measured at the drain voltage of 40 V (a) without (filled circles) and (b) with OTS treatment (open circles) of the gate dielectric surface. Solid and broken lines correspond to off-to-on and on-to-off traces, respectively; $L = 5\,\mu$m and $W = 1$ mm.

of the OTS treatment on bias-dependent trapping/detrapping dynamics in the $CuPc_6$ film and near its interface with the $SiO_2$ dielectric.

The sharp increase of $I_{DS}$ at negative values of $V_G$ indicates the formation of a p-type conductivity channel. The charges became completely depleted at $V_G = 5$ V, resulting in a drastic reduction in $I_{DS}$. The depletion width $d_F$ depends upon the maximum charge carrier density $N_A$ and the effective capacitance per unit area $C_i$ of the gate. This dependence is expressed as [39]

$$d_F = \frac{\varepsilon_0 \varepsilon_{pc}}{C_i}\left[\left(1 + \frac{2C_i^2 V_G}{q N_A \varepsilon_0 \varepsilon_{pc}}\right)^{1/2} - 1\right]. \tag{1}$$

The value of $d_F$ was taken as 70 nm since the depletion zone was expected to extend into the entire depth of the $CuPc_6$ film. The $C_i$ value for the OTS treated device was determined using the value of $1 \times 10^{-2}\,\mathrm{F\,m^{-2}}$ for the OTS monolayer [40]. The free permittivity $\varepsilon_0 = 8.85 \times 10^{-12}\,\mathrm{F\,m^{-1}}$, the electronic charge $q = 1.6 \times 10^{-19}$ C and the dielectric constant $\varepsilon_{pc} = 3$ of $CuPc_6$ were used for the calculations. The value of $N_A$ was estimated as $3.97 \times 10^{22}\,\mathrm{m^{-3}}$ for both untreated and OTS treated devices. This value is in good agreement with that determined from measurements on field-effect transistors using electrophoretically deposited copper phthalocyanine (CuPc) as an active layer [41].

Both OFETs showed good subthreshold slopes. The sub-threshold voltage swing S is defined as the voltage $V_G$ required to increase $I_{DS}$ by a factor of 10. It was calculated as 3.33 and 1.23 V $\mathrm{decade^{-1}}$ from the transfer characteristics for untreated and OTS treated transistors, respectively, using the formula

$$S = \frac{dV_G}{d\,(\log I_{DS})}. \tag{2}$$

This reduction of *S* due to the surface treatment is encouraging in light of the reported value of $\leqslant$2 V $\mathrm{decade^{-1}}$ for the OFETs with channel length of 20 $\mu$m and width of 220 $\mu$m prepared

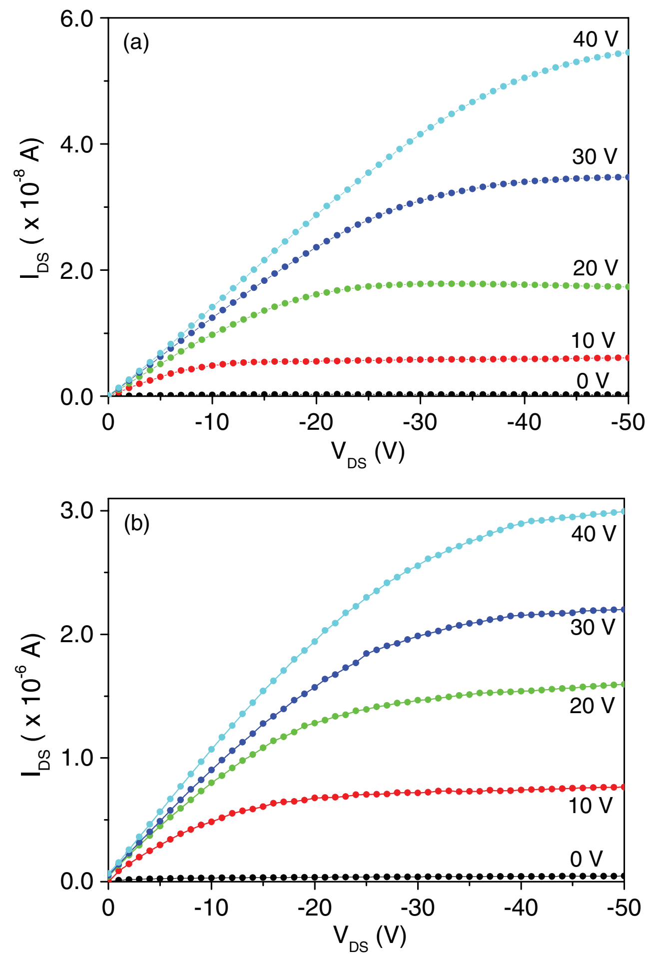


**Figure 4.** Drain-source current ($I_{DS}$) as a function of drain-source voltage ($V_{DS}$) for a $CuPc_6$ field-effect transistor, measured in air (a) without and (b) with OTS treatment. $L = 5\,\mu$m and $W = 1$ mm.

by evaporating CuPc at 100 °C on the OTS treated $SiO_2$ gate [42].

A set of typical output characteristics is depicted in figure 4 in terms of drain-source current ($I_{DS}$) as a function of $V_{DS}$. These characteristics were obtained for the OFETs with $CuPc_6$ active layers on both untreated and OTS treated $SiO_2$ surfaces as $V_G$ was varied from 0 to −40 V. For a given $V_G$, $I_{DS}$ increases linearly within the low $V_{DS}$ regime, implying a uniform charge density in the channel. The field-effect mobility $\mu_{lin}$ of the accumulated charge may be written in the form [39]:

$$\mu_{lin} = \left(\frac{L}{wC_i V_{DS}}\right)\frac{\partial I_{DS}}{\partial V_G}. \tag{3}$$

The median values of $\mu_{lin}$ at $V_{DS} = 5$ V were estimated as $6 \times 10^{-5}$ and $4 \times 10^{-6}\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ for untreated and OTS treated transistors, respectively.

At higher values of $V_{DS}$, $I_{DS}$ increased sublinearly with increasing $V_{DS}$ and then saturates at $I_{DS(sat)}$. This behaviour is generally described by the quadratic dependence of $I_{DS(sat)}$ on $V_G$ in the form [39]:

$$I_{DS(sat)} = \frac{WC_i}{2L}\mu_{(sat)}\,(V_G - V_T)^2. \tag{4}$$

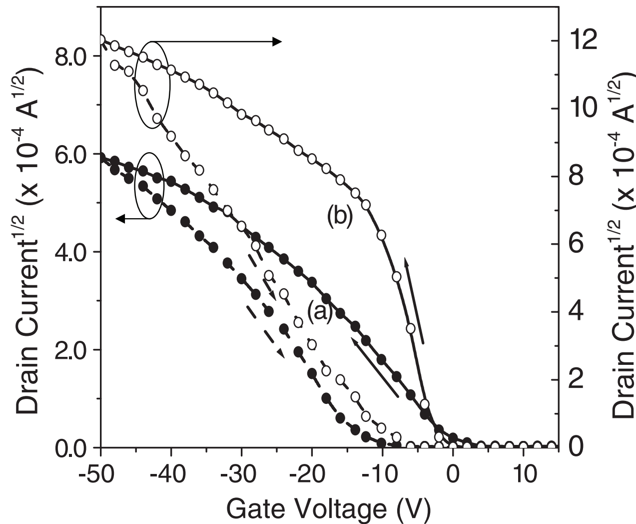


**Figure 5.** The square root of drain-to-source current $I_{SD(sat)}$ as a function of gate-to-source voltage $V_{GS}$ in the saturation regime $V_{DS} = 40$ V, (a) without (filled circles) and (b) with OTS treatment (open circles). Solid and broken lines correspond to off-to-on and on-to-off traces, respectively. $L = 5\,\mu$m and $W = 1$ mm.

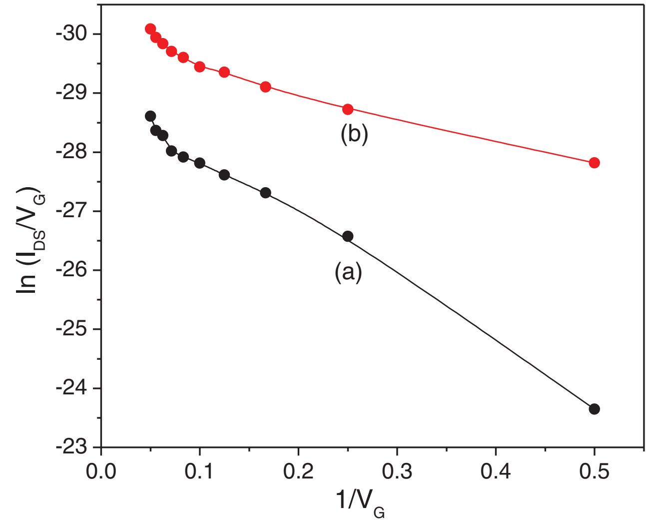


**Figure 6.** Levinson plot of $I_{DS}/V_G$ versus $1/V_G$ for $V_{DS} = 40$ V: (a) without and (b) with OTS treatment. $L = 5\,\mu$m and $W = 1$ mm.

The plot of $\sqrt{I_{DS(sat)}}$ versus $V_G$ at $V_{DS} = -40$ V in figure 5 shows the linear fit of experimental data to equation (4). Values of saturated mobility $\mu_{sat}$ and the threshold voltage $V_T$ were estimated from the slope and intercept on the abscissa, respectively. A one order of magnitude increase was observed in the value of $\mu_{sat}$ from $2 \times 10^{-3}$ cm$^2$ V$^{-1}$ s$^{-1}$ for untreated OFETs to $4 \times 10^{-2}$ cm$^2$ V$^{-1}$ s$^{-1}$ for treated OFETs. Meanwhile, the threshold voltage decreased from $V_T = 3$ V for untreated devices to $V_T = 2$ V for the device treated with an OTS SAM. A value of $5.32 \times 10^{-3}$ cm$^2$ V$^{-1}$ s$^{-1}$ was recently reported for OFETs fabricated by thermally evaporating CuPc on the $SiO_2$ gate without surface treatment [43]. A slightly improved value of $1.5 \times 10^{-3}$ cm$^2$ V$^{-1}$ s$^{-1}$ was obtained for 40 nm thick thermally evaporated CuPc active layers on the OTS treated $SiO_2$ gates in the top-contact OFETs using $MoO_3$/Al electrodes [44]. When, on the other hand, long-chain alkane tetratetracontane was used as a passivation layer on the $SiO_2$ gate, the mobility was estimated as $1.9 \times 10^{-2}$ cm$^2$ V$^{-1}$ s$^{-1}$ [45]. This value is, however, twice smaller than $\mu_{sat}$ of the transistors with the $CuPc_6$ active layer on the OTS treated $SiO_2$ gate. Our results also show an improvement over the value of $1.8 \times 10^{-2}$ cm$^2$ V$^{-1}$ s$^{-1}$ reported for Langmuir–Blodgett films of polymerizable octa-substituted copper phthalocyanine with styryl-terminated side chains as active layer [46]. This improvement may be a consequence of the $\pi$–$\pi$ stacking in an OTS SAM induced orientation of the solution-processed $CuPc_6$ molecules in the film which is believed to be favourable for charge flow. High mobility of 0.1–0.2 cm$^2$ V$^{-1}$ s$^{-1}$ was obtained for the solution-processed active layers of 5-hexylthiophene-fused copper porphyrazine on OTS treated Si/$SiO_2$ substrates in the top-contact OFET configuration. The on–off ratio is at least one order of magnitude smaller than one obtained in this investigation [47]. $CuPc_6$ is a thermotropic liquid–crystal compound, and a comparable mobility value of 0.12 cm$^2$ V$^{-1}$ s$^{-1}$ was obtained using the $CuPc_6$ film annealed at 50 °C.

The transistor parameters such as threshold voltage, sub-threshold voltage swing and on/off current ratio are influenced by the morphology of the $CuPc_6$ layer and the presence of the traps at its interface with the $SiO_2$ gate layer. A value of $9.10 \times 10^{12}$ cm$^{-2}$ is obtained for the density of traps $N_t$ without the OTS treatment using the equation [48]:

$$N_t = \left[\frac{S\log(e)}{(kT/q)} - 1\right]\frac{C_i}{q}. \qquad (5)$$

Here the Boltzmann constant $k = 8.61 \times 10^{-5}$ eV K$^{-1}$ and the operating temperature $T$ was taken as 300 K. A smaller value of $N_t = 1.3 \times 10^{12}$ cm$^{-2}$ was calculated for the $CuPc_6$ transistors with OTS treated gate. This reduction may be attributed to the decrease in surface roughness of the $CuPc_6$ layer on the OTS treated gate as shown in the AFM images of figure 2, as well as to the increase in the interfacial bonding between the active $CuPc_6$ layer and the OTS treated gate.

The dependence of $I_{DS}$ on the density $N_g$ of traps at the grain boundaries of the $CuPc_6$ layer is generally described by the Levinson model in the form [49]:

$$I_{DS} = \mu_0 V_{DS}\frac{W}{L}C_i V_G \exp\left(-\frac{q^3 N_g^2 t}{8\varepsilon_0\varepsilon_{pc}kTC_iV_G}\right), \qquad (6)$$

where $\mu_0$ is the trap-free mobility. Figure 6 shows the Levinson plots of $\ln(I_{DS}/V_G)$ versus $1/V_G$. Values of $8.79 \times 10^{12}$ and $4.21 \times 10^{11}$ cm$^{-2}$ for $N_g$ were obtained from the slopes of the best linear fits for the CuPc-based OFETs without and with OTS treatment. They indicate a one order of magnitude reduction in the grain-boundary trap density upon the OTS surface treatment of the gate dielectric. Values of $9.34 \times 10^{-2}$ and $8.45 \times 10^{-3}$ cm$^2$ V$^{-1}$ s$^{-1}$ for $\mu_0$ were obtained for untreated and OTS treated devices, respectively, from the intercepts of the Levinson plots.

Electrical measurements were repeated on OFETs that had been stored in the open laboratory environment for

**Table 1.** OFET parameters measured for the gate without and with OTS treatment.

| $CuPc_6$ transistors | $\mu_{sat}$ $\times 10^{-2}$ ($cm^2\,V^{-1}\,s^{-1}$) | $V_T$ (V) | Sub-threshold voltage (V decade$^{-1}$) | On/off current ratio | Interface trap density $\times 10^{12}$ ($cm^{-2}$) | Grain-boundary trap density $\times 10^{12}$ ($cm^{-2}$) |
|---|---|---|---|---|---|---|
| Untreated gate | | | | | | |
| As prepared | 0.2 | 3.0 | 3.33 | $\sim 10^4$ | 9.10 | 8.79 |
| 30 days old | 0.3 | 3.5 | 3.45 | $\sim 10^4$ | 9.89 | 9.59 |
| Change (%) | +50 | +16 | +3 | 0 | +8 | +9 |
| OTS-treated gate | | | | | | |
| As prepared | 4.0 | −2.0 | 1.23 | $\sim 10^6$ | 1.30 | 4.21 |
| 30 days old | 4.2 | −2.3 | 1.35 | $\sim 10^6$ | 1.37 | 4.62 |
| Change (%) | +5 | +15 | +9 | 0 | +7 | +9 |

30 days and values of transistor parameters were estimated following the same procedure as before. The results are summarized in table 1. The values of all parameters are similar to those obtained for freshly prepared $CuPc_6$ transistors, in agreement with the AFM data of figures 2(b) and (c). The $CuPc_6$ transistors thus show satisfactory stability to storage. The marginal changes may be related to the oxidation of the active semiconductor layer [50].

## 4. Conclusions

The non-peripherally octa-hexyl substituted copper phthalocyanine $CuPc_6$ was successfully solution processed at room temperature to fabricate an active layer for bottom-gate high-mobility organic field-effect transistors on silicon substrates. When the $SiO_2$ gate was chemically modified with a self-assembled monolayer of OTS, AFM images show that the interactions between the SAM and $CuPc_6$ film produced a compact morphology with larger grains possibly resulting from more overlap between the molecules. This film structure led to reduced grain-boundary scattering, which may partly be responsible for the increased field-effect mobility. The reduction of interfacial states due to the surface treatment improved the transistor performance in terms of a significant increase in the field-effect mobility ($4 \times 10^{-2}\,cm^2\,V^{-1}\,s^{-1}$) and on–off ratio ($10^6$), and a decrease in subthreshold slope ($1.23\,V\,decade^{-1}$) and hysteresis. These values compare very well with previously published data. The exploitation of solution-processable substituted phthalocyanine molecules, therefore, provides an alternative strategy for developing high-mobility organic electronic devices.

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