www.crt-journal.org

Crystal Research and Technology

Journal of Experimental and Industrial Crystallography
Zeitschrift für experimentelle und technische Kristallographie

Established by
W. Kleber and H. Neels

Editor-in-Chief
W. Neumann, Berlin

Consulting Editor
K.-W. Benz, Freiburg

Editor's Assistant
H. Kleessen, Berlin

Editorial Board
R. Fornari, Berlin
P. Görnert, Jena
M. Watanabe, Tokyo
K. Sangwal, Lublin

WILEY-VCH

REPRINT

Cryst. Res. Technol. **46**, No. 8, 795 – 800 (2011) / **DOI** 10.1002/crat.201000711

Synthesis of vertically-aligned GaAs nanowires on GaAs/(111)Si hetero-substrates by metalorganic vapour phase epitaxy

I. Miccoli[1], P. Prete*[2], F. Marzo[1], D. Cannoletta[1], and N. Lovergine[1]

[1] Dipartimento di Ingegneria dell'Innovazione, Università del Salento, Via Monteroni, 73100 Lecce, Italy
[2] Istituto per la Microelettronica e Microsistemi (IMM), Unità di Lecce, Consiglio Nazionale delle Ricerche, Via Monteroni, 73100 Lecce, Italy

Received 31 December 2010, revised 23 March 2011, accepted 2 April 2011
Published online 13 May 2011

Key words GaAs nanowires, III-V/Si hetero-epitaxy, MOVPE, vapour-liquid-solid growth.

We report on the Au-catalysed synthesis of GaAs nanowires on hetero-structured GaAs/(111)Si substrates by metalorganic vapour phase epitaxy. It is demonstrated that the deposition of a 40-50 nm thin GaAs epilayer onto Si guarantees a high percentage of straight and vertically-aligned GaAs nanowires. GaAs epilayers were grown at 400 °C and subsequently annealed at 700 °C. Growth experiments performed on 4°-miscut and exactly-oriented (111)Si substrates show that a higher yield (close to 90%) of vertical nanowires is obtained using miscut substrates, an effect ascribed to the smoother surface morphology of GaAs epilayers on these substrates. Comparison between the cross-sectional shape of nanowires grown on GaAs/(111)Si hetero-substrates and those on (111)A-GaAs and (111)B-GaAs substrates demonstrates that both GaAs epilayers and over-grown nanowires are (111)B-oriented.

© 2011 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

1 Introduction

Nanowires of III-V compound semiconductors are being considered ideal building blocks for the fabrication of novel types of nano-devices, such as bright single-photon sources [1], fast photo-detectors [2], and efficient photovoltaic cells [3,4]. In particular, recent theoretical and experimental studies have shown that dense arrays of nanowires could show both enhanced light absorption and reduced optical reflection [5,6]; these properties, together with the high collection efficiencies of photo-generated carriers expected for such nano-structures [7,8] could lead to the fabrication of nanowire-based solar cells with energy conversion efficiencies significantly greater than that of planar solar cells.

The growth of III-V nanowires on Si wafers, besides leading to a possible integration of nanowire devices based on these optically-active compounds with conventional Si-based electronics, would allow a significant reduction in the cost of materials, an especially important requirement in the field of photovoltaics. Indeed, the direct growth of GaAs nanowires on Si has been successfully reported [9-11], despite the large lattice mismatch between the two materials, thanks to the nanowire proclivity to elastically relieve the applied stress within a few atomic layers from the nanowire/substrate interface. In these studies III-V nanowires were grown on (111)Si wafers by the Au-catalyst assisted (the so-called Vapour-Liquid-Solid, VLS) mechanism [12]. Major issues arising in the use of Si as substrate are however, the high thermal stability of native silicon oxide surface layer [13] and the strong Au-Si chemical interaction [14]. Strict control over Si surface chemical treatments, annealing process, and nanowire growth temperatures was claimed necessary by Bao et al. [10] to obtain well-oriented nanowire arrays directly on Si. However, optimal conditions to achieve vertically-aligned III-V nanowires may turn up elusive (see results below), as they are strongly affected by actual laboratory and reactor ambient conditions: indeed, even trace levels (<1 ppm) of oxygen and humidity in the carrier gas or reactor chamber may influence the high-temperature interaction of Au-catalyst nanoparticles with Si [14,15], leading to modifications of the Au/substrate interface plane orientation and thus nucleation of III-V nanowires along uncontrolled substrate directions.

An alternative route to overcome these issues is based on the preliminary deposition of a very thin GaAs buffer layer onto the Si substrate, thus ensuring a complete chemical separation between Au and Si and

* Corresponding author: e-mail: paola.prete@le.imm.cnr.it

© 2011 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

adequate transfer of the substrate crystallography to the over-grown nanowires [16,17]. In particular, Kang et al. [17] demonstrated that dense arrays of vertically-oriented GaAs nanowires can be grown on 4°-miscut (111)Si hetero-substrates via deposition of a thin GaAs buffer layer. The use of miscut wafers in the GaAs hetero-epitaxy on (100)Si represents a common solution for the reduction of antiphase domains and improvement of GaAs crystallinity [18]. No data have instead, been reported to date on the effect of miscut (111)Si wafers on the properties of the overgrown GaAs epilayers, neither on the advantage of such substrates with respect to exactly-oriented ones in controlling the crystallographic alignment of GaAs nanowires.

In this paper we report on the Au-catalysed synthesis of GaAs nanowires on GaAs/(111)Si hetero-substrates by metalorganic vapour phase epitaxy (MOVPE), using either 4°-miscut or exactly-oriented (111)Si wafers. We study the morphology of GaAs epilayers grown on the two types of substrates and the resulting yields of vertically-aligned GaAs nanowires. Comparisons with the case of direct synthesis onto (111)Si and Ga- or As-terminated (111)GaAs wafers are also presented and discussed.

2 Experimental

GaAs epilayers were grown on Si substrates by low (50 mbar) pressure MOVPE in an Aixtron 200RD reactor, using trimethylgallium (Me_3Ga) and tertiarybutylarsine ($^tBuAsH_2$) as Ga and As precursors, respectively. In this respect, we have shown [19] that the use of $^tBuAsH_2$ in substitution of the toxic arsine, besides ensuring a safer process, allows the growth of GaAs nanowires at temperatures as low as 400 °C with good control of their size and shape. Si wafers either exactly (111)-oriented or miscut 4° towards a $<11\bar{2}>$ direction were used as substrates. They were cleaned in iso-propanol vapours for 1 h, etched at room temperature in diluted (5% by volume in H_2O) HF for 2 min to remove the native surface oxide layer, thoroughly washed in deionised water, and finally blown-dry in 6.0N pure N_2. Immediately (i.e., within 1-2 min) after this treatment the substrates were loaded into the reactor chamber and kept under a pure H_2 flow. To remove possible traces of residual oxides left on the Si surface after the above treatments, the substrates were heat-cleaned at 700 °C for 30 min under H_2. A 10 min annealing under a H_2 + $^tBuAsH_2$ flow was further performed to ensure As stabilisation of the Si surface [20,21]. A relatively thin (40–50 nm) GaAs layer was grown on as-treated substrates for 60 min at 400 °C, under a total 7.0 sl/min H_2 flow and a As:Ga precursors molar flow ratio in the vapour of 5:1; the reactor temperature was then ramped up to 700 °C in a H_2 + $^tBuAsH_2$ atmosphere, and the sample annealed under such conditions for 10 min to smooth down the surface morphology of as-deposited GaAs. The complete sequence of temperature steps and precursors supply during epilayer growth experiments is reported in figure 1.

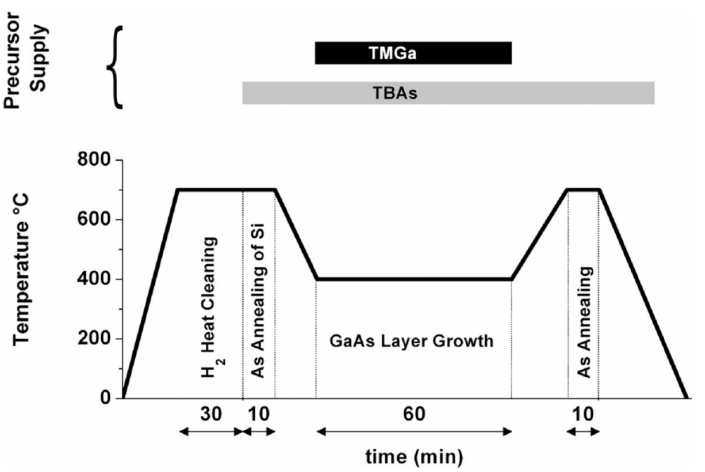

Fig. 1 Process temperature profile and precursors supply sequence during the growth of the GaAs buffer layer on (111)Si.

GaAs nanowires were synthesised on the as-grown GaAs/(111)Si samples and, for the sake of comparison, also on freshly etched (111)B-GaAs, (111)A-GaAs, and exactly (111)-oriented Si substrates (i.e., without the GaAs buffer layer) by Au-assisted MOVPE, using colloidal Au nanoparticles as catalysts for the VLS process. In this case the Si wafers were etched according to procedures reported in [10]. Au nanoparticles were deposited on the various substrates as described elsewhere [19], achieving nanoparticle surface densities around 10^7–

© 2011 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

10^8 cm^{-2}. After loading the as-prepared samples into the reactor chamber, their temperature was raised to 625 °C in a H_2 + ^{t}BuAsH_2 (H_2 in the case of Si) flow, and a sample annealing was performed for 10 min to desorb any residual surface oxides and organic contaminations originating from the Au nanoparticle synthesis. The nanowires were grown at 400 °C [19] (440 °C for the bare Si substrates [10]) using a precursors As:Ga ratio in the vapour of 5:1 and a total H_2 flow rate of 7.0 sl/min.

The surface morphology of as-grown GaAs buffer layers on Si, and that of GaAs nanowires were studied by field emission scanning electron microscopy (FE-SEM) observations using a JEOL microscope model JSM 6500F, with an electron beam acceleration voltage of 15 kV. The sample epitaxial relationships were studied by X-ray diffraction (XRD) patterns recorded in the Bragg geometry using a Rigaku D-Max/Ultima$^+$ diffractometer equipped with a MPA2000 thin-film attachment stage and a Cu-anode X-ray tube.

3 Results and discussion

Figure 2 shows the surface morphology of GaAs buffer layers grown on exactly-oriented and 4°-miscut (111)Si. The two samples were grown in the same experiment. Given the large lattice mismatch between the two materials, the growth of GaAs onto Si is expected to follow a 3-dimensional (Volmer-Weber) growth mode; indeed, we showed elsewhere [22] that the early growth of GaAs onto (111)Si proceeds through the dense nucleation of relatively flat nano-islands, whose lateral growth leads to the progressive coverage of the Si substrate; the surface morphology of the deposit before sample annealing (inset of fig. 2a) is reminiscent of this phenomenon. Noteworthy is also that the high temperature annealing treatment has a smoothing effect on the morphology of all samples. However, after annealing the deposit onto the perfectly-oriented substrate still reveals a high density (about 1×10^8 cm^{-2}) of holes, corresponding to an estimated 96% coverage of the initial Si surface, while the one onto the 4°-miscut substrate shows a complete coverage of the Si surface, and an overall smoother surface.

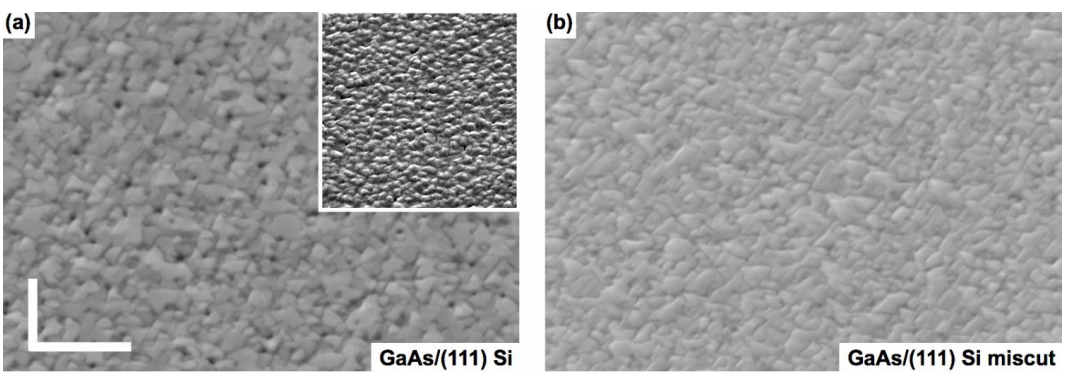

Fig. 2 Surface FE-SEM micrographs (60,000× magnification, 45°-tilt view) of GaAs buffer layers grown on (a) exactly-oriented and (b) 4° miscut (111)Si substrates. Inset in (a): surface morphology of the same GaAs layer before the high temperature annealing. White markers in micrograph (a) represent 1 μm.

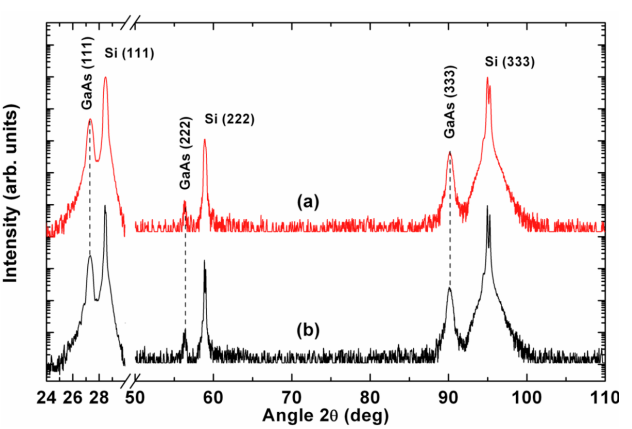

Fig. 3 θ-2θ XRD spectra of as-grown GaAs/(111)Si samples; Si substrates are (a) exactly (111)-oriented, and (b) 4° miscut towards a <11$\bar{2}$> direction. (Online color at www.crt-journal.org)

© 2011 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

The epitaxial relationship between the GaAs layers and the Si substrates is evidenced for both samples above by the high-angle θ-2θ XRD spectrum reported in figure 3. The spectra show only the (111), (222), and (333) diffraction peaks of both GaAs and Si, confirming that the GaAs layers are epitaxially grown along the same [111] direction of the substrate. Noteworthy is the appreciable broadening of the GaAs diffraction peaks with respect to the Si ones, ascribable to the Debye-Scherrer effect; indeed, cross-sectional FE-SEM images of the samples (not reported here) confirmed a GaAs thickness of around 40–50 nm, in quantitative agreement with the observed broadening of XRD peaks. Still, a detailed analysis of GaAs layers performed by recording both XRD pole figures and high-resolution XRD intensity maps around the GaAs [111] reciprocal lattice point reveals that all present layers possess a high degree of mosaicity and a large amount of twinned domains around the materials <111> equivalent lattice directions [22]. Furthermore, the thin layers above appear almost completely relaxed, in agreement with the small value (a few nm) of the critical thickness for the GaAs/Si system.

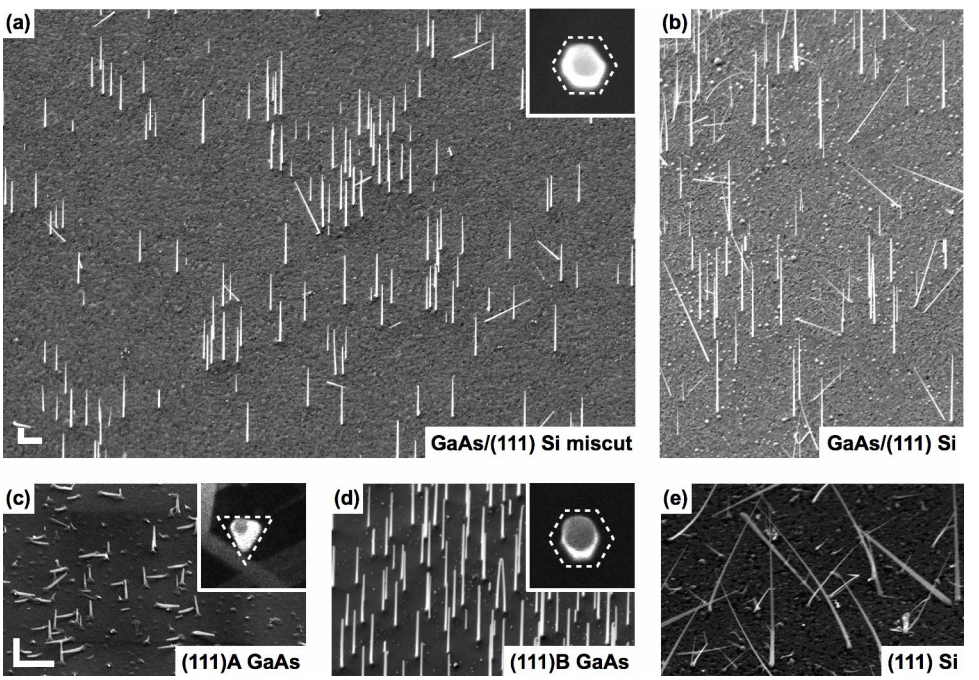

Fig. 4 FE-SEM micrographs (45°-tilt view) of GaAs nanowires grown on (a) 4°-miscut GaAs/(111)Si, (b) exactly-oriented GaAs/(111)Si, (c) (111)A-GaAs, (d) (111)B-GaAs, and (e) exactly-oriented (111)Si. Insets of (a), (c) and (d) are magnified plan-view micrographs of single GaAs nanowires grown on the substrate of the larger image. White markers in micrographs (a) [holding also for (b)] and (c) [holding also for (d) and (e)] represent 1 μm.

Figure 4 shows the morphology of GaAs nanowires grown on either the GaAs/Si hetero-substrates above (Fig. 4a and b) or the (111)A-GaAs, (111)B-GaAs, and (111)Si substrates (Fig. 4c-e). All these nanowires were grown in the same experiment, but those self-assembled directly onto (111)Si. Let us first discuss the latter case: it is noteworthy that despite all attempts made by the present authors to carefully reproduce the Si treatment and growth recipe recommended by Bao et al. [10] to obtain vertically-aligned nanowires, no preferential direction with respect to the substrate surface plane was achieved for these nanowires, some of them appearing also kinked or curled (Fig. 4e); a detailed analysis of the sample FE-SEM micrographs further shows that only a small fraction (1-2%) of the nanowires is aligned with their [111] axis normal to the substrate surface plane. This is in strike contrast to the (111)B-GaAs substrate case, where the yield of straight and vertically-aligned nanowires usually exceeds 99%. We reported elsewhere [14] that the high temperature annealing of Au/Si samples may lead to Au nanoparticles partly embedded in the Si substrate, as result of the partial dissolution of the Si crystal into Au. Upon cooling the samples to lower temperatures, excess Si atoms in the Au nanoparticles, besides being oxidised and evaporated in the form of SiO and/or SiO_2 molecules in the presence of trace oxygen, may also partly redeposit: this leads to the formation of a concave nano-facetted Au/Si interface, each nano-facet being parallel to a {n11} plane of Si. We suggest that these nano-facets give

© 2011 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

rise then to the VLS nucleation of GaAs nanowires with their axes along several alternative directions (as indeed observed in figure 4e), depending on the actual shape and crystallographic orientation of the Au-Si interface below each Au nanoparticle.

A significant improvement is however, observed for nanowires grown on the GaAs/Si hetero-substrates. In fact, a high fraction (~65%) of vertically-aligned nanowires is obtained when using exactly-oriented (111)Si substrates (Fig. 4b), which further increases up to ~87% for the 4°-miscut substrates (Fig. 4a). Noteworthy is also that the latter figure is higher than that (~75%) reported by Kang et al. [17] for nanowires synthesised onto similarly-grown (but un-annealed) single GaAs buffer layers on 4°-miscut Si substrates, and comparable to the 85% yield obtained by the same authors upon deposition of a second GaAs layer at 700 °C. While Kang et al. ascribed the improvement in the vertical-nanowire yield for the double GaAs layer case to a combination of its reduced defects content and better surface smoothness [17], present result emphasises that the latter is likely the most critical factor in determining the fraction of vertical nanowires. In this regard, the significant discrepancy observed in the yield of vertical nanowires grown on the GaAs/Si hetero-substrates, between using exactly-oriented and 4° miscut Si wafers, should be mostly ascribed to the different buffer layer morphologies. A further increase of the vertical-nanowire yield is thus expected upon decreasing the surface roughness beyond that achieved for present buffer layers.

Finally, it is well-known that the cross-section of GaAs nanowires homo-epitaxially grown on a GaAs substrate depends on the underlying substrate crystal polarity: this is demonstrated by the inset of figure 4c-d showing that GaAs nanowires vertically-grown on (111)A-GaAs exhibit triangular cross-sections with side edges normal to one of the three $<11\bar{2}>$ equivalent in-plane substrate directions, while nanowires grown on (111)B-GaAs exhibit hexagonal cross-sections, with side edges normal to one of the three $<11\bar{2}>$ or the three $<\bar{1}\bar{1}2>$ in-plane substrate directions [19]. We observed hexagonal cross-section for all GaAs nanowires grown onto the GaAs/Si hetero-substrates (inset of fig. 4a) with their side edges normal to one of the three $<11\bar{2}>$ or the three $<\bar{1}\bar{1}2>$ in-plane substrate directions, indicating that these nanowires, and thus also the underlying GaAs buffer layers, are always (111)B-oriented. This finding rules out the occurrence of antiphase domains in the present GaAs epilayers.

4 Conclusion

We reported on the growth by Au-catalysed MOVPE of GaAs nanowires on GaAs/(111)Si hetero-substrates, using either 4°-miscut or exactly-oriented (111)Si wafers and, for the sake of comparison, on bare (111)Si and (111)A- or (111)B-oriented GaAs substrates. GaAs epilayers were grown on Si in a single step at 400 °C and subsequently annealed at 700 °C under As-rich atmosphere to smooth down their surface roughness. While direct synthesis of GaAs nanowires on (111)Si does not lead to nanowires of well-defined alignment, pre-deposition of a 40-50 nm thin GaAs buffer layer appears critical to obtain the growth of vertically-aligned nanowires. The yield of vertical nanowires reaches then ~65% for GaAs epilayers grown onto exactly-oriented (111)Si wafers, but increases above ~87% for the 4°-miscut wafers. Such difference is ascribed almost entirely to the smoother surface morphology of GaAs epilayers grown on the latter substrates. Finally, the hexagonal cross-sections observed for GaAs nanowires grown on the GaAs/(111)Si hetero-substrates indicates, by comparison with the homoepitaxy case, that both buffer layers and over-grown nanowires are (111)B-oriented.

Acknowledgements The authors would like to acknowledge Nano Grass Solar, llc. (Philadelphia, PA) for the partial financial support of this work.

References

[1] M. T. Borgström, V. Zwiller, E. Müller, and A. Imamoglu, Nano Lett. **5**, 1439 (2005).
[2] H. Pettersson, J. Trägårdh, A. I. Persson, L. Landin, D. Hessman, and L. Samuelson, Nano Lett. **6**, 229 (2006).
[3] H. Goto, K. Nosaki, K. Tomioka, S. Hara, K. Hiruma, J. Motohisa, and T. Fukui, Appl. Phys. Expr. **2**, 035004 (2009).
[4] C. Colombo, M. Hei, M. Grätzel, and A. Fontcuberta i Morral, Appl. Phys. Lett. **94**, 173108 (2009).
[5] L. Hu and G. Chen, Nano Lett. **7**, 3249 (2007).

 © 2011 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

[6] L. Tsakalakos, J. Balch, J. Fronheiser, M.Y. Shih, S. F. LeBoeuf, M. Pietrzykowski, P. J. Codella, B. A. Korevaar, O. Sulima, J. Rand, A. D. Kumar, and U. Rapol, J. Nanophoton. **1**, 01355 (2007).
[7] B. M. Kayes, H. A. Atwater, and N. S. Lewis, J. Appl. Phys. **97**, 114302 (2005).
[8] Y. Zhang, L.W. Wang, and A. Mascarenhas, Nano Lett. **7**, 1264 (2007).
[9] T. Mårtensson, C. P. T. Svensson, B. A. Wacaser, M. W. Larsson, W. Seifert, K. Deppert, A. Gustafsson, L. R. Wallenberg, and L. Samuelson, Nano Lett. **4**, 1987 (2004).
[10] X. Y. Bao, C. Soci, D. Susac, J. Bratvold, D. P. R. Aplin, W. Wei, C. Y. Chen, S. A. Dayeh, K. L. Kavanagh, and D. Wang, Nano Lett. **8**, 3755 (2008).
[11] V. Khorenko, I. Regolin, S. Neumann, Do, Q.T. Prost, W. Prost, and F.-J. Tegude in: Procs. of the 2005 Intern. Conf. on Indium Phosphide and Related Materials, Glasgow, Scotland, (UK), May 2005, pp. 363-366.
[12] R. S. Wagner and W. C. Ellis, Appl. Phys. Lett. **4**, 89 (1964).
[13] H. Döschern, S. Brückner, and T. Hannappel, J. Cryst. Growth (2010), in press.
[14] E. Piscopiello, L. Tapfer, M. Vittori Antisari, P. Paiano, P. Prete, and N. Lovergine, Phys. Rev. B **78**, 035305 (2008).
[15] P. Prete and N. Lovergine, MOVPE self-assembly and physical properties of free-standing III-V nanowires, in: Nanowires, Ed. P. Prete (Intech, 2010).
[16] S. Roddaro, P. Caroff, G. Biasiol, F. Rossi, C. Bocchi, K. Nilsson, L. Froberg, J. B. Wagner, L. Samuelson, L. E. Wernersson, and L. Sorba, Nanotechnology **20**, 285303 (2009).
[17] J. H. Kang, Q. Gao, H. J. Joyce, H. H. Tan, C. Jagadish, Y. Kim, D. Y. Choi, Y. Guo, H. Xu, J. Zou, M. A. Fickenscher, L. M. Smith, H. E. Jackson, and J. M. Yarrison-Rice, Nanotechnology **21**, 035604 (2010).
[18] Y. B. Bolkhovityanov and O. P. Pchelyakov, Physics Uspekhi **51**, 437 (2008).
[19] P. Paiano, P. Prete, N. Lovergine, and A. M. Mancini, J. Appl. Phys. **100**, 094505 (2006).
[20] M. Kawabe, T. Ueda, and H. Takasugi, Jpn. J. Appl. Phys. **26**, L114 (1987).
[21] J. R. Patel, P. E. Freeland, M. S. Hybertsen, D. C. Jacobsen, and J. A. Golovchenko, Phys. Rev. Lett. **59,** 2180 (1987).
[22] I. Miccoli, P. Prete, L. Tapfer, and N. Lovergine, J. Appl. Phys., submitted (2011).

© 2011 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim