RIVER Architecture

Reconfigurable Pre-Synthesized-Streaming Architecture for Signal Processing on FPGAs

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- **Pre-Synthesized**
- **Real-Time streaming**
- **High-bandwidth**

Performance

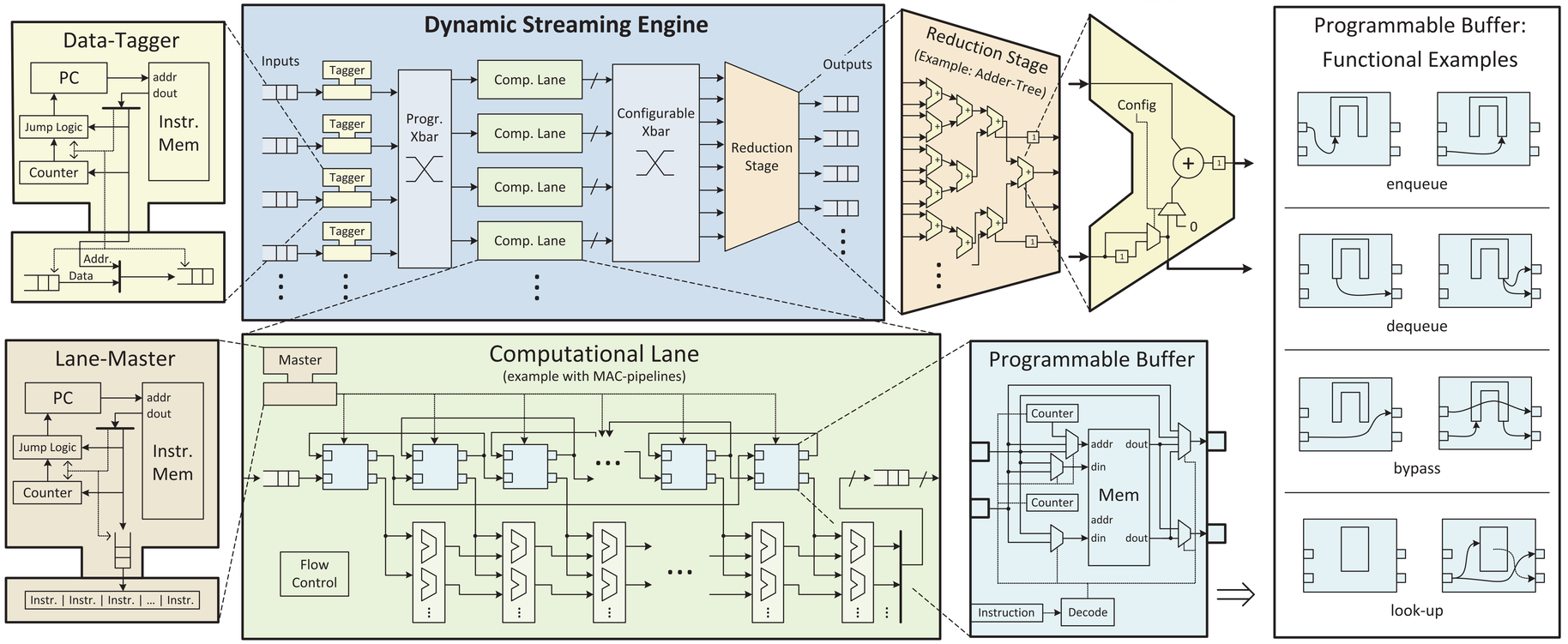
8-core DSE	**250** GMACs
4-core TI TMS320C6670 DSP	**154** GMACs
Tensilica ConnX BBE64	**128** GMACs
Tesla C2050 (Fermi)	**589** GMACs

Frequency
- 145 MHz (8-Core DSE)
- 300 MHz (individual cores)

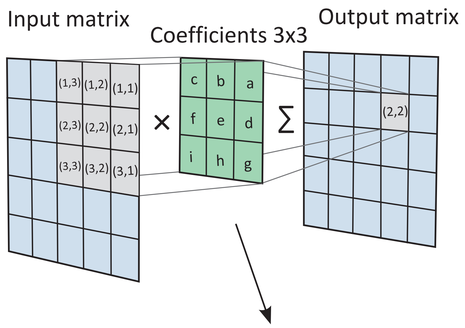
Area 51% of a Virtex 7 (XC72000T)

Bandwidth 10 GB/s

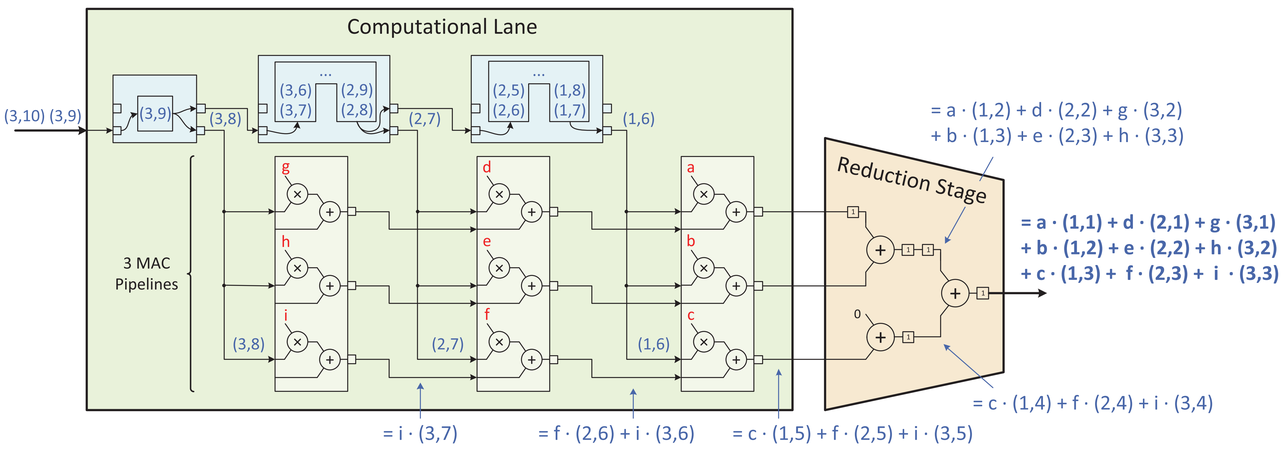
Dynamic-Streaming-Engine (DSE)



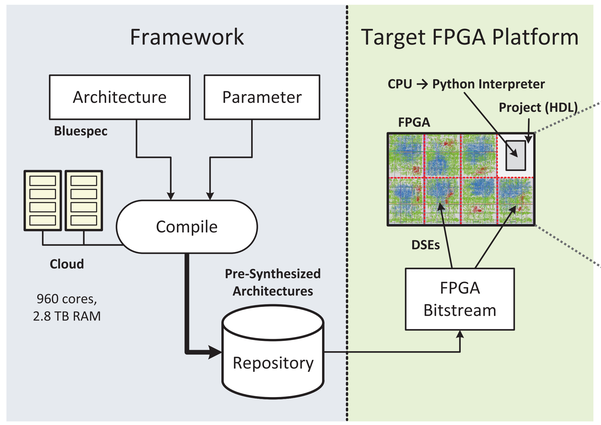
2D - Convolution Filter



Example: Mapping 3x3 filters to DSEs



Design Flow



8-core DSE