Measuring the coefficient of thermal expansion of silicon carbide thin films using digital image correlation

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Motivation

Silicon carbide (SiC) is an attractive material for high-temperature MEMS applications due to its superior mechanical properties, chemical inertness and electronic properties at elevated temperatures. Within the BMBF project *SiC-Tech*, polycrystalline LPCVD and amorphous PECVD SiC films with thicknesses ranging from 1 to 3 µm are fabricated and investigated for high temperature sensor applications.
With respect to thermal stresses, the coefficient of thermal expansion (CTE) is of great importance. The common methods for bulk materials for analyzing the CTE which are rod-based dilatometry and X-ray diffraction, cannot be applied for SiC thin films due to their small thickness and amorphous structure, respectively. Therefore, we use digital image correlation (DIC) to measure the in-plane displacement as a function of temperature and hence calculate the CTE for specially designed SiC test-structures.

Design and fabrication of chip based test structures

Silicon wafers with 150mm diameter are used for the deposition of the SiC thin films. Based on FEM simulations, we chose two different types of freestanding SiC test-structures: a single clamped beam and a square plate suspended by four cantilevers (Fig. 1). In case of SiO_2 as the sacrificial layer, additional etch holes are included in the mask layout.
The basic process flow for the fabrication of the test structures is shown in Fig. 2. We start with a Si-wafer and firstly deposit the sacrificial layer followed by the deposition of the SiC layer. The SiC is structured by RIE after the photolithography has been performed. Afterwards the sacrificial layer release follows. In case of SiO_2 we use HF vapor etching and for SiGe a highly selective dry etching process based on ClF_3 [1]. Finally, FeO particles are sprayed on top of the surface for a better contrast in the DIC procedure.

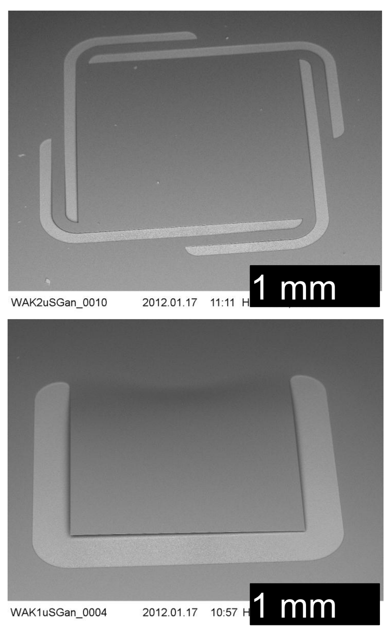
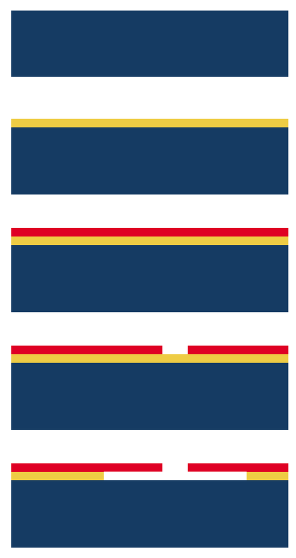


Fig. 1 SEM images of the released test structures

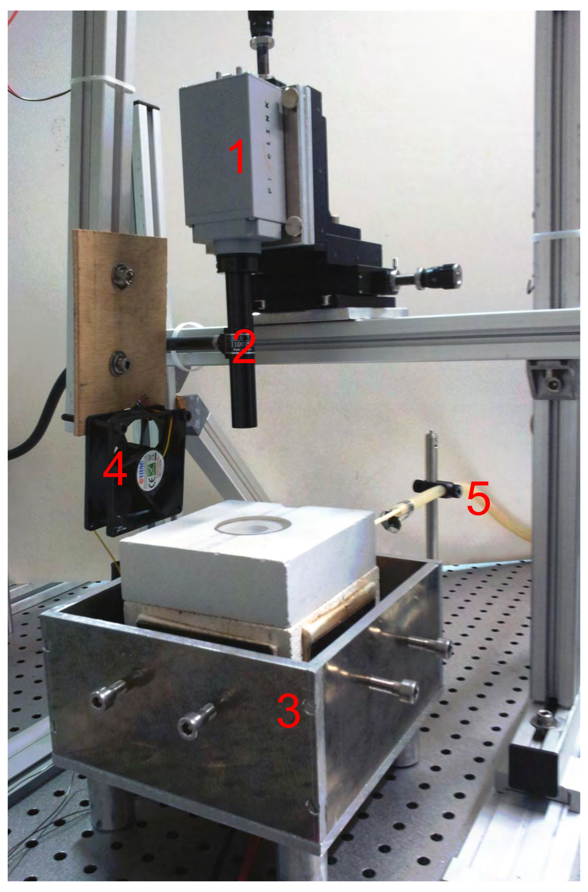


1. Starting with a 150mm Si-substrate
2. Sacrificial layer deposition (SiGe / SiO_2)
3. SiC deposition
4. Photolithography and SiC structuring (RIE)
5. Sacrificial layer release ($ClF3$ / HF vapor)

Fig. 2 Basic process flow for the fabrication of the test structures

Measuring CTE with digital image correlation in a custom build setup

Custom-build Setup:



1 Camera (6 MP)
2 Telecentric optic (4x)
3 Furnace (RT-1300 K)
4 Fan
5 Supply inert gas (Ar,N_2)

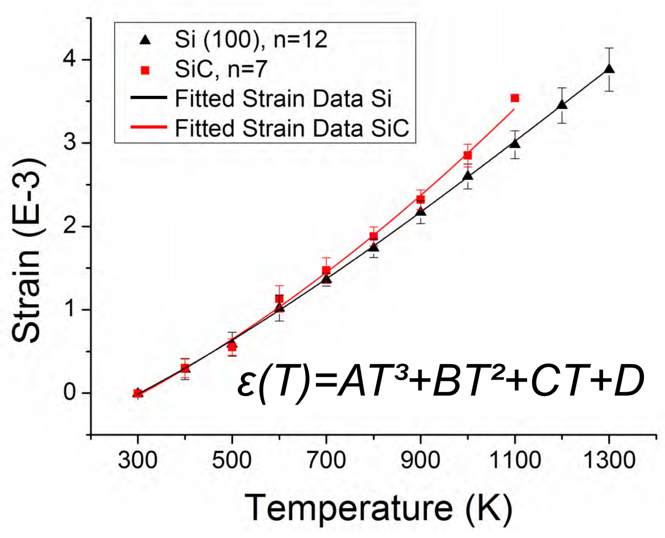
General Procedure:

Stepwise heating and image capturing

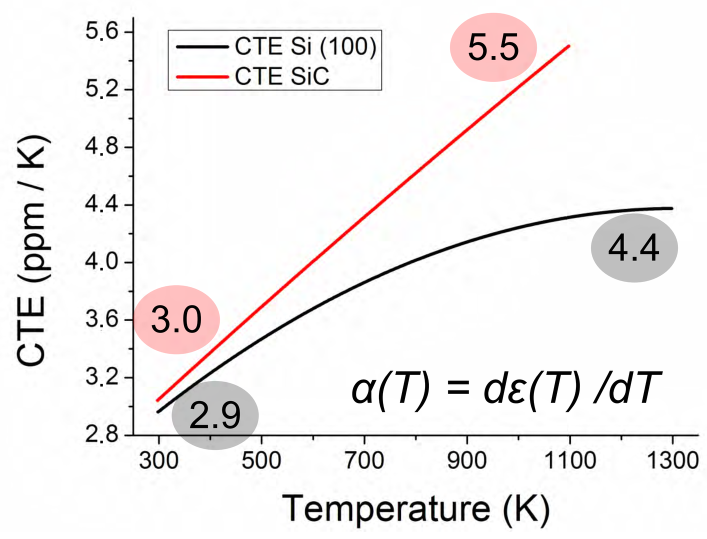
Strain calculation by DIC with a free MATLAB code [2]

Fitting process and calculation of CTE:
$\alpha = d\varepsilon(T) / dT$

Results Thermal Strain:



Results CTE:



Factors influencing DIC measurements at high temperatures:

- Image rotation leads to artificial strains in the DIC process due to the projected geometry → Image rotation is corrected in a post process.
- Out-of-plane displacement leads to artificial strains with normal lenses → telecentric lenses are used. In addition, the sample holder is made of fused silica with low CTE and is mechanically decoupled from the furnace in order to minimize the effect of expansion in out-of-plane direction.
- Contrast changes with temperature due to the infrared (IR) radiation → A high power in-line illumination is used to outshine the IR radiation to achieve a constant illumination.
- Index of refraction changes locally in the surrounding air above the viewport, resulting in high noise and image distortions → a fan is used to randomize the refraction changes.
- Index of refraction of the viewport itself is changing with temperature leading to systematic errors → The system is calibrated with single-crystalline Si (100).

Summary & Outlook

- For characterizing the CTE of SiC thin films, we designed special teststructures and implemented a custom build setup to measure the in-plane displacement by DIC as a function of temperature.
- The CTE of SiC thin films was found to be higher compared to Si and increases from 3.0 ppm / K at room temperature to 5.5 ppm / K at 1100 K.
- In future, microtensile tests at elevated temperatures will be performed to characterize the (thermo-) mechanical properties such as the yield strength, Young's modulus and creep effects of SiC thin films.

Acknowledgment

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References

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[2] C. Eberl, D.S. Gianola and R. Thompson, *MatLab Central (Natick, MA: The Mathworks, Inc., 2006), File* ID:12413