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The Trigger Unit for the Detector Array of the KASCADE Experiment

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Abstract

The Trigger Unit for the Detector Array of the KASCADE Experiment

The Trigger electronics for the array part of the KASCADE experiment is presented. The logical functions of the devices together with the hardware implementation are described. The links to the frontend modules and to the transputer network of the array electronics are shown.

Zusammenfassung

Die Trigger Einheit für das Detektor Array des KASCADE Experiments

Die Triggerelektronik für den ausgedehnten Array -Teil des KASCADE Experiments wird dargestellt. Die logischen Funktionen der Moduln und die hardwaremäßige Implementierung werden beschrieben. Die Verknüpfungen der Triggereinheit mit der modularen Frontendelektronik sowie mit dem Transputernetz der Array - Elektronik werden erläutert.

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Chapter 1

Introduction

KASCADE is a new experiment being under construction at the Kernforschungszentrum Karlsruhe since 1990 [1]. Its objective is to study cosmic ray extensive air showers induced by high energy particles above 10^{14}eV. Its main goal is to obtain information on the chemical composition of the primary cosmic rays. In addition, the arrangement will be able to identify point sources of energetic neutral particles in the quoted energy range.

The experimental setup consists of an extended array of detector stations with more than 1000 scintillation detectors, spread on a square of 40 000 m^2 , and of a central detector with 16x20 m^2 lateral size for the detection of high energy hadrons and muons, especially in the cores of the extensive air showers.

A detailed description of the KASCADE experiment is given in [1,2].

The array consists of 252 detector stations positioned on a rectangular grid of 13 m grid size. They are grouped in 16 clusters, each of them having 16 (15 around the central detector) detector stations. A cluster is a basic subunit of the array and on its level the acquisition of the experimental data collection is organized in the form of the cluster electronics.

Chapter 2

Array Cluster

2.1. Cluster Layout

The layout of a cluster is shown in fig.1. All 16 detector stations, grouped in 4 quadrants, are connected with the cluster electronics station. All signal cables leading there are of equal length and put in tubes underground, as indicated in fig.1 [2]. Details of the detector station design are shown in fig.2 and may be found in [3]. In the station there are 4 electron/gamma detectors, marked A, B, C, D and four muon detectors below them, shielded by an absorber plate of 10 cm of lead and 4 cm of steel.

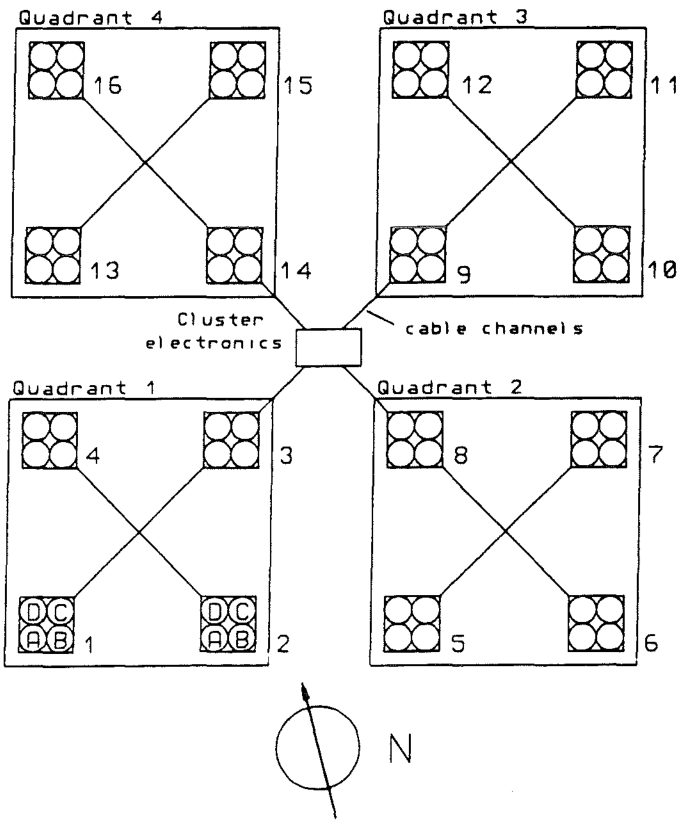

Fig. 1. Sixteen detector stations groupped as a cluster

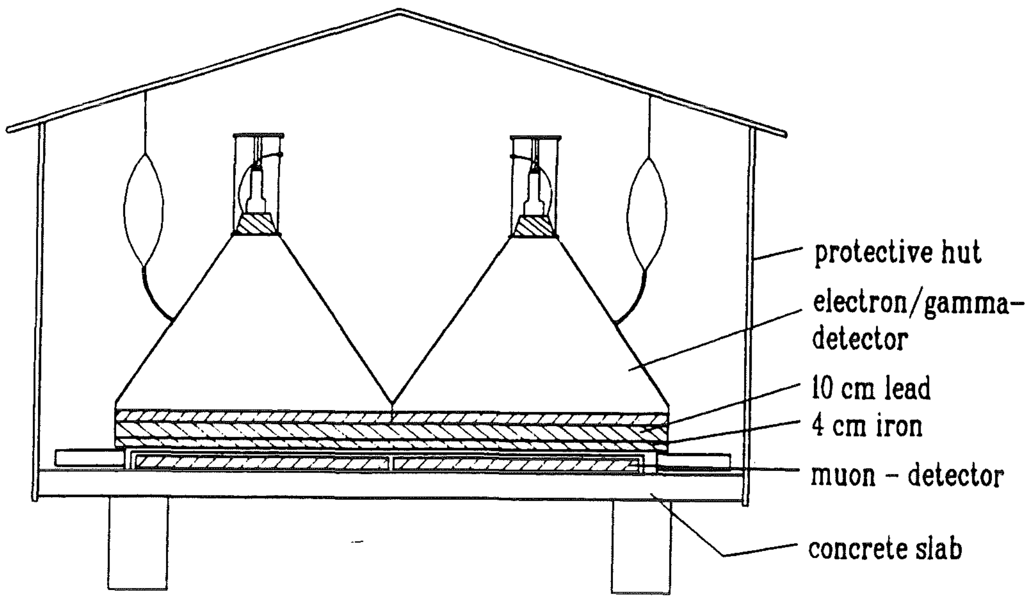

Fig.2. Schematic view of a station of the KASCADE array

2.2. Cluster electronics

The cluster electronics is based on the general philosophy, that each cluster of the KASCADE array acts as a small independent air shower experiment [2]. Data from different clusters are correlated by means of a common clock (time label) running synchronously in each cluster. All detector signals above the hardware threshold level are converted into temporary data containing the time label. The determination of an 'event' is done by the trigger electronics, which generates a trigger (EVENT) signal, when a certain multiplicity condition in the cluster is fulfilled.

The structure of the cluster electronics is shown in fig.3. It is housed in two VME crates, both controlled by TVC (Transputer-based VME Controller) modules, designed by H.Leich from DESY-IfH Zeuthen . The upper crate contains a HV control module, a clock module and the Trigger Unit (TU), occupying 6 VME slots. Crate 2, the lower one, is a frontend electronics crate housing 8 KAFE (KASCADE Array Frontend Electronics) modules for signal processing from all of the 16 array stations. A summary of the KAFE functions may be found in [2,p.10-11] .

In general, a KAFE module acquires signals from the station detectors, converts them into digital form and stores data temporarily in a FIFO (first-in-first-out) memory including the time labels. At the same time the signals exceeding the preset discriminator thresholds pass through pulse shapers and are sent to the Trigger Unit via the Trigger Bus (figs. 3&4). Upon recognition of the software defined shower condition the TU sends an EVENT signal to the TVC1, which sends a message to the TVC2 to start the search for data belonging to the detected event in its memory. These data have been readout from the FIFOs and stored in the memory of the TVC2 in a continuous polling procedure.

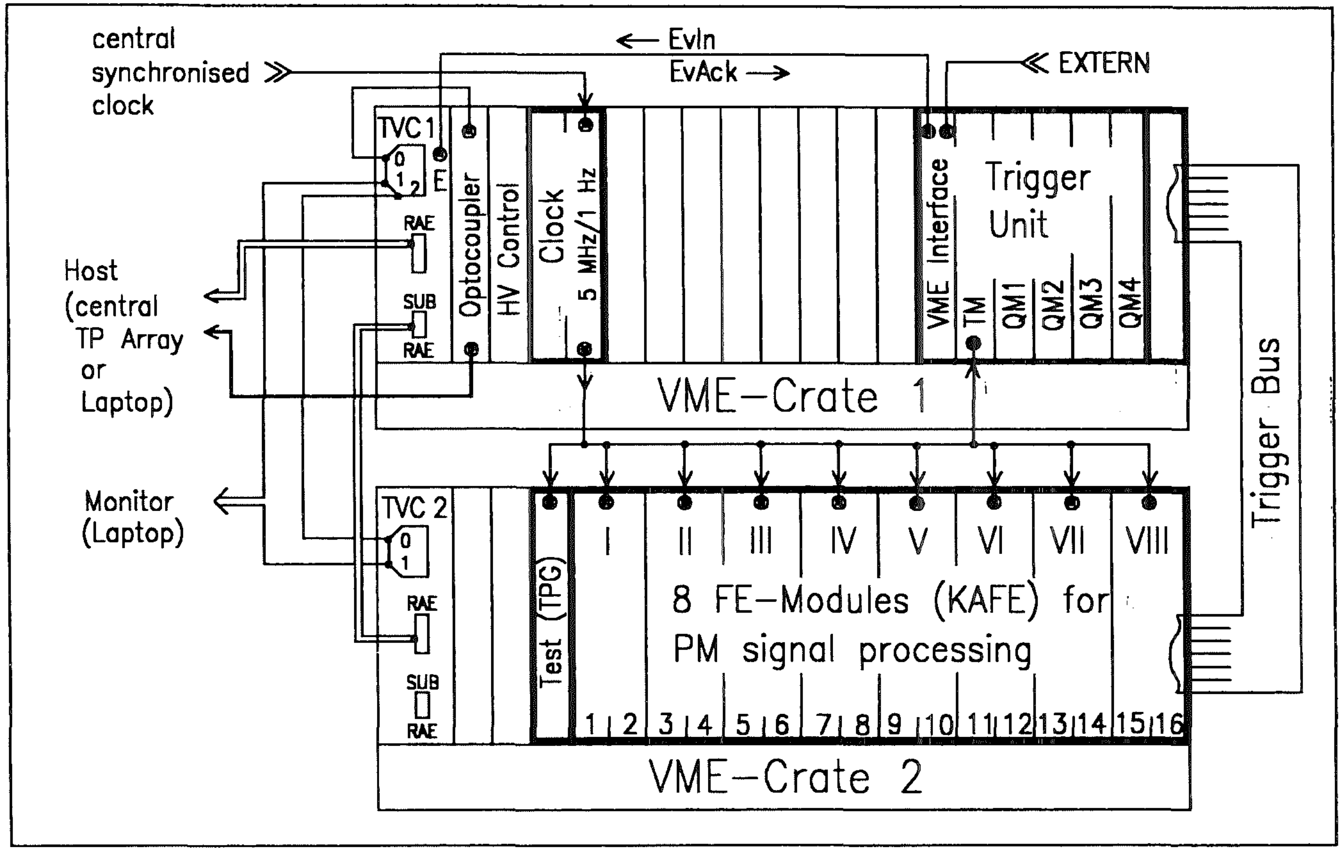

Fig.3. Structure of the Cluster Electronics

Chapter 3

Trigger Unit

3.1. General description

The Trigger Unit has to perform the following tasks:

- Detection of air shower events by checking the fulfillment of one or both of the following conditions:
  - **L**ocal **H**igh **D**ensity (LHD) condition
  - **C**luster **H**igh **D**ensity (CHD) condition,
- Identification of **S**ingle **M**uon (SM) events for calibration of the e/γ– and the muon detectors,
- Detection of rare local events -- **S**ingle **H**igh **D**ensity (SHD) condition,
- Tracing the system CLOCK time (**T**ime **L**abel -- TL) and the Modified **J**ulian **D**ate.

Fig.4 shows the functional block diagram of the TU, corresponding to the task list above. There are two types of modules :

1. Task modules:
- LHD
- CHD
- SHD
- SM
- Clock & Julian Date
- Control

2. Registers:
- Status Register (SR)
- Local High Density Pattern Word (LHDPW) register
- Cluster Flag Register (CFR)
- Single Muon Flag Register (SMFR)
- Single Muon Suppression Factor Register (SMSFR)
- Time Label 1 (TL1) register
- Time Label 2 (TL2) register
- Julian Date Register (JDR)

The task modules receive the signals from the KAFE modules via the **Trigger Bus**. For every detector station there are 9 digital (TTL, active LOW) signals supplied. As mentioned in 2.2

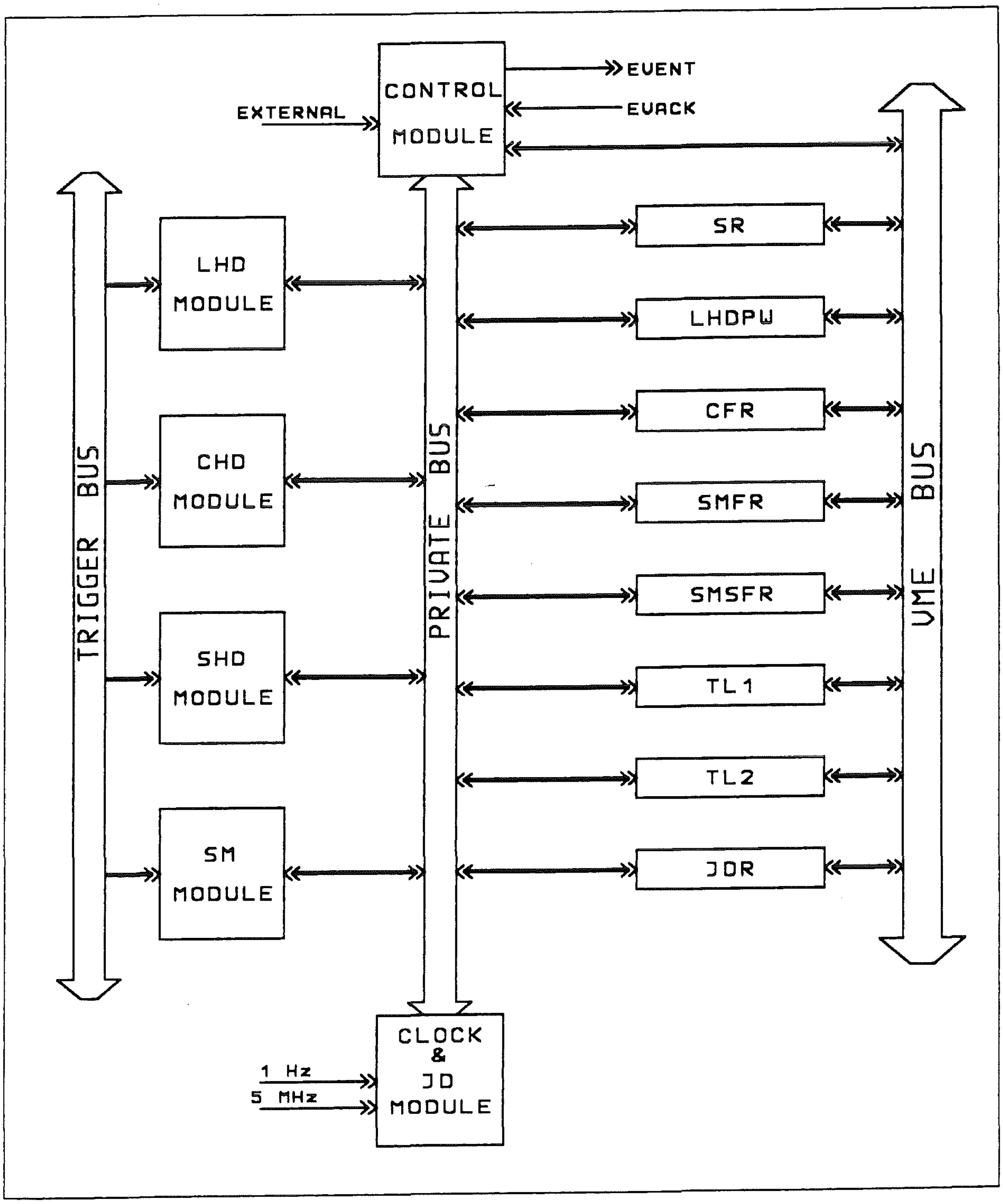

Fig.4. Functional block diagram of TU

above, their presence means, that in the corresponding scintillation detector the pulse amplitude exceeded the preset discriminator level.

These signals are:

- **T1, T2, T3, T4** - from the **A, B, C** and **D** e/γ detectors respectively,
- **Tm1, Tm2, Tm3, Tm4** - from the muon detector PM tubes **1, 2, 3,** and **4** resp.,
- **Dy** - from the sum of dynode signals of the e/γ detectors in a station.

The task modules exchange data between themselves and communicate with the registers via the **Private Bus**. Registers are accessed from the **VME Bus**.

3.1.1. Local High Density Module

One of the defined air shower conditions is the presence of a certain density of particles in the e/γ detectors in a station (the gate for coincidence in the frontend electronics is open for ~ 270 ns after arrival of the first detector signal in the station). The LHD module is just a part of the TU, detecting such local high densities of particles.

The required levels of densities may be changed by software means (loaded to SR). It has been decided to use only three values: "2 out of 4 detectors hit" or "3 out of 4 detectors hit" or "4 out of 4 detectors hit".

This condition, once preset, is valid for all 16 stations in a cluster. The logical decisions are performed on the **T** signals.

Upon detection of such density in at least one station the TU sends a LHDI pulse to the Control Module and loads the LHDPW register with the data showing, which stations have detected a "high density" of particles.

The Control Module latches the Time Label value in the TL1 register and the Julian Date value in the JDR, produces a VETO signal for the TU logic and sends an EVENT signal to the TVC1. The TVC then starts to readout SR, LHDPW, CFR, TL1 and JDR and sends back an Event Acknowledge (EVACK) signal, canceling the VETO status of the TU. The Cluster Flag Register is read also since the TVC does not know in advance the source of the EVENT signal.

The LHD condition may be switched off by software.

3.1.2. Cluster High Density Module

This module checks for the main air shower condition, i.e. that in the whole cluster N **out of** the **64** e/γ detectors "simultaneously" (with existing gate open time and array size it means " in about 400 ns time interval") have registered particles. The value of N is software controlled and is stored in the Cluster Multiplicity Bits of the Status Register. Logical decisions are made also on the **T** signals. Detecting at least N of **T** signals the CHD module sends a CHDI pulse to the Control Module and stores in the Cluster Flag Register (CFR) the number of e/γ detectors being hit by particles of the shower.

The Control Module latches the Time Label value in TL1 register and the Julian Date value in JDR, produces a VETO signal for the TU logic and sends an EVENT signal to the TVC1. Again, the TVC reads out the registers SR, LHDPW, CFR, TL1 and JDR, and sends back the Event Acknowledge (EVACK) signal, cancelling the VETO status in the TU. By similar reasons as in 3.1.1 the LHDPW is read here also.

The CHD condition may be switched off by software.

3.1.3. Single High Density Module

The Single High Density module is designed to indicate the possible case, when only one of the e/γ detectors in a station has registered a large number of particles not being correlated with an extensive air shower (a large multiplicity of detector hits).

If a **D** signal comes from a station and nowhere in the cluster the shower conditions are fulfilled (no LHDI or CHDI signals generated) the SHD module sends SHDI signal to the Control Module. In this case the actions of the Control Module and the TVC are the same as described in 3.1.1 and 3.1.2.

Analyzing the contents of the LHDPW and the CFR (they both contain zeros) the TVC software recognizes, that the source of the EVENT signal was a SHDI pulse.

The SHD condition may be switched off by software.

3.1.4. External trigger pulse

The TU is capable to generate the whole event handling routine upon receiving an external trigger signal (see figs.3 & 4).

In such a case the Control Module sets an External Bit in SR, latches the time values in TL1 and JDR and sends an EVENT signal to TVC1. The TU logic is also blocked by VETO. The TVC software, after the readout procedure as described above, examining the SR may discover, that the source of the EVENT was an external signal and undertake the necessary actions.

3.1.5. Single Muon Module

The Single Muon module was designed especially for calibration purposes. Checking valid logical combinations of **T** and **Tm** signals from a station it detects particles (i.e. single muons), passing an e/γ detector and the underlying muon detector pair.

Having detected such a coincidence the SM module sends a SMI pulse to the Control Module and stores in the Single Muon Flag Register (SMFR) information about the corresponding station and detector pair. The Control Module latches the Time Label in TL2 register and presents a SM Interrupt, on one of the VME interrupt lines, to the TVC1. The service routine for this interrupt reads out the TL2 and SMFR data.

The SM interrupt has lower priority than the EVENT signal and, in some cases (if the TVC is busy with shower data), may be not processed at all. No VETO signal is generated in this case.

It is possible to suppress the number of processed single muons by means of loading the SMSFR with the required value. To analyze every **m**-th single muon the SMSFR must be loaded with the binary number equal to 2^{16}- 1 - **m**. In this case only every **m**-th muon will cause the SMI signal to be generated.

3.1.6. Clock and Julian Date Module

The Trigger Unit receives two clock frequencies: 1 Hz and 5 MHz. In the Clock&JD Module they are used in two counters. One is the Time Label clock, counting 5 MHz pulses. Every 1 Hz pulse resets this clock.

Another one is the Julian Date Clock. At the start-up of the experiment it is loaded (via the JDR) with the current Julian Date value, which the TVC1 receives from the central computer. Then it is incremented every second thus keeping track of the Julian Time in the cluster.The Control Module latches the current values of those clocks in registers, as it was stated above.

Every 1 Hz pulse, after incrementing the Julian Date Clock, also latches the new value in the JDR, so the TVC may check it between the events. When VETO is present no such rewriting takes place. The Julian Date Clock runs, of course, all the time.

3.1.7. Control Module

The main task of the Control Module is to provide the VME protocol for all communications with the TVC1 via the VME bus. It also, as it was already mentioned, generates the EVENT and VETO signals, takes care of providing the proper Time Label and Julian Date values for each event. It recognizes an external trigger pulse and undertakes the necessary actions as well.

The Control Module is also responsible for the proper initialization of the hardware on power-up.

3.2. Programmer's model of the Trigger Unit

From the programmer's point of view the TU is a VME slave module, conforming to the VME-bus specification (Revision IEEE-1014-1987). It works in the A24:D16 mode. As an interrupter it is preset to give an IRQ5 interrupt upon acquisition of a single muon calibration event, which is to be processed.

The modules base address has been assigned to FFFE00 (may be changed by switches to any value in the range from 000000 to FFFF00) and the address space is divided into eight 64 bit gaps, each of them corresponding to one of the TU registers.

The address modifier is set to: Standard User Access.

To the TVC in the VME crate the TU presents itself as a set of various registers, which may be accessed in a predefined way and order. A special Trigger Unit Test Program, "TUMAIN", has been written, by means of which all functions of the TU, being available to the TVC, are tested prior to incorporating the TU in a real experimental setup.

Let's discuss now the registers, shown in fig.4, in detail.

3.2.1. Internal registers of the Control Module

Apart from the registers shown in fig.4 there are also internal registers in the Control Module, listed below with their corresponding addresses:

◆ Active Edge Register (AER)	FFFE02
◆ Data Direction Register (DDR)	FFFE04
◆ Interrupt Enable Register A (IERA)	FFFE06
◆ Interrupt Enable Register B (IERB)	FFFE08
◆ Interrupt Mask Register A (IMRA)	FFFE12
◆ Interrupt Mask Register B (IMRB)	FFFE14
◆ Vector Register (VR)	FFFE16

A full description of the internal structure of those registers may be found in [4].

These registers have to be loaded with predefined values every time the power in the crate containing the TU is switched on (initialization of the TU). Below there is a list of these values, together with the description of their meaning.

Register	Value loaded	Meaning
AER	00	High to Low active Edge
DDR	00	All lines are inputs
IERA	00	IRQ5 enabled,
IERB	80	other disabled
IMRA	00	only IRQ5
IMRB	80	unmasked
VR	A0	S=0 (automatic end of interrupt mode),
		A - signature value

3.2.2 Status Register

The status register in TU is a 16 bit wide register.Bits 7, 10 and 11 are not used, and if not being masked in the TVC, they will be read as logical "1".

Bits 0 - 6 are the Cluster Multiplicity Bits. The number N loaded there is a required minimum multiplicity in the event. It may have a value from 1 to 64. Loading **N > 64** switches off the cluster multiplicity condition in the cluster.

Bits 8 and 9 are the Local Multiplicity Bits and the binary number loaded there corresponds to the minimum local (i.e. in one station) multiplicity of e/γ detectors required by the TU to accept an event.

The four possible binary values have the following effect:

- "0" - disables the logic detecting the local multiplicity conditions
- "1" - multiplicity 2 out of 4
- "2" - multiplicity 3 out of 4
- "3" - multiplicity 4 out of 4

Bit 12 is used to disable the SHDI. When it is set (set always means here writing logical "1") a single high density condition will not cause the generation of an EVENT signal. This bit is set and reset by software (via TVC) only.

Bit 13 is set by an external trigger signal connected to TU's front panel. It may be either a trigger from another cluster of detectors, from the Central Detector system or from a test signal. This bit is cleared upon removal of the VETO after serving the EVENT interrupt.

Bit 14 is a Check Bit. It becomes logical "1" if in the time interval between writing a new value to the JDR and canceling the VETO by the **initialization write** to the SR, a "1 Hz" pulse arrived. Since the Julian Date Clock in TU is enabled to be incremented only after this initialization write, it would mean, that the Julian Date value stored in the TU would differ from the real one in the rest of the experiment. In such a case the TVC software undertakes the necessary actions to correct the problem.

This bit has to be reset (to logical "0") by software at the beginning and at the end of the **initialization procedure**, and after any procedure containing the change of the Julian Date value.

Bit 15 is a VETO Bit. In the TU there are two different ways of setting this bit. Depending on the way it was set its resetting is also done in different ways.

First, VETO is set when the TU detects an event, i.e. a Cluster, Local or Single high density condition has been fulfilled. In this case an EVENT signal is being sent to TVC and maintained until the EVACK signal is sent back to TU. Bit 15 is cleared with the trailing edge of the EVACK signal.

If VETO was set by the event conditions it may be removed only by the EVACK signal. No software action will reset bit 15 in the SR in such a case!

Second, between the events, it may be set at any time by the TVC writing "1" to VETO bit 15 in the SR. It is then reset also by the TVC.

When VETO is set, all the logics for the detection of an event condition is disabled. VME interrupts from single muons are disabled in TU as well.

The Status Register is accessed at two addresses in different ways:

FFFE40 - used during initialization write

FFFE42 - used to read/write the SR at any other time.

The initialization write enables the Julian Date Clock to be incremented with "1 Hz" pulses, therefore it must be used always after writing a new value to the JDR (this write operation disables incrementing the Julian Date Clock).

3.2.3. Local High Density Pattern Word Register

This is a 16 bit register containing the information, which station in the cluster has had the multiplicity of e/γ detector hits equal or greater than preset in Local Multiplicity Bits of the SR.

If the local multiplicity condition for a station is fulfilled, then its corresponding bit in the LHDPW register is set:

bit 0 for station # 1,

bit 1 for station # 2, etc.

For the TVC software this is a read-only register, located at the hex address FFFF00.

3.2.4. Cluster Flag Register

This register uses only one byte, the low byte, where in case that the cluster multiplicity event condition is fulfilled, the actual number of the detectors active in the event (the real value of the event multiplicity) is being stored.

For the TVC software this is also a read-only register, located at the address FFFEC0.

3.2.5. Single Muon Flag Register

This register should be discussed in conjunction with the layout of the detectors in the station, shown in the top view in fig.5. In order to register a single muon, passing for instance, through detector A, the TU must check for the coincidence of the following signals :

T1 (A output), Tm1 (PM1 output) and Tm2 (PM2 output).

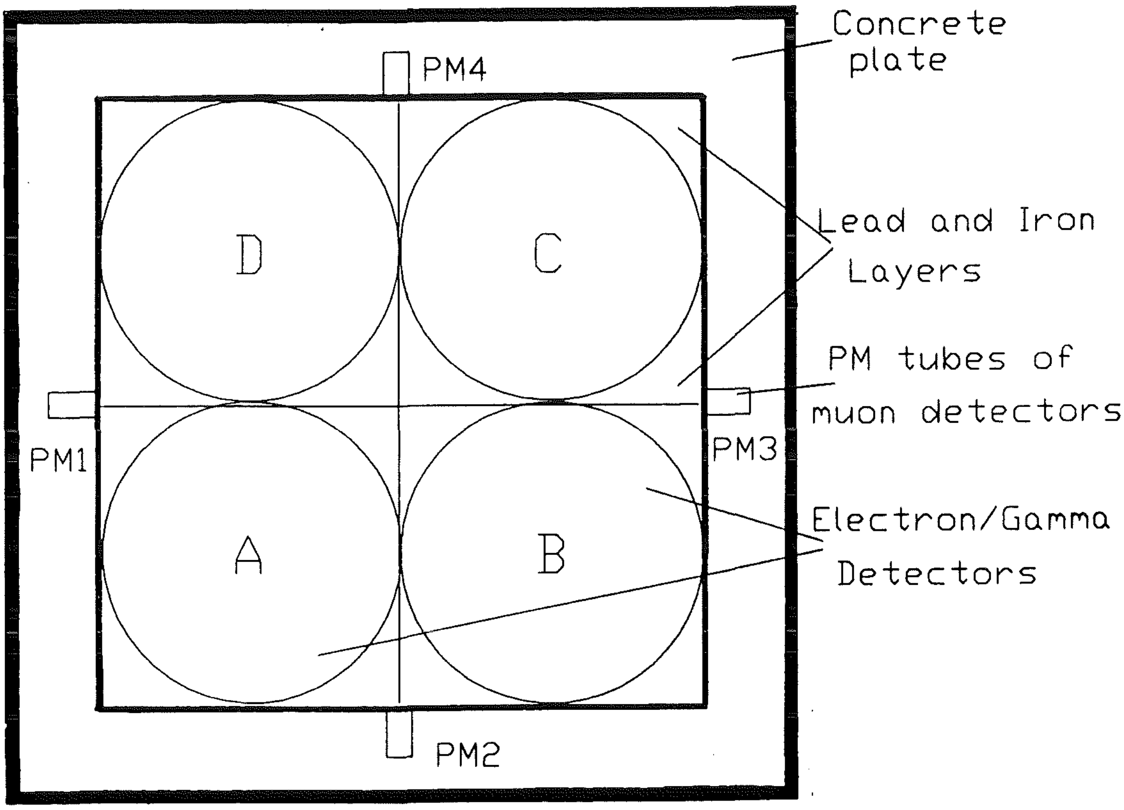

Fig.5. Top view of the detectors in one station

The logic function here contains also the requirement of anticoincidence of all the other signals (only one e/γ detector PM and two corresponding muon detector PMs in coincidence).

The following combinations of coincidences are possible:

- **a** => A +(PM1 & PM2)   [T1+(Tm1 & Tm2)]
- **b** => B +(PM2 & PM3)   [T2 +(Tm2 & Tm3)]
- **c** => C +(PM3 & PM4)   [T3 +(Tm3 & Tm4)]
- **d** => D +(PM4 & PM1)   [T4 +(Tm4 & Tm1)]

These combinations are stored in bits 4 - 7 of the SMFR. An active combination is marked by "1" in its corresponding bit position.

Bits 0 - 3 contain the binary number, describing, to which station this particular single muon belongs. Decimal "0" (0000H) is assigned to the station #1, so decimal "15" (1111H) will point to the station #16 in the cluster. Only the low byte of this 16bit register is used.

For the TVC software the SMFR is a read-only register, located at the address FFFF40.

3.2.6. Single Muon Suppression Factor Register

The purpose of this register is to receive from the TVC a prescaling number for counting the single muons. If the suppression factor is **m**, the TVC must load the SMSFR with the binary number: 2^{16}-1-m.

For the TVC software this is a read/write register, located at the address FFFE80.

3.2.7. Time Label registers (TL1 and TL2)

These registers are 32 bit wide but only the 24 lower bits contain the time label (TL) information. The high byte should be masked.

The TL1 register contains a micro time (in 200 ns steps) information of the internal (local, cluster or single high density condition fulfilled) or external event. For the TVC software it is a read-only register, located at the following addresses: FFFEC0 (low word) and FFFEC2 (high word).

The TL2 register contains the micro time information for the single muon being processed. The structure of this register is the same as of TL1 and its hexadecimal addresses are: FFFFC4 (low word) and FFFFC6 (high word).

3.2.8. Julian Date Register

This is a 32 bit wide register of the read/write type, which , during the initialization, is loaded with the proper Julian Date value.

The current Julian Date is sent to the JDR with every shower event detected and every 1 Hz pulse after actualization (providing that there is no VETO condition in TU).

Writing a new value to the JDR disables incrementing of the Julian Date Clock and only initialization write to the SR, afterwards, enables this function again.

The read/write to the JDR is made in two 16 bit accesses:
at address FFFF80 - low word
at address FFFF82 - high word.

3.3. Hardware implementation

As it was already mentioned (fig.3), the TU is built as a set of six VME modules of single width. Four layer PC-boards of EUROCARD type, size 160 x 230 mm^2, with both P1/J1 and P2/J2 VME bus connectors are used.

A physical structure of the TU, showing the partitioning of the design into separate VME modules together with all external connections, is given in fig.6.

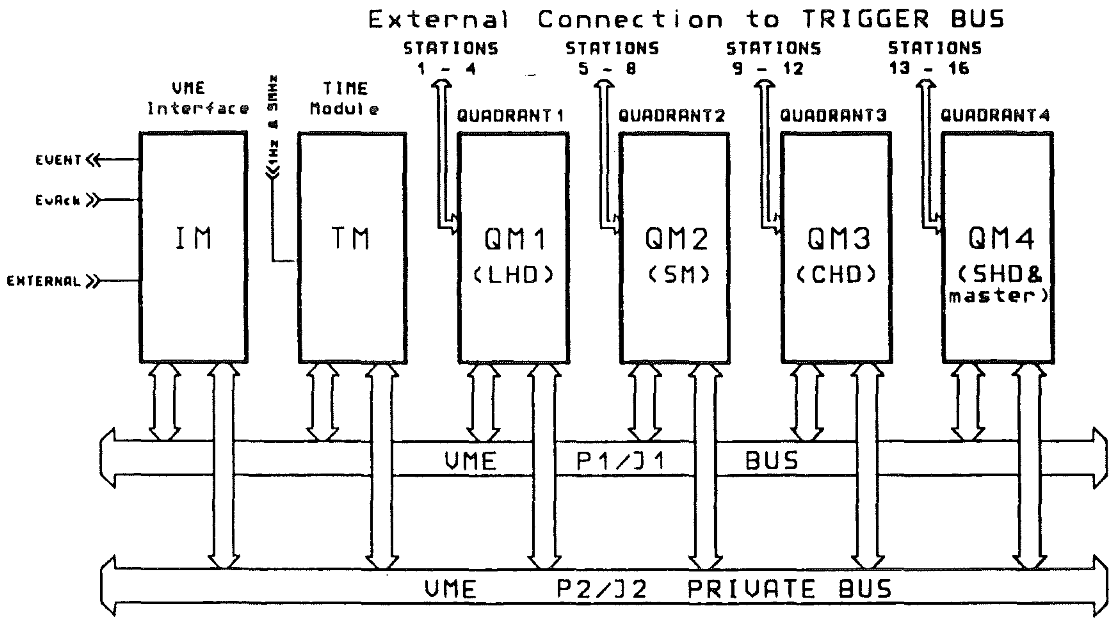

Fig.6. Physical structure of the Trigger Unit

The Trigger Unit consists of the following VME modules:

- Interface Module (IM) - VME interface
- Time Module (TM)
- Quadrant Module 1 (QM1) - main LHD function
- Quadrant Module 2 (QM2) - main SM function
- Quadrant Module 3 (QM3) - main CHD function
- Quadrant Module 4 (QM4) - main SHD & master function

There is no straight correspondence between the functional task modules from fig.4 and the VME modules here. For instance, a subtitle "LHD" in the QM1 module means only, that the main part of the functional LHD Module from fig.4, responsible for the generation of LHDI signal, is located here.

The Control Module circuits are mainly in IM and QM4; however, in fact they are present at every VME module.

All VME modules have access to the VME P1/J1 bus and to the Private Bus, wired on the VME P2/J2 bus.

The Trigger Bus, connecting the QM1 - QM4 modules with the KAFE cards, consists of 16 flat band cables equipped with 24 pin connectors. The sockets for those connectors are on the front panels of the modules. All other external connections are made with coaxial cables using LEMO connectors.

In the following paragraphs a brief description of the design will be presented.

3.3.1. Interface Module

The Interface Module is built using the WRAP-1/68K VME prototyping board from ELTEC [4]. The VME interface on this board is based on the multifunction peripheral (MFP) chip TS68901 from Motorola. The main task of this module is to provide a VME protocol for all the traffic on the VME bus, related to the register read/writes and VME interrupt routine (SM interrupts).

The interface module houses also necessary interface circuits for the connections with the "outer world" (LEMO connectors for EVENT, EVACK and EXTERN signals) as well as two LED indicators on the front panel, one for EVENT (green) and another one for VETO (red).

3.3.2. Time Module

The time module contains both clocks: the Time Label (micro time) Clock and the Julian Date Clock. All three time registers (TL1, TL2 and JDR) are also there. For time keeping purposes two clock frequencies : 5 MHz and 1 Hz are supplied via front panel LEMO connectors from the Clock Module in the crate.

Fig.7 shows a schematic diagram of the Time Label Clock and the Time Label Registers. The clock circuit is built using 74LS161A chips as a 24 bit synchronous binary counter which is incremented by the 5 MHz pulses. Every 1 Hz pulse clears the counter.

The Time Label 1 register is formed by U38, U10 and U40 - 74ALS374 8 bit latches with 3-state outputs. The current micro time value is latched there by TL1SET pulse supplied by the Control Module when an event was detected. The register presents its data to the VME bus when it is addressed by the EN7TL1W0 (low word) and EN7TL1W1 (high word) signals.

The Time Label 2 register (U39, U11, U41) works in similar way latching the time with the TL2SET command for single muon calibration purposes.

The Julian Date Clock is also based on 74LS161A binary counters having capability of being loaded in parallel, which is used when setting the initial value of the Julian Time.

Fig.8 shows a photograph of the Time Module.

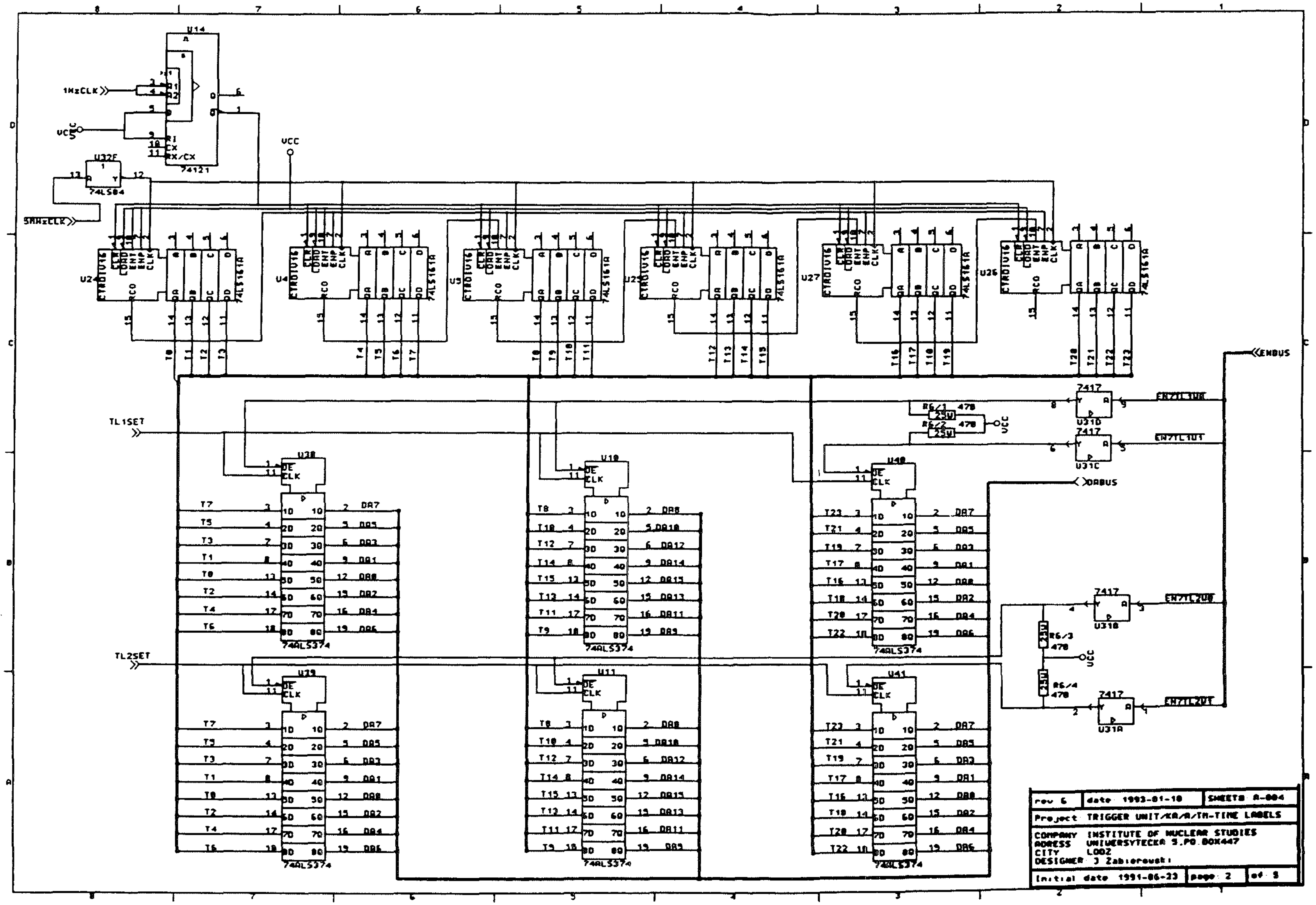

Fig.7. Time Label Clock and Time Label Registers

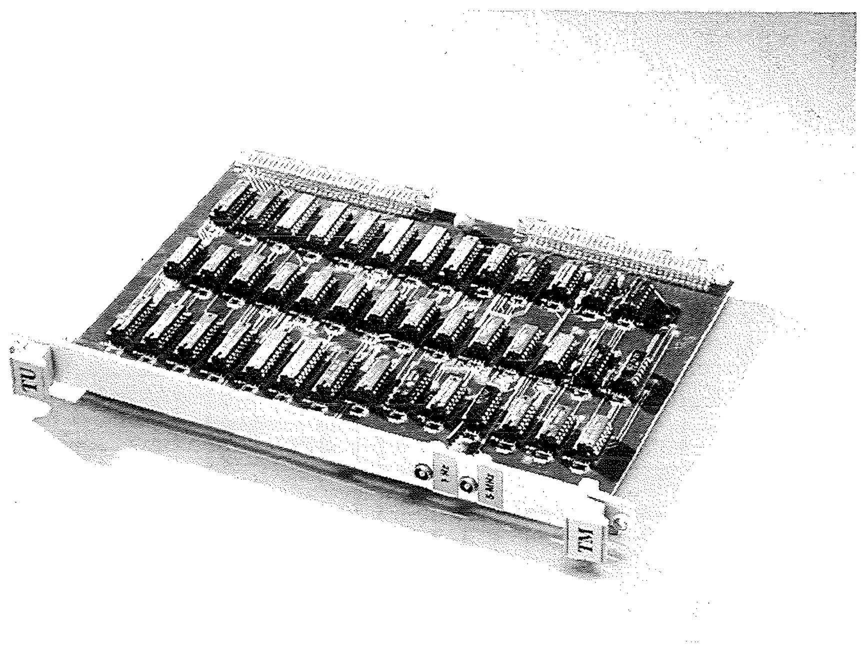

Fig.8. Time Module

3.3.3. Quadrant Module 1

This module receives signals describing the situation in the detectors of the first quadrant of the cluster (stations 1 - 4). Its basic task is to perform first level logic decisions on those signals.

Fig.9 shows the block diagram of the module. Signals from the Trigger Bus arrive to four Station Submodules, which receive also signals from the Control Module via the Control Bus. Output signals from the Station Submodules, via several busses are distributed either locally on the QM1 itself or are sent, via the Private Bus of the TU, to other modules.

A schematic diagram of a Station Submodule is shown in fig.10 and for all the stations it looks the same way. The logic of the submodule checks for Local High Density condition in the station (LHDM-1 GAL16V8) and for the presence of the single muon (SMDM1, GAL20V8) status.

LHDM-1 receives the logical signals T1 - T4 (T1/1 in the schematic indicates the signal from station 1) from the Trigger Bus and various signals from the Control Module (X, Y, VETO, RESET, ENABLE). When the LHD condition is fulfilled, the LHDPW bit is set in the internal register (pin 19 of U6) and a LHD pulse is sent to the LHD/SHD bus (pin 15), showing that this station detected an event.

SMDM1 uses as input T1 - T4 and Tm1- Tm4 signals and at one of it's outputs a pulse, indicating a single muon detection (SM1 on pin 20), is present. Other outputs are "combination" outputs: M1 (a), M2 (b), M3 (c) or M4 (d), showing the actual combination of the pulses detected in coincidence. These pulses are sent to the SM Bus of the TU.

The Station Submodule also converts the number of e/γ detectors hit (0 to 4) into a binary number, used for the cluster density calculations. This conversion takes place in a 4bit full adder type 74F283 (U16) [5] and its result is present on the CHDL Bus of the QM1. Such binary numbers from all four stations are next added in the CHD First Level Summing Submodule and the resulting binary number is sent to the CHD Bus of the TU.

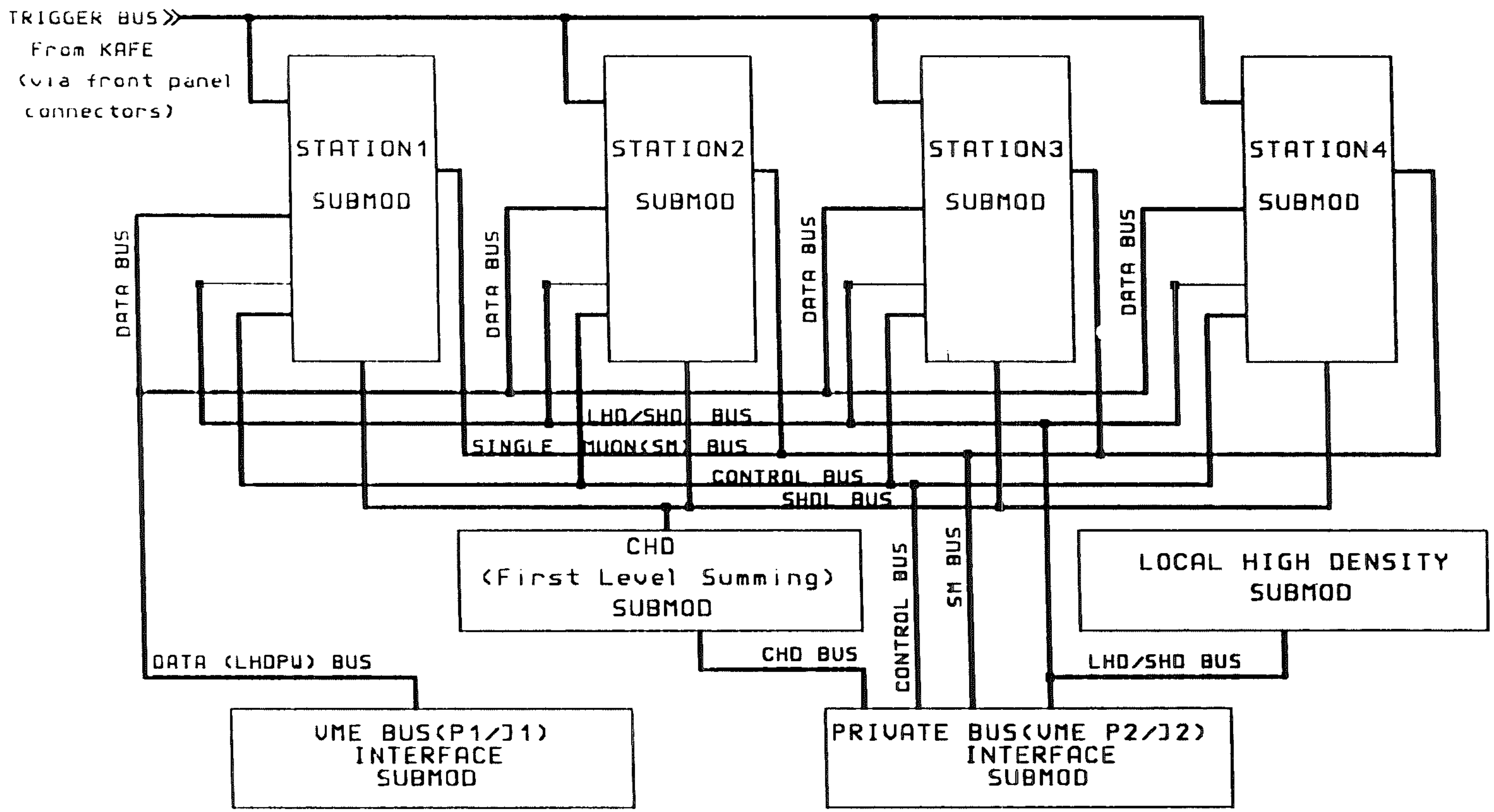

Fig.9. Quadrant Module 1 block diagram

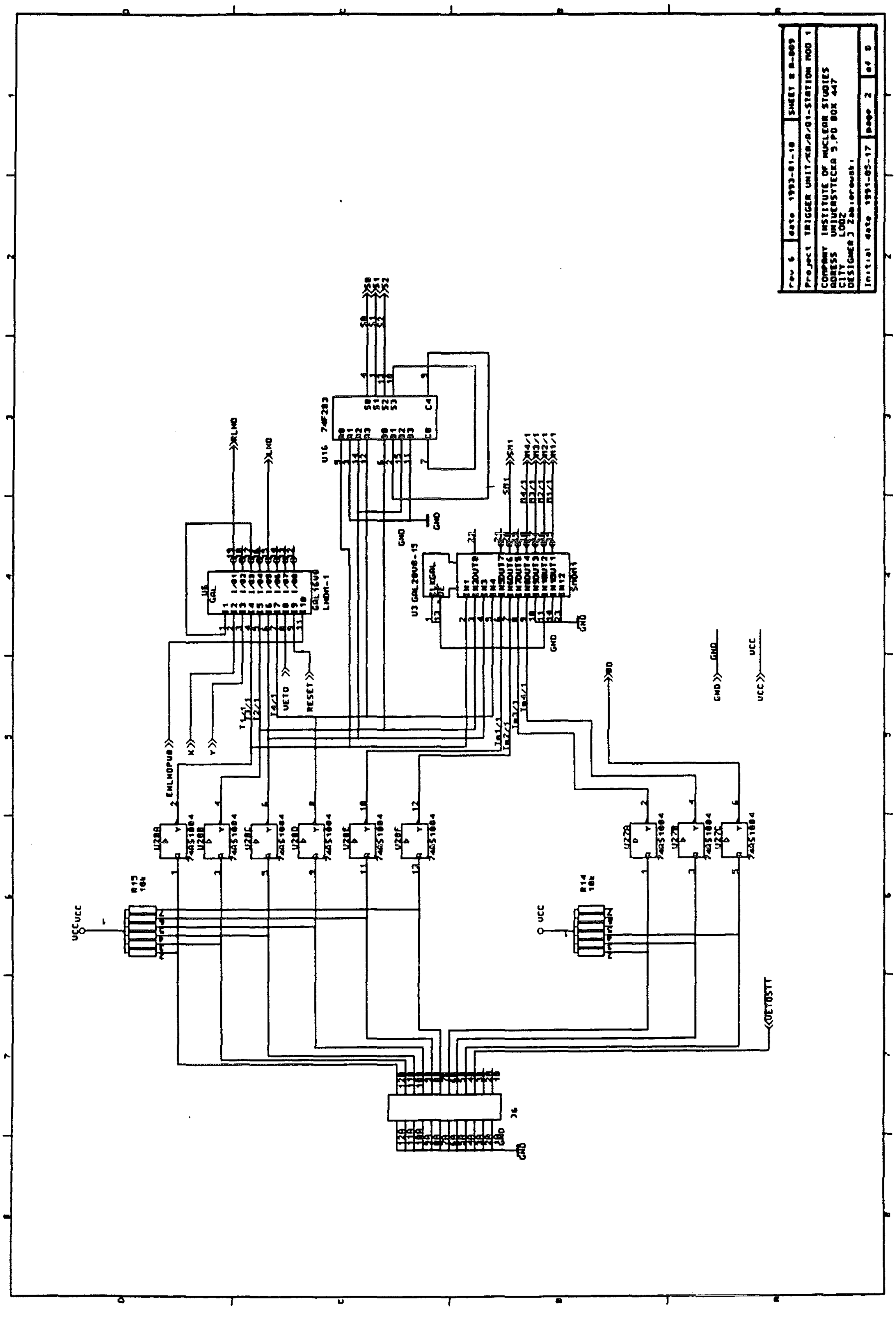

Fig.10 Station Submodule

In fig.10 the signal BD is a buffered dynode (Dy) signal, used for SHD detection in the Single High Density task module.

The Local High Density Submodule in fig.9 receives the LHD pulses from all the Station Submodules and generates a LHDI signal, being sent to the Control Module via the Private Bus.

3.3.4. Quadrant Module 2

In fig.11 there is a photograph of this Trigger Unit module. The labelled ICs are GALs.

The structure of this module is similar to the structure of QM1. It can be seen in the block diagram in fig.9. There are also four Station Submodules (for processing the signals from the stations 5 - 8), the CHD Submodule and the two bus interface submodules. The only difference is, that instead of the LHD Submodule, here we have the Single Muon Detection Submodule, shown in detail in fig.12.

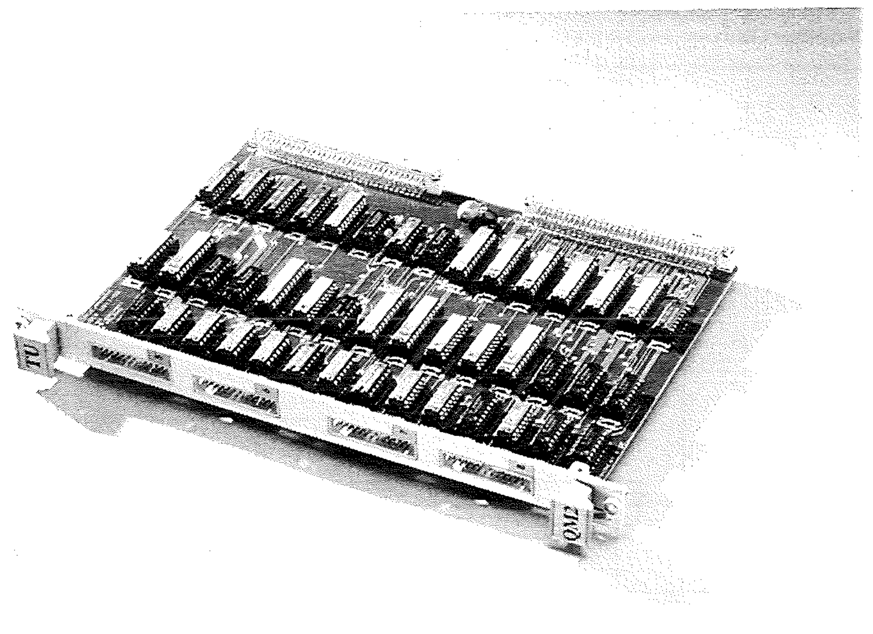

Fig.11. Quadrant Module 2

The logic, preparing the information for the SMFR, (station number and PM combination of the single muon) is programmed in several GALs. The SM signals from all Station Modules (SM1 in SMDM1 in fig.10) are combined in a logical OR in SMDM-2 and sent to the 16 bit binary counter (U27, U26, U39, U37). This counter may be preloaded with the suppression factor stored in SMSFR (U42, U40).

The combination data is decoded in the SMDM-3 GALs and the station number in SMDM-4. They are presented to the input of SMFR (U43), where they are latched with every single muon event giving an overflow in the counter (PSM signal). At the same time the SMI signal is sent to the Control Module that generates the VME interrupt. The Control Bus shown in fig.12 supplies the signals necessary to organize the data flow between the parts of the circuit.

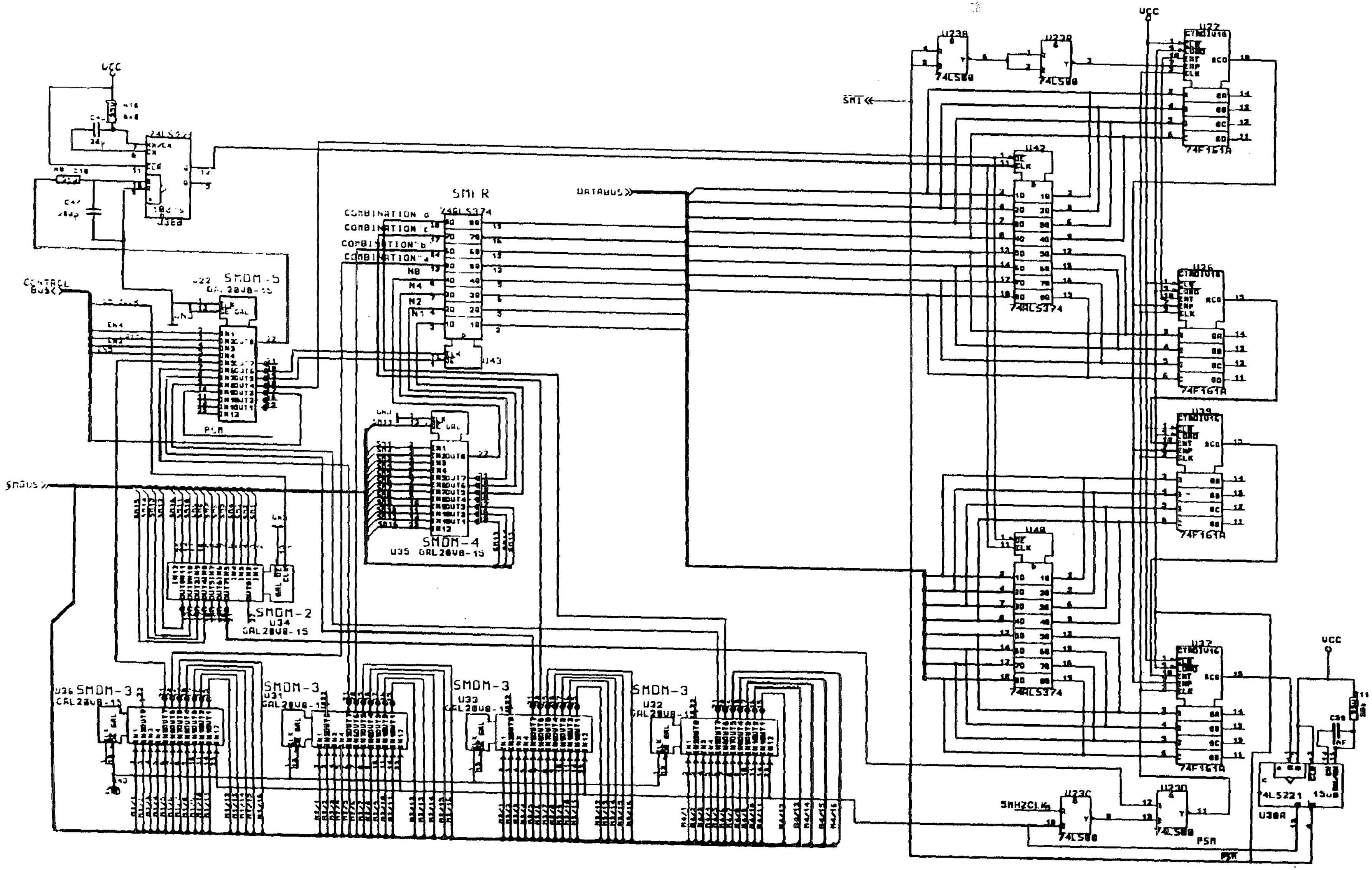

Fig. 12. Single Muon Detection Module

3.3.5. Quadrant Module 3

This module, apart from the "station related" circuits, contains the Cluster High Density Submodule, responsible for the generation of the CHDI signal (cluster density shower condition fulfilled).

The principle of determination of this "cluster high density" is that of a multiplicity logic unit, implemented here in digital way and described in [6].

The schematic diagram of this submodule is shown in fig.13. Output signals from the CHD (First Level Summing) Submodules on QM1 - QM4 (see fig.10) are inputs to the circuit in fig.13. Here, in 74F283 4bit full adders, summing is performed, and the resulting 7 bit number appears at the P0 - P6 inputs of the U39 (8 bit comparator, type 74AS885). This number is the total number of e/γ detectors in the cluster, hit simultaneously. It is compared with the value N, preloaded by software to the Cluster Multiplicity Bits of the Status Register (U41). If it is greater or equal N, a CHDI signal is generated. At the same time the number is latched in the Cluster Flag Register (U36), being then available for readout by TVC1 software. The CHDM-3 GAL (38) ensures, that the CFR is cleared after readout. This is important, because the readout of the CFR is made with every EVENT pulse generated by the TU or externally and the next event may not contain data in this register (external, LHD or SHD type of events).

The CHDM-1 and CHDM-2 GALs contain logic for proper control of the data flow between various parts of the circuit.

3.3.6. Quadrant Module 4

In fig.6 this module has a subtitle "SHD & master". This corresponds to its functions, additional to "station related" tasks (for stations 13 - 16 of the cluster). Via Private Bus (its LHD/SHD part) it receives BD signals (see fig.10) showing, that somewhere a Single High Density has been detected. As a result the SHDI signal is generated.

The name "master" shows, that it contains some important parts of the Control Module, organizing the data flow on the Private Bus as well as the internal relations between the various parts of the TU logic. This is also the place, where the EVENT and VETO signals (the two most important signals in the Trigger Unit) are produced.

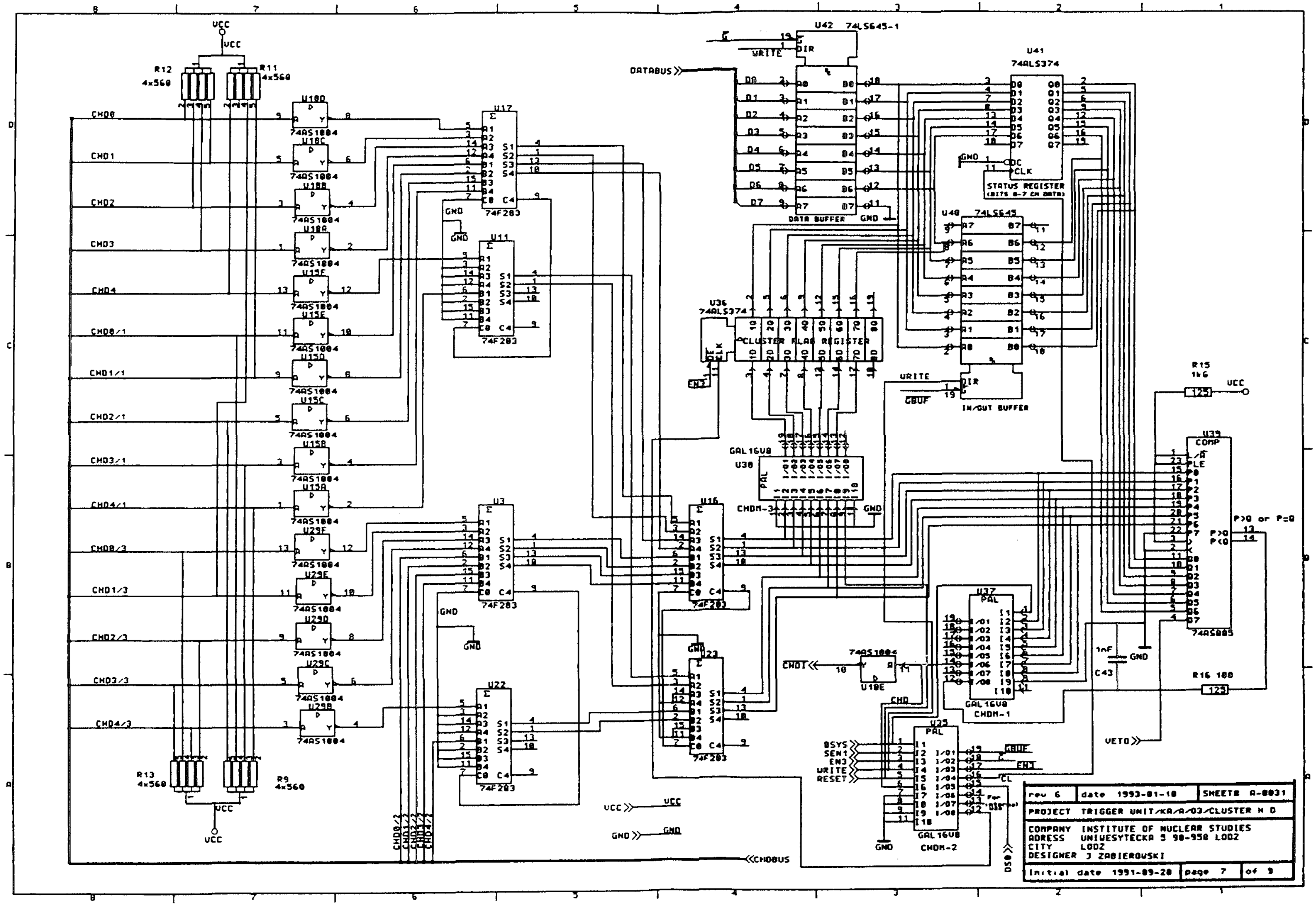

Fig.13. Cluster High Density Submodule

Chapter 4

Concluding remarks

The Trigger Unit was designed and built as a part of the scientific collaboration between the Kernforschungszentrum Karlsruhe (Institut für Kernphysik 1 and 3), Karlsruhe, Germany and the Soltan Institute of Nuclear Studies, Department of Cosmic Ray Physics, in Lodz (Poland). The collaboration itself and the production of the TU modules were sponsored by the Polish Government Commitee for Scientific Research (KBN Grant 941/2/91).

The prototype TU was built in Lodz in 1993 and tested in KfK with a Test Module, also built in Lodz for this purpose. TU Test Software and the test stand shown in fig.14 were used for this purpose. Since spring 1994 prototype is working in the first cluster of the KASCADE experiment together with the first set of front-end electronics KAFE modules. The serial production has started in Lodz and the delivery of all TUs is scheduled for 1994.

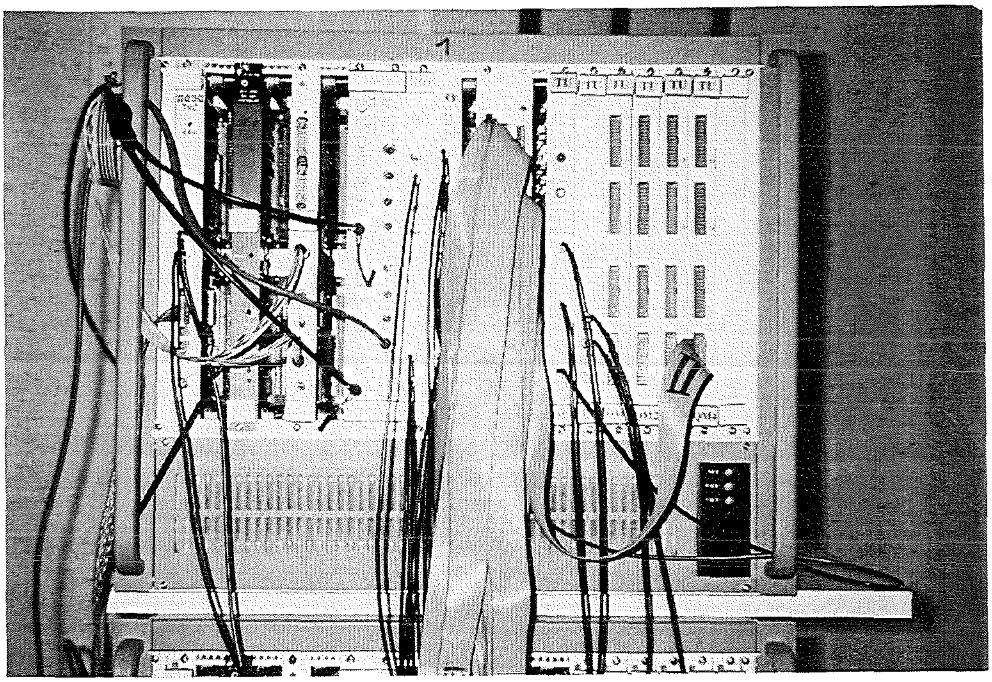

Fig.14. Test stand

The authors acknowledge the big help on the technical side (in getting necessary data, sample parts and test equipment) from G.Schmalz, H.Keim and H. Mueller.

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