Components for Software Radio Wideband Receivers: A space segment survey

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***Abstract*—Many interesting scenarios are emerging on the horizon of satellite communication: communication system flexibility is a keyword for revenue enhancement and Software Defined Radio (SDR) is a means for achieving it. However, its development on the satellite side is slowed down by several constraints that the harsh space environment imposes on the satellite technology. This paper outlines the main scenarios for space-borne SDR and digs into the details of some application requirements. The goal consists in highlighting the capabilities of the current technology for SDR receivers, through a survey that compares space with ground market for two of the main receiver components: ADC and FPGA.**

I. Introduction

Design flexibility in a satellite is considered a key aspect for optimizing the use of in-orbit resources, especially in those satellite subsystems functionalities that are strongly affected by the evolution of the ground applications. Communication payload and subsystem ones certainly belong to this category [1].

In perspective, during the 15 years lifetime of telecommunication satellites, adaptable regenerative On Board Processor (OBP) would allow modifications to the existing air interface or the full implementation of new ones [2], depending on the required compatibility with the legacy waveforms. Such option represents for satellite operators an interesting opportunity to protect and develop their market assets in new areas of services, type of applications. Moreover, this opportunity concerns all market segments, that is, Fixed Satellite Service/Direct Broadcast Satellite (FSS/DBS), Mobile Satellite Service (MSS), institutional/governmental applications, and all categories of satellite operators (Global or Regional players).

Generally, technologies for reconfigurable systems bring the following remarkable advantages to a satellite system:

- Standardization as much as practicable of the baseline design so as to optimize the overall cost and delivery schedule of the mission(s), whilst offering options for functional customization of the payload after completion of the design phase (pre-launch flexibility).
- Maximization of the satellite revenue-generating potential throughout its life by enabling in-orbit reconfiguration of the communications mission to suit evolving market needs (post-launch flexibility).

The pre-launch flexibility represents for satellite manufacturers the ability to refine the ultimate payload design in the latest stage of the satellite manufacturing process or even right before the launch. Standard design could then be easily adaptable to different mission requirements at reduced development cost.

Scenarios that would benefit from such capabilities are those where client requirements undergo any kind of variations until a late stage in the design phase, or mission frequency band assignment from ITU is not yet confirmed at the expected date. In this case, as the frequency assignment process is generally lengthy and costly, multi-band capabilities for the targeted communication subsystem would allow the last minute selection of the agreed frequency channels to be used during the mission. Telecommand/Telemetry and Ranging (TT&R) satellite subsystem would also strongly benefit from that.

On the other hand, as post-launch flexibility, extended on-flight TT&R reconfigurability is not recommended because of the high reliability currently required to the performed functions [3].

Alternatively, space-borne software defined radio (SDR) architectures and their on-flight reconfigurability find interesting applicability for micro satellite synthetic aperture radar (SAR), where digital beam former (DBF) algorithms can obtain multi angular SAR data and enhance the signal-to-noise ratio. Indeed, SDR DBF system would allow several operation modes (e.g. multiple beam, direction-of-arrival estimation and null-steering operation) at the cost of one unique hardware platform, thus giving rise to re-usability of hardware, scalability and power efficiency [4].

Furthermore, inter-satellite and proximity links would also benefit from flexible hardware architecture. In the scenario of LEO micro satellites formation, such capability would allow changes in the code rate according to the inter-satellite communication distance, thus optimizing the related link budget [5].

Additionally, multi-mission capabilities are strongly required in communication scenarios similar to the Mars orbiter scenario, where orbiters with data-relay capabilities and long lifetime need to communicate with several landers that implement different air interfaces [6]. Here, the SDR approach can play a key role in guaranteeing the pre- and post-launch agility mentioned above.

In conclusion, SDR is applicable to several current scenarios of all mission phases (post-launch and pre-launch), provided that the typical constraints of satellite platforms are satisfied: power consumption and market availability of space qualified

components.

By now, ESA and NASA have widely surveyed the SDR approach in the space segment [7], [8], the latter supporting and promoting the necessity for an open architecture in the radio design, possibly customized to the space communication constraints. However, high performance SDR implementations are still extremely challenging due to the current status of space qualified components for the data conversion and digital processing cores, especially in small platforms with limited power budget. This paper aims at providing an updated survey on the available radiation-hardened components for on-board implementation, with a special focus on ADCs and FPGAs.

II. Scenarios and preliminary subsystem requirements

From the considerations above, it follows that SDR currently finds applicability in the TT&R satellite subsystems as well as in its payload, within the described scenarios. Limited power resources and high reliability imposed by the mission lifetime drive for careful selection of components, with special attention on those that are highly populated by transistors, such as memory, DAC, ADC and FPGAs.

With regard to these last ones, their requirements can usually vary considerably according to the mission features (flying orbit, overall satellite mass and volume, thereby available power budget). Here, two representative scenarios are presented as a framework to carry out a market survey of the core components for space-borne receivers: TT&R (in geostationary and low earth orbits) and inter-satellite link (ISL) receivers.

The TT&R subsystem is of vital importance for the control and management of a generic space platform. Relevant cost and manufacturing time reductions can be obtained when it presents an easy adaptibility (here intended as pre-launch flexibility) to an undefined set of requirements. Alternatively, the SDR design approach would make an ISL transceiver open to any type of considered satellite network, thus enlarging the set of possible air interfaces for the same hardware device.

The proposed ISL scenario refers to an hypothetical RF link between satellites in a LEO constellation that present variable information bit rate and/or transmit power in order to improve the throughput of the time-varying satellite link [9].

With regard to the TT&R subsystem, two example missions have been selected: GEO-COM and AISCOM. GEO-COM is a typical GEO communication platform, with Ku band TT&R subsystems, that incorporates advanced payload technology like DVB S2 processors and active antennas. AISCOM is a prototype platform composed by three satellites that will demodulate and collect AIS (Automatic Identification System) data, currently exchanged between each ship and transceivers on the closest coast, in order to extend the localization service to the shipping fleet in the ocean [10].

A. GEO-COM and AISCOM

In GEO-COM, the uplink receiver implements tone ranging demodulation, compensation of the Doppler frequency offset up to 300 kHz, as well as FM/PM modulation for the carrier and subcarriers and FSK/BPSK for the command data modulation.

Besides, AISCOM uplink receiver implements a 8-PSK demodulation schemes with an LDPC channel code and up to 10 KHz of Doppler frequency offset is compensated.

The overall power consumption budget for the uplink receiver of GEO-COM and AISCOM is reported in table I.

Table I
Overall TT&R receiver Power Consumption

Application	GEO-COM	AISCOM
Max tot. Power cons. [W]	13	4

B. ISL between LEO satellites

Inter-satellite links represent an interesting alternative to a multi-hop ground station network for the operation and control of a LEO satellites constellation. Indeed, the communication links between satellites would increase the visibility time of each, with a direct advantage of a drastic reduction in the number of the required ground stations [11].

Although the choice between RF and optical technology for the physical layer depends on the application trade-off analysis, here it is assumed a general scenario where the ISL functionality is not the main payload of the satellite (up to 700 Kg satellite) and RF technology is preferred for its robustness and reduced complexity [12], [13].

The hypothetical constellation is composed by cross-plane ISL, in particular between satellites located at a LEO orbit with 900 and 800 Km of altitude, both belonging to the same orbital plane. For the sake of simplicity, neither external interference and blocking signals nor atmospheric propagation perturbations are considered in the link. This hypothesis turns out to be quite realistic in contexts where high directive, possibly steerable, antennas are utilized and the maximum reachable link is the one right above the height of 20 km from the Earth's surface (thereby excluding the related perturbations to the communication system).

Additionally, as the satellite platform belongs to a medium class, no high constraints are also imposed to the overall receiver power consumption (see table II).

Table II
Overall ISL receiver Power Consumption

Application	LEO sat. ISL
Max tot. Power cons. [W]	15

III. Survey on space-qualified ADCs

The data conversion, together with the antenna input bandwidth and the processing capabilities, is one of the three main bottlenecks of an ideal multi-band/multi-mode software radio architecture [14]. Indeed, despite the recent technological advancements, it is still the main actor of the trade-off analysis that is carried out at a preliminary design phase of a wideband receiver. Its performance affects the overall dynamic range of the receiver as well as its sensitivity, therefore asking for

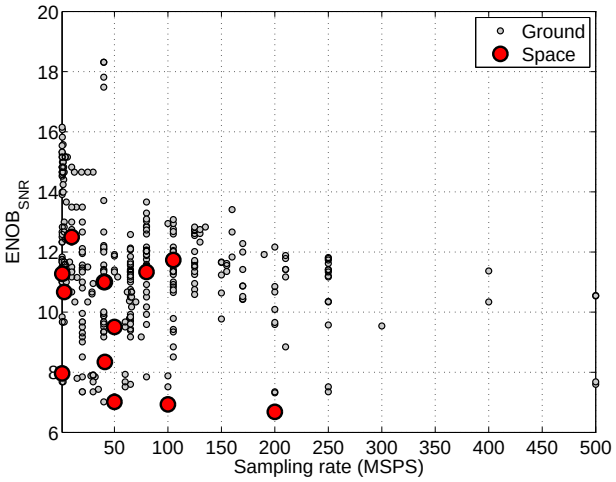

Figure 1. Available space qualified ADCs: SNR

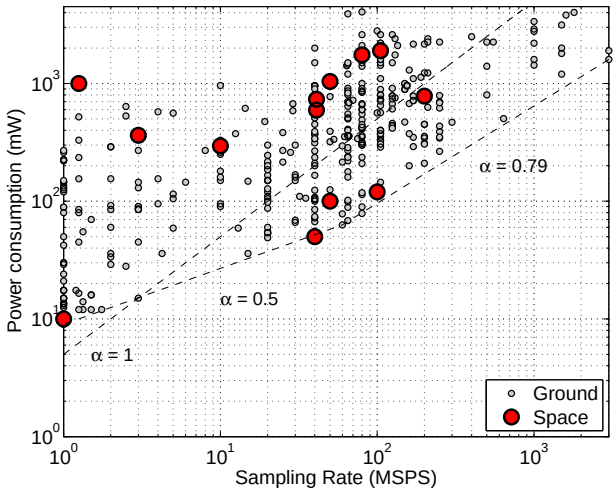

Figure 2. Available space qualified ADCs: power consumption

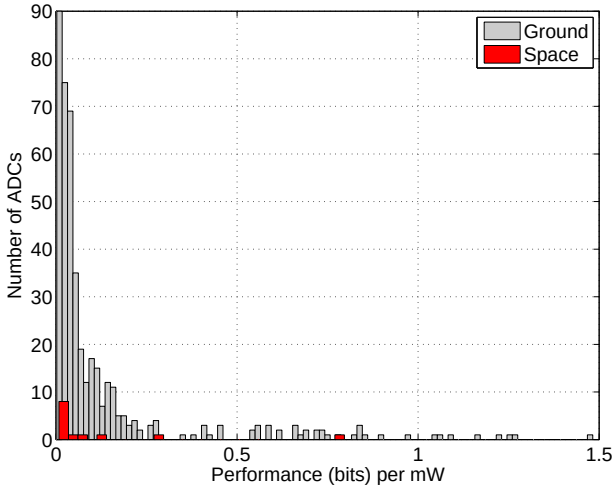

Figure 3. Available space qualified ADCs: Performance per power consumption

several architecture compromises on the RF front-end side necessary to satisfy the application requirements [15].

With regard to the effect on the overall subsystem power consumption, analogue-to-digital converters play an important role on its budget analysis, especially in SDR architectures where ADC are located as close as possible to the antenna in order to enhance the digital processing section of the respective receiver.

ADC are characterized by a list of parameters that are commonly provided by every manufacturer. One of these is the ADC effective number of bits (ENOB), defined as:

$$\text{ENOB}_{\text{SNR}} = (\text{SNR}(\text{dB}) - 1.76)/6.02 \tag{1}$$

where SNR (signal to noise ratio expressed in dB) is the value provided by the manufacturer; the noise power considers quantization noise, circuit noise, aperture uncertainty, and comparator ambiguity.

Another measure of the ADC performance, motivated by the fact that sampling frequency can be traded against bit resolution via oversampling, is the hypothetical number of effective bits after downsampling to 1 Hz:

$$M = \text{ENOB}_{\text{SNR}} + \frac{\log_2(f_{\text{samp}})}{2} \tag{2}$$

A general figure of merit that includes each of the above measures is

$$F = \frac{M}{P} = \frac{\text{ENOB}_{\text{SNR}} + 0.5\log_2(f_{\text{samp}})}{P}\,, \tag{3}$$

where P is the stated ADC power consumption in mW.

To assess the market offer for the space segment subsystems, a specific survey has been carried out, involving totally more than five hundred ADCs, most of them designed for ground applications (see the Appendix A for the complete list of space ADCs).

The figures in this page show the results of the survey.

From Figure 1 it is evident that 50% of the available space components present an effective number of bits much lower than the devices for ground application with the same maximum sampling rate.

Secondly, Figure 2 and Figure 4 point out that space devices are generally much more power-hungry than the ground ones with equivalent performances (described by M in (2)). In particular, Figure 2 shows that the power consumption the most power-efficient devices is proportional to the square root ($\alpha = 0.5$) for low frequencies and approximately proportional to $f_{\text{samp}}^{0.79}$ for higher frequencies from 100 Msps on.

Finally, Figure 3 highlights the number of devices with a specific performance per power unit (described by F in (3)), from here it ensues that only one space-qualified component present a good performance per unit power.

A. Scenario 1: GEO-COM and AISCOM

The following table reports some of the preliminary requirements for the ADC components in the TT&R subsystem receiver of GEO-COM and AISCOM. A fast look to the table in the Appendix shows that such requirements are easily satisfied by most of the current ADCs.

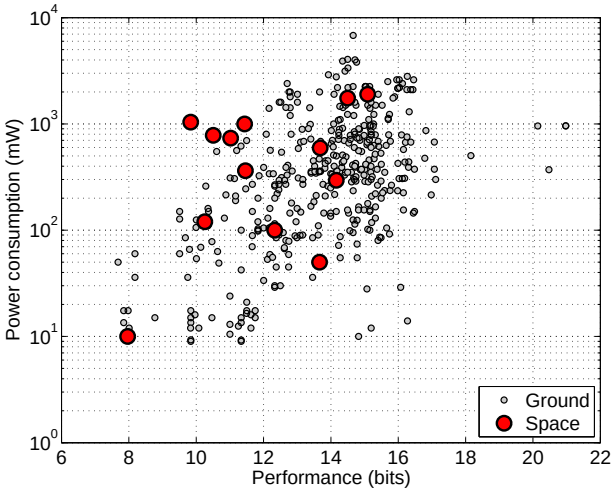

Figure 4. Available space qualified ADCs: Performance per power consumption

Table III
ADC PRELIMINARY REQUIREMENTS FOR GEO-COM AND AISCOM UPLINK RECEIVER

Application	GEO-COM	AISCOM
SNR [dB]	63	54
Max Pow. cons [W]	1.3	0.4
Sampling rate [Ksps]	> 10	> 900

B. Scenario 2: ISL between LEO satellites

According to the scenario briefly described in II-B, a simplified link configuration would involve two satellites at a minimum distance of 100 km or at maximum distance of 6809 km (Figure 5, case 1 and case 2 respectively).

In this case, a maximum Doppler frequency offset of 1.25 MHz should be considered [16].

Given the simple channel model, the dynamic range of the receiver signal power can be computed as the ratio of the free space loss for the two distance ranges.

Additionally, assuming a BER of 10^{-6}, the signal to noise ratio requirement for the ADC can be retrieved by the following set of formulas [15]:

$$\text{Dynamic range}\,[\text{dB}] = 10\log_{10}\left(\frac{D_{max}^2}{D_{min}^2}\right) \tag{4}$$

$$\text{CNR}\,[\text{dB}] = \frac{E_b}{N_0} + 10\log_{10}\left(\frac{R_b}{B}\right) \tag{5}$$

$$\text{SNR}_{\text{req}}[\text{dB}] = \text{Dynamic range}[\text{dB}] + \text{CNR}[\text{dB}] \tag{6}$$

where R_b and B are the bit rate and bandwidth of the signal respectively[15], D_{max} and D_{min} the maximum and minimum distance between the two spacecrafts and E_b/N_0 the ratio between the bit energy and the noise density.

Table IV provides the features of an hypothetical air interface for ISL link, whereas the following one (table VI) presents the consequent requirements for a suitable ADC.

Table IV
ISL AIR INTERFACE FEATURES

Carrier frequency [GHz]	25
Data rate [Mbps]	150
Mod. Scheme	QPSK
LDPC coding rate	2/3
E_b/N_0 **(on a frame of 43200 bits) [dB]**	3
Filter Roll-off	0.4
Max Doppler freq. offset [MHz]	1.25
Bandwidth [MHz]	158.75

Table V
ISL ADC REQUIREMENTS

Sampling rate [Msps]	> 317.5
SNR [dB]	39.4
Max Power Cons. [W]	1.5

From the listed ADC requirements, it is evident that there are not yet components able to directly fulfill them (see Appendix). However, as current ADC technology for space application can also provide a sampling rate up to 200 Msps with a SNR of 42 dB, suitable solutions for such a waveform would be available at the cost of a reduced data rate. Indeed, assuming a data rate of 90 Mbps, therefore requiring a bandwidth of 95.75 MHz, Nyquist sampling could still be approached by the mentioned device.

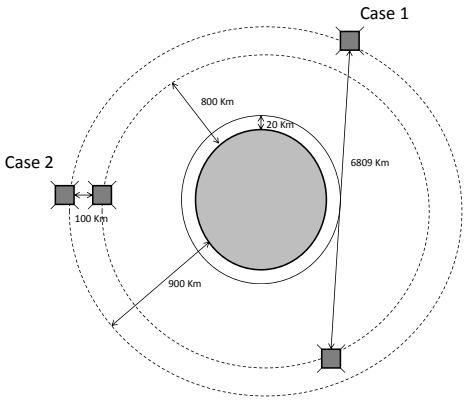

Figure 5. Maximum and minimum range of a simplified ISL scenario

IV. SPACE-QUALIFIED FPGAS

In space-borne SDR applications FPGA performance is predominantly determined by size, i.e., number of available logic cells and multipliers. The main limiting factor to its widespread usage is the related power consumption.

Estimation of FPGA power consumption is difficult, as it depends on the concrete signal processing design architecture. For the sake of our survey, in order to gain a rough worse case estimate, we have referred to a configuration setup where the clock frequency was set to 100 MHz and all logic resources (look-up tables, flip-flops, multipliers) were used on each device.

Figure 6 shows the power consumption per logic element of state-of-the-art ground FPGAs (Altera Stratix III, Virtex

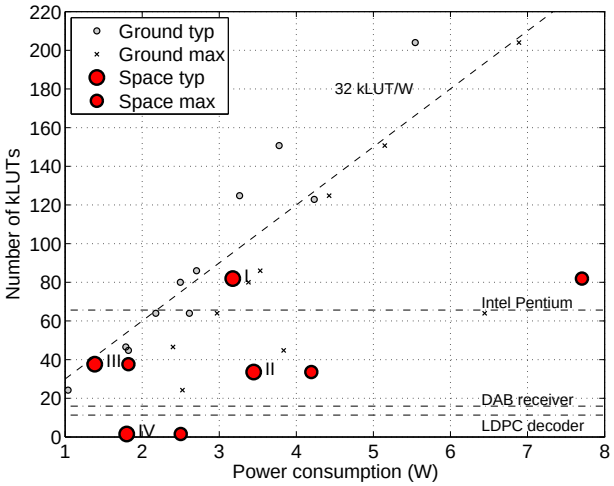

Figure 6. Available space qualified FPGAs: Size versus power consumption

6) as estimated with the respective company design tool, Altera PowerPlay and Xilinx XPE. In particular, it reports the number of look-up tables, usually the limiting factor in DSP processing, versus the resulting typical and maximum power consumption estimate.

Not surprisingly, the number of LUT in the space-qualified FPGAs are much less than those of the more commercial ones, moreover in one case (Virtex 5, indicated in the figure with I), its maximum power consumption can reach very high value (7.7 W), almost one Watt more than the Virtex 6.

One further observation that can be retrieved from the figure is that ground applications FPGAs implement nearly 32 kLUT per consumed watt, whilst space qualified ones do not follow this trend.

Finally, in order to give an idea of the real capabilities of such devices, the figure also reports the number of LUT that have been used for the implementation of some typical waveforms, retrieved from the literature [17], [18], [19]. These include: a LDPC decoder (10 kLUT), a Digital Audio Broadcasting receiver (18 kLUT) and a Intel Pentium microprocessor (67 kLUT). According to these values, the best performing space-qualified device offers enough space for more complex algorithms.

V. Conclusion

In conclusion, the paper has presented a set of space scenarios where SDR can play a key role. Besides, issues related to the core components for a space-borne SDR receiver have been discussed and current commercial-off-the-shelf solutions have been presented.

The performed survey on ADCs and FPGAs has highlighted a considerable market delay for the space-qualified devices with respect to their commercial counterparts, as well as showing the most relevant differences in the behavior of some characterizing measures. Such delay could be roughly estimated by assuming that the specific commercial component presents the requested features for the considered application. In that case, as in average the gap between the release date of the commercial version and its space-qualified one amounts to 9.6 years for the ADCs and 2.8 years for the FPGAs, such delay can be roughly estimated to be the same value [20], [21], [22], [23], [24], [25], [26], [27].

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Appendix

The following tables contain the part of the survey related to the space qualified components [20], [21], [22], [23], [24], [25], [26], [27].

Table VI
SPACE-QUALIFIED ADC

Manufacturer	**Part Number**	**Resolution** [bits]	**Sample rate** [Msps]	**Power** [mW]	**SNR** [dB]	**SINAD** [dB]	**SFDR** [dBc]
Analog Devices							
	AD1671	12	1.25	750	69.65	68	74.5
	AD1672	12	3	363	66	63	65
	AD6645	14	80	1750	72	71.5	76
	AD9054	8	200	781	42	40	54
	AD9042	12	41	735	52	52	50
	AD9058	8	50	1040	44	43.3	50
	AD9283	8	100	120	43.5	42.5	49
Texas Instruments							
	ADS5424SP	14	105	1900	72.4	71.3	82.5
National Semiconductor							
	ADC081S101	8	1	10	49.7	49	68
Maxwell							
	9240LP	14	10	295	77	76	90
	9042	12	41	595	68	67.5	90
ST Microelectronics							
	RFH1201	12	50	100	59	56.5	57
S3Group							
	S3AD40M13BC90S	13	40	50	68	67	79

Table VII
SPACE-QUALIFIED FPGAS

	Xilinx	**Actel**	**Actel**	**Aeroflex**
	Virtex 5 (FX)	RTAX-DSP	RT ProAsic 3	Eclipse
Device	SIRF	RTAX4000D	RTA3PE3000L	Eclipse
Technology	SRAM-65nm	CMOS antifuse -150 nm	Flash - 130 nm	CMOS Antifuse - 250 nm
Clock Frequency (MHz)	550	350+	250	150
Top level block combination	11200 CLBs	30 Core Tiles		
Higher level block combination	20480 Slices	8400 Superclusters		
Elementary block combination	131072 Logic Cells	16800 Clusters	75264 Tiles	
LUT number	81920	33600	75264	4002
LUT input number	6	5	3	17
Flip-flop number	81920	33600	75264	4002
DSP block number	320	120	75264	4002
Power (W) at 100 MHz	3.1 (typ.), 7.7 (max)	3.5 (typ.) and 4.2 (max)	1.4 (typ.) 1.8 (max)	1.8 (typ.) 2.5 (max)