42.7 Gbit/s electro-optic modulator in silicon technology

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Abstract: CMOS-compatible optical modulators are key components for future silicon-based photonic transceivers. However, achieving low modulation voltage and high speed operation still remains a challenge. As a possible solution, the silicon-organic hybrid (SOH) platform has been proposed. In the SOH approach the optical signal is guided by a silicon waveguide while the electro-optic effect is provided by an organic cladding with a high $\chi^{(2)}$-nonlinearity. In these modulators the optical nonlinear region needs to be connected to the modulating electrical source. This requires electrodes, which are both optically transparent and electrically highly conductive. To this end we introduce a highly conductive electron accumulation layer which is induced by an external DC "gate" voltage. As opposed to doping, the electron mobility is not impaired by impurity scattering. This way we demonstrate for the first time data encoding with an SOH electro-optic modulator. Using a first-generation device at a data-rate of 42.7 Gbit/s, widely open eye diagrams were recorded. The measured frequency response suggests that significantly larger data rates are feasible.

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1. Introduction

One of the most important properties of an optical modulator is its modulation speed or bandwidth, which should be at least as fast as the available electronics. Transistors having transit frequencies well above 100 GHz have already been demonstrated in 90 nm silicon technology, and the speed will further increase as the minimum feature size is reduced [1]. However, the bandwidth of present-day silicon-based modulators is limited. Silicon does not possess a $\chi^{(2)}$-nonlinearity due to its centro-symmetric crystalline structure. The use of strained silicon has led to interesting results already [2], but the nonlinearities do not yet allow for practical devices. State-of-the art silicon photonic modulators therefore still rely on free-carrier dispersion in *pn* or *pin* junctions [3–5]. Forward biased junctions have been shown to exhibit a voltage-length product as low as $V_\pi L$ = 0.36 V mm, but the modulation speed is limited by the dynamics of minority carriers. Still, data rates of 10 Gbit/s have been generated with the help of a pre-emphasis of the electrical signal [4]. Using reverse biased junctions instead, the bandwidth has been increased to about 30 GHz [5,6], but the voltage-length product rose to $V_\pi L$ = 40 V mm. Unfortunately, such plasma effect phase modulators produce undesired intensity modulation as well [7], and they respond nonlinearly to the applied voltage. Advanced modulation formats like QAM require, however, a linear response and pure phase modulation, making the exploitation of the electro-optic effect (Pockels effect [8]) particularly desirable.

2. SOH approach

Recently, the silicon-organic hybrid (SOH) approach has been suggested [9–12]. An example of an SOH modulator is shown in Fig. 1(a). It consists of a slot waveguide guiding the optical field, and two silicon strips which electrically connect the optical waveguide to the metallic electrodes. The electrodes are located outside the optical modal field to avoid optical losses [13], Fig. 1(b). The device is coated with an electro-optic organic material which uniformly fills the slot. The modulating voltage is carried by the metallic electrical waveguide and drops off across the slot thanks to the conductive silicon strips. The resulting electric field then changes the index of refraction in the slot through the ultra-fast electro-optic effect. Since the slot has a width in the order of 100 nm, a few volts are enough to generate very strong modulating fields which are in the order of magnitude of the dielectric strength of most materials. The structure has a high modulation efficiency since both the modulating and the optical fields are concentrated inside the slot, Fig. 1(b) [14].

Indeed, first implementations of SOH modulators with sub-volt operation [11] have been already shown, and sinusoidal modulation up to 40 GHz was demonstrated [15,16]. However, the challenge in building low-voltage high-speed SOH modulators is to create a highly conductive connecting strip. In an equivalent circuit the slot can be represented by a capacitor C and the conductive strips by resistors R, Fig. 1(b). The corresponding RC time constant determines the bandwidth of the device [10,14,17,18]. In order to decrease the resistance R, it has been suggested to dope the silicon strips [10,14]. While doping increases the conductivity of the silicon strips (and therefore increases optical losses), one pays an additional loss penalty because the electron mobility is impaired by impurity scattering [10,14,19]. Moreover, the most recent fabrication attempts showed unexpectedly low conductivity [20,21].

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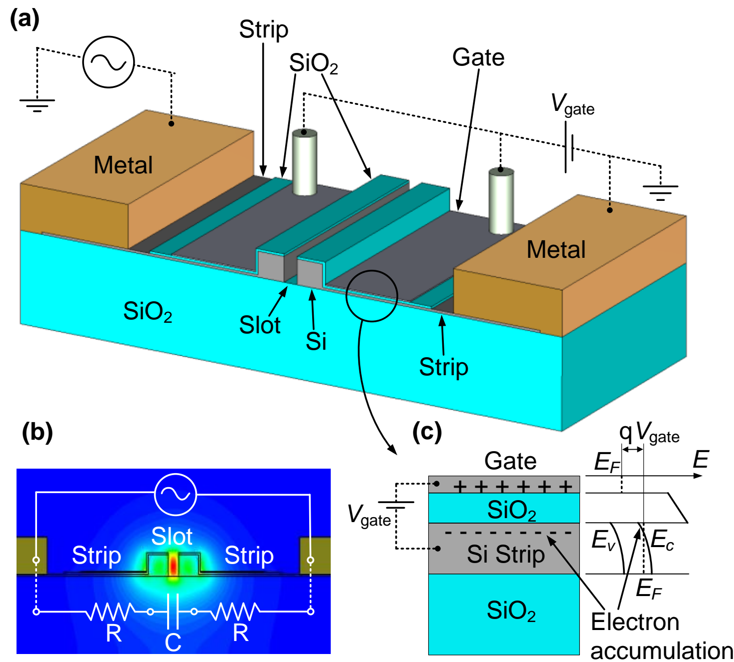

Fig. 1. Vision for a future SOH-modulator. (a) The optical active region is connected to the metal electrodes by means of thin silicon strips. On top of the silicon strips an SiO_2 film is deposited and covered with the gate electrode. (b) Cross-section of the waveguide and electric field distribution of the optical mode; the light is concentrated in the slot. Lower inset: Equivalent RC circuit for the transfer of the voltage between metallic electrodes to the voltage dropping across the slot (slot capacitance C, strip resistance R). (c) When a positive gate voltage is applied across the gate oxide, a highly conductive electron accumulation layer is formed in the silicon strips. Under the effect of the gate voltage V_{gate} the energy bands in the strip are bent. $E_{F,C,V}$ are Fermi energy, conduction and valence band energy, respectively; q is the elementary charge.

3. The vision

We present an SOH-based slot-waveguide phase modulator, where the conductivity of the silicon strips connecting the slot region to the modulation electrodes is increased with a novel method which does not create significant optical loss. This enables the first experimental demonstration of data encoding with an SOH modulator. Even though our demonstrator is our very first specimen, which has not at all been optimized, the performance can already compete with that of state-of-the-art plasma-effect modulators [4,5,22]. The data rate of 42.7 Gbit/s that we achieved was limited by the available equipment; the modulator performance suggests, however, that significantly higher data rates are possible.

The structure of the modulator we propose is shown in Fig. 1(a). The slot region in the center, where both the optical and the modulating microwave fields interact, is connected to the metal electrodes by thin silicon strips. On top of these strips a slightly conductive layer ("gate") is deposited, isolated from the strips by a thin silicon oxide film. The structure obtained in this way is similar to the well-known metal-insulator-semiconductor (MIS) [23]. When a positive voltage V_{gate} is applied across the oxide (see Fig. 1(a)), the energy bands in the strips are bent (Fig. 1(c)), and a high-mobility electron accumulation layer is formed at the Si/SiO_2 interface. Since the strip conductivity is proportional to the mobility and the free-electron density, the limiting frequency $f_{RC} = 1/(2\pi RC)$ increases with increasing gate voltage. For convenience the structure is referred below as an accumulation-layer electro-optic modulator (ALMod).

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The gate of the device depicted in Fig. 1(a) must be optically transparent. This can in principle be achieved by using a thin layer of *n*-doped polysilicon driven to depletion. The ion concentration is adjusted such that when the desired gate voltage is applied all free carriers in the polysilicon are removed. In this way the net positive charge of the gate is mainly caused by fixed nuclei which cannot cause free-carrier absorption.

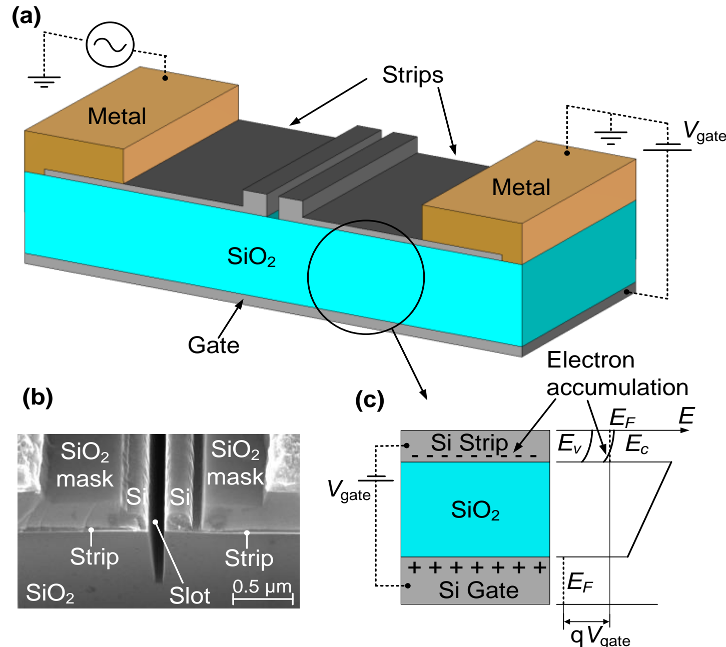

Fig. 2. The SOH modulator used in this work. (a) The slightly conductive silicon substrate is used as a gate. (b) SEM picture of the cross section of the fabricated device. The SiO_2 mask was used as a protection layer during fabrication and lies on top of the strips. In the center the silicon optical waveguide is visible. The slot extends for about 1 µm into the SiO_2 substrate for fabrication issues. (c) When a positive gate voltage is applied across the 2 µm thick SiO_2 substrate a highly conductive electron accumulation layer forms in the strips. The thickness of the strips is 60 nm; for clarity they are not drawn to scale. The gate voltage V_{gate} bends the energy bands in the strips [23]. $E_{F,C,V}$ are Fermi energy, conduction and valence band energy, respectively; q is the elementary charge.

4. The fabricated device

In order to validate the ALMod concept we fabricated the technologically simpler structure depicted in Fig. 2. Here, the gate voltage is applied between the metal electrodes and the silicon substrate. Since the silicon substrate has a conductivity $\sigma = 0.05\ \Omega^{-1}\ \text{cm}^{-1}$, the gate voltage drops essentially across the 2 µm silicon oxide which separates the optical layer from the silicon substrate, Fig. 2(a). To avoid any damage to the chip, we did not apply gate voltages larger than 270 V. This corresponds to an electric field $E_{gate} = 0.135$ V/nm in the 2 µm thick SiO_2, which is much smaller than the breakdown voltage of 1 V/nm achievable in state-of-the art thin SiO_2 films [24]. The gate voltage of 270 V can be reduced by more than two orders of magnitude when using few-nanometers-thick gate oxides, as in the optimized structure envisaged in Fig. 1. The device was fabricated in a CMOS fab using deep-UV lithography (see Appendix B), and the commercially available [25] organic material M1 was subsequently deposited and poled *in situ* (see Appendix D). The material M1 consists of chromophores dispersed in amorphous polycarbonate (APC), has a nonlinear electro-optic coefficient up to $r_{33} = 70$ pm/V (see Appendix D) and an index of refraction n = 1.67 ± 0.02, both measured at the wavelength of 1550 nm. The RF dielectric constant is $\varepsilon_r = 3.3 \pm 0.1$ (3.1

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± 0.1) at 10 GHz (60 GHz). A thermal study indicates that operation at 85°C over 25 years results in a change of the nonlinear coefficient by less than 20% [26].

The slot waveguide has a "rail" width and a slot width of 240 nm and 120 nm respectively. The light is coupled by means of grating couplers [27], whose separation is 2.6 mm. The optical waveguide comprises the 1.7 mm long phase shifting section, two tapers and two 67 µm long strip-to-slot waveguide converters [28]. The silicon strips used for connecting electrically the slot waveguide have a thickness of 60 nm (about 10 nm have been oxidized during the high temperature annealing). The ground-signal (GS) metal electrodes have a gap of 4 µm, and their nominal line impedance is 50 Ω. The length of the electrodes is 3.0 mm and comprises two tapered regions for contacting with a length of 0.55 mm each. On the output side, the 50 Ω line is connected to another transmission line which has a length of 3.0 mm and a line impedance of 75 Ω. This transmission line belongs to a second device and is not terminated. It could not be cleaved away since this would lead to an electrical breakdown at the chip edge when applying the gate voltage. The presence of the 75 Ω line is responsible for the local maximum in the S_{21} parameter around 10 GHz as shown in Fig. 4(a); this deviation was not observed in cleaved samples.

In this first prototype the optical losses are high due to a fabrication error (outlined in Appendix B) which led to an increased surface roughness of the waveguides. This resulted in a fiber-to-fiber loss as high as 40 dB, 10 dB of which is due to the grating couplers, 1 dB is due to the two strip-to-slot converters, and 17 dB/mm is due to the rough waveguide. To verify that these limitations come from fabrication issues rather than from fundamental problems, we fabricated test structures and found losses lower than 3.5 dB/mm. While this is already an acceptable value we anticipate fiber-grating losses as little as 1 dB per facet [29] and losses below 1.5 dB/mm based on our previous results [30].

5. Device characterization

To demonstrate the high-speed capabilities of the phase modulator we performed a 42.7 Gbit/s data modulation experiment. A 1550 nm laser was used as an optical source, and a pseudorandom bit sequence (PRBS) with a length of 2^{31}–1 controlled the modulator. A one-bit delay-interferometer (DI) on the receiver side was used to convert phase modulation to intensity modulation, which was then detected with a photodiode. The DI has the further effect of cutting off the low frequency modulation components. The RF voltage swing was set to V_{pp} = 4.1 V (measured before the probe), and the device was terminated with an external broadband 50 Ω resistor. When the gate field was increased from zero to its maximum value, the optical loss increased by less than 1 dB. The gate leakage current was always below 10 nA, corresponding to a gate power consumption of less than 3 µW. Clear and open eye diagrams at 42.7 Gbit/s were found with the highest gate field, Fig. 3. Bit-error-ratios (BER) smaller than 3×10^{-10} were recorded, demonstrating the usability of our device in real data links.

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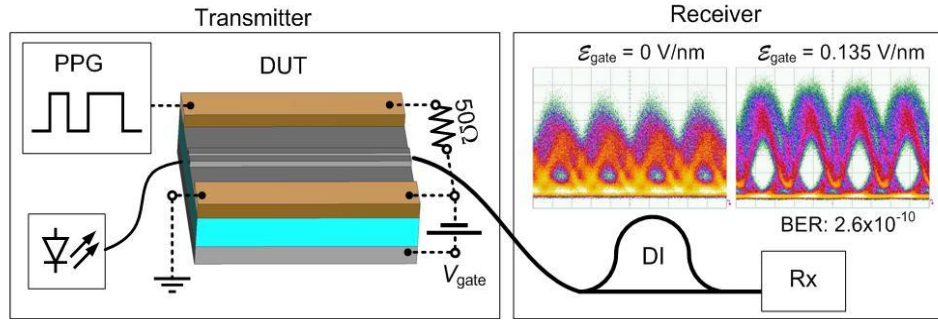

Fig. 3. Setup of the modulation experiment. A pulse pattern generator (PPG) creates a 42.7 Gbit/s electrical signal. Light from a 1550 nm laser is launched into the slot-waveguide. The device is electrically terminated with an external 50 Ω resistor. A gate voltage is applied between the silicon substrate and the silicon strips. The 50 Ω resistance is responsible of keeping both strips at the same electrical DC potential. On the receiver side a delay-interferometer converts the phase modulation into intensity modulation for detection. By increasing the gate voltage to V_{gate} = 270 V (gate field E_{gate} = 0.135 V/nm) clear and open eyes are found.

We further determined the frequency response of the device by applying a sinusoidal voltage with frequencies f_{mod} between 1 kHz and 60 GHz. The chip was contacted as in the data modulation experiment. The RF power at the probe input was kept constant at 10 dBm (1.0 V amplitude). We measured the resulting phase modulation index η, which represents the achieved phase shift in radians. The data are shown in Fig. 4(a) for different gate fields together with the electrical transmission characteristic of the metal electrodes (S_{21} voltage ratio). By increasing the gate field from E_{gate} = –0.025 V/nm to E_{gate} = 0.135 V/nm, the modulation index increases by more than a factor of five in the frequency range above 1 GHz. For the highest gate field, a voltage length product of $V_\pi L$ = 9 V mm (58 V mm) was measured in the low frequency limit and at 60 GHz, respectively. For our 1.7 mm long device this corresponds to a π-voltage of V_π = 5.3 V (34 V). Above 2 GHz, the frequency response is essentially flat (less than 3dB decrease between 2 GHz and 60 GHz) suggesting that data rates could be extended well beyond the 42.7 Gbit/s limit of our equipment.

In order to better investigate the effect of the gate, we recorded the modulation index as a function of the gate field for selected frequencies, Fig. 4(b). For more positive gate fields, an increasing number of electrons accumulate in the silicon strips. The strip resistance decreases accordingly, leading to higher modulation indices. Our simulations indicate that the sheet resistance of the silicon strips becomes smaller than 1500 Ω/sq for gate fields E_{gate} > 0.135 V/nm, which could otherwise be achieved only by doping the silicon strips with an ion-concentration as high as 3×10^{18} cm^{-3}. At the gate field E_{gate} = –0.025 V/nm, a minimum in the modulation index is observed. This indicates that the silicon strips have become highly insulating. Our simulations indicate indeed that for this gate field the slightly *n*-doped strips are fully depleted of free electrons. At more negative gate fields, the modulation index increases again because of the formation of a conductive hole inversion layer.

Charge density and resistance of the real structure were simulated as a function of the gate voltage by means of the two-dimensional simulation package DESSIS [31]. For a qualitative confirmation, both quantities were then compared with the numerical solution of the one-dimensional MIS equations [23]. Both methods predicted the three different regimes (accumulation, depletion and inversion), as observed in our experiments.

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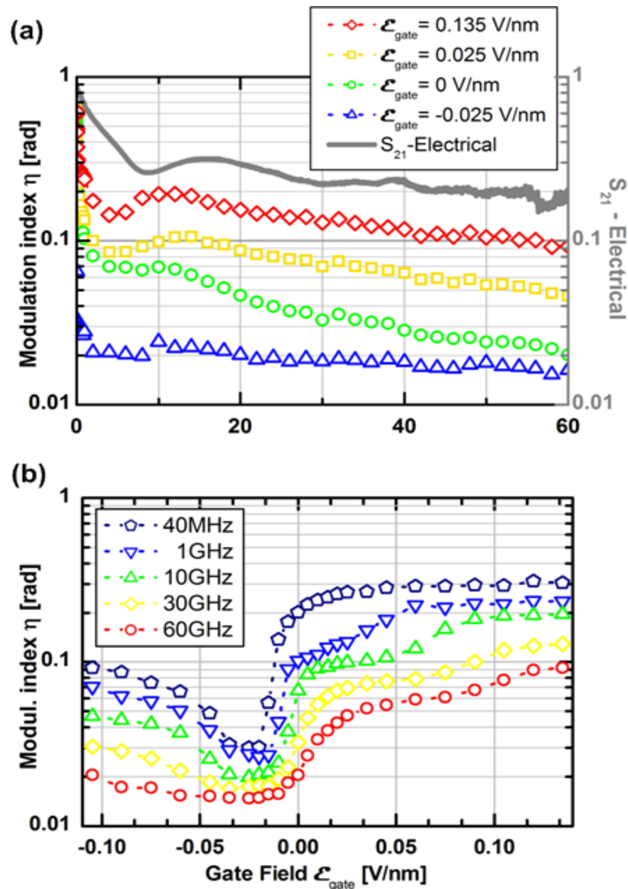

Fig. 4. Response of the DUT vs. frequency and gate field for 1 V modulation amplitude. (a) Phase modulation index η vs. frequency for selected electrical gate fields. The measured modulation frequency range is 1 kHz to 60 GHz. When varying the gate field from −0.025 V/nm to 0.135 V/nm the silicon strips become more conductive, and the modulation index increases accordingly. The gray curve is the S_{21} electrical transmission of the metallic electrical waveguide (voltage ratio); the decrease to 0.3 is an undesired effect of the electrical losses of our test device. (b) Modulation index vs. gate field for selected modulation frequencies. Each curve reaches a plateau at high gate fields. For a gate field strength of E_{gate} = −0.025 V/nm the silicon strips become highly insulating, therefore a minimum is observed. At more negative fields the modulation increases again because of the formation of a conductive hole inversion layer in the silicon strips.

6. Discussion and conclusion

In this first implementation, the poling of the organic cladding is incomplete. By exploiting the full potential of organic electro-optic materials, the drive voltage can be decreased by a factor of eight (see Appendix D). Moreover, the electrical performance of the current metal electrodes is not optimal, Fig. 4(a). This can be improved in future devices by increasing the thickness of the metallization [14], or by using a distributed on-chip RF driver [32].

The ALMod structure proposed in Fig. 1 offers a number of advantages when compared with structures made conductive by ion implant [10,14]. First, the silicon strips of Fig. 1 can be made notably thinner than the 60 nm used in Fig. 2. In fact, thin strips are good enough since for gate fields of 0.135 V/nm or higher, more than 90% of the free carriers are already concentrated in the first 10 nm from the Si/SiO_2 interface. Also, for thin strips the optical field is concentrated more strongly inside the slot leading to a more efficient modulation [14].

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The second advantage is that the strips do not require doping anymore, so that the electron mobility remains unperturbed and high [33], leading to lower optical losses for a given conductivity (see Appendix A). Third, when using thin gate oxides (in the order of 10 nm), gate fields seven times larger than those used in our work can be applied [24] decreasing the strip resistances even more. This will become important once narrower slots are fabricated, since then an additional factor ten in the modulation efficiency can be gained [14], at the price of a larger slot capacitance.

In summary, we demonstrated the first 42.7 Gbit/s operation of an SOH electro-optic modulator. We introduced a method for increasing the conductivity of the thin silicon electrodes by using a novel electron accumulation-layer technique. This way, the modulation increased by a factor of five at 60 GHz while the optical loss increased by less than 1 dB.

Appendix

A. Optical absorption caused by injected carriers

The well-known empirical equations of Soref and Bennett [34] relating the optical absorption in silicon to the free carrier density is based on experimental data where the free carriers come from impurity ionization and not from carrier injection. Soref and Bennett explicitly assumed equivalence between the two cases [34]. Instead, the Drude-Lorenz model predicts that the optical absorption coefficient is proportional to the free carrier density N and to the inverse of the mobility μ. In doped samples the mobility is strongly impaired by scattering at impurities, while this is not the case for injected carriers in pure silicon [33]. As an example, the electron mobility drops from roughly 1200 $\mathrm{cm}^2/(\mathrm{Vs})$ to less than 300 $\mathrm{cm}^2/(\mathrm{Vs})$ passing from an impurity concentration of 10^{16} cm^{-3} to 10^{18} cm^{-3} [35]. As a consequence, for a given free electron concentration N_e, not only the conductivity $\sigma = q\, N_e\, \mu_e$ is lower for doping than for injection, but also the optical loss $\alpha_{\mathrm{Drude}} \propto N_e/\mu_e$ is higher. This indicates that injected carriers have an intrinsic advantage over carriers coming from impurity ionization when both, high conductivity and low optical loss, are required [36].

B. Waveguide fabrication

The waveguides were fabricated within the ePIXfab framework by CEA-LETI according to standard processes of the microelectronic industry [37]. Two silicon-on-insulator (SOI) wafers were used, with layers of 220 nm thick crystalline silicon and 2 µm thick silicon oxide. The wafers were first implanted with arsenic for reaching a uniform ion concentration of $10^{17}/\mathrm{cm}^{-3}$. To this end, a dose of $5 \times 10^{12}/\mathrm{cm}^2$, energy of 150 keV, tilt 0°, and twist 0° was used. Grating couplers [27] were then created by means of a 248 nm DUV lithography followed by 70 nm silicon etch performed with HBr. A high temperature oxide (HTO) layer of 130 nm used as a hard mask was grown and subsequently structured by means of 193 nm DUV lithography. A 150 nm silicon etch was used to define the waveguides. Taking advantage of the self-alignment with the pre-existing hard-mask, a 248 nm lithography defined the regions for a full silicon etch inside the slots. A thermal oxidation at 1100°C for 10 minutes was performed for reducing the surface roughness. A 248 nm DUV lithography defined the high-doping regions for the formation of ohmic contacts beneath the metal electrodes. To this end, the wafers were implanted with arsenic using a dose of $2 \times 10^{15}/\mathrm{cm}^2$ and an energy of 30 keV. The ions were activated with a 1050°C annealing for 15 minutes. At this point, one wafer was not processed further for future optical loss measurements. Waveguides belonging to this wafer, but also coated with the nonlinear organic material, had an insertion loss of 16 dB (10 dB of which is caused by the grating couplers). A 500 nm thick silica protection layer was deposited on the entire wafer. A 248 nm DUV lithography was followed by a silica etch down to the silicon layer. A Ti/TiN/AlCu metal stack having a total thickness of 600 nm was deposited by physical vapor deposition (PVD) on the entire wafer. A 248 nm DUV lithography and a reactive ion etch (RIE) with chlorine was used to structure

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the metal electrodes. The wafer was then annealed for 30 minutes at 425°C. Finally, the slots were opened by means of a silica etch. The waveguides were spin-coated with the nonlinear organic material and poled *in situ*. The insertion loss of the waveguide is 40 dB. This 24 dB increase is mostly due to an error that occurred in the last silica etch step, which considerably increased the surface roughness of the waveguide. We are currently working on improving this process.

C. Method used for determining the modulation index

In the frequency range between 40 MHz and 60 GHz we derived the phase modulation index η by evaluating the ratio $J_0^2(\eta)/J_1^2(\eta)$ between the central intensity peak and the first sideband intensity of the phase modulated signal (J_v is the Bessel function of the first kind). The spectra were recorded with an optical spectrum analyser (Apex AP2050). In the frequency range between 1 kHz and 40 MHz we inserted the phase modulator in one arm of a fiber-based Mach-Zehnder interferometer. The interference was recorded by means of a wide-band photodetector (Thorlabs PDA10CF) and a 1 GHz oscilloscope. The achieved phase modulation was derived from the amplitude of the intensity modulation.

D. Poling of the electro-optic material and origin of the phase shift

The commercially available nonlinear material M1 [25] was poled by applying 16 V to the metal electrodes while the device was heated from room temperature to 141°C and then rapidly cooled as soon as this temperature was reached. Unpoled samples showed no detectable spectral sidebands (phase modulation smaller than 0.002 rad/V), demonstrating that the measured phase shift is actually due to the cladding nonlinearity and is not caused by free carriers. From the modulation index in the low frequency limit we estimate an actual nonlinearity coefficient of r_{33} = 20 ± 2 pm/V. There is large potential for further increasing this value: The same material is used in commercially available polymer modulators where values of r_{33} = 70 pm/V are routinely achieved by parallel plate poling. In SOH systems, values as high as r_{33} = 40 pm/V have been reported [21]. The highest r_{33} value achieved by *in situ* poling amounts to 170 pm/V [38]. This would result in a reduction of the operation voltage by a factor of eight.

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