Multi-Chip Integration by Photonic Wire Bonding: Connecting Surface and Edge Emitting Lasers to Silicon Chips

T.Hoose^{1,2}, M. Billah^{1,2}, M. Blaicher^{1,2}, P. Marin², P.-I. Dietrich^{1,2}, A. Hofmann³, U. Troppenz⁴, M. Moehrle⁴, N. Lindenmann⁵, M.Thiel⁵, P. Simon⁵, J.Hoffmann⁵, M. L. Goedecke⁶, W. Freude², C. Koos^{1,2}

¹Ins. of Microstructure Technology (IMT), Karlsruhe Institute of Technology (KIT), H.-von-Helmholtz-Platz 1, 76344 Eggenstein, Germany ²Institute of Photonics and Quantum Electronics (IPQ), Karlsruhe Institute of Technology (KIT), Engesserstrasse 5, 76131 Karlsruhe, Germany ³Institute of Applied Computer Science (IAI), KIT, Hermann-von-Helmholtz-Platz 1, 76344 Eggenstein, Germany

⁴Fraunhofer Institute for Telecommunications, Heinrich Hertz Institute (HHI), Einsteinufer 37, 10587 Berlin, Germany ⁵Now with Nanoscribe GmbH, Hermann-von-Helmholtz-Platz 1, 76344 Eggenstein, Germany ⁶Now with Institut für Technische Optik (ITO), University Stuttgart, Pfaffenwaldring 9, 70569 Stuttgart, Germany tobias.hoose@kit.edu, christian.koos@kit.edu

Abstract: We demonstrate coupling of surface and edge emitting InP lasers to silicon photonic chips using photonic wire bonding. We confirm that back-reflections from the silicon chip do not deteriorate the linewidth of the lasers.

OCIS codes: (130.6622) Subsystem integration and techniques; (220.4241) Nanostructure fabrication; (200.4650) Optical Interconnects

1. Introduction

Silicon photonics has become a mainstay of photonic integration for a wide range of applications [1]. One of the remaining challenges is the integration of light sources on the silicon platform. Several approaches to overcome this obstacle have been explored in the past. Electrically pumped Ge-on-Si lasers show an interesting path towards largescale monolithic integration [2], but the performance of these devices still cannot compete with that of conventional InP-based light sources. As an alternative, epitaxial growth and wafer bonding of III-V semiconductors on silicon substrates have shown promising results [3, 4], but elaborate front-end processing outside established CMOS fabrication workflows is required. A simpler approach relies on mounting of pre-processed laser dies on silicon photonic chips [5]. This concept allows integration of known-good InP devices on the silicon platform, but requires high-precision alignment and leads to a large on-chip footprint. These disadvantages can be overcome by the concept of photonic wire bonding [6], which enables low-loss single-mode connections across chip boundaries. Photonic wire bonding does not require precise mechanical alignment of chips, and is therefore well suited for automated production. The viability of the technique has been demonstrated by coupling silicon photonic chips to each other [6] or to multi-core fibers [7]. The concept is also applicable to multi-chip integration of InP-based light sources, where photonic wire bonding of horizontal-cavity surface-emitting lasers (HCSEL) [8] to silicon photonic circuitry has previously been demonstrated [9]. However, coupling to HCSEL still requires dedicated surfaceemitting coupling structures based on proprietary fabrication processes, whereas commercially available InP photonic circuitry usually relies on butt-coupling interfaces. Moreover, only single interfaces have been realized up to now, whereas photonic wire bonding lends itself to a co-integration of device arrays. Further, considering the fact that the laser is coupled to the silicon photonic chip without an intermediate optical isolator, it was still unclear if back-reflections into the laser cavity impact the laser linewidth.

In this paper we show that photonic wire bonding can be used to connect silicon photonic chips to standard edgeemitting InP light sources. In a proof-of-principle experiment, we achieve a coupling loss of 4.3 dB with potential for further improvement. Moreover, we realize photonic wire bond interfaces of an array of four HCSEL to an array of silicon photonic waveguides, thereby demonstrating the scalability of the concept. Measuring the linewidth of the lasers before and after photonic wire bonding, we confirm that back-reflections from the silicon photonic chip do not lead to increased phase noise. The experiments demonstrate that photonic wire bonding can serve as a generic concept for connecting photonic multi-chip modules comprising InP-based light sources and silicon-based photonic circuits.

2. Multi-chip integration of an edge-emitting laser

The concept of multi-chip integration of silicon photonic circuitry with edge-emitting InP lasers is illustrated in Figure 1(a). The laser die and the silicon-on-insulator (SOI) chip are mounted on a common carrier. Precise alignment between the laser facet and the SOI waveguides is not required, since the trajectory of the photonic wire bond is adapted to the positions of the interfaces on the chips. Matching of mode fields is achieved by three-dimensional tapers at both ends of the photonic wire bond (PWB). At the interface to the silicon photonic chip, inversely tapered SOI waveguides are used to realize low-loss transitions to the photonic wire bond [6]. A grating

coupler is used to interface the SOI waveguide to a standard single-mode fiber (SMF) for device characterization. The light coupled to the SMF can be analyzed by a power meter (PM) and an optical spectrum analyzer (OSA). An SEM image of the fabricated device is depicted in Figure 1(b). The PWB spans a gap of about 100 µm between the laser die and the SOI chip. To estimate the insertion losses of the PWB interface, we first measure the currentpower characteristic of the bare laser die using an integrating sphere as a detector, see black curve in Figure 1(c), which refers to the power scale on the left-hand side. We then connect the laser to the silicon photonic chip using a PWB embedded into a low-index polymer cladding, and measure the power coupled to the SOI waveguide (red solid line, right-hand scale). The insertion loss of the PWB interface amounts to 4.3 dB, including coupling from the laser to the PWB, propagation within the PWB, and coupling from the PWB to the SOI waveguide. The losses of the interface between the SOI waveguide and the SMF amount to 5.2 dB for a 7.5° inclination of the SMF with respect to the vertical. This number was obtained from separate measurements using reference waveguides with nominally identical grating couplers on the same chip. Notably, the photonic wire bonding does not change the threshold current of the laser, Figure 1(c). This experiment represents the first demonstration of a PWB interface between a silicon photonic chip and an edge-emitting InP device, with vast potential for further improving the coupling efficiency. The current insertion loss is very likely dominated by the coupling loss from the laser facet to the fundamental mode of the PWB. Systematic investigations of laser mode field diameters and the exact position of the emission spot are currently conducted in order to improve the coupling.

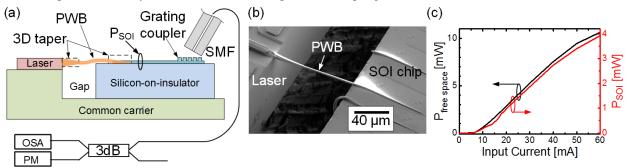


Figure 1: Concept of a photonic wire bond (PWB) connecting an edge-emitting InP laser emitting at a wavelength of 1593 nm to a silicon photonic circuit on a silicon-on-insulator (SOI) substrate. (a) Laser and SOI chip are mounted on a common carrier. The PWB trajectory is adapted to the positions of the coupling interfaces on the chips. The mode fields are matched by three-dimensional tapers at both ends of the PWB. The photonic wire bond is embedded in a low-index cladding (not depicted). For measuring the insertion loss, a grating coupler interfaces the SOI waveguide to a standard single-mode fiber (SMF). (b) SEM picture of the fabricated multi-chip module before applying a low-index overcladding. (c) Power-current characteristic of the bare laser die (solid black, left vertical axis) and of the bonded device (red, right axis). Photonic wire bonding does not change the laser threshold. The insertion loss of the PWB interface amounts to 4.3 dB, comprising coupling to and from the PWB as well as propagation losses in the PWB.

3. Linewidth measurement and multi-chip integration of surface-emitting laser

Previously we demonstrated that photonic wire bonding can be used to connect silicon photonic circuitry to HCSEL [9]. Whereas first experiments concentrated on single PWB interfaces, we now demonstrate multi-chip integration of HCSEL arrays with arrays of SOI waveguides. Figure 2(a) shows an SEM image of a fabricated multi-chip module comprising 4 HCSEL, which are bonded to a SOI chip. For avoiding contamination of the nearby electrical contact pads,, we did not apply a cladding to the PWB interface prior to characterization. For HCSEL 1, 2, 3, and 4, we measure insertion losses of 4.2 dB, 4.9 dB, 4.4 dB, and 5.8 dB, respectively. These loss figures can be further reduced by applying a low-index overcladding [9].

In our multi-chip modules, the lasers are coupled to the silicon photonic chip without an intermediate optical isolator. This leads to a back-reflection of optical power into the laser cavity, an influence which might impact the laser linewidth. To investigate this aspect, we measure and compare the linewidth of the lasers before and after photonic wire bonding, Figure 2 (b). The linewidth is obtained by recording the beat signal of the emitted light with that of a high-quality external-cavity (ECL) reference laser, and by evaluating of the corresponding variance of the phase increments [10]. The ECL linewidth amounts to 14 kHz and can safely be neglected compared to the linewidth of the distributed-feedback (DFB) HCSEL, which roughly range between 2 MHz and 5 MHz. Figure 2(b) shows the power spectrum of the beat signal obtained from HCSEL 1. As proposed in [10], the optical linewidth Δf of this laser can be inferred from the variance of the phase increments for small time delays and amounts to 5.3 MHz before and 4.9 MHz after photonic wire bonding. Likewise, for HCSEL 2, 3, and 4, the linewidths do not change significantly

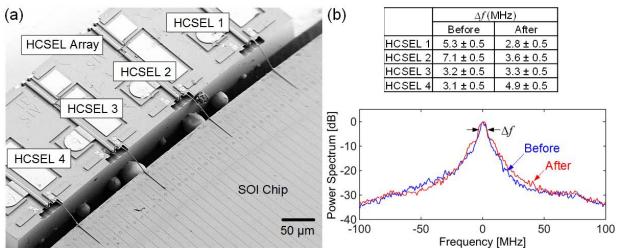


Figure 2: Array of horizontal-cavity surface-emitting lasers (HCSEL) connected to an array of silicon-on-insulator (SOI) waveguides by photonic wire bonding together with laser linewidth measurements. (a) SEM picture of the fabricated multi-chip module. For HCSEL 1, 2, 3, and 4, we measure insertion losses of 4.2 dB, 4.9 dB, 4.4 dB, and 5.8 dB, respectively. (b) We measure and compare the linewidth of the lasers before and after photonic wire bonding. The linewidth of the distributed-feedback (DFB) HCSEL ranges roughly between 2 MHz and 5 MHz. The power spectrum of the beat signal obtained from HCSEL 1 is plotted as a function of the frequency offset from the carrier. The optical linewidth Δf of this laser can be inferred from the variance of the phase increments for small time delays and amounts to 5.3 MHz before and to 4.9 MHz after photonic wire bonding. Likewise, for HCSEL 2, 3, and 4, the linewidths do not change significantly by photonic wire bonding, and we conclude that potential reflections from the PWB interface and from the connected SOI circuit do not deteriorate the laser spectra.

by photonic wire bonding, and we conclude that potential reflections from the PWB interface and from the connected SOI circuit do not deteriorate the laser spectra.

4. Summary

We demonstrated that photonic wire bonding enables multi-chip modules that combine standard InP edge-emitting lasers with standard silicon photonic circuitry. We show the first connection between an edge-emitting DFB laser and a standard silicon-on-insulator (SOI) waveguide, achieving a coupling loss of 4.3 dB. Moreover, we demonstrate photonic wire bonding of an array of four HCSEL to an array of silicon photonic waveguides. Measuring the linewidth of the lasers before and after photonic wire bonding, we confirm that back-reflections from the PWB interface and from the silicon photonic chip do not lead to increased phase noise. The experiments demonstrate that photonic wire bonding can serve as a generic concept for photonic multi-chip modules that combine InP-based light sources and silicon-based photonic circuits.

This work is supported by BMBF Project PHOIBOS (Grant 13N12574), by the Helmholtz International Research School for Teratronics (HIRST), by the European Research Council (ERC Starting Grant 'EnTeraPIC', number 280145), by the EU-FP7 project BigPipes, by the DFG funded project CRC 1173 "Wave Phenomena", and by the Alfried Krupp von Bohlen und Halbach Foundation.

5. References

- [1] M. Hochberg and T. Baehr-Jones. "Towards fabless silicon photonics", Nature Photon. Vol. 4, 492 494, 2010.
- [2] R. Camacho-Aguilera, et al., "An electrically pumped germanium laser", Opt. Express, Vol. 20, No. 10, 11316-11320, May 2012.
- [3] S. Feng et al., "Epitaxial III-V-on-silicon waveguide butt coupled photodetectors", Opt. Lett., Vol. 37, No. 19, 4035-4037, 2012.
- [4] H. Park et al., "Device and Integration Technology for Silicon Photonic Transmitters", IEEE J. Sel. Topics Quantum Electron., Vol. 17, No. 3, 671-688, May/June 2011.
- [5] S. Tanaka et al., "Flip-Chip-Bonded, 8-Wavelength AlGaInAs DFB Laser Array Operable up to 70°C for Silicon WDM Interconnects", ECOC Cannes – France, Tu.1.1.4, 2014.
- [6] N. Lindenmann et al., "Photonic wire bonding: a novel concept for chip-scale interconnects", Opt. Express 20, 17667-17677 (2012)
- [7] N. Lindenmann *et al.*, "Connecting Silicon Photonic Circuits to Multi-Core Fibers by Photonic Wire Bonding", J. Lightw. Technol. 33, 755-760 (2015).
- [8] Moehrle, M. et al., "Ultra-low threshold 1490 nm surface-emitting BH-DFB laser diode with integrated monitor photodiode," in Indium Phosphide & Related Materials (IPRM), 2010 International Conference
- [9] M. R. Billah et al., "Multi-Chip Integration of Lasers and Silicon Photonics by Photonic Wire Bonding", CLEO: 2015, OSA Technical Digest (online) (Optical Society of America, 2015), Paper STu2F.2.
- [10]Kazuro Kikuchi, "Characterization of semiconductor-laser phase noise and estimation of bit-error rate performance with low-speed offline digital coherent receivers," Opt. Express 20, 5291-5302 (2012).