Hybrid 2D/3D Photonic Integration for Non-Planar Circuit Topologies

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Abstract *We present a concept for realizing crossing-free photonic integrated circuits (PIC) using 3D freeform waveguides. We prove the viability of the approach using a silicon photonic 4 × 4 switch-and-select device. The method is applicable to a wide range of PIC technologies.*

Introduction

Photonic integrated circuits (PIC) are often described as the optical analogue of electrical integrated circuits (EIC). However, due to the different natures of light and electricity, some technological problems that are trivial for EIC may present quite a challenge for PIC. For example, complex non-planar circuit topologies often require a large number of crossovers, which can be realized quite easily in EIC by using several conductive layers which are interconnected through vias. PIC design, in contrast, is essentially limited to a single layer, and complex non-planar PIC topologies may require large numbers of planar waveguide crossings (PWC). These PWC lead to signal impairments such as insertion loss, crosstalk, back reflection, or multi-mode excitation. While losses as low as 0.028 ± 0.009 dB and crosstalk of -37 dB at 1550 nm have been reported[1] for optimized high index-contrast silicon photonic PWC with a footprint of 9×9 µm², other PIC platforms have lower refractive index contrasts, which makes compact PWC with low loss and low crosstalk difficult. Moreover, for advanced PIC such as the switch-and-select (SAS) switching fabric[2], the number of PWC can be quite large and non-uniform across different waveguide paths, which is undesirable in particular if strict requirements in terms of crosstalk need to be fulfilled.

In this paper we describe a concept for designing and realizing PWC-free PIC based on three-dimensional (3D) freeform optical waveguides to cross over planar waveguides. The waveguides are realized in-situ by 3D direct laser writing using two-photon polymerization lithography[3]. This technique has previously been used for fabrication of so-called photonic wire bonds[4,5] that enable low-loss single-mode connections across chip boundaries and is well suited for automated production. In a proof-of-principle experiment, we demonstrate a 4×4 SAS device realized in silicon photonics. Moreover, to identify the potential of our approach, we analyze the general case of an $m \times n$ SAS switching fabric using graph theory. We show that our approach enables PWC-free implementation by using a number of 3D optical waveguides (3D-WG) that scales as the square root of the number of otherwise required PWC. This result has particular importance for PIC topologies that require a very large number of PWC.

The concept of 3D optical crossovers

The concept of using 3D-WG as crossovers is illustrated in Fig. 1. Fig. 1(a) and (b) show side and top views of a 3D-WG connecting two silicon-on-insulator (SOI) strip waveguides. The top SiO_2 cladding is selectively etched down to the buried oxide (BOX) layer to provide access to inversely tapered SOI strip waveguides that need to be interconnected by the 3D-WG. The 3D-WG is fabricated by direct laser writing and is tapered at its ends to enable low-loss coupling to the SOI waveguides[4]. Fig. 1(c) displays a falsely colored SEM image of two 3D-WG crossovers on our demonstrator device. The positions of the SOI waveguides are automatically detected by machine vision with the help of position markers. The footprint of the 3D-WG amounts to approximately 15×160 µm² – more than an order of magnitude smaller than previously demonstrated 3D waveguide crossovers in low index-contrast planar waveguide circuits (PLC)[6,7].

The PWC-free PIC design principle

For a theoretical analysis of the design approach, we use a SAS switching fabric, and model it with the maximal bipartite graph $K_{m,n}$ consisting of two sets of vertices, where each vertex of the first set (input ports) is connected to each vertex of the second set (output ports). The minimum number of PWC necessary to realize the switch is equal to the crossing number of the associated graph. PIC topologies of different SAS fabrics are depicted in Fig. 2. Two cases must be distinguished: In the first case, waveguides may pass behind the input ports (I_1, I_2, … I_m) or output ports (O_1, O_2, … O_n), Fig. 2(a). This corresponds to an implementation where ports are based on grating couplers on the chip surface. Finding the minimum crossing number $\nu_{m,n}$ and the corresponding topology for such a graph is an NP-complete problem[8], and up to date, the crossing number formula is only conjectured[9]. The relation is given at the top of Fig. 2(a). Conversely, for butt-coupled fiber interfaces or for fabrics embedded into an on-chip network, waveguides must not pass behind the input ports or the output ports, Fig. 2(b). In this

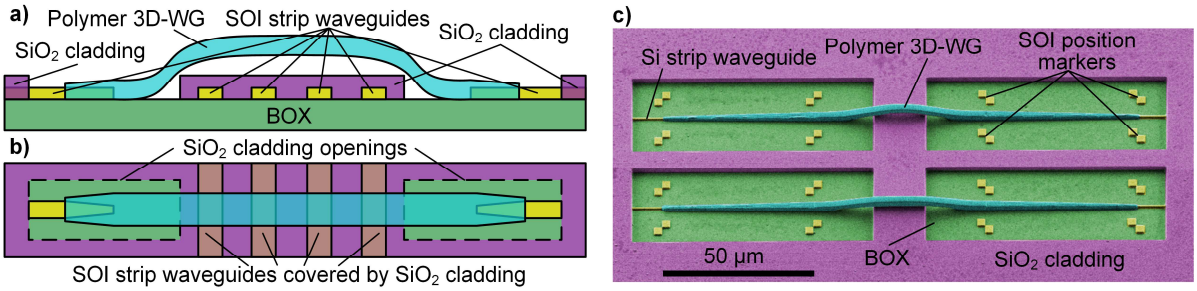

Fig. 1: Concept of 3D optical waveguide (3D-WG) crossovers on the silicon-on-insulator (SOI) platform. (a) Side view, illustrating a polymer 3D-WG, connecting two and crossing over four buried SOI strip waveguides. The SiO_2 cladding has been selectively etched down to the buried oxide (BOX) layer to make the ends of the two SOI strip waveguides accessible. (b) Top view: Both the 3D-WG and the SOI strip waveguide ends are tapered to improve optical coupling efficiency. The black dashed rectangles denote the areas from which the SiO_2 cladding has been removed. (c) Falsely colored SEM image of the two 3D-WG crossovers on the demonstrator device: Position markers are used to automatically determine the position of SOI waveguide ends, based on which the 3D-WG trajectory is calculated. The markers are made by etching of the SOI layer and are not displayed in (a) and (b). The SOI waveguides bridged by the 3D-WG are covered by the SiO_2 cladding and are invisible on the SEM image.

Table 1: Comparison of the number of needed PWC and 3D-WG for realization of $n \times n$ SAS switching fabric

Switch (n × n)	Vertically Coupled		Butt Coupled	
	$\nu_{n,n}$	$\mu_{n,n}$	$\nu'_{n,n}$	$\mu'_{n,n}$
4 x 4	4	2	36	5
8 x 8	144	18	784	25
16 x 16	3 136	98	14 400	113
32 x 32	57 600	450	246 016	481
64 x 64	984 064	1 922	4 064 256	1985

case, the minimum number $\nu'_{m,n}$ of crossings can be directly calculated along with the optimum topology. Avoiding the PWC by 3D-WG leads to the SAS topologies depicted in Fig. 2(c) and (d). It can be shown that for both cases of input ports, there is a simple algorithm to find a PWC-free topology with (not necessarily minimum) numbers $\mu_{m,n}$ and $\mu'_{m,n}$ of 3D-WG, for which each link contains at most one 3D-WG[10]. The relations for μ and μ' are given at the top of Fig. 2 (c) and (d). For increasing port counts of the $m \times n$ SAS fabric, the numbers μ and μ' of 3D-WG scale as the square root of the minimum numbers ν and ν' of otherwise necessary PWC. Table 1 indicates the numbers of PWC and 3D-WG for various different $n \times n$ SAS fabrics. Note that, already for a 16×16 switch, the number of 3D-WG is two orders of magnitude smaller than that of PWC.

Experimental demonstration

For proving the viability of the approach, we use a 4×4 switching fabric on the SOI platform based on a topology similar to the one shown in Fig. 2(c). The device contains two 3D-WG, each connecting two SOI strip waveguides. The silicon photonic base structures were fabricated through a commercial foundry using 248 nm optical lithography[11]. For fabrication of the 3D-WG, we used 3D two-photon polymerization lithography. In the SAS structure, each of the four inputs is connected to each of the four outputs by eight 1×4 switches, each of which consists of three 1×2 switches. Each 1×2 switch contains two multi-mode interfererence (MMI) couplers and two thermal phase shifters in a balanced Mach-Zehnder modulator (MZM) configuration. In total, the PIC contains 24 1×2 switches and 48 thermal phase shifters. The minimum number of drive signals is 16 (two for each of the eight 1×4 switches). All phase shifters share a common ground.

We measured transmission spectra for all 16 optical links. To couple light to the chip, we used grating couplers along with a total internal reflection fiber array (TIRFA) at one side, and a single mode fiber (SMF) at the other side. To

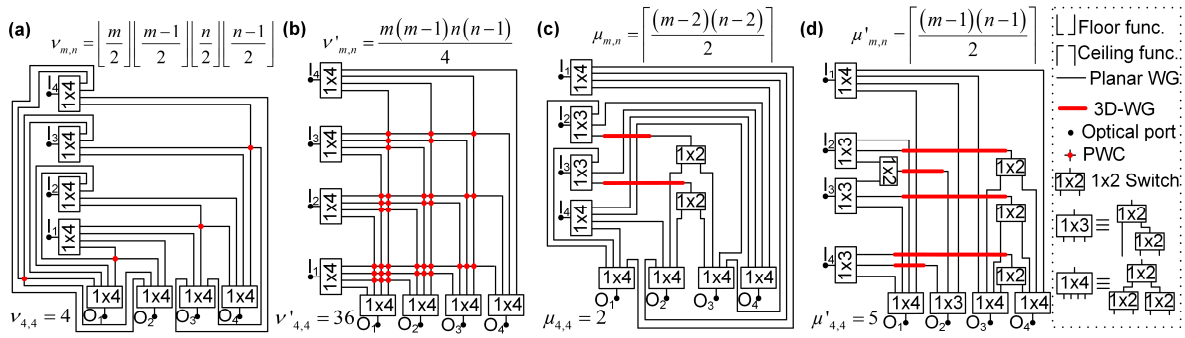

Fig. 2: Topologies of 4×4 SAS switching fabrics along with relations for the minimum numbers ν and ν' of required PWC and the numbers μ and μ' of 3D-WG. **(a)** Optimum topology of a 4×4 SAS fabric for the case that waveguides may pass behind the input ports I_1, I_2, I_3, I_4 or output ports O_1, O_2, O_3, O_4. This corresponds to fiber interfaces based on vertical emission from a grating coupler. The minimum number of required PWC amounts to $\nu_{4,4} = 4$ (in general, $\nu_{m,n}$ is conjectured) **(b)** Optimum topology of a 4×4 SAS fabric for the case that waveguides must not pass behind the input ports or the output ports. This corresponds to butt-coupled fiber interfaces or to a structure embedded into an on-chip network. The minimum number of required PWC amounts to $\nu'_{4,4} = 36$. **(c)** PWC-free topology of a 4×4 SAS fabric for the same case as described in (a). The number of 3D-WG amounts to $\mu_{4,4} = 2$. **(d)** PWC-free topology of a 4×4 SAS fabric for the same case as described in (b). The number of 3D-WG amounts to $\mu'_{4,4} = 5$.

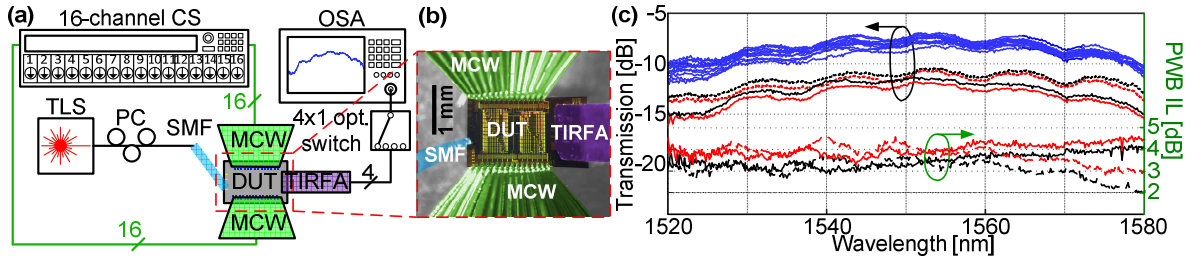

Fig. 3: (a) Experimental setup: CS – current source, OSA – optical spectrum analyzer, TLS – tunable laser source, PC – polarization controller, SMF – single mode fiber, MCW – multi contact wedge, DUT – device under test, TIRFA – total internal reflection fiber array. **(b)** Microscope image of electrically and optically contacted DUT. **(c)** Upper part: Measured transmission spectra between all of the inputs and all of the outputs of the DUT. Blue graphs denote transmission spectra of the 12 links that do not contain 3D-WG, whereas black and red denote transmission spectra of the two links that contain 3D-WG. Lower part: Excess insertion loss (IL) for the 3D-WG vs. wavelength. For calculating the excess loss, we use the transmission spectrum from reference links that do not contain 3D-WG and apply a correction for the different lengths of the on-chip SOI waveguide.

contact the chip electrically, we used two multi contact wedges (MCW) with multiple DC probes. The device was driven by 16 current sources that were switched between the DC probes. The results are displayed in Fig. 3(c). In the upper part, blue graphs denote transmission spectra for the 12 links that do not contain 3D-WG, whereas black and red is used for the four links with one 3D-WG. In these measurements, fiber-chip interfaces have already been taken into account by referencing all spectra to the transmission of short SOI waveguide with two grating couplers. For calculating the excess loss of the two 3D-WG bridges, we use a reference transmission spectrum taken through the same output grating coupler, and we consider the length differences of the respective on-chip waveguides. The results are depicted in the lower part of Fig. 3(c); the average losses of the two 3D-WG bridges amount to 3.3 dB and 3.9 dB. These insertion losses are significantly higher than 1.6 dB previously obtained from comparable photonic wire bond structures[4]. This is attributed to a non-optimum waveguide trajectory. We expect that systematic optimization can bring these losses down to approximately 1 dB. Similarly, the rather high on-chip insertion losses of the SOI switch structure (approximately 7 dB at 1550 nm) may be improved. Each path through the switch contains 8 MMI splitters, 4 thermal phase shifters, and up to 6.2 mm of SOI strip waveguides. Assuming optimized devices with MZM insertion losses of 0.33 dB, waveguide propagation losses of 0.6 dB/cm, and reduced waveguide lengths of less than 3 mm, we expect on-chip insertion losses of less than 2 dB for the SOI waveguide structures. Moreover, by using ultra-compact 2×2 switching cells based on liquid-crystal phase shifters[12], the footprint of the device might be considerably reduced.

Summary

We have introduced a concept for designing and realizing non-planar PIC topologies. Planar waveguide crossings are replaced by 3D freeform waveguides. In a proof-of-principle experiment, we have demonstrated the viability of the approach using a silicon photonic 4×4 switch-and-select (SAS) structure. We further perform a theoretical analysis that shows that the hybrid 2D/3D concept has clear advantages in terms of scalability to port-count SAS switch structures. The design method is independent from the underlying PIC technologies. We believe that the results pave the way towards highly complex non-planar PIC.

Acknowledgements

We acknowledge support from the Erasmus Mundus Joint Doctorate program EUROPHOTONICS (Grant No. 159224-1-2009-1-FR-ERA MUNDUS-EMJD), the Deutsche Forschungsgemeinschaft (DFG) through CRC 1173 (Wave Phenomena), the European Research Council (ERC Starting Grant 'EnTeraPIC', number 280145), the BMBF project PHOIBOS, the Alfried Krupp von Bohlen und Halbach Foundation, the Initiative and Networking Fund of the Helmholtz Association, the Karlsruhe School of Optics & Photonics (KSOP), the Helmholtz International Research School for Teratronics (HIRST), the EU-FP7 projects PHOXTROT and BIGPIPES, and the Karlsruhe Nano-Micro Facility (KNMF). We further acknowledge fruitful discussions with M. Nöllenburg and M. Axenovich, KIT, Germany.

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