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13. Sept. 2016

Title:	Novel DC-AC Converter Topology for Multilevel Battery Energy Storage Systems
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Institute:	Karlsruhe Institute of Technology (KIT) Elektrotechnisches Institut (ETI)
Type:	Conference Proceedings
Initially published at:	PCIM Europe - International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management Nuremberg, 14 - 16 May 2013 Date of Conference: 14 – 16 May 2013 Page(s): 699 – 706 Conference Location: Nuremberg, Germany Publisher: Mesago PCIM GmbH, VDE Verlag GmbH ISBN: 978-3-8007-3505-1 ISSN: 2191-3358
Hyperlinks:	URL: http://www.pcim-europe.com

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Novel DC-AC Converter Topology for Multilevel Battery Energy Storage Systems

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Abstract

This paper presents a novel DC-AC converter circuit, especially for the application in multilevel battery energy storage systems (BESS), see fig. 1c. A drawback of the commonly used cascaded H-bridge is that the RMS values of the battery currents can reach multiples of the mean DC battery currents. Additional DC-DC converters in the cells can reduce the AC components of the battery currents, but cause additional semiconductor losses and require large inductors. The circuit presented in this paper reduces these AC contents with less semiconductor losses and smaller inductors than standard DC-DC converters connected to H-bridges.

1 Introduction

1.1 The novel converter topology

The novel converter topology is cell-based and presented in fig. 1. Every cell (fig. 1a) is connected to its own battery. The cell circuit consists of a DC-DC converter with reduced voltage (S5-S6) and a DC-AC converter (S1-S4). Converters can be built in two configurations: in single cell configuration (fig. 1b) and in multilevel-configuration (fig. 1c) with series connected cells. The aim of the novel circuit is loss-reduction, compared to state of the art circuits.
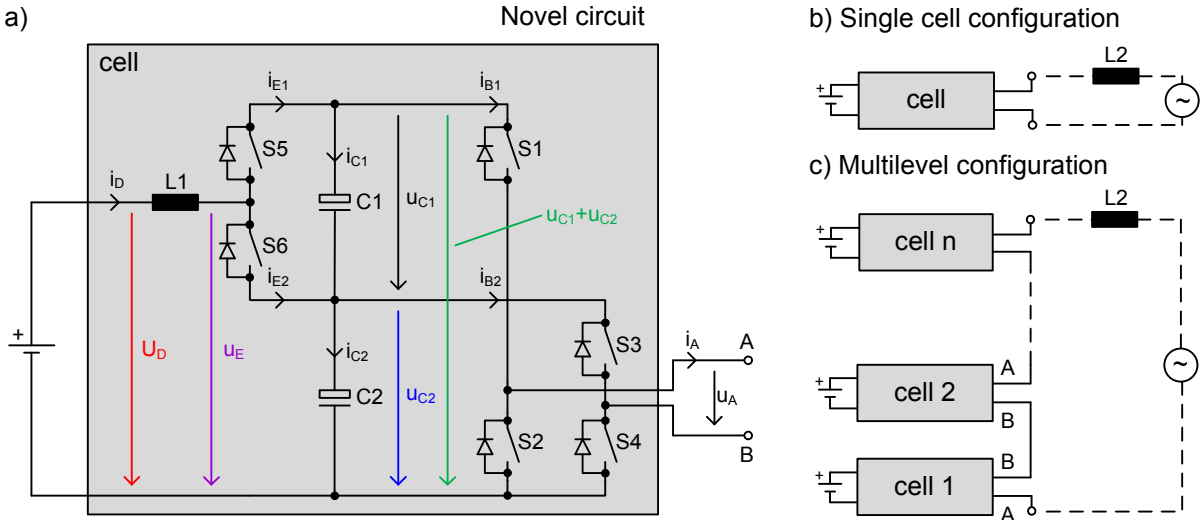

Figure 1:
a) The novel cell circuit b) Single cell configuration
c) Principle of connecting cells to a multilevel structure

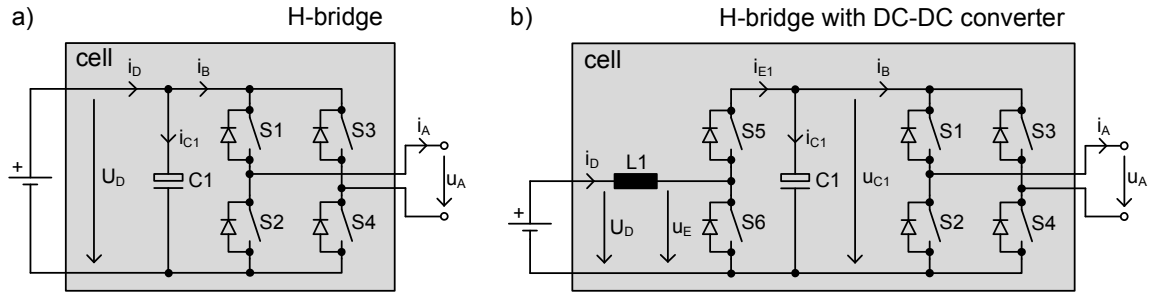## 1.2 State of the art multilevel converter topologies and their drawbacks

Figure 2: a) H-bridge b) H-bridge with DC-DC converter

A well-known multilevel topology is the cascaded H-bridge, which is described in [1] and [2]. The topology is based on series-connected H-bridge cells with or without additional DC-DC converter (fig. 2). Every cell is connected to its own battery. Without additional DC-DC converter (fig. 2a), current components with switching frequency or higher frequencies can be filtered by the capacitor C1. The power at the AC side is pulsating with twice the AC fundamental frequency. Current components with lower multiples of the AC fundamental frequency cannot be filtered sufficiently with an adequate size of C1. This causes the RMS value of i_D to be larger than the mean value of i_D, which leads to additional losses at the internal resistance of the battery and can lead to accelerated battery aging. When using an additional DC-DC converter (fig. 2b), the energy pulsation can be stored in C1 and the battery current i_D can be controlled to be nearly free of harmonics of the AC fundamental frequency. However, the DC-DC converter causes additional losses and requires an inductor with large volume.

1.3 Function and advantages of the novel converter topology

The battery current i_D is held constant by the novel cell circuit (fig. 1a), while the power at the AC-side is pulsating. The capacitors C1 and C2 buffer the pulsating energy. This causes the voltages u_{C1} and u_{C2} to vary periodically. For low losses, the voltage u_{C1} shall be as small as possible. However, the following condition has to be maintained at every time: $u_{C2} < U_D < u_{C1} + u_{C2}$. The battery current i_D is then controllable by S5-S6.

The voltage u_A at the AC-side can reach four levels, depending on the states of S1 - S4. The switching states (1) to (3) are sufficient for the PWM scheme shown in fig. 3, as long as $\cos(\varphi_{UI})$ at the AC-side is non-zero.

switching state	closed switches	voltage	current	current
(1)	S2, S4	$u_A = 0$	$i_{B1} = 0$	$i_{B2} = 0$
(2)	S1, S4	$u_A = u_{C1} + u_{C2}$	$i_{B1} = i_A$	$i_{B2} = 0$
(3)	S2, S3	$u_A = -u_{C2}$	$i_{B1} = 0$	$i_{B2} = -i_A$
(4)	S1, S3	$u_A = u_{C1}$	$i_{B1} = i_A$	$i_{B2} = -i_A$

In the novel circuit, u_{C1} is much smaller than in the state of the art circuit, according to fig. 2b. u_{C1} is a fraction of U_D and also a fraction of the peak value of u_A. This leads to the following advantages:

- The mechanical volume and the costs of the inductor L1 depend on the switched voltage u_{C1} at constant switching frequency. If u_{C1} is reduced, L1 can be smaller and cheaper.

- In a multilevel converter, S5-S6 will have higher switching frequencies than S1-S4. The switching losses in S5-S6, decrease if the switched voltage u_{C1} is reduced [3], [4]. The necessary blocking voltage of S5-S6 is also reduced, due to the lower peak value of u_{C1}. Semiconductors with lower blocking voltage typically cause less conduction losses.

- If the lower voltage u_{C1} allows an increased switching frequency, compared to the circuit in fig. 2b, the volume and costs of L1 will be further reduced.
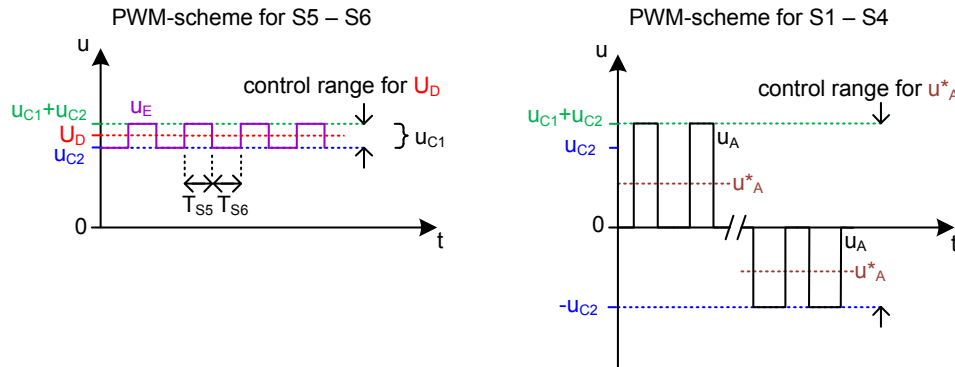

Figure 3: PWM-scheme

In a multilevel converter with cells, based on the novel circuit, it is advantageous to use an even number of cells and to connect point B of cell i with point B of cell $i + 1$ and point A of cell $i + 1$ with point A of cell $i + 2$ (fig. 1c). So the reachable voltage levels are symmetrical.

1.4 Control of the circuit

The novel circuit contains three elements with integrative behaviour (L1, C1 and C2). With a cascaded control scheme (fig. 4), the current i_D through L1 and one of the voltages u_{C1}, u_{C2} or the sum voltage $u_{C1} + u_{C2}$ can be controlled. A mathematical analysis of the circuit (section 2.2) shows, that it is sufficient to control u_{C2}, if the active power P_A at the output is positive and to control u_{C1}, if the active power P_A is negative. The voltage of the other capacitor automatically reaches a stable voltage level. This process is called "natural balancing".
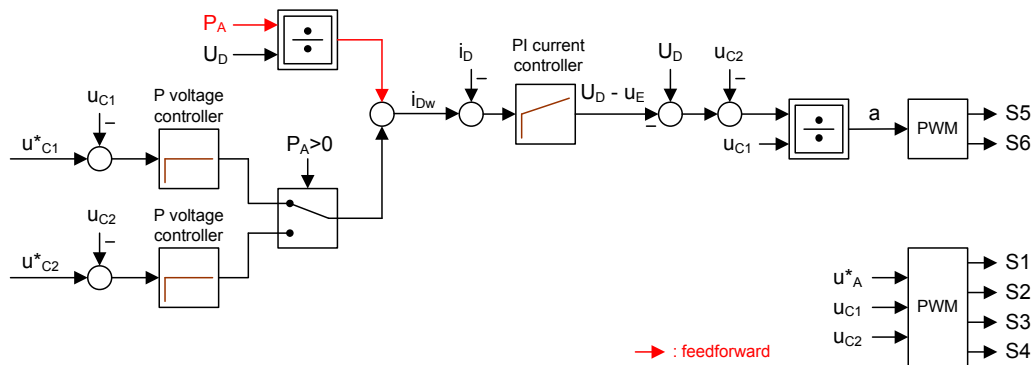

Figure 4: Control of the novel DC-AC converter circuit

The capacitor voltages u_{C1} and u_{C2} vary periodically because of the power pulsation at the AC-side. If fixed reference values are used for the voltage controllers, the periodic variations of u_{C1} and u_{C2} cause a current ripple on i_D. The amplitude of this ripple depends on the gain

of the voltage controllers. To minimize the ripple, time-variant reference values u_{C1}^* and u_{C2}^* for the capacitor voltages are used. They are continuously calculated (fig. 5 / section 2.3) and synchronized to the AC-side.
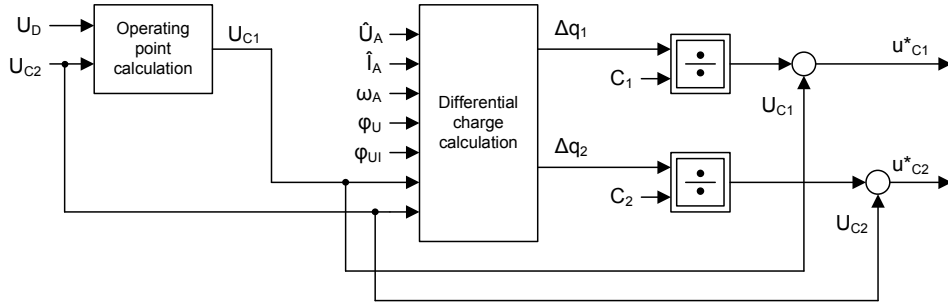

Figure 5: Calculation of time-variant reference voltages

Fig. 6 shows simulation results of the novel circuit in single cell configuration according to fig. 1b with the controller structure of fig. 4-5. The reactive power at the AC-side is zero. At $0s \leq t < 0,1s$ the sign of the active power P_A is positive and u_{C2} is controlled. At $0,1s \leq t \leq 0,2s$ the sign of P_A is negative and u_{C1} is controlled. The sign of the battery current changes at $t = 0,1s$ as result of the reversed power P_A.
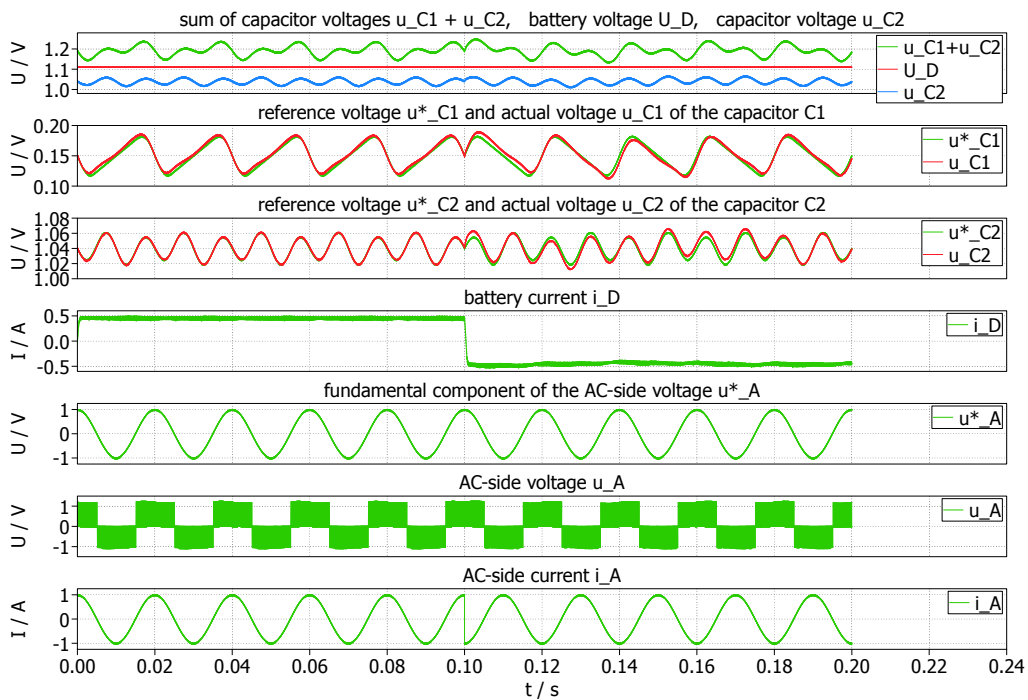

Figure 6: Simulation results

2 Mathematical analysis of the circuit

2.1 Operating points of the capacitor voltages

The power pulsation at the AC-side causes the voltage u_{C1} to vary periodically around an operating point U_{C1} and causes u_{C2} to vary around an operating point U_{C2}. U_{C1} and U_{C2}

cannot be set independently. They are linked by the natural balancing process. The relation between U_{C1} and U_{C2} is identified by analyzing the schematic of the novel circuit (fig. 1a). It is assumed, that the capacitors are very large ($C_1 \to \infty$ and $C_2 \to \infty$). The capacitor voltages u_{C1} and u_{C2} then remain at a constant level ($u_{C1} = U_{C1}$ and $u_{C2} = U_{C2}$) and some mean values can be used.

The switches S5 and S6 are controlled by a PWM-scheme with the duty-cycle a. The PWM-scheme leads to the following equations, where $T = \frac{1}{f_S}$ is the reciprocal of the switching frequency f_S:

$$T_{S5} = a \cdot T \tag{1}$$

$$T_{S6} = (1 - a) \cdot T \tag{2}$$

$$a = \frac{U_D - U_{C2}}{U_{C1}} \tag{3}$$

$$I_{E1} = a \cdot I_D \tag{4} \qquad\qquad I_{E2} = (1 - a) \cdot I_D \tag{5}$$

I_D, I_{E1} and I_{E2} are mean values per period T of the corresponding currents i_D, i_{E1} and i_{E2}. At a stationary operating point, the mean values of the capacitor currents are zero ($\int i_{C1} \, \mathrm{d}t = 0$ and $\int i_{C2} \, \mathrm{d}t = 0$). I_{B1} and I_{B2} are mean values per AC-period of the currents i_{B1} and i_{B2}. If the PWM-scheme in fig. 3 is used and the mean AC-side power during the positive half-wave of u_A^* is the same as during the negative half-wave of of u_A^*, I_{B1} and I_{B2} can be calculated with the following equations:

$$I_{B1} = I_{E1} = \frac{1}{2} \cdot \frac{P_A}{U_{C1} + U_{C2}} \tag{6} \qquad\qquad I_{B2} = I_{E2} = \frac{1}{2} \cdot \frac{P_A}{U_{C2}} \tag{7}$$

The operating point U_{C1} is calculated by solving the equations (3) to (7). It depends on the operating point U_{C2} and on the battery voltage U_D. U_{C2} shall be chosen as high as possible under fulfilling the condition $u_{C2} < U_D < u_{C1} + u_{C2}$ to minimize the switching losses in S5-S6. If U_{C2} is decreased, U_{C1} and $U_{C1} + U_{C2}$ increase.

$$U_{C1} = \frac{2 \cdot (U_D - U_{C2}) \cdot U_{C2}}{2 \cdot U_{C2} - U_D} \qquad\qquad | \; 0,5 \cdot U_D < U_{C2} < U_D \tag{8}$$

If the power, delivered during the positive half-wave of u_A^* isn't the same as during the negative half-wave of u_A^*, natural balancing is still achieved, but equation (8) cannot be applied.

2.2 Analysis of the natural balancing process

The cascaded control scheme according to fig. 4 can only control the voltage of one of the capacitors C1/C2 by controlling the current i_D. The following analysis proves, that there is a natural balancing process and the other capacitor automatically reaches a stable operating point, dependent on the sign of the active AC power P_A.

To simplify the calculations, the per-unit variables d_1 and d_2 are introduced. d_1 and d_2 are linked by equation (8), see (11). The allowed ranges of d_1 and d_2 are taken from the schematic diagram.

$$U_{C1} = d_1 \cdot U_D \qquad\qquad | \; U_{C1} > 0 \qquad\qquad \Rightarrow d_1 > 0 \tag{9}$$

$$U_{C2} = d_2 \cdot U_D \qquad\qquad | \; 0 < U_{C2} < U_D \qquad\qquad \Rightarrow 0 < d_2 < 1 \tag{10}$$

$$\qquad\qquad\qquad\qquad | \; U_{C1} + U_{C2} > U_D \qquad\qquad \Rightarrow d_1 + d_2 > 1$$

$$d_1 = \frac{2 \cdot (1 - d_2) \cdot d_2}{2 \cdot d_2 - 1} \tag{11}$$

The AC-side power, delivered during the positive half-wave of u_A^* is assumed to be the same as during the negative half-wave of u_A^*. As the natural balancing process is slow, compared to the frequency of the AC-side, i_{B1} and i_{B2} are expressed as mean values per AC-period.

$$a = \frac{U_D - u_{C2}}{u_{C1}} \tag{12}$$

$$i_{B1} = \frac{1}{2} \cdot \frac{P_A}{u_{C1} + u_{C2}} \tag{13} \qquad\qquad i_{B2} = \frac{1}{2} \cdot \frac{P_A}{u_{C2}} \tag{14}$$

$$i_{E1} = a \cdot i_D \tag{15} \qquad\qquad i_{E2} = (1 - a) \cdot i_D \tag{16}$$

$$i_{C1} = i_{E1} - i_{B1} \tag{17} \qquad\qquad i_{C2} = i_{E1} + i_{E2} - i_{B1} - i_{B2} \tag{18}$$

Natural balancing analysis: the controller for the voltage of C1 is active

u_{C1} is now controlled to remain at a constant value U_{C1}. The current i_{C1} is kept to zero by the voltage controller ($u_{C1} = \frac{1}{C_1} \int i_{C1}\, dt$). The value of u_{C2} can be different from it's operating point U_{C2}. This is described with Δd_2. The allowed range of $d_2 + \Delta d_2$ is taken from the schematic diagram. The capacitor current i_{C2} (22) is calculated with (9) to (21). In equation (22), d_1 and d_2 are listed separately, although they are linked by (11). This leads to a simpler equation.

$$u_{C1} = d_1 \cdot U_D \tag{19}$$

$$u_{C2} = (d_2 + \Delta d_2) \cdot U_D \qquad\quad | \ 0 < u_{C2} < U_D \qquad\quad \Rightarrow 0 < d_2 + \Delta d_2 < 1 \tag{20}$$

$$\qquad\qquad\qquad\qquad\quad | \ u_{C1} + u_{C2} > U_D \qquad\quad \Rightarrow d_1 + d_2 + \Delta d_2 > 1$$

$$i_{C1} = 0 \tag{21}$$

$$i_{C2} = \Delta d_2 \cdot P_A \cdot \frac{\overbrace{(d_1 + d_2 - 1)}^{>0} + \overbrace{(d_2 + \Delta d_2)}^{>0}}{U_D \cdot \underbrace{(d_2 + \Delta d_2)}_{>0} \cdot \underbrace{(d_1 + d_2 + \Delta d_2)}_{>0} \cdot \underbrace{(1 - d_2 - \Delta d_2)}_{>0}} \tag{22}$$

Natural balancing of u_{C2} is achieved for $sign\,(i_{C2}) = -sign\,(\Delta d_2)$. The highlighted signs (> 0) of the expressions in equation (22) show, that this condition is true for $P_A < 0$.

Natural balancing analysis: the controller for the voltage of C2 is active

u_{C2} is now controlled to remain at a constant value U_{C2}. The current i_{C2} is kept to zero. The value of u_{C1} can be different from it's operating point U_{C1}. This is described with Δd_1. The capacitor current i_{C1} is calculated with (9) to (18) and (23) to (25). Again, d_1 and d_2 are linked by (11).

$$u_{C1} = (d_1 + \Delta d_1) \cdot U_D \qquad\quad | \ u_{C1} > 0 \qquad\qquad \Rightarrow d_1 + \Delta d_1 > 0 \tag{23}$$

$$u_{C2} = d_2 \cdot U_D \tag{24}$$

$$i_{C2} = 0 \tag{25}$$

$$i_{C1} = -\Delta d_1 \cdot P_A \cdot \frac{\overbrace{(1 - d_2)}^{>0}}{U_D \cdot \underbrace{d_1}_{>0} \cdot \underbrace{(d_1 + \Delta d_1)}_{>0} \cdot \underbrace{(d_1 + \Delta d_1 + d_2)}_{>0}} \tag{26}$$

Natural balancing of u_{C1} is achieved for $sign\,(i_{C1}) = -sign\,(\Delta d_1)$. The highlighted signs in the expressions of equation (26) show, that this condition is true for $P_A > 0$.

2.3 Calculation of the time-variant differential charges

The pulsating power at the AC-side causes the voltages and therefore the charges of the capacitors C1 and C2 to vary periodically. In fig. 5, time-variant reference values u_{C1}^* and u_{C2}^* are calculated with the time-variant differential charges Δq_1 and Δq_2. These are the differences between actual capacitor charge and mean capacitor charge at the corresponding operating points. Δq_1 and Δq_2 can be approximated, if the AC-side voltage u_A^* and the AC-side current i_A are sinusoidal and the battery current i_D is constant. u_A^* and i_A are described by the following equations, where φ_{UI} is the phase shift between voltage and current:

$$u_A^* = \hat{U}_A \cdot \cos\left(\varphi_U\right) \tag{27}$$

$$i_A = \hat{I}_A \cdot \cos\left(\varphi_U - \varphi_{UI}\right) \tag{28}$$

$$\varphi_U = \omega_A \cdot t \qquad\qquad\qquad | \ 0 \leq \varphi_U < 2\pi \tag{29}$$

The actual power p_A and the active power P_A at the AC-side are:

$$p_A = u_A^* \cdot i_A = \hat{U}_A \cdot \hat{I}_A \cdot \cos\left(\varphi_U\right) \cdot \cos\left(\varphi_U - \varphi_{UI}\right) \tag{30}$$

$$P_A = \frac{\hat{U}_A \cdot \hat{I}_A}{2} \cdot \cos\left(\varphi_{UI}\right) \tag{31}$$

The calculations can be simplified, if the following approximations are made: the currents $i_{E1} = I_{E1}$ and $i_{E2} = I_{E2}$ are assumed as constant. The differences between the operating points and the actual capacitor voltages $U_{C1} - u_{C1}$ and $U_{C2} - u_{C2}$ are assumed as small relative to U_{C2}. The currents I_{E1}, I_{E2}, i_{B1} and i_{B2} are then approximated by:

$$I_{E1} = \frac{1}{2} \cdot \frac{P_A}{U_{C1} + U_{C2}} \tag{32} \qquad\qquad I_{E2} = \frac{1}{2} \cdot \frac{P_A}{U_{C2}} \tag{33}$$

$$i_{B1} = \begin{cases} \dfrac{p_A}{U_{C1} + U_{C2}} & | \ u_A^* \geq 0 \\ 0 & | \ u_A^* < 0 \end{cases} \tag{34} \qquad i_{B2} = \begin{cases} 0 & | \ u_A^* \geq 0 \\ \dfrac{p_A}{U_{C2}} & | \ u_A^* < 0 \end{cases} \tag{35}$$

The charge differences Δq_1 and Δq_2 can be calculated by integrating the capacitor currents i_{C1} and i_{C2}. The initial differential charges Δq_{10} and Δq_{20} are defined by the condition, that Δq_1 and Δq_2 shall be free of a mean value over a period of $0 \leq \varphi_U < 2\pi$.

$$i_{C1} = I_{E1} - i_{B1} \tag{36} \qquad\qquad i_{C2} = I_{E1} + I_{E2} - i_{B1} - i_{B2} \tag{37}$$

$$\Delta q_1 = \frac{1}{\omega_A} \int_0^{\varphi_U} i_{C1}\,\mathrm{d}\varphi_U + \Delta q_{10} \tag{38} \qquad \Delta q_2 = \frac{1}{\omega_A} \int_0^{\varphi_U} i_{C2}\,\mathrm{d}\varphi_U + \Delta q_{20} \tag{39}$$

$$\int_0^{2\pi} \Delta q_1\,\mathrm{d}\varphi_U = 0 \tag{40} \qquad\qquad \int_0^{2\pi} \Delta q_1\,\mathrm{d}\varphi_U = 0 \tag{41}$$

3 Experimental results

A single prototype cell with the circuit of fig. 1a and the controller structure of fig. 4-5 has been built (fig. 7). The AC-side is connected via an inductor L2 and a transformer to the AC-grid. The DC-side was first connected to a DC power supply, then to a lead-acid battery. The sinusoidal current i_A is PLL-synchronized to the secondary transformer voltage u_T. The circuit is stable and has been successfully tested with different phase angles φ_{UI} and both signs of the active power P_A. The battery current i_D is close to a DC current. Fig. 7 shows that the mechanical size of the DC-side inductor L1 is smaller than that of the AC-side inductor L2, when S1-S6 are operated with the same switching frequency.
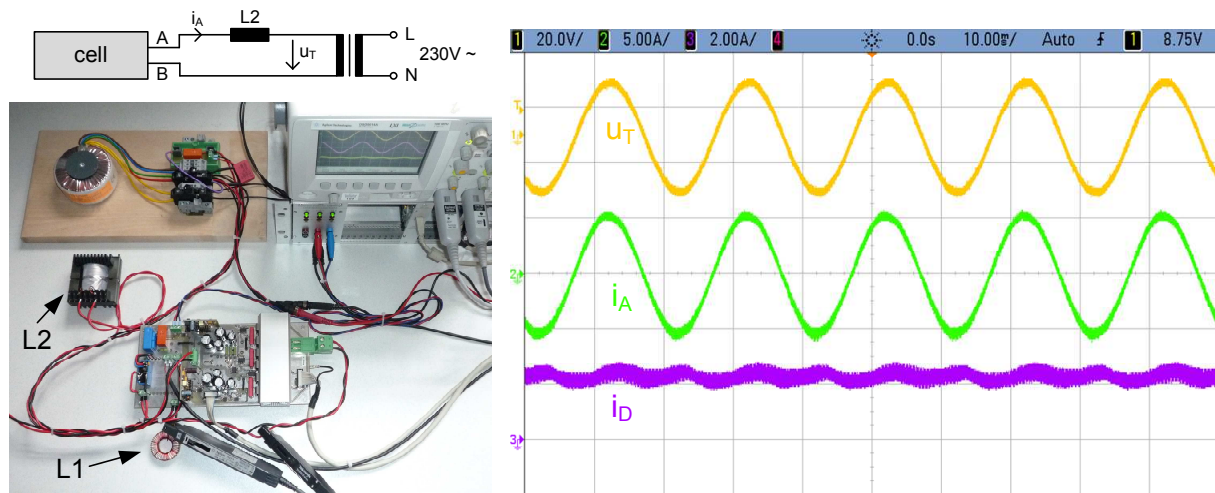
Figure 7: Experimental setup; measured voltage and currents
$U_{Teff} = 12V$; $f_A = 50Hz$; $U_d = 26V$; $U_{C1} = 4,4V$; $U_{C2} = 24V$; $C1 = C2 = 4000\mu F$; $L1 = 330\mu H$; $L2 = 2,2mH$; $f_{S(1-6)} = 8kHz$

4 Conclusion

A novel DC-AC converter circuit for battery usage is introduced (fig. 1a) and analyzed. It is especially designed for multilevel application, but can also be operated in single-cell configuration. The RMS value of the battery current and therefore the losses at the internal battery resistance are reduced, compared to the cascaded H-bridge (fig. 2a). Semiconductor losses, inductor volume and inductor costs are significantly reduced, compared to the cascaded H-bridge with conventional DC-DC converter (fig. 2b).

An appropriate control strategy for the novel circuit with usage of a natural balancing process is presented. The circuit has been simulated, built and successfully tested in single-cell configuration.

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