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Analyzing a Gate-Boosting Circuit for Fast Switching

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***Abstract*—A challenge in fast switching of voltage-controlled power semiconductor devices such as MOSFETs and IGBTs is fast charging of the gate capacitance. As gate drive circuit and device leads both involve stray inductance, the rise rate of the gate current is limited. To achieve higher current rise rates, an overvoltage might be applied to the gate leads (so called gate-boosting) [1]. In this work, a simple gate-boosting circuit has been investigated. It allows using a gate drive voltage in the order of 80 V whereas the voltage across the internal gate capacitance is kept well below the limit for the gate-emitter voltage as given in the datasheet. Hence, damage to the gate oxide layer is prevented. For the design process, it is of advantage to verify the voltage directly across the internal gate capacitance by measurements. For such measurements, the protective plastic housing of a TO-247 package around the die has been partly removed by means of an etching process. With a probe specifically modified for low inductance, measurements of the voltage across the gate capacitance in direct vicinity to the die have been performed. This work presents steps towards achieving a fast rising voltage across the gate capacitance within permissible limits, whereas the voltage across the device leads outside of the housing exhibits high inductive peaks. As result, improvements of the load current's rise rate in hard switching conditions by a factor of around 8 up to 4.2 kA/µs at a rise time of 50 ns for a commercially available Si IGBT have been demonstrated. For a SiC MOSFET a 3-fold increase of current rise time up to 2.6 kA/µs at 20 ns rise time has been achieved.**

Keywords— Pulse power generation, Fast switching, SiC MOSFET, Insulated Gate Bipolar Transistor, Gate boosting.

I. INTRODUCTION

For voltage-controlled power semiconductor devices such as MOSFETs or IGBTs, the charging speed of the gate capacitance is a key merit for a fast transition from off- to on-state. Since stray inductance in the gate drive circuit cannot be completely avoided, the application of higher voltages to the device leads is being used to achieve a high gate current rise rate. The gate drive circuit investigated in this work features a very simple implementation without additional active elements and allows for the use of drive voltages up to 80 V while maintaining a maximum of 15 V across the internal gate capacitance. This work discusses the circuit, its adaptation to new devices, correct gate voltage measurement techniques and presents results for Si IGBTs and SiC MOSFETs.

II. FAST GATE CHARGING

A. Limitations due to stray inductance

Besides stray inductance in the gate drive circuit, device leads and bond wires introduce additional parasitic inductance into the gate drive circuit [2]. The so-formed second order low-pass filter comprised of the parasitic inductance and the gate capacitance hinders fast gate charging. This issue has been addressed by various researches in terms of using a higher gate drive voltage either in form of a capacitor being discharged into the gate or by using different voltage levels during transient turn-on and steady-state [3], [4]. Another approach to foster a fast gate current rise time is the employment of current source gate drive circuits [5]. All the before mentioned circuits work well, however, they introduce additional active elements into the circuit and thus increase the complexity. The gate boosting circuit analyzed in this work does not include additional active elements (besides the drive voltage source) and allows for a precise control of the switching moment.

B. Gate-boosting circuit under investigation

The gate-boosting circuit investigated in this work is shown in fig. 1. It consists of a MOSFET driver (M1, M2) to switch the gate drive voltage V_{GD} of up to 80 V via damping resistors (R1, R2, R3) onto the capacitive divider comprised of the coupling capacitor C_C and the internal IGBT gate capacitance C_G. The combination of C_C and C_G is chosen such, that 15 V across the internal gate capacitance are achieved for the respective gate drive voltage. In the picture, IGBT T is considered to be an ideal switch, with its internal components such as lead stray inductance L_P and gate capacitance C_G drawn as discrete components. In steady on-state a gate voltage of 15 V is achieved by the combination of D1, R4 and R5 which compensate possible charge loss via parasitic leakage resistors. The gate voltage settles to 0 V in steady off-state by means of diode D2.

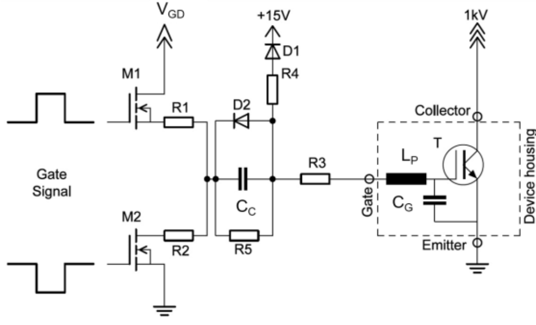

Fig. 1. The gate-boosting circuit under investigation with internal IGBT components drawn as discrete elements.

C. Equivalent circuit and adaptation procedure

For analysis, the gate drive circuit can be represented by the equivalent circuit shown in fig. 2 with damping resistors R_D.

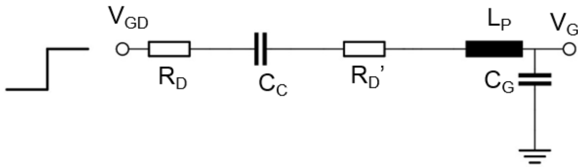

Fig. 2. Equivalent circuit of the gate-boosting circuit under investigation.

The transfer function of the equivalent circuit is hence:

$$\frac{V_G}{V_{GD}} = G(s) = \frac{\frac{1}{C_G \cdot s}}{R_D + \frac{1}{C_C \cdot s} + R_D' + L_P \cdot s + \frac{1}{C_G \cdot s}} \tag{1}$$

After using the series capacitance of C_C and C_G

$$C = \left(\frac{1}{C_C} + \frac{1}{C_G}\right)^{-1} \tag{2}$$

and the sum of the damping resistors

$$R = R_D + R_D' \tag{3}$$

eq. (1) can be simplified to

$$G(s) = \frac{C}{C_G} \cdot \frac{1}{L_P \cdot C \cdot s^2 + R \cdot C \cdot s + 1} \tag{4}$$

the characteristic equation of eq. (4) equals

$$L_P \cdot C \cdot s^2 + R \cdot C \cdot s + 1 = 0, \tag{5}$$

which is similar to that of a simple RLC circuit with natural frequency $\omega = 1/\sqrt{L_P \cdot C}$. When increasing the drive voltage V_{GD}, the coupling capacitor C_C needs to be lowered in order to achieve the same gate voltage V_G. According to eq. (2), this lowers the equivalent capacitance of the whole circuit and thereby increases the natural frequency and, hence, the charging speed of the gate capacitance. Fig. 3 shows the voltage across the gate capacitance according to eq. (1) after transformation into time domain (R_D=4Ω, L_p=25nH, C_G=18nF). As can be seen, a high gate drive voltage significantly shortens the gate charging process. In order to achieve best performance for the intended application, the circuit needs to

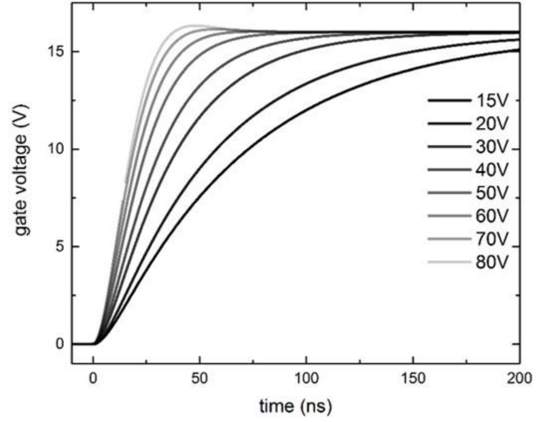

Fig. 3. The increase in gate charging speed for increasing gate drive voltage.

be tailored to the application. For maximum charging speed, a high gate drive voltage is desirable. The maximum gate drive voltage is only limited by practical considerations, as the driving MOSFET half bridge needs to have a rise time significantly shorter than the desired rise time of the gate voltage. The minimum damping required in the circuit depends on the circuit layout (parasitic inductance) as well as on the employed MOSFET switches (parasitic capacitance). If the circuit is designed to operate in slightly underdamped conditions, a further increase in charging speed is achievable. The maximum permissible voltage overshoot hereby depends on the device specifications. A high gate drive voltage leads to the final gate voltage being sensitive to the exact value of the gate capacitance. Fig. 4 shows the final gate voltage as function of the gate capacitance. For high gate drive voltages, there is a significant variation. This variation in gate voltage may cause a slightly different switching behavior for devices with different gate capacitances. Hence, if many devices are operated at the same time and identical switching behavior is desired, the maximum gate drive voltage may be limited by the expected variations of the respective gate capacitances.

For reliable circuit design, hence, exact knowledge of the stray parameters is important.

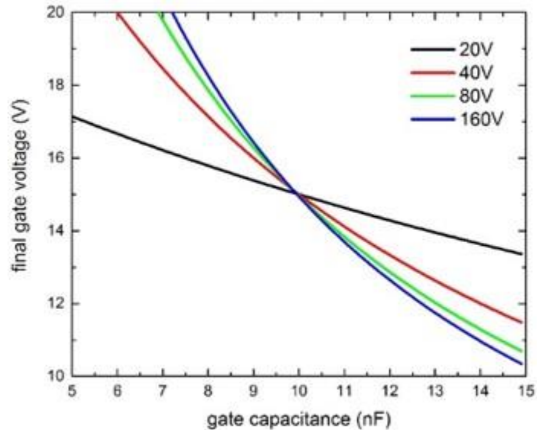

Fig. 4. Dependence of the final gate voltage on the gate capacitance for different gate drive voltages.

III. Determination of Stray Parameters

A. Challenges related to gate voltage measurements

When measuring the gate voltage across the external device leads as indicated in fig. 1, the measurement always includes the voltage drop across the internal parasitic inductance. The measured signal shows, as can be seen in fig. 5, voltage spikes that make the determination of stray parameters challenging.

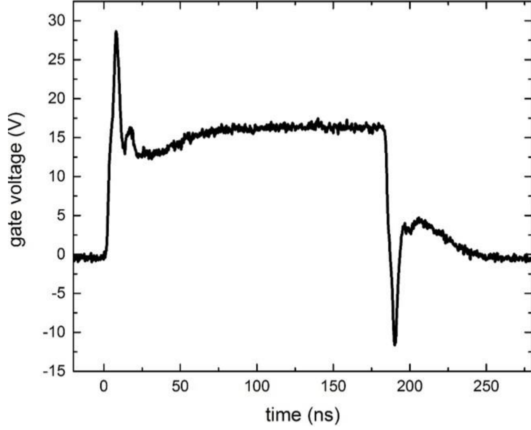

Fig. 5. Signal as measured across the external device pins, showing high peaks.

B. Opening of the package

For accurate determination of the stray parameters, the measurement of the voltage across the internal gate capacitance is of advantage. To this end, we used fuming nitric acid (>90 %) at elevated temperature (above 90 °C) to dissolve the protective epoxy housing around the IGBT die [6]. Using this process, measurements on the bond wires and at the internal gate capacitance become feasible. Due to the passivizing properties of the highly concentrated nitric acid, the device remains functional up to blocking voltages in the order of 600 V. Above this voltage, surface flashovers may occur, destroying the device. The presented measurements have been performed with a low inductance high voltage probe in order to minimize the inductive signal pickup caused by the fast varying signals.

C. Measurements at the die

To illustrate the influence of the stray inductance of the bond wires, fig. 6 shows voltage measurements along the gate bond wire with respect to the grounded emitter pin (position marked by black dot). As can be seen, the voltage spikes are continuously reduced when moving the probe along the bond wire towards the gate contact (Position 1 to 3).

By measuring the voltage across the internal gate capacitance accurately, the internal stray parameters can be determined by the comparision of measurement and simulations of a circuit according to fig. 2. Thereby, the damping conditions can be chosen as required by the application. Fig. 7 shows voltage measurements across the internal gate capacitance (gate contact – emitter contact at the die) for underdamped and critically damped conditions.

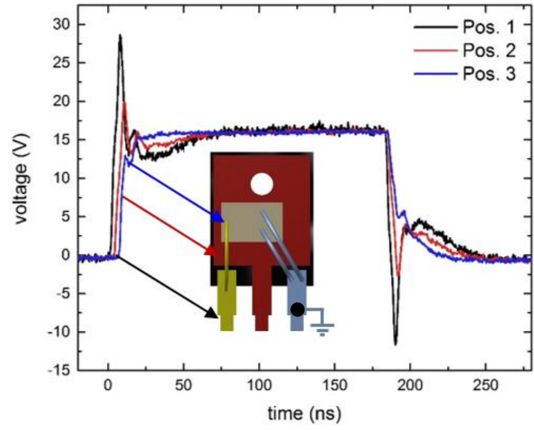

Fig. 6. Voltage measurements when measuring on the opened IGBT along the gate bond wire (black: outside of the housing, red: middle of the gate bond wire, blue: gate contact) with respect to the position marked by the black dot. The decrease of the voltage spikes at the beginning and the end of the pulse when moving towards the gate contact illustrate the influence of the parasitic gate bond wire inductance.

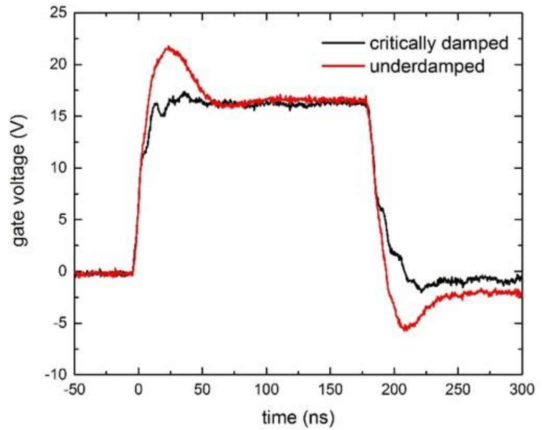

Fig. 7. Voltage measurements directly on the internal gate capacitance for underdamped and critically damped conditions.

IV. Increase in Switching Speed

The investigated circuit is able to speed up the switching speed of voltage controlled semiconductors such as MOSFETs and IGBTs. Exemplary, the circuit has been adapted for the SiC MOSFET C2M0080120D [7] and the Si IGBT NGTB40N120IHLWG [8], both in TO-247 packages. The devices were operated under hard switching conditions (load circuit inductance < 60 nH) at 1 kV blocking voltage. The load current was set to 80 % maximum rated pulsed current in single pulse mode for each device. The complete test environment has been described in [1].

Fig. 8 shows the collector current of the IGBT NGTB40N120IHLWG for a pulse with varying gate drive voltage. The 15 V trace represents the standard gate drive with the coupling capacitor shorted. The strong increase in current rise time is in good agreement with increase in gate charging speed.

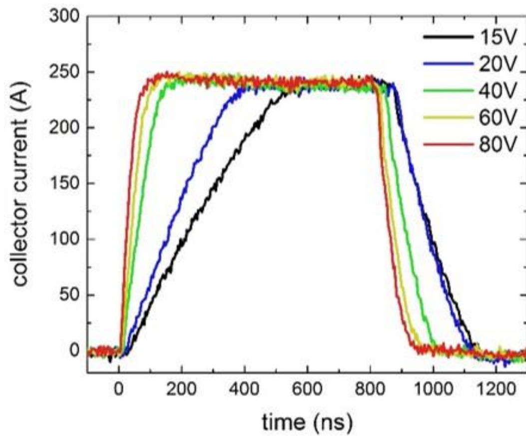

Fig. 8. Collector current measurements for the IGBT NGTB40N120IHLWG under hard switching conditions for increasing gate drive voltage.

As for the Si IGBT, also the current rise time of the SiC MOSFET can be increased by operating the device at high gate drive voltages. Fig. 9 shows the drain current (80 % maximum pulsed current) for increasing gate drive voltage. Here, the 20 V trace represents the standard gate drive conditions as recommended in the datasheet.

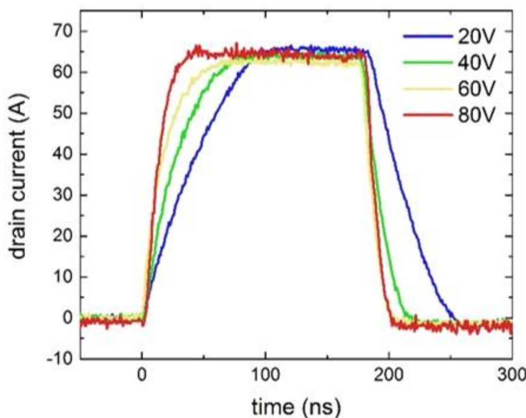

Fig. 9. Drain current measurements for the SiC MOSFET C2M0080120D under hard switching conditions for increasing gate drive voltage.

Fig. 10 shows the current rise times for both the SiC MOSFET and the Si IGBT. As can be seen, the current rise time (measured at 10 % to 90 %) decreases nearly exponentially with rising gate drive voltage in case of the IGBT, whereas the decrease of current rise time is slightly less pronounced in case of the SiC MOSFET. However, the switching time of the SiC MOSFET can be reduced from 71 ns (under standard gate drive conditions) down to 20 ns (at 80 V V_{GD}), which corresponds to an increase in current rise rate from 0.7 kA/µs to 2.6 kA/µs. For the Si IGBT, the switching time was reduced from 402 ns (under standard gate drive conditions) to 49 ns (at 80 V V_{GD}). With respect to current rise rates, this results in an eight-fold increase in current rise rate from 0.5 kA/µs to 4.2 kA/µs.

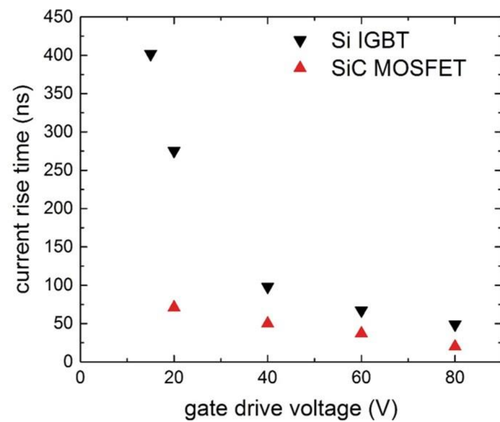

Fig. 10. Comparision of the current rise time dependence on the gate drive voltage for the Si IGBT and the SiC MOSFET. For the Si IGBT, an increase in switching speed from 402 ns (standard gate drive) to 49 ns (80 V V_{GD}) as been achieved as compared to 71 ns to 20 ns for the SiC MOSFET.

V. Conclusion

The simple gate-boosting circuit presented in this work allows for employing comparably high gate drive voltages of up to 80 V for overcoming the limiting influence of stray inductances in the gate terminal leads on the switching speed. Precise adaptation of the circuit to a new device based on a gate voltage measurement directly at the die has been successfully demonstrated. As result a standard IGBT showed a considerable improvement in switching time from 400 ns down to 49 ns, whereas the current rise time of a SiC MOSFET was decreased from 71 ns to 20 ns.

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