A SINGLE-PHASE MULTI-LEVEL D-STATCOM INVERTER USING MODULAR MULTI-LEVEL CONVERTER (MMC) TOPOLOGY FOR RENEWBLE ENERGY SOURCES

by

PEDRAM SOTOODEH

M.S., Sharif University of Technology, 2010

AN ABSTRACT OF A DISSERTATION

submitted in partial fulfillment of the requirements for the degree

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Abstract

This dissertation presents the design of a novel multi-level inverter with FACTS capability for small to mid-size (10–20kW) permanent-magnet wind installations using modular multi-level converter (MMC) topology. The aim of the work is to design a new type of inverter with D-STATCOM option to provide utilities with more control on active and reactive power transfer of distribution lines. The inverter is placed between the renewable energy source, specifically a wind turbine, and the distribution grid in order to fix the power factor of the grid at a target value, regardless of wind speed, by regulating active and reactive power required by the grid. The inverter is capable of controlling active and reactive power by controlling the phase angle and modulation index, respectively. The unique contribution of the proposed work is to combine the two concepts of inverter and D-STATCOM using a novel voltage source converter (VSC) multi-level topology in a single unit without additional cost. Simulations of the proposed inverter, with 5 and 11 levels, have been conducted in MATLAB/Simulink for two systems including 20 kW/kVAR and 250 W/VAR. To validate the simulation results, a scaled version (250 kW/kVAR) of the proposed inverter with 5 and 11 levels has been built and tested in the laboratory. Experimental results show that the reduced-scale 5- and 11-level inverter is able to fix PF of the grid as well as being compatible with IEEE standards. Furthermore, total cost of the prototype models, which is one of the major objectives of this research, is comparable with market prices.

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Major Professor
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Thank you!

Dedication

I would like to dedicate this dissertation to the love of my life, Farinaz. She was really supportive through all steps of my PhD. She was the only one that could make me calm and happy when I was disappointed and tired of spending long hours in lab. I am sure I could not have done this dissertation without her help. She has unbelievably put a lot of effort on our marriage over the last three years.

Thank you, Farinaz!

Glossary of Acronyms

5L-HNPC-Five Level Hybrid Neutral Point Clamped

3L-ANPC-Three Level Active Neutral Point Clamped

5L-ANPC-Five Level Active Neutral Point Clamped

AWEA-American Wind Energy Association

CHB-Cascaded H-Bridge

D-STATCOM- Distribution Static Synchronous Compensator

FACTS-Flexible AC Transmission Systems

FC-Flying Capacitor

FFT-Fast Fourier Transform

HVDC-High Voltage DC

IGBT-Insulated Gate Bipolar Transistor

IGCT-Integrated Gate-Commutated Thyristor

MMC-Modular Multilevel Converter

MPPT-Maximum Power Point Tracker

NPC-Neutral Point Clamped Inverter

NREL-National Renewable Energy Laboratory

OHSW-Optimized Harmonic Stepped Waveform

PCC- Point of Common Coupling

PV-Photovoltaics

SHEM-Selective Harmonic Elimination Modulation

SMC-Stacked Multi-cell Converter

SPWM-Sinusoidal Pulse Width Modulation

SSSC- Static Series Synchronous Compensators

STATCOM- Static Synchronous Compensator

SVC-Static VAR Compensator

SVM-Space Vector Modulation

TCSC-Thyristor Controlled Series Capacitor

THD-Total Harmonic Distortion

VSC-Voltage Source Converter

Chapter 1 - Introduction

1.1 The Electric Power Grid

Traditionally, large power plants use fossil fuels to generate electricity. Each power grid consists of three major parts: generation, transmission, distribution. Electric energy is generated by large generators, transmitted to load sites by transmission system, and then distributed among loads (customers) by the distribution systems. The generation of electric energy typically is performed in large power plants which are located outside of cities. Generated power is then transferred to loads through long transmission lines. These power lines have many loops (to increase reliability) and carry large amounts of power to the distribution systems. Distribution systems consist of smaller lines that carry smaller amounts of power from distribution stations to the loads, ranging from small residential customers to large industrial factories. These systems usually take advantage of radial structures and act as the interconnection point between transmission systems and customers.

Recently, renewable energy systems have become more prominent in electricity production. Renewable energy sources, such as wind or solar energy, have been playing an important role in energy production. Figure 1.1 illustrates a modern power grid in which electricity is made by conventional power plants and renewable energy power sources.

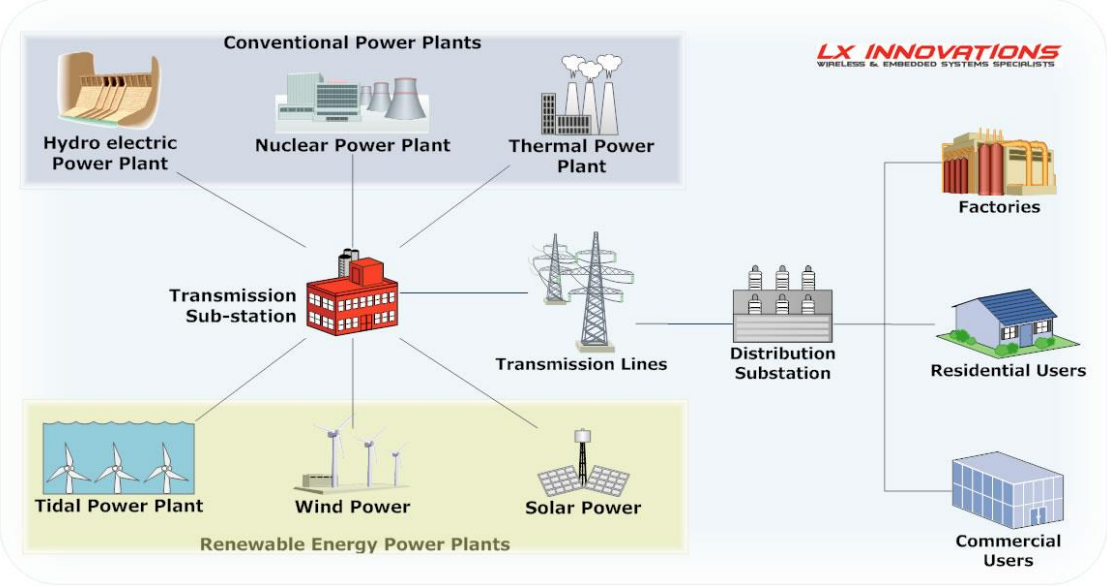


Figure 1.1 The modern electric power grid [1]

1.2 Introduction to Renewable Energy Systems

The electric utility industry has begun to update more and more in recent years. Relevant issues such as global warming, toxic emissions, energy cost, power market, and increasing energy demand have affected power industry growth. Over the past decade, utilities have shown decreased willingness to invest in large-scale power plants and, consequently, have shifted to smaller distributed energy sources closer to loads [2]. In addition, power facility upgrades are essential in order to make a profit in the competitive power market. Thus, renewable energy sources such as wind, solar, biomass, and geothermal are attractive alternatives for power utilities.

A majority of regions in the United States have the potential to use one or more types of renewable energy. Renewable energy sources originate from a wide variety of sources such as wind, sunlight, or internal heat from the earth. Each renewable energy source is in a unique stage of development. For example, in December 2011, total installed wind power in the United States was 46,919 MW [2]-[2], while total photovoltaic (PV) peak power capacity was 4500 MW.

Renewable energy has grown significantly since the past decade. Between 2000 and 2009, the installed capacity of renewable energy sources tripled [3]. In 2009, 12% of total installed capacity and more than 10% of total energy generation in the United States was provided by renewables, including hydropower. In 2011, total energy consumption of renewable energy sources was 9 quadrillion ($9 * 10^{15}$) Btu, approximately 9% of total energy consumed in the United States, or 13% of electricity produced nationally. Renewable energy systems are abundant, but most are modular and not distributed uniformly. For instance, while 34 of 50 states in the US have good capacities of wind sources, wind capacity of North Dakota is as much as 36% of total electricity consumption of the lower 48 states [5].

Renewable energy systems offer several advantages over conventional energy sources such as natural gas or coal. First, renewable energy systems are clean sources of energy found in most regions, and they emit no greenhouse gases. Renewable energy sources are also abundant, free, and generally not affected by political instability. Although the initial capital cost for most renewable energy sources is greater than conventional natural gas or coal power plants, renewables may be more cost-effective long term as compared to conventional sources because of lower operating and maintenance costs.

However, renewable sources also have several disadvantages, including a primary disadvantage that they are commonly located in remote areas at great distances from large loads. In addition, renewable energy source use is restricted by limited availability.

Recently, energy consumption has increased significantly. Estimates project that energy consumption will increase 44% worldwide by 2030 [6]. The need for cleaner, greener energy has led to improvements in the capture of renewable energies to produce power. Traditionally, most energy is produced and transmitted through power lines to the loads, meaning great loss as well as cost for operation and maintenance. Conversely, the theory that the end customer need not be a passive load but an active supplier of energy, has produced the method of using distributed generation (DG) to the power system. In this case, renewable energy sources, such as wind and solar energy, can be locally connected to the grid. Renewable energy sources cannot support the entire power demand, but they can be added to main grids to help feed the loads.

1.3 Power Electronics and Its Application in Renewable Energy Systems

The first power conversion device was developed in 1864 by Dr. Antonio Pacinotti. Pacinotti invented the first dynamo able to convert mechanical power to electrical power. His machine was directly connected to a power source without any additional control system. Since Pacinotti, various control systems have been developed, including the invention of power electronics. A power electronic device consists of several semiconductor components used to perform specific functions in a system. A power electronic system has several main sub-systems, such as control, protection, and cooling systems. Nowadays, power electronics is a crucial tool for controlling power conversion. The use of power electronic devices has many advantages, but the most important benefit is the capability to control and manage the flow of electrical power. The use of power electronics allows AC or DC sources to connect to each other with different voltage or frequency levels. Power electronics application is expanding in all aspects of power. All active filters, static VAR compensators (SVCs), motor drives, battery storage systems, switching power supplies, inverters and converters use power electronics. Power electronic technology has significantly improved during the recent decade, and the capacity of various switching components has also increased. Recent achievements in semiconductor technology have resulted in the production of large-capacity power electronic elements.

The rapid development of power electronics as well as increasing energy demand has increased power electronics usage in renewable energy systems. In addition, DG application in power systems has led to increased use of power electronics to regulate renewable energy sources tied to main grids. Figure 1.2 shows the configuration of power electronics for wind energy sources.

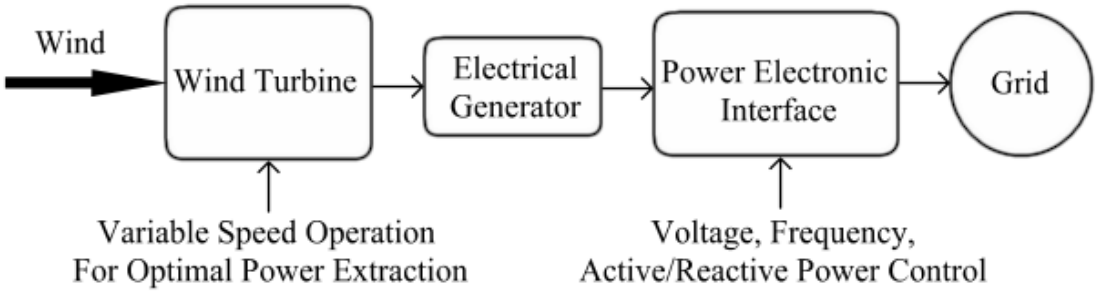


Figure 1.2 Application of power electronics in wind energy systems

1.3.1 Wind Energy

Wind energy generation began in the 1980s when wind turbines with only a few tens of kW rating were connected to power grids without much control. Due to variations of wind speed, generated power was associated with pulsations applied directly to the grid. Furthermore, this system had no control on active and reactive power transfer. Today, great improvements in wind energy generation necessitate the use of power electronics in order to control active and reactive power transfer between wind turbines and main grids.

With the exception of hydro, wind energy currently has the greatest share in renewable energy sources. The capacity of wind has more than doubled during the last two decades and the cost has decreased by one-sixth [5]. Rapid progress in wind technology has reduced wind energy cost to such an extent that it is competitive with conventional energy. Most commercial wind systems include a horizontal-axis wind turbine, and a generator connected to the grid using power electronic converters. Generally, wind generation systems utilizing permanent magnet (PM) generators possess a rectifier associated with a maximum power point tracker (MPPT) and an inverter. Figure 1.3 provides the configuration of a PM-based wind system.

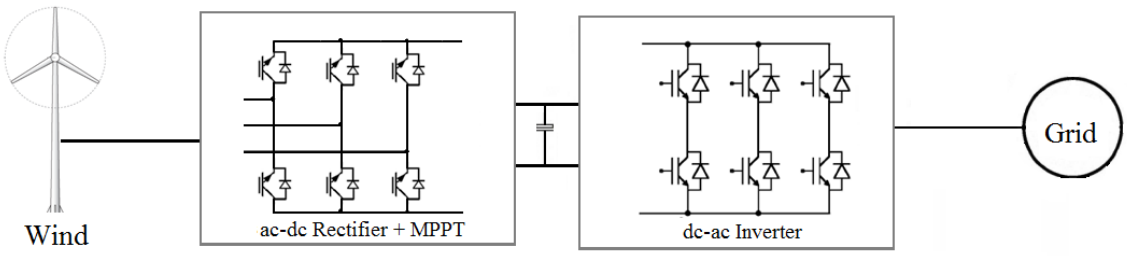


Figure 1.3 Configuration of a PM-based wind system

1.3.2 Photovoltaic (PV) Energy

Among utility-connected DG sources, photovoltaic (PV) energy ranks second only after wind energy. PV devices use semiconductors to produce energy from sunlight and they are extremely modular which allows them to be placed in small cells and panels. A PV panel consists of a series of solar cells [6], and a complete PV system includes several PV panels connected in series or parallel to increase total power. Recent progress in semiconductor technologies has significantly developed PV systems since they were first used in the early 1980s. As a result, the cost of solar-generated electricity has continuously decreased over the past years.

A common configuration for PV systems is shown in Figure 1.4. The PV power electronic system is used to convert DC energy to AC energy. PV arrays resemble variable current sources, and MPPT output is fairly constant. At the first stage, a DC-DC boost stage is used to raise the voltage level to the desired value for DC-Link. The produced DC power is then connected to the grid through an inverter and a low-pass filter.

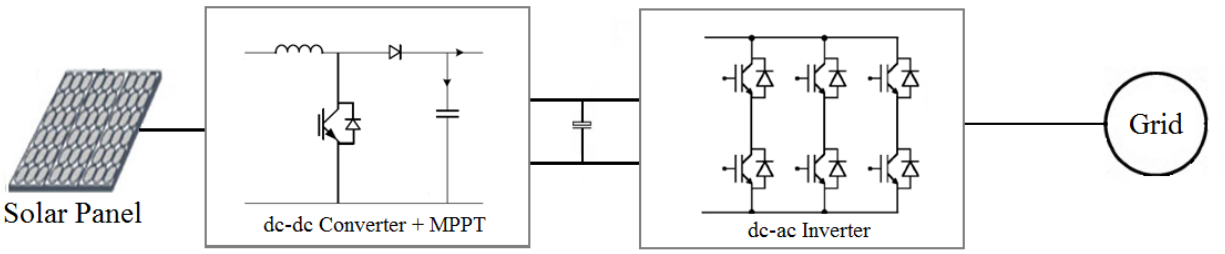


Figure 1.4 Configuration of a PV system

1.4 Power Electronics in Distribution Systems

Distributed generation has recently been introduced to modern power systems to avoid generating and transmitting power over a long distance. Relatively small power generators, such

as small wind or solar energy systems, are an approach to spread renewables throughout the power systems. Small renewable energy sources are connected to the low side of distribution systems, or in other words, end customers act not only as consumers in modern power systems, but also as active power suppliers to generate electric power. Deployment of small renewable energy sources in distribution systems results in paying more attention to power quality issues at the end point, specifically when the amount of installed renewable energy becomes significant compared to the total power of the system. Among all power quality concerns, control of active and reactive power transferred to or from the power grid requires major attention. This attention currently is possible through the use of power electronic circuits.

Power electronic-based flexible AC transmission systems (FACTS) have been developed in order to enhance control of active and reactive power transfer on feeder lines. FACTS components have been found to be the most efficient and economical method to control power transfer in interconnected AC transmission systems. FACTS systems include a wide range of power electronic devices used in power systems to ensure secure power transmission in AC systems [7],[8]. One of the most well-known FACTS device is the static synchronous compensator (STATCOM), also known as static synchronous condenser (STATCON). Conceptually, a STATCOM is a power electronic device based on a voltage source converter (VSC). The STATCOM is able to connect in parallel with a power system and act as a source, or sink, of reactive power in order to enhance power quality of the systems. It can also provide active power if connected to a source of power such as a renewable energy source.

Traditionally, capacitor banks have been used to control the reactive power on a power grid, but because of the development of power electronics, STATCOMs were created and have consequently received prominent attention. The theory governing a STATCOM includes the connection of a small source of energy, such as one or a group of several capacitors, to the AC system. If the STATCOM is applied on a distribution system, it is called distribution STATCOM (D-STATCOM). The application of D-STATCOM is very similar to a regular STATCOM. STATCOMs are typically utilized on the high-voltage side of the distribution systems because of their high cost. Deploying STATCOMs at the consumer level is not economically feasible. The aim of this work is to combine the two concepts of inverter and D-STATCOM in a single unit in order to enjoy the benefits of an inverter with D-STATCOM capability with no additional cost.

The inverter with FACTS (D-STATCOM) capability is a power electronic device that is placed between the renewable energy source and the distribution grid (identical to a regular inverter) not only to provide active power, but to control reactive power transfer on the system as well. The proposed inverter in this work could replace existing inverters used for renewable energy systems, specifically in regards to small- to mid-size wind applications. In other words, the proposed inverter is a cost-effective inverter equipped with D-STATCOM capability to control the power factor (PF) of the feeder lines by regulating active and reactive power transferred between the wind turbine and the distribution grid. Deployment of the proposed inverter can provide utilities with more information and control, specifically at end points that utilities do not monitor adequately, with no additional cost.

1.5 Research Motivation

Tremendous growth has occurred in the integration of distributed energy systems to power systems utilizing FACTS technology. A majority of FACTS applications for renewable energy sources have been introduced over the past decade. A complete list of literature explaining FACTS application in renewable energy systems is given in [9], but no literature has combined all the concepts considered for the current research.

The unique contribution of the current work is the combination of an inverter and a D-STATCOM for renewable energy sources in single-phase systems, using a new multi-level topology. Several key factors are considered throughout all stages of the work: 1) cost-effectiveness, 2) efficiency, and 3) compatibility with IEEE standards. In this research, a new single-phase inverter with D-STATCOM capability, using a new multi-level topology called modular multi-level converter (MMC), is introduced. The proposed inverter is designed for grid-connected wind turbines in the small- to mid-sized (10kW-20kW) range. This new inverter regulates DC link voltage as well as active and reactive power injected to the grid through the distribution transformer in order to set the grid PF at a target value established by the user (utility). The proposed system provides high dynamic performance and power quality for power transmitted between the renewable energy source and the distribution grid. The 5- and 11-level inverter is simulated in MATLAB/Simulink environment to demonstrate the performance of the proposed MMC inverter. To validate the simulation results, a reduced scale experimental

configuration of the 5- and 11-level inverter was built and tested in the laboratory. The following sections describe key terms of the current research.

1.5.1 Single-Phase System

Industry standards categorize the power applications as: 1) small-size, for power rating lower than 50 kW, 2) mid-size, for power rating between 50 kW and 500 kW, and 3) large-size (utility-scale) for power rating more than 1 MW. The focus of this research is mostly on small-sized wind power applications which usually take benefit of single-phase systems.

With the exception of hydro, the two major shares of renewable energies currently are wind and solar. Although grid integration basics for wind and solar are similar, this specific research focuses on wind application. Recently, large-scale wind applications have attracted more attention than small wind applications. However, two primary advantages exist for small wind projects utilizing single-phase power systems: 1) ease of installation and ability to finance, and 2) involvement of many small businesses and farms utilizing single-phase power lines.

The beginning of small wind applications dates back to about 100 years ago. In the 1920s and 1930s, farm families in the United States began to use wind energy to produce electricity for lights and motors. Although producing energy from wind was not supported by the government at that time, the energy crisis in the 1970s and the need for green and environmentally responsible sources of energy re-introduced the use of renewable energy. Currently, farm and home owners in remote locations use wind to produce needed energy [10]. Small wind applications help farmers and rural homeowners avoid the high cost of power lines extended to their locations. When considering high initial costs of wind projects, these sources are competitive with conventional energy sources because of lower lifetime costs. A small wind-turbine using single-phase power lines can be a suitable long-term investment for private properties that have wind generation capabilities. Figure 1.5 shows additional and cumulative capacity for small wind turbines at the end of 2011 [11].

In general, because a large amount of single-phase distribution systems currently exist in the United States, especially in rural regions, the use of small wind applications are more reasonable.

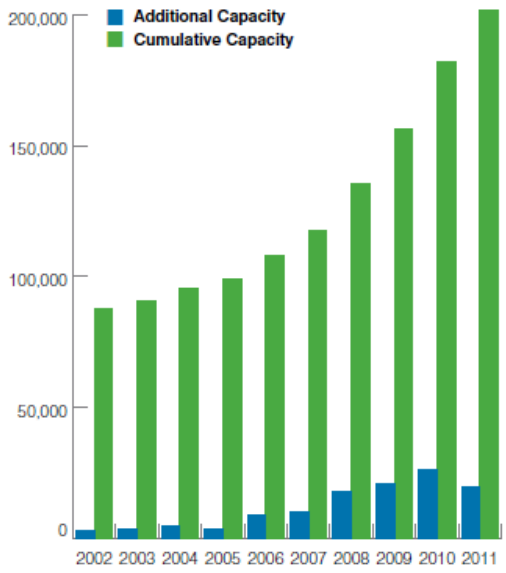


Figure 1.5 New and cumulative capacity for small wind turbines at the end of 2011 [11]

1.5.2 Multi-Level Topology

Numerous industrial applications require medium to high power capability. Some medium-voltage motor drives or utility applications require medium voltage and megawatt power levels. For a medium- to high-voltage power application, rating limitations of power electronic components do not allow to connect only a single power semiconductor switch. Therefore, a multi-level converter can be a suitable alternative for these applications. Multi-level converters can also be a suitable choice for renewable energy systems. During the past three decades, several multi-level topologies have been developed [12],[13].

Modular multilevel converter (MMC) topology is a new multi-level topology that recently has gained much attention, specifically for mid- to high-voltage applications. Primary benefits of MMC topology include: modular design based on identical converter cells, simple voltage scaling by a series connection of cells, simple realization of redundancy, and the possibility of a common DC bus [14],[15],[16].

1.5.3 D-STATCOM Capability

For modern wind power applications, one of the primary goals is to increase use of wind energy inverters (WEIs) as FACTS devices in order to improve power quality. In other words, FACTS-like performance can be combined with wind energy inverters. In this research, the

proposed converter is capable of acting as an inverter as well as a D-STATCOM with no additional cost. The proposed inverter with FACTS capability can be regarded as an inverter unit and a D-STATCOM unit combined into a single unit. For normal situations, the power inverter is capable of controlling the PF of the grid regardless of wind speed. This inverter is located between the wind turbine and the distribution grid. The power inverter is separated from the wind turbine with a rectifier combined with a MPPT system and is connected to the grid through the distribution transformer. The complete configuration of the system is shown in Figure 1.6.

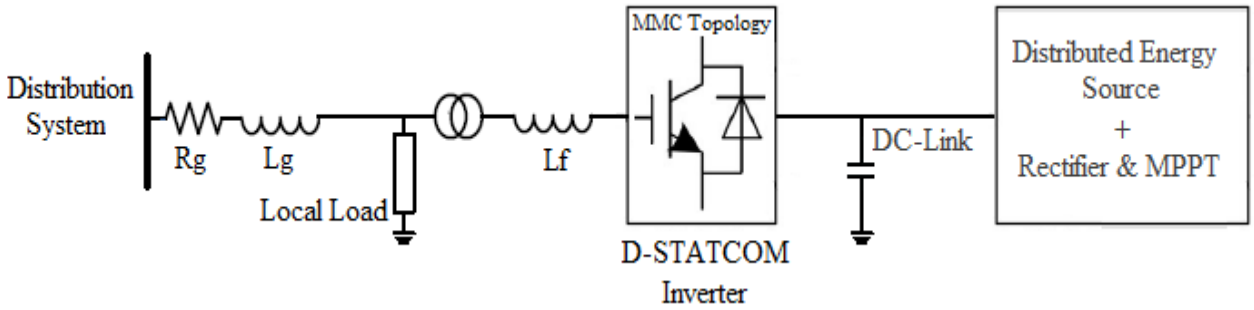


Figure 1.6 Complete configuration of the proposed inverter system

1.6 Dissertation Outline

In this research, design steps of the proposed inverter with FACTS capability are investigated. Various multi-level topologies, modulation schemes, and FACTS devices are explained in the following chapters. Design objectives and steps to implement the simulation and experimental configuration of the new inverter are also described in detail. At the end of the dissertation, conclusion will be presented and future work will be suggested.

Chapter 2 begins with introducing three fundamental multi-level inverter topologies, including diode-clamped (DC), flying-capacitor (FC), and cascaded h-bridge (CHB) topologies, followed by an explanation of newer multi-level topologies, such as 5-level h-bridge neutral point-clamped (5L-HNPC), 3-level active NPC (3L-ANPC), 5L-ANPC, hybrid-clamped (HC), and others. Chapter 2 also introduces MMC topology and compares all multi-level topologies. In addition, various modulation schemes used for multi-level inverters, including fundamental and high switching frequency techniques, are described.

In Chapter 3, FACTS devices and their history are presented. Several different FACTS devices, such as STATCOM, are introduced. Principals, operating modes, and benefits of STATCOM are then explained in detail.

Chapter 4 presents design objectives, topology, and control strategy used for the proposed inverter with FACTS capability. In this chapter, a controller system is described in detail. Active and reactive power control, voltage balancing, and PWM generation of the inverter is also fully explained. Section 4.5 provides detailed explanation regarding implementation of the proposed system in a Simulink environment.

Chapter 5 shows simulation results from the Simulink environment for the 5- and 11-level inverter. Section 5.2 describes results for the 5-level model, followed by results for the 11-level configuration. In this chapter, results of the two different systems (5- and 11-level) in similar order are extensively presented.

Chapter 6 provides the experimental setup used for the 5- and 11-level models. This chapter presents figures from the bench setup, implemented boards such as inverter and isolation board, and additional hardware used for the implements.

Chapter 7 states experimental results obtained from the 5- and 11-level implementation. This chapter explains test conditions and modes used for the two configurations.

In Chapter 8, the conclusion and future work are presented. This chapter provides a summary of the 5- and 11-level configurations and compares the two different systems from various aspects.

Appendix A and Appendix B provide the MATLAB-code used for the PWM generation block of the simulations and experiments of the 11-level inverter. Figure 1.7 illustrates the dissertation outline.

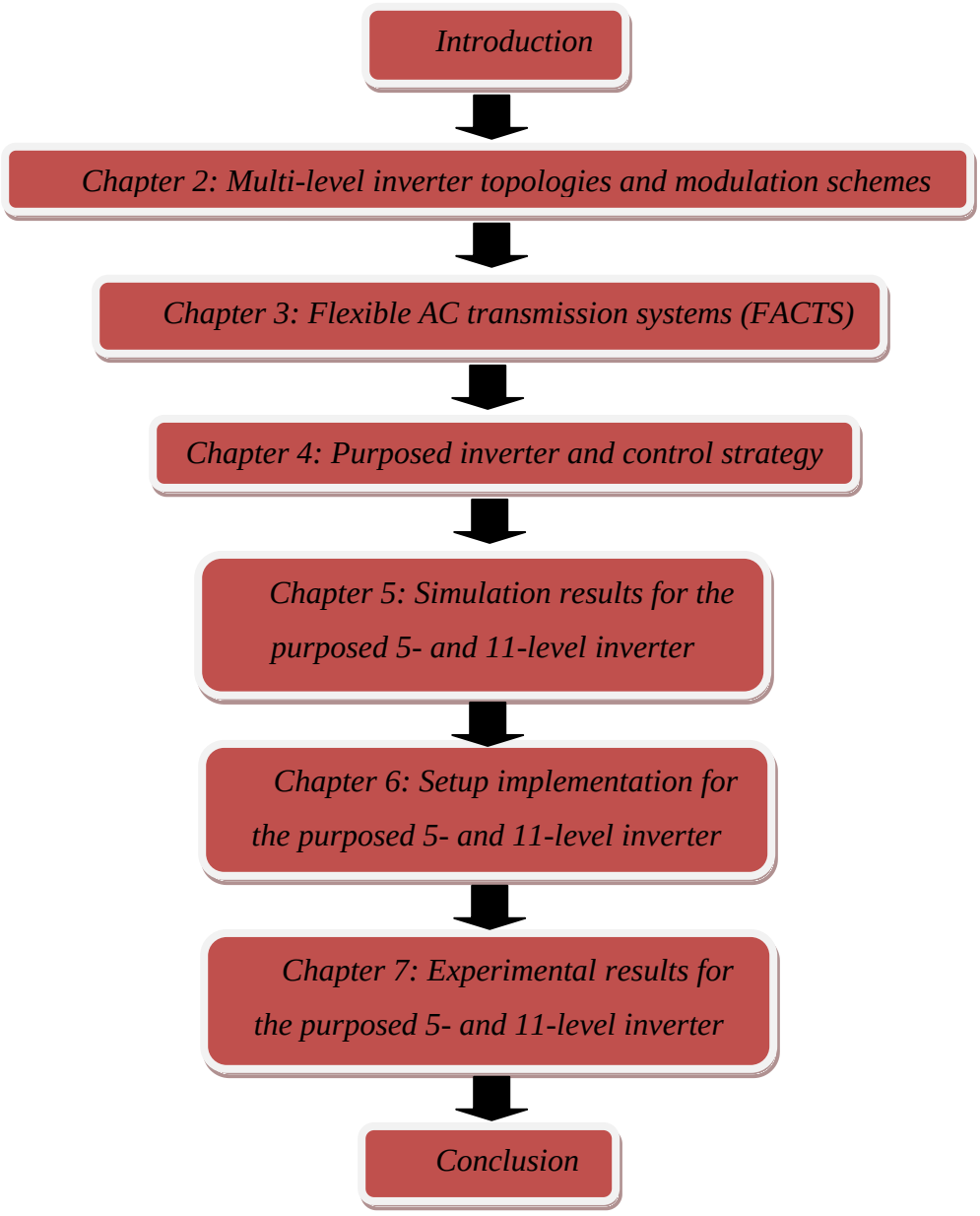


Figure 1.7 Organization of the contents

Chapter 2 - Multi-level Inverter Topologies and Modulation Schemes

2.1. History of Multi-level Inverters

Conventional two-level topology is the most common inverter topology and has been used for many years in industry. The term "two-level" is derived from the number of output voltage levels the inverter can generate. If the DC link voltage of a two-level inverter is assumed to be V_{dc}, its output voltage has the values $\{V_{dc}$ and $0\}$, or $\{+{}^{V_{dc}}/_{2}$ and $-{}^{V_{dc}}/_{2}\}$. This family of inverters typically takes advantage of simple structure and control strategy. A three-phase two-level inverter contains six semiconductor switches, thus requiring a modulation scheme depending on the inverter application. The primary disadvantage of two-level inverters is that they usually operate in higher switching frequencies, consequently increasing the total loss of the system. Moreover, the output waveform of a two-level inverter contains a large number of harmonics, resulting in the use of more expensive output filters.

Many industrial applications have recently begun to require more power or voltage. For higher voltage or power applications, connecting conventional inverters directly to the DC source may cause problems due to the voltage and current limits of semiconductor elements. Therefore, multi-level inverters have been introduced for medium- to high-voltage applications. At first multi-level inverters were used only for high voltage applications, but currently, multi-level inverters are used even in low voltage applications such as motor drives. A wide range of applications exist for multi-level inverters, such as electric vehicles (EVs), large motor drives, and renewable energy applications such as wind or solar applications [17],[18],[19].

The history of multi-level inverters dates back to the 1970s [20]. Multi-level inverters are based on the concept of using a number of small voltage levels to gain higher powers. Several advantages are possible for this structure. The switching frequency for multi-level inverters is lower, resulting in the production of less switching losses and consequently higher efficiency. Moreover, staircase output voltage possesses lower distortion and improves the total harmonic distortion (THD). As the output waveform contains less numbers of undesired harmonics, smaller output filters can be used to reduce the total cost of the system. In addition, the staircase waveform provides additional voltage steps between the highest and lowest voltage levels, thus

reducing voltage stress on semiconductor components and resulting in less $^{dv}/_{dt}$ on the switches which can also enhance electromagnetic compatibility (EMC). However, several disadvantages are present for multi-level inverters, which may restrict them to be used for lower power applications. The primary disadvantage of multi-level structures is the requirement of more components as compared to conventional two-level inverters. The structure of all multi-level topologies is based on the utilization of a number of switches in series to increase the power and voltage capability of the inverter. Although lower-ratings semiconductor components should be used for multi-level inverters, the total cost of the system may be increased.

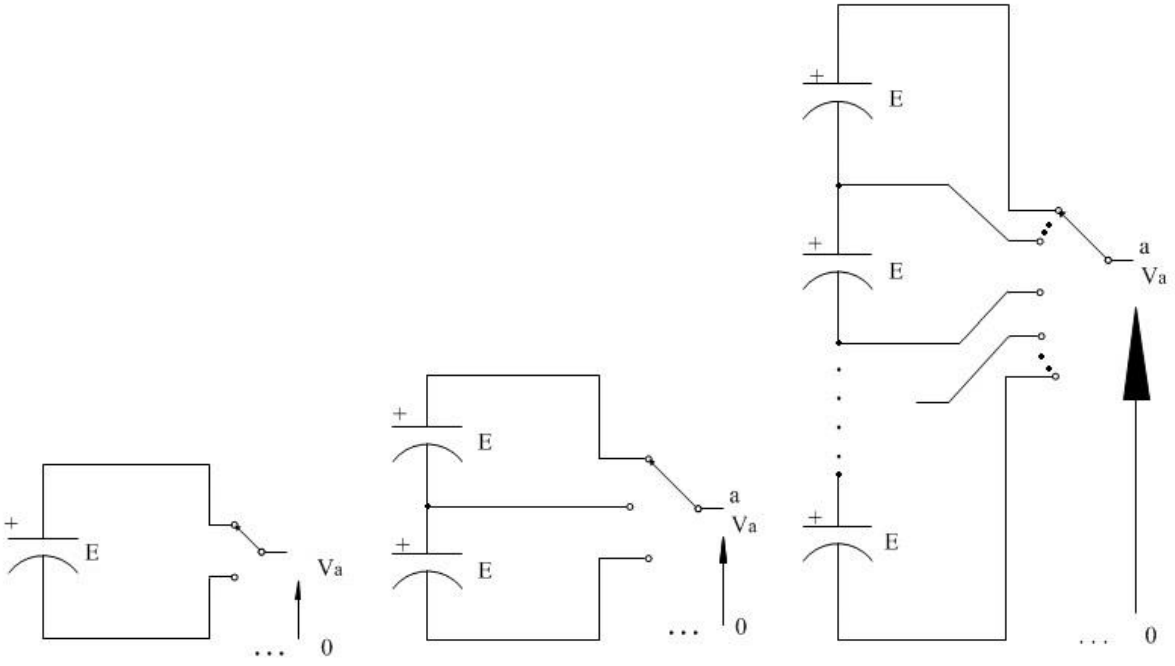
A large number of multi-level topologies and modulation schemes have been introduced in past years, but among all multi-level topologies, three fundamental multi-level topologies are present. The basic multi-level topologies include: neutral point clamped (NPC) topology (also known as diode-clamped (DC) topology), capacitor-clamped topology which is also known as flying-capacitor (FC) topology, and cascaded H-bridge (CHB) topology. Other multi-level topologies originate from these three basic structures. Each single multi-level topology has individual advantages and disadvantages, so selection of proper topology is completely dependent on the intended application. Many modulation schemes have been introduced for multi-level topologies such as sinusoidal pulse width modulation (SPWM), carrier-based pulse width modulation (CPWM), space vector modulation (SVM), selective harmonic elimination (SHE), and optimized harmonic stepped waveform (OHSW) technique.

In this chapter, multi-level topologies and their modulation schemes are reviewed. The following section begins with fundamental multi-level topologies, followed by other multi-level topologies stemming from the fundamental topologies. Advantages and disadvantages of each topology are explained and, at the end of the chapter, a comparison between these topologies is presented.

2.2. Fundamental Multi-level Topologies

In general, a multi-level inverter employs a number of series power switches in order to increase the voltage and power capability of an inverter. This concept utilizes multiple small voltage levels, such as capacitors or batteries to create DC sources, resulting in the use of lower-rated semiconductors. In fact, the term, “multi-level inverter,” began with the 3-level inverter. By increasing the number of levels, a better output AC voltage with less distortion can be achieved

while the control algorithm becomes more complex. Figure 2.1 illustrates a multi-level inverter versus a conventional two-level inverter in which all power switches have been substituted with an ideal switch, thus providing different voltage level on the output [17]. In a two-level inverter if the DC link voltage is assumed to be E, the output voltage can be 0 or E. In a 3-level inverter, the output voltage can be 0, E, or $2E$. In general, an n-level inverter can have various voltage levels in the output as 0, E, $2E$, $3E$, etc.



(a) **(b)** **(c)**

Figure 2.1 One phase leg of an inverter with a) two levels, b) three levels, and c) n levels

2.2.1. Diode-Clamped (DC) Topology

The diode-clamped (DC), also called neutral-point clamped (NPC), topology is based on the utilization of a number of diodes in order to block small DC sources. The configuration of a single-phase 3-level and 5-level diode-clamped inverter is shown in Figure 2.2.

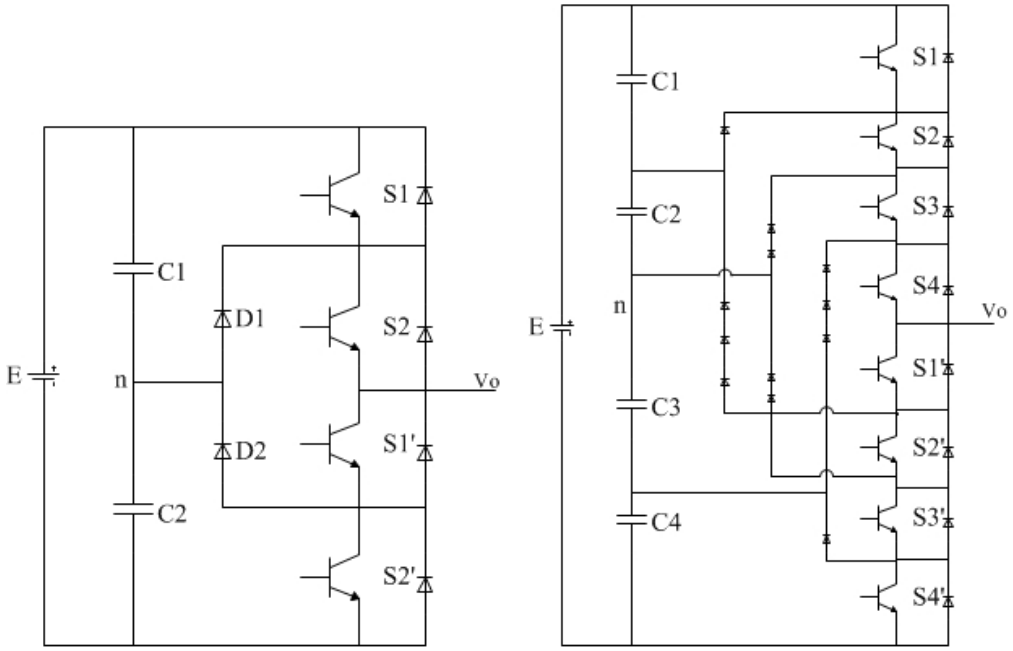


Figure 2.2 Single-phase 3-level and 5-level DC topology

The DC topology can easily be extended to a generic n-level configuration. In a 3-level diode-clamped inverter, the DC bus voltage is divided by capacitor banks into two equal steps. Operation of the inverter is simple. The name of the DC topology originates from the fact that the voltage between two switches is clamped through the clamping diodes. When switches $(S1, S2)$ are *on* and $(S1', S2')$ are *off*, output voltage of the inverter is equal to the voltage of $C1$, which is equal to $^{+E}/_{2}$. Likewise, when switches $(S1, S2)$ are *off* and $(S1', S2')$ are *on*, output voltage of the inverter is equal to the voltage of $C2$, which is equal to $^{-E}/_{2}$. When $(S2, S1')$ are *on* and $(S1, S2')$ are *off*, output voltage of the inverter is equal to 0.

In a 5-level diode-clamped inverter, the DC bus voltage is split into four equal voltage steps. In this case, the number of diodes required to clamp the voltage changes point by point. Each diode is sized to provide voltage blocking for the voltage across one capacitor. For instance, $D1$ is represented only by one diode, while $D1'$ is represented by three diodes equal to $D1$, which are in series because it must block voltage across capacitors $C2$, $C3$, and $C4$, meaning that it is allowed to use one diode with higher blocking capability or three diodes in series with equal blocking capability to $D1$. Considering the diode reverse voltage for an n-level inverter, calculated by $V_r = {}^{E}/_{n-1}$, the diode reverse voltage for a 5-level inverter is equal to $^{E}/_{4}$, thus demonstrating that increasing the number of levels results in decreased voltage stress on the

components. Operation of 3- and 5-level NPC topology is shown in Table 2.1 and 2.2, respectively.

Table 2.1 Switching table for the 3-level DC topology

Switches				Output Voltage
S1	S2	S1’	S2’	Vo
1	1	0	0	$+E/2$
0	1	1	0	0
0	0	1	1	$-E/2$
1	0	0	1	N/A

Table 2.2 Switching table for the 5-level DC topology

Switches								Output Voltage
S1	S2	S3	S4	S1’	S2’	S3’	S4’	Vo
1	1	1	1	0	0	0	0	$+E/2$
0	1	1	1	1	0	0	0	$+E/4$
0	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	$-E/4$
0	0	0	0	1	1	1	1	$-E/2$

In Table 2.1 and 2.2, the on-state and off-state of the switches is shown by 1 and 0, respectively. Any shortcut should be avoided in each of the switching states, meaning that all switches cannot be turned on simultaneously. In addition, S_i and S_i', where i is the number of the switches, should be switched in a complementary way. For instance, when S_1 is *on*, S_1' should be *off* and vice versa. This has to happen for all the other switches.

An important advantage of this topology is that it does not require an insulated DC source, allowing it to be used for a wide range of applications, specifically renewable energy applications in which only one DC source is available. In this structure, DC voltage steps are created by several equal DC capacitors. In addition, the control strategy for this inverter is quite simple because it can be controlled by a simple extension of a conventional PWM method.

Numerous applications are relevant for diode-clamped topology. One application of the multi-level diode-clamped inverter is the variable speed drive for high-power medium-voltage (2.4 to 13.8 kV) motors [19]. Another application of this topology is its use as an interface between a

high-voltage DC (HVDC) transmission line and an AC transmission line**Error! Reference source not found.**.

In diode-clamped topology, higher number of levels necessitates greater number of components. In general, the number of switches, clamping diodes, and DC link capacitors used in a single-phase n-level diode-clamped inverter is equal to $2(n-1)$, $(n-1)(n-2)$ and $(n-1)$, respectively. In fact, increasing one level of the topology adds one capacitor, two switches and several clamping diodes to the inverter, meaning that the relation between level number and number of blocking diodes is quadratic. For high-level inverters, the number of diodes becomes great, which may cause complications because of diode recovery times. On the other hand, the reverse voltage drop changes among the components. An other disadvantage of diode-clamped topology is that mean current through the switches is different. In a 5-level inverter, it can be proved that the mean current flowing through S_4 is smaller than that mean current of S_1. In fact, finding various kinds of switches with identical reverse voltage and dynamic performance with different current ratings is difficult. These disadvantages make this topology unsuitable for renewable energy applications where a high-level inverter is typically necessary. Moreover, diode-clamped topology is not able to deliver real power from DC source to AC source for high levels [21], which is necessary for renewable energy inverters.

2.2.2. Flying Capacitor (FC) topology

This topology is similar to diode-clamped topology in which diodes are replaced by capacitors in order to maintain voltage levels across DC link capacitors. Figure 2.3 shows the structure of a single-phase 3-level and 5-level flying-capacitor inverter. The topology has a ladder structure of DC dice capacitors, in which, the voltage on each capacitor differs from voltage of the next capacitor. FC topology can easily be extended to higher levels. Voltage across each capacitor is given by:

$$\mathbf{V_c = {E}/{n-1}} \tag{2.1}$$

This voltage is the reverse voltage drop each switch can withstand when all capacitors are fully charged. These capacitors are known as clamping capacitors because their function of them is similar to the clamping diodes in diode-clamped topology because they maintain the voltage drop between the buses to which they are connected.

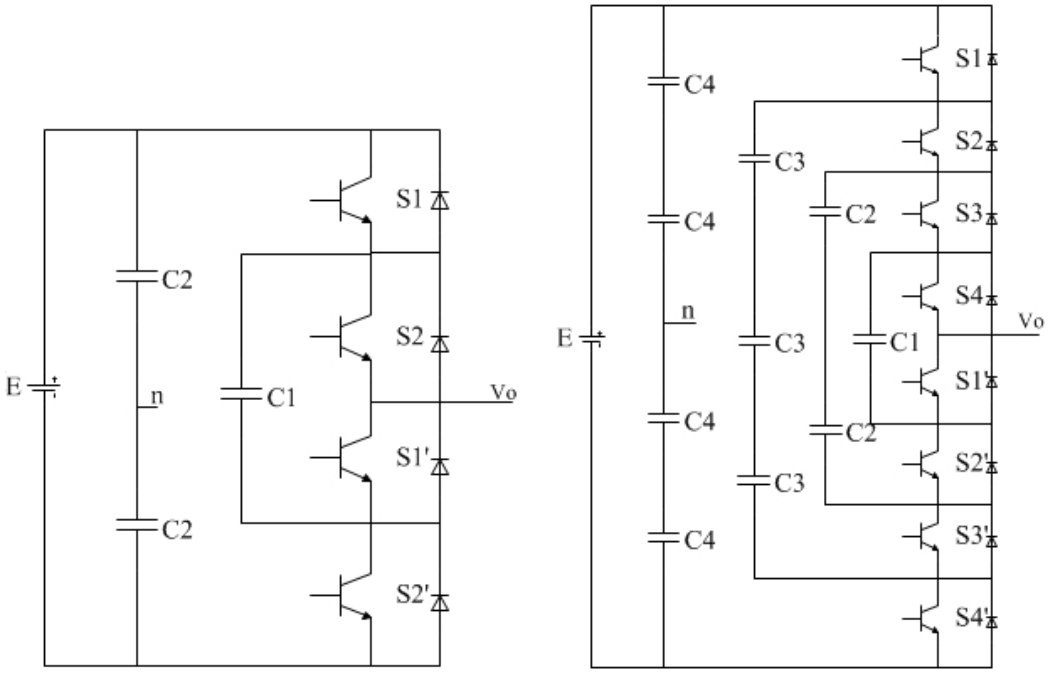


Figure 2.3 Single-phase 3-level and 5-level FC topology

The operation of a 3-level flying-capacitor is similar to the 3-level diode-clamped inverter. When switches($S1, S2$) are *on* and ($S1', S2'$) are *off*, output voltage of the inverter is equal to $^{+E}/_{2}$, and when switches ($S1, S2$) are *off* and ($S1', S2'$) are *on*, output voltage of the inverter is equal to $^{-E}/_{2}$. When ($S1, S1'$)are *on* and ($S2, S2'$) are *off*, voltage of the capacitor C_1 is increased and when ($S2, S2'$) are *on* and ($S1, S1'$) are *off*, the capacitor C_1 is in discharging mode. In the latter two cases, output voltage of the inverter is equal to0. By switching between these two states, charge on the capacitor C_1 maintains balanced. These two switching states are called intra-phase redundant states. In the 3-level inverter, various switch configurations cannot occur. S_i and S_i', where$i$ is the number of switches, should be switched in a complimentary way. Possible configurations for a single-phase n-level flying-capacitor inverter are as:

$$N = 2^{(n-1)} \tag{2.2}$$

For this topology the number of possible configurations is greater than the number of possible output voltage levels. The total number of possible switching states for a 5-level flying-capacitor inverter is 16 whereas the possible number of output voltage levels is 5, while creating 11 redundancies. Therefore, maintaining voltage balancing for this inverter is complicated. Table 2.3 and 2.4 show switching states for 3- and 5-level FC topology, respectively.

Table 2.3 Switching table for the 3-level FC topology

Switches				Output Voltage
S1	S2	S1'	S2'	Vo
1	1	0	0	$+E/2$
1	0	0	1	0
0	1	1	0	0
0	0	1	1	$-E/2$

Table 2.4 Switching table for the 5-level FC topology

Switches								Output Voltage
S1	S2	S3	S4	S1'	S2'	S3'	S4'	Vo
1	1	1	1	0	0	0	0	$+E/2$
1	1	1	0	0	0	0	1	$+E/4$
1	1	0	1	0	0	1	0	$+E/4$
1	0	1	1	0	1	0	0	$+E/4$
0	1	1	1	1	0	0	0	$+E/4$
1	1	0	0	0	0	1	1	0
1	0	1	0	0	1	0	1	0
1	0	0	1	0	1	1	0	0
0	1	1	0	1	0	0	1	0
0	1	0	1	1	0	1	0	0
0	0	1	1	1	1	0	0	0
1	0	0	0	0	1	1	1	$-E/4$
0	1	0	0	1	0	1	1	$-E/4$
0	0	1	0	1	1	0	1	$-E/4$
0	0	0	1	1	1	1	0	$-E/4$
0	0	0	0	1	1	1	1	$-E/2$

Considering Table 2.3 and 2.4, coclusion can be made that output voltage of a generic n-level flying-capacitor inverter is given by:

$$V_0 = \left(\frac{E}{(n-1)}\sum_{i=1}^{n-1} S_i\right) - \frac{E}{2} \tag{2.3}$$

where S_i denotes the state of a generic upper switch.

The flying-capacitor topology inverter has phase redundancies, whereas the diode-clamped inverter has only line-line redundancies [17]. One advantage of this topology is the ability of these redundancies allow a choice of charging or discharging specific capacitors. Depending on the choice of switching states shown in Tables 2.3 and 2.4, each capacitor can be in a charging or

discharging mode and thus can have different voltage values. A suitable control strategy is necessary to keep capacitor voltage balanced properly. In general, in a single-phase n-level flying-capacitor inverters have $(n-1)$ DC link capacitors, $(n-1)(n-2)/2$ auxiliary clamping capacitors, and $2(n-1)$switches, meaning that the number of capacitors has a quadratic relationship with the number of levels. Voltage control for the 3-level inverter is easy due to having only one clamping capacitor. A 5-level and 7-level flying capacitor inverter consist of 10 and 21 capacitors that must maintain balanced, thus requiring a complicated control strategy as the number of levels increases. In fact, experimental inverters with this topology are limited to 3-5 levels. Large numbers of capacitors are more expensive than clamping diodes in diode-clamped inverters, and packaging is also more difficult in high-level inverters. In addition to this problem, flying-capacitor topology is not able to balance the DC link capacitor for purely reactive applications [22]. Although this topology requires only one DC source and is able to control both active and reactive power, which are necessary for renewable energy applications, FC topology cannot be a proper candidate for FACTS applications for renewable energy sources in which the inverter may be required to operate in a purely reactive mode.

2.2.3. Cascaded H-bridge (CHB) topology

The third fundamental multi-level topology is the cascaded H-bridge (CHB). This topology was invented before the other two basic topologies and follows a completely different configuration. Figure 2.4 demonstrates the structure of the 3-level and 5-level CHB inverter.

Each DC source is connected to an H-bridge inverter. The AC outputs of each H-bridge inverters connected in series such that the synthesized voltage waveform is the sum of the inverter outputs.

The name of this topology comes from the modules of H-bridge, or cells, which construct the inverter legs. Tables 2.5 and 2.6 show the allowed switching states for 3-level and 5-level CHB inverter, respectively. As with the other two basic topologies, there are some switching states that should be avoided in order to prevent a shortcut. For instance, switches S_1 and S_1' cannot be turned *on* simultaneously because it makes a shortcut of the source. This topology has intra-phase redundant states because the number of allowed configurations is more than the number of required output voltage levels. The reverse voltage drop for this topology is equal to $V_r = E$ which is greater than the other two fundamental topologies. Operation of the 3-level CHB inverter is

quite easy. When switches (S_1, S_2') are *on* and (S_2, S_1') are *off*, the output voltage is $+E$. Likewise, when switches $(S_2, S_1')$are *on* and (S_1, S_2') are *off*, output voltage is $-E$. Two redundant exist for the output of 0. When (S_1, S_2) are *on* and (S_1', S_2') are *off* or (S_1', S_2') are *on* and (S_1, S_2) are *off*, output of the inverter is equal to 0. Output voltage for the 5-level CHB inverter can be constructed the same as the 3-level because each cell is able to generate voltage of $+E$, 0, and $-E$.

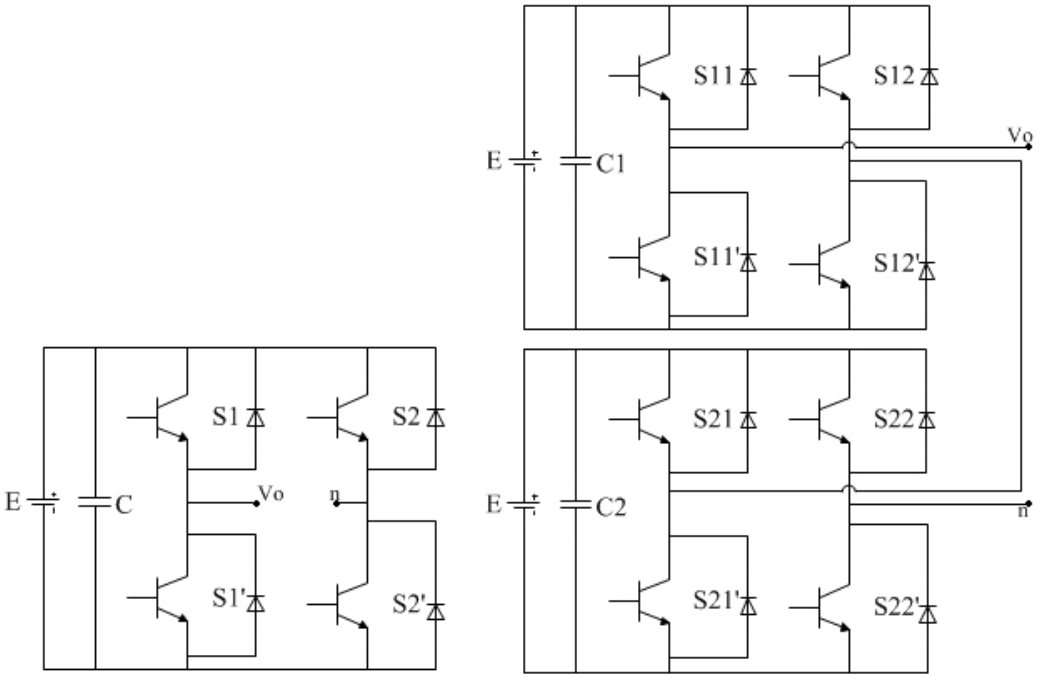


Figure 2.4 Single-phase 3-level and 5-level CHB topology

This topology is limited in that it constructs only an odd number of levels. The first cell generates three levels as each other cell adds two more levels. The topology is very modular and thus easily scalable to higher levels. Each cell has a highly reasonably low cost, as well as desirable reliability which affect the quality of the whole product. In addition, this topology has the advantage of requiring the minimum number of components as compare to the other topologies. Generally, a single-phase n-level CHB inverter consists of $2(n-1)$ switches, and $(n-1)/2$ independent DC sources. The primary disadvantage of this inverter is that it requires more than one independent DC source, which is not practical for wind energy applications because only one DC source may be available.

Table 2.5 Switching table for the 3-level CHB topology

Switches				Output Voltage
S1	S2	S1’	S2’	Vo
1	0	0	1	$+E$
1	1	0	0	0
0	0	1	1	0
0	1	1	0	$-E$

Table 2.6 Switching table for the 5-level CHB topology

Switches								Output Voltage
S11	S12	S21	S22	S11’	S12’	S21’	S22’	Vo
1	0	1	0	0	1	0	1	$+E/2$
1	1	1	0	0	0	0	1	$+E/4$
1	0	0	0	0	1	1	1	$+E/4$
1	0	1	1	0	1	0	0	$+E/4$
0	0	1	0	1	1	0	1	$+E/4$
1	1	1	1	0	0	0	0	0
1	1	0	0	0	0	1	1	0
1	0	0	1	0	1	1	0	0
0	1	1	0	1	0	0	1	0
0	0	1	1	1	1	0	0	0
0	0	0	0	1	1	1	1	0
0	1	1	1	1	0	0	0	$-E/4$
0	0	0	1	1	1	1	0	$-E/4$
0	1	0	0	1	0	1	1	$-E/4$
1	1	0	1	0	0	1	0	$-E/4$
0	1	0	1	1	0	1	0	$-E/2$

Indeed, this topology is very helpful for solar or battery-fed applications in which several insulated DC sources are necessary. Additionally, CHB inverters have been suggested for use as the main traction drive electric vehicles (EV) which require several batteries [23], [24].

2.3. Other multi-level topologies

Introduction of the first multi-level topologies dates back to almost three decades ago. However, new concepts of multi-level topologies have emerged in recent years. In addition to basic multi-level topologies introduced in Section 2.2, numerous other multi-level topologies originate from the fundamental topologies; however, not all topologies have made their way to

the industry yet. Most of these topologies are a derivation of basic topology or a combination of two topologies also called hybrid topologies. These multi-level voltage source inverter topologies belong to medium-voltage high-power applications considered from 2.3 to 6.6 kV and 1-50 MW. Figure 2.5 shows configuration of multi-level voltage source converters including basic topologies [25].

Some newer multi-level topologies that have found practical applications or are currently under development are 5-level H-bridge NPC (5L-HNPC), 3-level active NPC (3L-ANCP), 5-level active NPC (5L-ANPC), hybrid-clamped (HC), transistor-clamped converter (TCC), multi-level matrix converters, the CHB fed with unequal DC sources (asymmetric CHB), CHB with single DC source, hybrid multi-level topologies (NPC+CHB and FC+CHB), stacked multi-cell, and modular multi-level converter (MMC). All of these topologies are shown in Figure 2.5. The following sections briefly review these topologies.

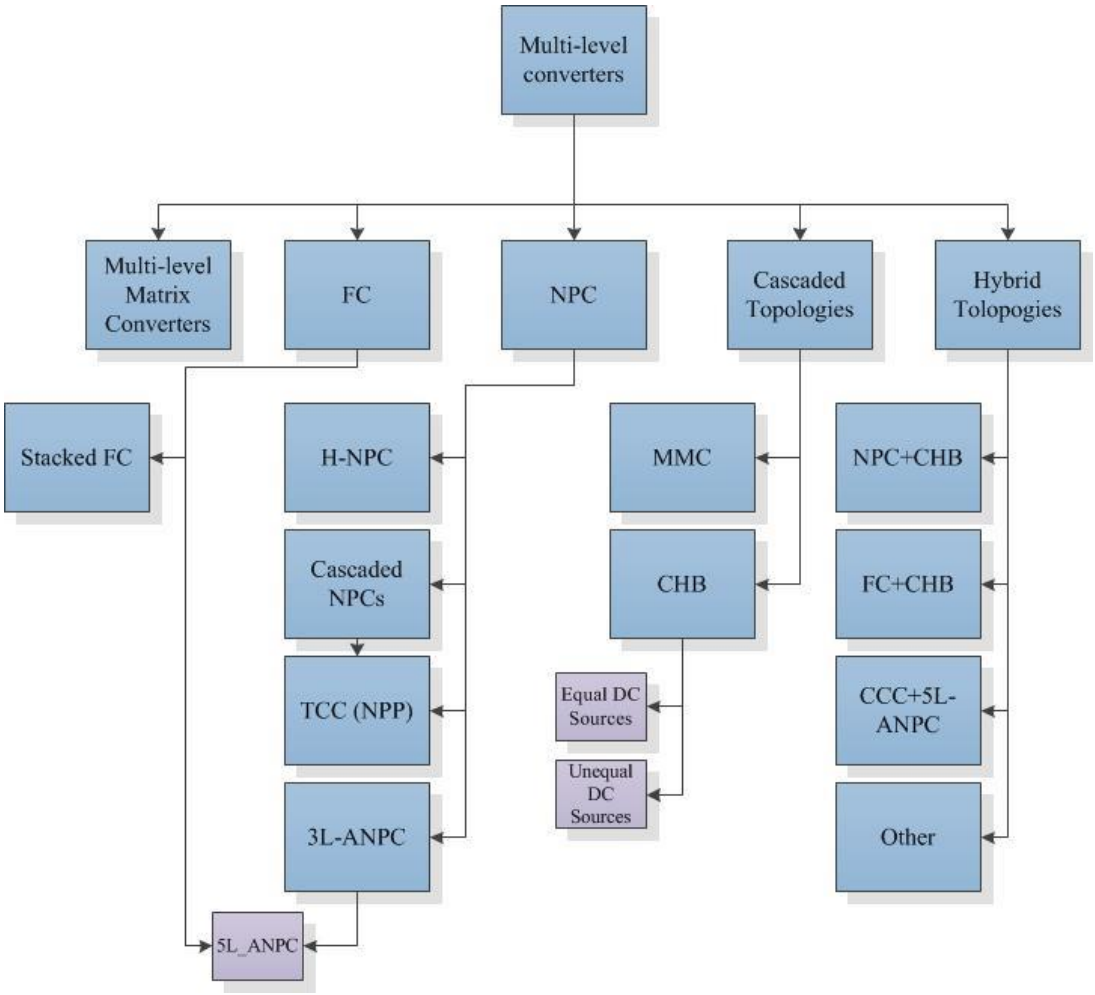


Figure 2.5 Classification of multi-level voltage source converters

2.3.1. 5L-HNPC topology

Figure 2.6 shows configuration of a 5-level H-bridge NPC converter. The 5L-HNPC consists of H-bridge connection of two regular 3L-NPC phase legs. The combination of output voltage of each 3L-NPC phase, which are $+E/2$, 0, $-E/2$, results in five output voltage levels for the 5L-HNPC, which are $+E$, $+E/2$, 0, $-E/2$, and $-E$. References [26],[27] show that various modulation techniques such as selective harmonic modulation (SHE), sinusoidal pulse width modulation (SPWM), and space vector modulation (SVM)can be utilized for the 5L-HNPC. This topology has been commercialized for medium voltage drives by ABB and TMEIC-GE [25]. Voltage balancing across DC-Link capacitors is performed using redundant switching states.

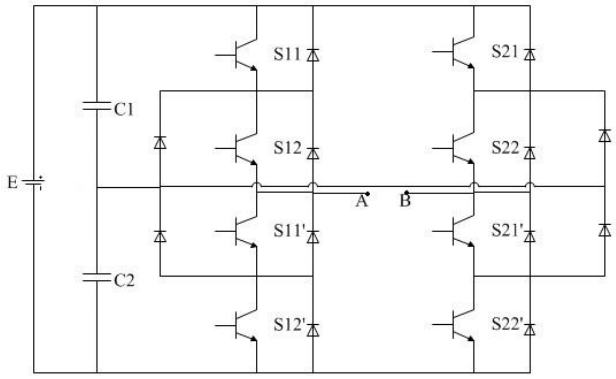


Figure 2.6 Single-phase 5L-HNPC

The primary drawback of this topology is identical the H-bridge topology in that, it requires an isolated DC source for each H-bridge making it undesirable for wind energy applications. A practical implementation of this converter can be found for up to 22 MW power range [28], however, the power range can be increased by stacking additional cascaded cells in order to reach higher-levels such as 9-Level, as shown in Figure 2.7 in which two 5L-HNPC cells are cascaded. Moreover, cascading additional 5L-HNPC cells may result in complications with the main NPC topology such as active power flow problems or voltage balancing issues.

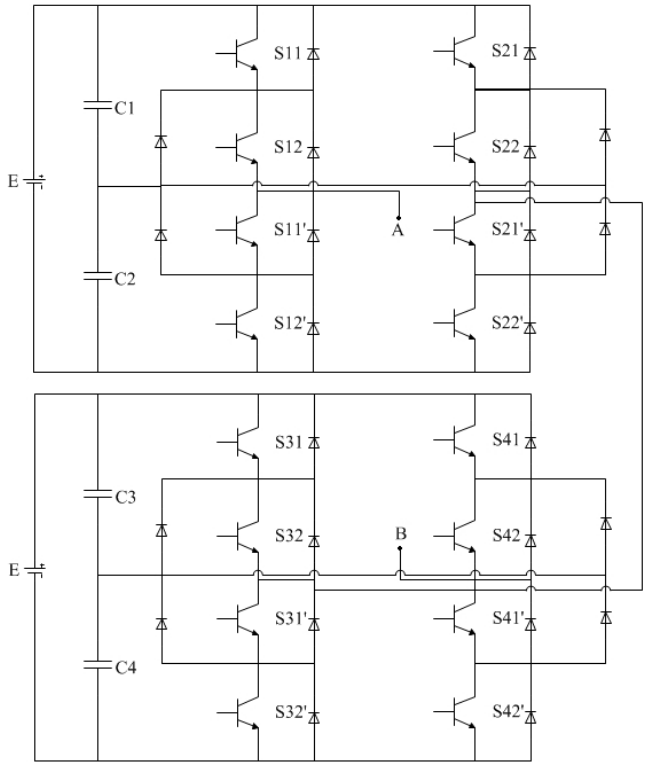


Figure 2.7 Single-phase 9L-HNPC

2.3.2. 3L-ANPC and 5L-ANPC topologies

Figure 2.8 shows configuration of a 3-level active NPC (3L-ANCP). This topology has been recently developed and commercialized with back-to-back configuration and is generally used for motor drives application in which higher fundamental frequency is needed. 3L-ANPC has been introduced to resolve unequal losses between inner and outer switching devices in basic 3L-NPC topology. In the regular 3L-NPC topology, switching devices are cooled with a separate heat sink, thus; affecting the cooling system design and, as a result, limiting the maximum ratings of the converter [29]. The 3L-ANPC is similar to the regular 3L-NPC topology in which two clamping diodes are replaced by additional switches in order to control neutral current paths and, consequently, control power loss distribution. In fact, the use of additional switches forces current to flow through the upper and lower clamping paths when the zero voltage level is generated, while in the classic 3L-NPC topology, current goes through the upper and lower clamping diodes. This makes the power loss control easier in the 3L-ANPC and increases the power rating of the converter. A complete power loss analysis of this topology is explained in [29],[30].

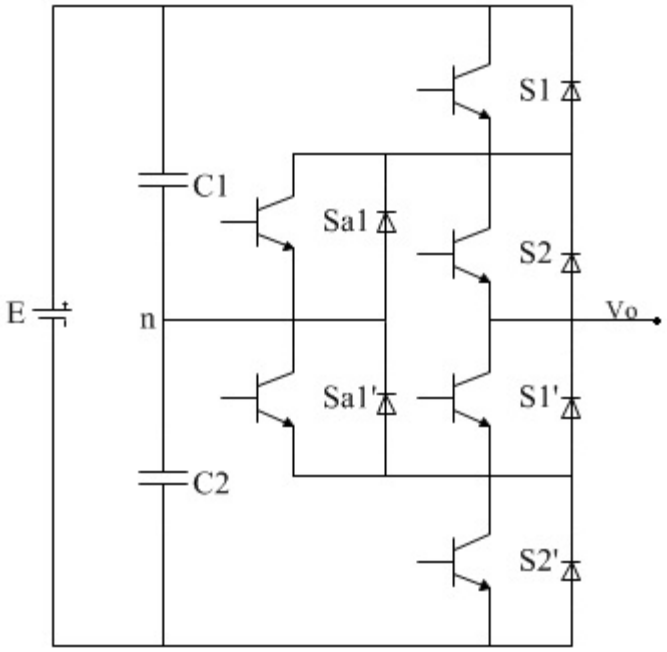


Figure 2.8 Single-phase 3L-ANPC

Recently, another configuration of the 3L-ANPC, 5L-ANPC has been developed combines two concepts of 3L-ANPC with a 3-level flying-capacitor (FC) topology, as shown in Figure 2.9 [31][32][33]. This topology increases the voltage levels to $+E/2$, $+E/4$, 0, $-E/4$, and $-E/2$ and operate based on the basis of redundant switching states, identical to FC topology, in order to maintain proper balance of the floating capacitor. The primary advantage of the 5L-ANPC is that this topology has the benefits of a 5L-NPC topology with only one floating capacitor which makes the capacitor voltage easier to balance; however, a more complex structure and control system is required as compared to basic topologies. In this topology, the device power rating is still limited by the ANPC part and only the power is increased as the FC part adds intermediate levels to the output voltage. Although, theoretically this topology can be expanded to n-levels, floating capacitor limitations have affected practical implementations of this topology [34]. The major disadvantage of this topology is that its operation becomes more complicated for applications requiring more than five levels because of difficulties with balancing capacitor voltage for added floating capacitors. In practical applications, series-connected IGBTs are typically used in the NPC part, thus increasing converter losses as compared to converters using IGCTs. A commercial version of the 5L-ANCP, produced by ABB, is available [35] as a suitable choice for STATCOM applications with SHE technique. In [32]it is shown that utilizing the

correct control strategy allows- active and reactive power to be controlled separately- by using redundant switching states, added by the FC part and virtual-flux direct power control methods [36].

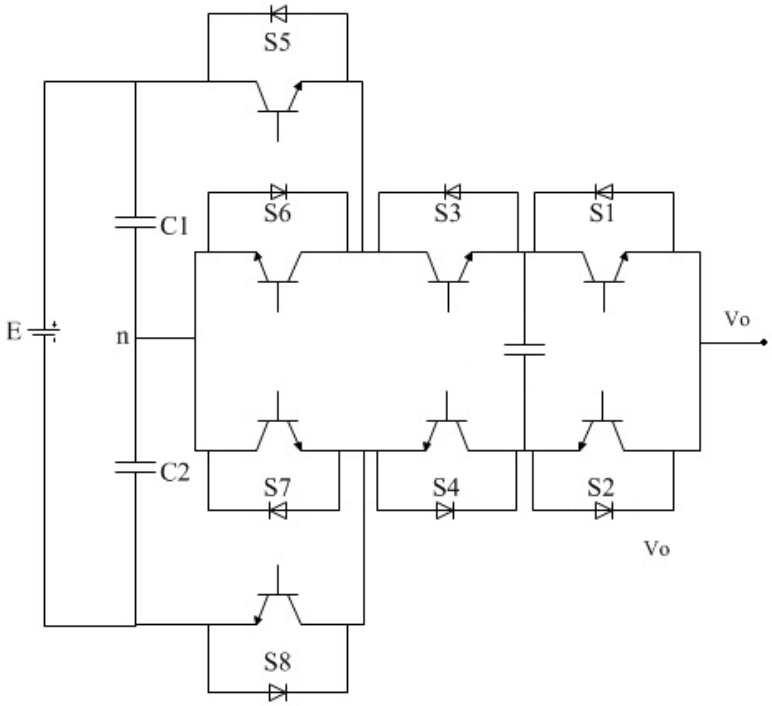


Figure 2.9 Single-phase 5L-ANPC

2.3.3. Hybrid-Clamped topology

This topology is a combination of NPC and FC topologies [37],[38],[39],[40]. The HC topology is similar to the flying-capacitor topology in which clamping capacitors contribute to voltage synthesis. The functions of added clamping capacitors include balancing the dc-link capacitor voltage, providing blocked voltages for the inner switches at turn-off, and providing bidirectional current paths. Both diode-clamped (DC) and flying-capacitor (FC) topologies have redundant switching states of middle voltage levels in order to balance capacitor voltages. As with FC topology, topology cannot keep capacitor voltages balanced in pure reactive applications, making it a less-than-ideal choice for reactive power compensation [37]. Figure 2.10 shows a generalized 5-level topology with self-voltage balancing [41]. This topology can be used in active and reactive power applications regardless of load characteristics, but its primary disadvantage is that it requires a large number of devices. A better configuration with neutral-point voltage balancing ability is shown in Figure 2.11 which requires. This topology can

maintain balance across DC link capacitors regardless of load characteristics or mode of operation, making HC topology an ideal choice for STATCOM applications. In this topology, eight switches ($S1 - S4$ and $S1' - S4'$) are the main switches used to produce desired output voltage, six auxiliary switches ($Sc1 - Sc6$) are the clamping switches, and twelve diodes ($Dc1 - Dc12$) are the clamping diodes. Switching states of the inverter are governed by Table 2.3[37]. This topology maintains balance of DC link capacitors by using the auxiliary switches $Sc1 - Sc6$, and auxiliary clamping capacitors $C5 - C7$. Operation of the hybrid-clamped balances voltages of the DC link capacitors. The primary concern regarding the structure of this topology is that proper size of capacitors should be chosen or; otherwise the topology can become unstable.

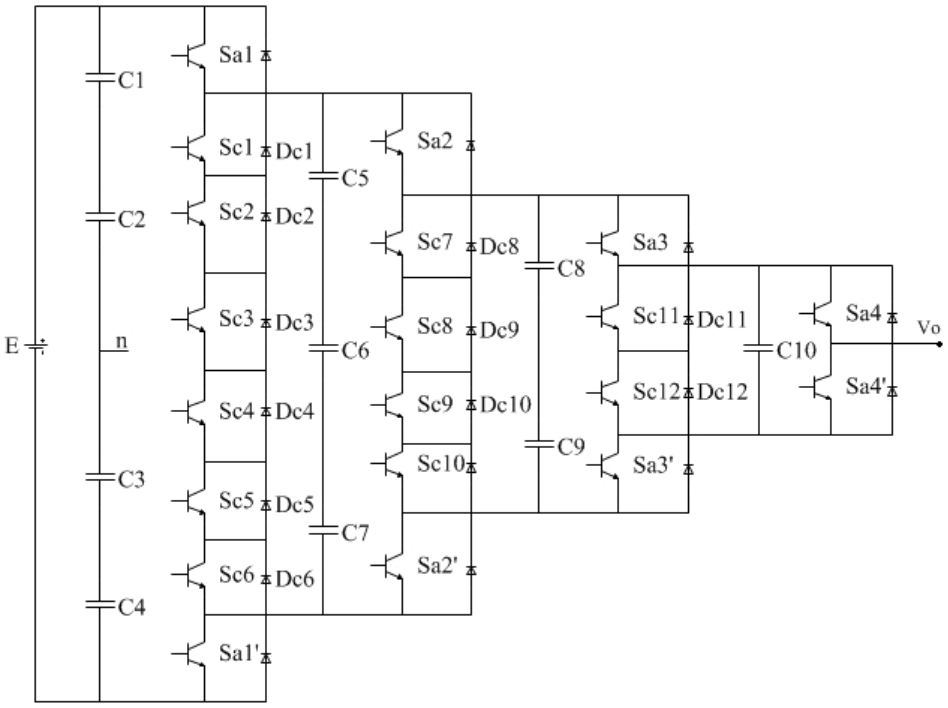


Figure 2.10 Generalized 5-Level circuit shown in [41]

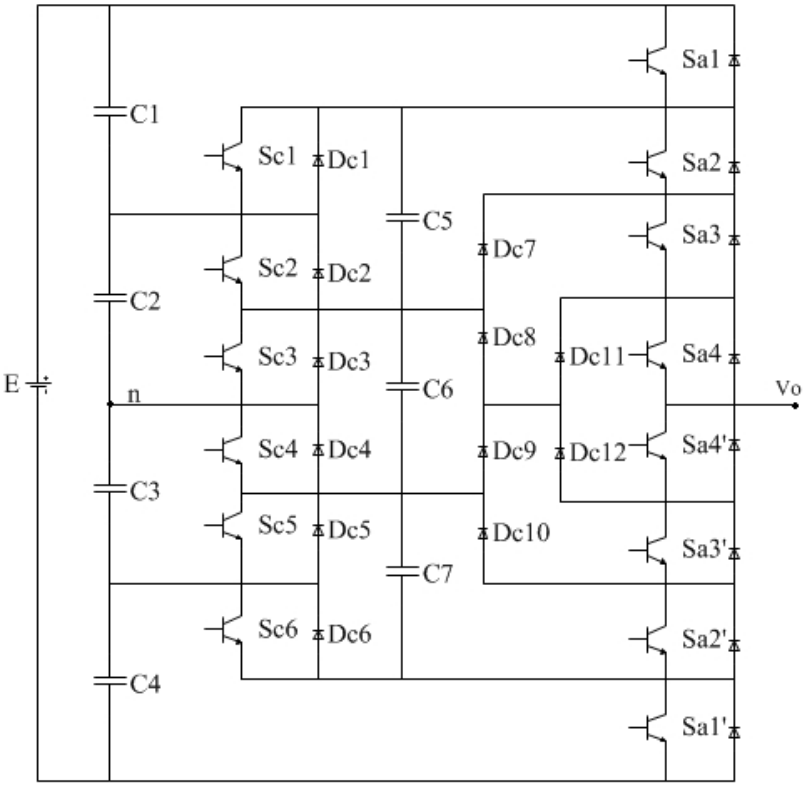


Figure 2.11 5-level hybrid-clamped inverter topology

Table 2.7 Switching States for the 5-level hybrid-clamped topology [37]

Switches								Capacitor Paths	Output Voltage
Sa1	Sa2	Sa3	Sa4	Sa4’	Sa3’	Sa2’	Sa1’	Capacitors	Vo
1	1	1	1	0	0	0	0	$C1 + C2 + C3 + C4$	$+2E/5$
0	1	1	1	0	0	0	1	$C5 + C6 + C7$	$+E/5$
1	0	1	1	1	0	0	0	$C1 + C2 + C3 + C4 + C5$	$+E/5$
0	0	1	1	1	0	0	1	$C6 + C7$	0
1	0	0	1	1	1	0	0	$C1 + C2 + C3 + C4 + C5 + C6$	0
0	0	0	1	1	1	0	1	C7	$-E/5$
1	0	0	0	1	1	1	0	$C1 + C2 + C3 + C4 + C5 + C6 + C7$	$-E/5$
0	0	0	1	1	1	1	1	-	$-2E/5$

HC topology can be expanded to any voltage levels, but it requires the maximum amount of components compared to all multi-level topologies. The large amount of components necessary for HC is the main disadvantage when considering higher-level applications. In a single-phase n-level HC topology, $2(n-1)$ main switches, $2(n-2)$clamping switches,$(n-1)$DC-

linkcapacitors,$(n-2)$ auxiliary capacitors,and $(n-1)(n-2)$ clamping diodes generally are needed. Based on this topology structure, all switches and diodes experience identical voltage stress and all capacitors have identical voltage. The ability of the DC link capacitor voltage balancing scheme to manitain balanced voltages regardless of the load characteristics_ is the primary advantage of HC topology when used for STATCOM applications.

2.3.4. Transistor-clamped converter (TCC) topology

Transistor-clamped converter (TCC) was first introduced in1977 [25] . Figure 2.12 shows the structure of (TCC) topology, which is similar to diode-clapmed topology. In TCC topology, connection points are clamped by bidirectional switches which make a controllable current path, similar to ANPC topology instead of clamping connection points between switches and capacitors through diodes, bidirectional. In other words, the major advantage of TCC topology is that it is able to control current paths to control power loss distribution. As with ANPC topology, this leads to a higher power range, consequently allowing the converter to be used in higher-power applications. Moreover, the controllable power loss distribution enables the device to operate in higher frequencies. As a result TCC topology can be used effectively for high-speed applications.In [25], a commercialized implementation of this topology made by Eaton for medium voltage and high power applications is presented.

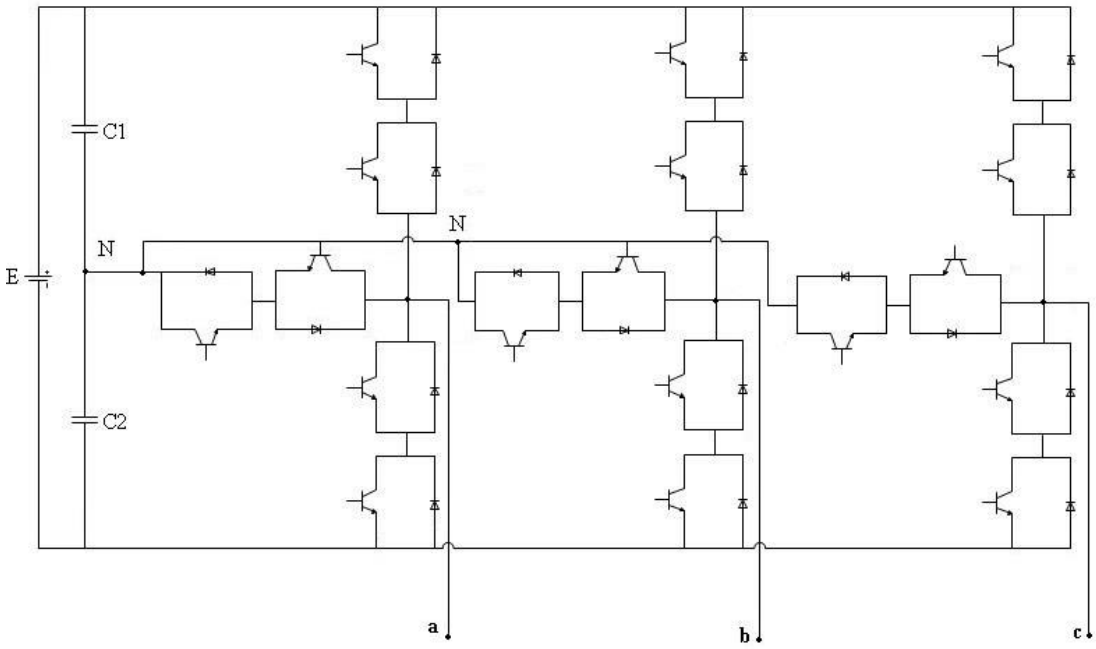


Figure 2.12 Structure of the three-phase three-level TCC

2.3.5 Multi-level matrix converter topologies

Conventional matrix converters (CMCs) are currently used for various applications in power electronics; however, they have significant disadvantages. The primary drawback of conventional MCs is low fundamental component of output voltage and high level of the total harmonic distortion. Matrix converters convert the input ac signal to output ac signal without any mid-stage DC conversion, shown in Figure 2.13. Hence, matrix converters are categorized under direct conversion converters. Multi-level MCs were created for applications which require good harmonic and conversion factors. They are typically used for transportation applications such as electric vehicles (EVs). This type of converters utilizes bi-directional switches in order to transfer energy back and forth, enabling four-quadrant operation. Matrix converters offer the potential for significant size and weight reductions in power converter applications due to the lack of large energy storage elements, such as DC link capacitors or inductors.

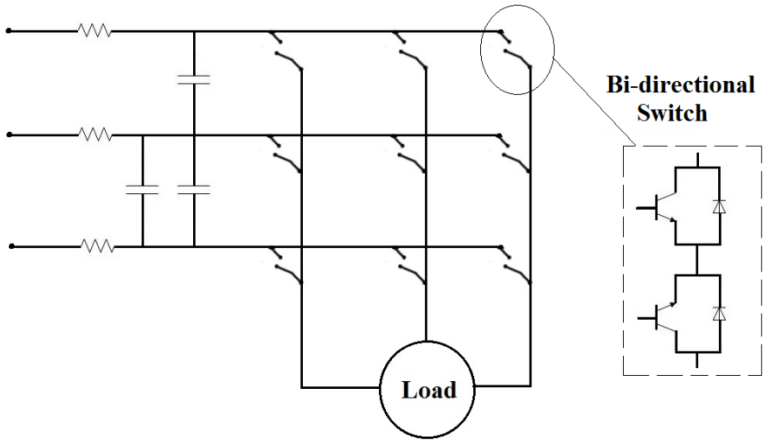


Figure 2.13 Multi-level matrix converters

Multi-level matrix converter topologies stem from a combination of the three basic multi-level topologies with standard matrix converter topologies resulting in FC matrix converter, indirect matrix-NPC, and CMC as shown[42],[43]. These topologies have the advantages of direct power conversion as well as improved waveform quality. Table 2.8 shows a summary of multi-level matrix converter topologies.

Table 2.8 Multi-level matrix combinations

Matrix Converter Topology	Multi-Level Converter Topology	Resulting Multi-Level Matrix Converter Topology
Two-stage Matrix Converter	Diode-Clamped Converter	Two-stage, Three-Level Matrix Converter
Standard Matrix Converter	Capacitor-Clamped Multi-Level Converter	Flying-Capacitor Multi-Level Matrix Converter
Standard Matrix Converter	H-bridge Multi-Level Converter	H-bridge Multi-Level Converter

Indirect matrix converter is an alternative for traditional matrix converter topologies. In order to generate an additional level from a two-stage matrix converter, a diode-clamped multi-level inverter can be connected to the output of a 3-phase to 2-phase matrix converter. In the FC multi-level matrix converter, capacitors can be utilized to generate extra levels, as in the classic FC topology. Capacitors in the circuit are controlled to fix on a voltage which is half the relevant line-to-line voltage. Similar to conventional MCs, the operation of multilevel matrix converters have constraints from passive elements inside the converter. The CMC is the only one that has recently found commercial presence [25]. This topology effectively increases the converter power rating and, elevates the voltage by the series connection of power modules, as with CHB topology.

2.3.6 Asymmetric CHB topology

CHB multilevel inverters with unequal DC source (hybrid or asymmetric CHB inverters) have been introduced in [44]. This topology is similar to the classic CHB configuration but differs in that the isolated DC sources have unique voltages. In CHB with unequal DC sources, several redundant states are avoided, and with identical amounts of power cells more different voltage levels are generated- thus reducing the number of components used for the topology which consequently and lowering the size and cost of the converter while improving reliability. For example, a regular CHB with three cells can generate seven voltage levels where a three-cell CHB with unequal DC sources can generate 27 voltage levels.

Furthermore, the converter can be appropriately controlled to reduce switching losses, especially in fast-switching applications. The major disadvantage of this topology is that different power ratings of cells may need specific design for each power cell, even with different switching devices, for each power cell thus affecting the modular structure of the topology.

Unlike the equally fed CHB topology, input current harmonic cancellation cannot be achieved in this topology. Another disadvantage of this topology is unequal power losses and heat distribution among various power-rating cells.

The asymmetry produces $3K$ different voltage levels. This topology still requires more than one DC source which makes it a non-ideal choice for wind applications where only one DC source is desired. Figure 2.14 and Table 2.9 show the structure of a nine-level CHB with unequal DC source and its switching states, respectively [44],[45][46].

2.3.7 CHB topology with single DC source

Unlike classic CHB topology which utilizes multiple isolated DC sources, CHB with single DC source uses only one DC source. The interest here is interfacing a single DC power source with a cascade multilevel inverter in which other DC sources are capacitors. To operate a cascade multilevel inverter using a single DC source, capacitors are used as DC sources for all but the first source. In other words, this topology replaces all but the DC sources with capacitors which requires a complex control technique to keep the DC voltage levels intact [47],[48]. Figure 2.15 shows a simple cascade multilevel inverter with two H-bridges. The DC source for the first H-bridge is a DC power source with an output voltage of E, while the DC source for the second H-bridge is a capacitor voltage to be held at $E/2$.

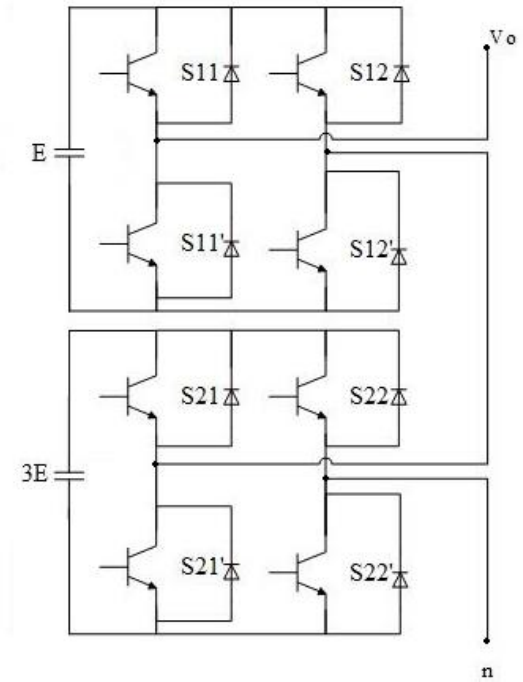


Figure 2.14 Structure of a nine-level CHB with unequal DC source

Table 2.9 Switching state for a nine-level CHB with unequal DC sources

S11	S12	v_{o1}	S21	S22	v_{o2}	Output voltage
1	0	$+E$	1	0	$+3E$	$+4E$
0	0	0	1	0	$+3E$	$+3E$
1	1	0	1	0	$+3E$	$+3E$
0	1	$-E$	1	0	$+3E$	$+2E$
1	0	$+E$	0	0	0	$+E$
1	0	$+E$	1	1	0	$+E$
0	0	0	0	0	0	0
0	0	0	1	1	0	0
1	1	0	0	0	0	0
1	1	0	1	1	0	0
0	1	$-E$	1	1	0	$-E$
0	1	$-E$	0	0	0	$-E$
1	0	$+E$	0	1	$-3E$	$-2E$
1	1	0	0	1	$-3E$	$-3E$
0	0	0	0	1	$-3E$	$-3E$
0	1	$-E$	0	1	$-3E$	$-4E$

The output voltage of the two DC source cascade multilevel inverter is $v(t) = v_1(t) + v_2(t)$. By choosing the proper switching states, the output voltage of the inverter can have the values $-3E/2, -E, -E/2, 0, E/2, E, +3E/2$. This topology has the advantage of using only one DC source which is desired for wind applications in the expense of requiring a sophisticated control system to balance the DC voltages especially during active power conversion [49].

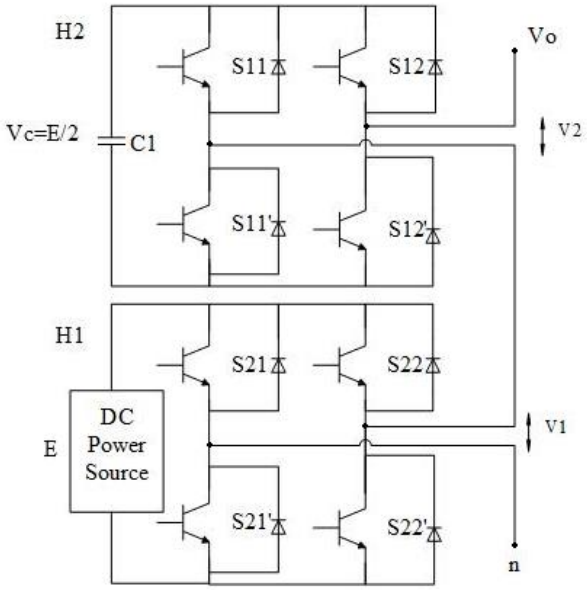


Figure 2.15 Structure of a single-phase seven-level CHB with one DC source

2.3.8 Hybrid Multilevel Topologies

Several new multi-level topologies, based on a combination of two basic topologies and classified as hybrid topologies, have recently been proposed. Hybrid multilevel topologies promise significant improvements for medium voltage and high power industrial drives. Each power module of a hybrid multi-level can be operated at distinctive DC voltage and switching frequency. These topologies minimize total harmonic distortion (THD) of output voltage without increasing the number of power devices. In other words, hybrid topologies increase convert ratings as well as level numbers of while reducing switching frequency. By adding or subtracting various power sources- such as capacitors or inductors, hybrid topologies are able to generate-different voltage levels with the same amount of components. More popular hybrid topologies are NPC-CHB, and FC-CHB.

Figure 2.16 shows the structure of a NPC-CHB topology. As the name suggests, this topology is a hybrid between two classic multi-level topologies, 3L-NPC and single-phase CHB cells connected in series, typically varying between one or two H-bridge cells [25], [50],[51],[52],[53]. The H-bridge part does not have effect the active power rating of the converter but adds additional distinct voltage levels. The CHB part of the topology operates as an active filter which develops power quality; however it converts power losses.

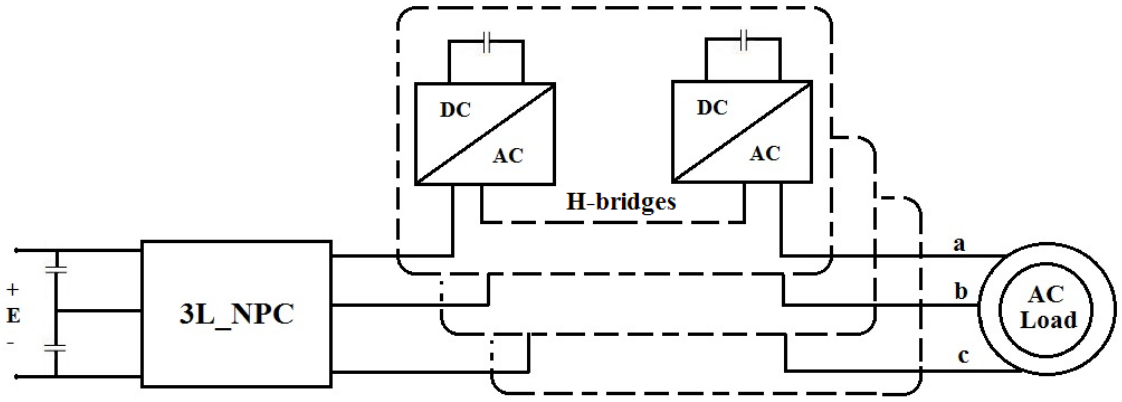


Figure 2.16 Structure of a NPC-CHB topology

The FC-CHB topology is a combination of a three-level flying capacitor inverter cascading with an H-bridge power cell in each phase[54]. This topology has redundant switching states in which capacitor voltages maintain balance by choosing proper switching states. FC-CHB has the capability of generating more different voltage levels as compared to classic FC topology.

2.3.9 Stacked multi-cell (SMC) topology

Stacked multicell converter (SMC), developed and validated about a decade ago is a multi-level topology dedicated to high-power medium-voltage applications. SMC allows converters to reach higher output voltage, power, and performances than classical multicell converters. All converters use flying capacitors and the voltage across these flying capacitors must be balanced to allow a correct operation of multicell topologies. SMC enables higher voltages to be reached and increases the number of voltage levels using lower switching frequency[25]. The SMC converter is based on a hybrid association of elementary commutation cells as shown in Fig. 2.17 **Error! Reference source not found.**[55].The structure of this topology allows the splitting of input voltage into several fractions. As a result, lower-rating power switches can be used for this topology as well –in addition, this topology reduces energy stored in flying capacitors as well as losses in the semiconductor devices. The primary disadvantage of this topology is the need for a high number of capacitors, thus affecting the advantages of this topology. Moreover, it requires an independent DC source for each flying-capacitor module that is stacked in series [56]. SMC topology has not yet found industrial presence.

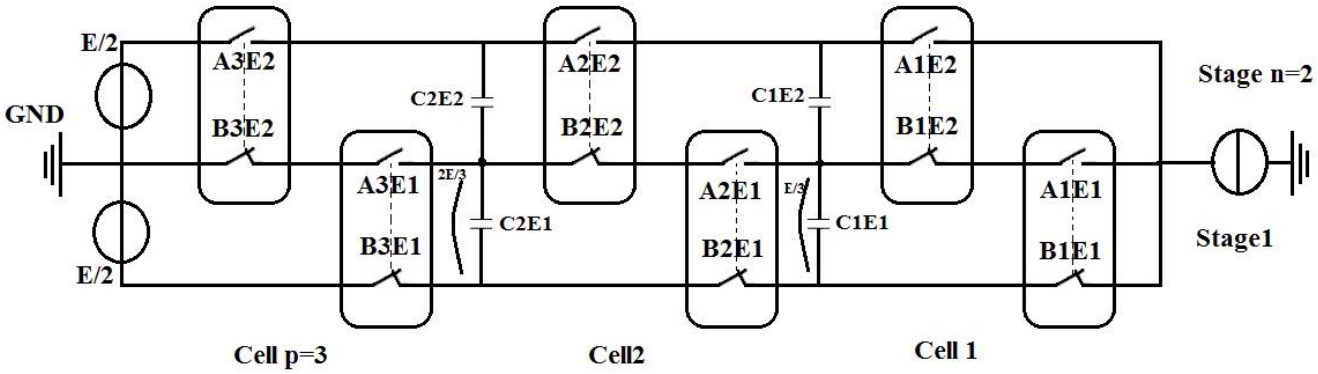


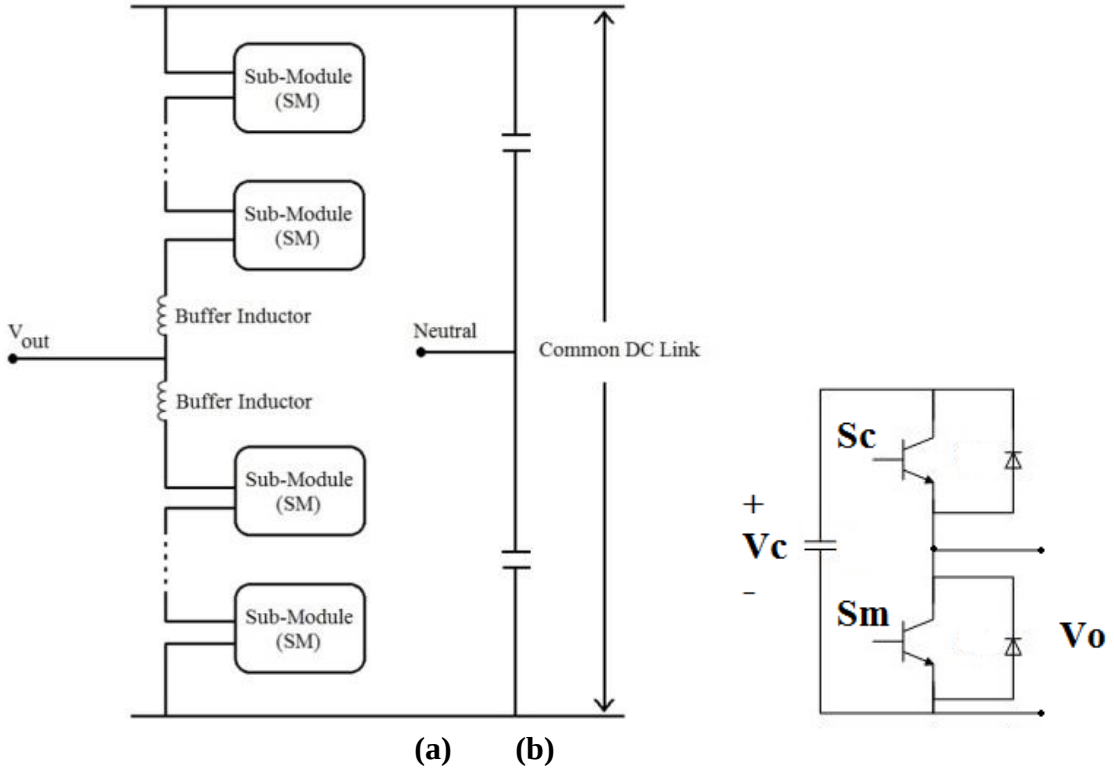
Figure 2.17 Structure of an SMC with 3 cells and 2 stacks (3*2)

2.3.10 Modular multi-level converter (MMC)

The final topology is the modular multilevel converter (MMC or M2C) which is one of the most advanced topologies that has gained specific attention for mid- to high-voltage applications such as renewable energy converters. MMC is used by SIEMENS for HVDC Plus technology [57],[58]. The topology itself was developed in the early 2000s and has received a large amount of attention [25]. MMC topology is composed of multiple H-bridges called sub-module (SM). The number of power modules must be even in order to generate an equal number of positive and negative levels. To achieve higher number of levels, the power modules are stacked. Each SM consists of a floating capacitor and two switches. This topology is an ideal choice for FACTS applications if capacitors voltages remain balanced. MMC is able to transfer active and reactive power regardless of load characteristics. The primary drawback of this topology is that it requires large capacitors, as compared to similar topologies which may affect the total cost of the inverter. However, no need for any type of snubber circuit for MMC can alleviate this problem.

The main benefits of MMC topology include: modular design based on identical converter cells, simple voltage scaling by a series connection of cells, simple realization of redundancy, and possibility of a common DC bus. Figure 2.18(a) shows circuit configuration of a single-phase MMC. The converter is composed of an arbitrary number of identical sub-modules (SMs). An n-level single-phase MMC consists of a series connection of $2(n-1)$ basic SM and two buffer inductors. Figure 2.18(b) shows the structure of each SM consisting of two power switches and a floating capacitor. Two switches of the SMs are controlled in a complementary manner. The output voltage of each SM is equal to zero if the main switch (S_m) is *On* and the auxiliary switch (S_c) is *Off* or is equal to the SM's capacitor voltage (V_c) if S_m is Off and S_c is *On*.

A complicated control strategy is required in order to keep the capacitors voltages balanced. In other words, each SM has two distinct states in normal operation. The first state is when the capacitor is *On* (S_c is *On* and S_m is *Off*). Depending on the capacitor charge, current either flows into the capacitor through the freewheel diode of S_c or flows out of the capacitor through S_c. The second state is when the capacitor is in the off mode (S_c is *Off* and S_m is *On*). Depending on the polarity at the SM terminals, current either flows through S_m or its freewheel diode. By properly switching between these two states, proper voltage can be maintained for each SM. Therefore, the total DC side is the sum of all capacitors voltages in one leg. In this topology, the high number of levels reduces the average switching frequency without compromising of power quality. This topology has found practical applications with up to 200 SMs per phase and up to 400 MW [25]. The structure and operating modes of MMC topology are discussed in details in Chapter 4.



(a) (b)

Figure 2.18 Configuration of the MMC topology, b) A sub-module (SM)

2.4 Comparison of multi-level topologies

The most common multi-level inverter topologies have been reviewed in the previous sections. The multilevel concept was introduced with diode-clamped topology in the 1980s, and

since then these topologies have increasingly gained attention for medium- to high-power applications due to numerous benefits such as lower voltage stress on semiconductor devices, low power dissipation, consequently higher efficiency, and minimalizing harmonic contents at the output power. Multi-level inverters have been widely used in various industrial applications including motor drives, active filters, renewable energy converters, flexible AC transmission systems (FACTS), and static synchronous compensators (STATCOM).

Each topology has unique advantages and disadvantages and choosing the proper topology depends absolutely on the application and its characteristics. Diode-clamped topology (DC), especially three-level configuration, has been widely used in motor drive applications because of its capability to reduce THD with robust control of selective harmonic elimination (SHE) [59], in which a restriction of complexity and pre-defined switching angles for higher-level applications would be present. However, this problem can be alleviated with the use of proper modulation techniques. Furthermore, diode recovery-time problems have become a significant issue for structure higher than three levels structures. Although this topology only needs one DC source, according to mentioned problems for higher-level applications, it is not a good choice for wind applications. In addition to applications in motor drive configurations, DC topology is present in several other industrial applications such as active filters and STATCOM in high voltage grid interconnections.

The flying-capacitor (FC) topology is similar to DC topology in which diodes are replaced by capacitors. It can deliver active and reactive power but operating in purely reactive compensations may cause capacitor voltage balancing troubles. FC topology is used primarily in motor drive and active filter applications. In higher-level topologies, the number of components becomes significant that makes balancing the capacitor voltage a sophisticated problem, hence designer must incorporate a pre-charge controller system. Major advantages of this topology include prevention of the filter demand control of the active and reactive power flow besides phase redundancies.

As compared to all three classic types of multi-level topologies, CHB topology requires the minimum components for a given number of voltage levels. This topology can be controlled with various modulation strategies and is able to deliver both active and reactive power. CHB topology previously has been designed for STATCOMs and motor drives; however, it is currently being used for renewable energy systems as well, especially solar applications.

Although this topology has many advantages, it cannot be an ideal candidate for wind applications because only one DC source is required.

The 5L-HNPC allows for a reduction in the overall number of components and is able to deliver both active and reactive power. The primary drawback of this topology is that it requires isolated DC source for every additional module. Moreover, practical implementation over 5-level eliminates its effectiveness in delivering active power and DC link balancing.

The 3L-ANPC topology can deliver active and reactive power for 3-levels. The main benefit of this topology is that it is able to spread power losses equally among all semiconductor devices, thus increasing the inverter power ratings. Although 3L-ANPC topology advantages, expansion of this topology to more than 3-levels results in voltage balancing issues and active power flow problems. A hybrid configuration of this topology, called 5L-ANPC, can deliver both active and reactive power. Although this topology is scalable to additional levels and reduces floating capacitors over NPC and FC topologies, the increased number of levels beyond 5-level increases the number of floating capacitors and reduces the inverter's range of operation.

Hybrid-clamped (HC) topology is a combination of diode-clamped and flying capacitor topologies with the advantages of requiring only one DC source, balancing DC link voltages without redundant switching states regardless of load profile, and not requiring a sophisticated control system. However, the overall cost and power losses of the system may increase due to the need for a large number of components.

TCC topology can deliver both active and reactive power. This topology allows the current path to be controlled which consequently spreads power losses equally among the switches, thus allowing higher power ratings and switching frequencies. The primary disadvantage of this topology is that, as with NPC, its expansion to more than 3-levels encounters voltage balancing problems and active power flow issues. CHB with unequal DC sources has fewer components and can generate a greater number of levels for any given DC source, as compared to the classic CHB, but requires independent DC sources and cause unequal power dissipation among power switches. CHB with single source requires only one DC source and requiring a reduced number of components in comparison to the regular CHB, but the control system to balance DC link capacitors can becomes complex limiting the inverter operating range.

Matrix converters require no energy storage devices, such as capacitors or inductors, leading to smaller physical size and weight. Although these topologies operate in four-quadrant, multi-level matrix converters are still limited to low power and small application scope.

NPC-CHB topology, which is a member of hybrid topologies, is a combination of two fundamental topologies. This topology introduces more voltage levels as compared to the original 3L-NPC, but this does not effectively increase the active power rating of the overall converter. NPC-CHB topology enhances the output power quality with the expanse of more power losses and more complex control system and additional voltage sensors.

SMC topology has the advantage of fewer components and reduced voltage across capacitors as compared to the classic FC topology, but requires an independent DC source for each stacked module. MMC topology has advantages of being modular and easily-scalable to any level. It does not need snubber circuits and is able to deliver both active and reactive power, but with the expense of a more complex control strategy. The main disadvantage of this topology is that it utilizes large capacitors for its SMs, which can increase the total cost of the system; however, this problem can be offset by the lack snubber circuits. The following Tables depict a general comparison of the required number of components for each 5- and 11-level topology [60].

Table 2.10 Number of components for 5-level inverters[60]

5-Level							
Comparison of Components For Different Single-Phase Multi-Level Topologies	Switches	DC Link Capacitors	Clamping Diodes	Auxiliary Capacitors	Inductors	DC Sources	Total
NPC	8	4	12	0	0	1	25
FC	8	4	0	6	0	1	19
CHB	8	0	0	0	0	2	10
5L-HNPC	8	2	4	0	0	1	15
5L-ANPC	8	2	0	1	0	1	12
HC	14	4	6	3	0	1	28
CHB-Single Source	8	1	0	0	0	1	10
CHB-Unequal Sources	8	0	0	0	0	2	10
SMC	12	0	0	2	0	2	16
MMC	16	2	0	8	2	1	29

Table 2.11 Number of components for 11-level inverter[60]

11-Level							
Comparison of Components For Different Single-Phase Multi-Level Topologies	Switches	DC Link Capacitors	Clamping Diodes	Auxiliary Capacitors	Inductors	DC Sources	Total
NPC	20	10	90	0	0	1	121
FC	20	10	0	45	0	1	76
CHB	20	0	0	0	0	5	25
HC	38	10	72	9	0	1	130
CHB-Single Source	20	4	0	0	0	1	25
SMC	20	0	0	8	0	2	30
MMC	40	2	0	20	2	1	65

2.5 Multi-level control schemes

Harmonic elimination is a major concern for all inverter topologies including conventional 2-level or multi-level topologies. Many research papers target various aspects of different modulation schemes. Deployment of each modulation technique is greatly dependent on the application and structure of the inverter [61],[62].

All pulse width modulation (PWM) strategies used for conventional 2-level inverters can be modified for use with multi-level inverter. The function of modulation techniques used for the multi-level inverters is to generate the proper voltage level required for each phase. This voltage

level generation in the proper switches configuration is performed by implemented hardware or software. All modulation techniques described in this chapter can be used in all multilevel applications. In [61] two possible ways to classify modulation schemes are presented. Figure 2.19 shows classification of modulation schemes described in [62]. Modulation schemes typically produce average output voltage proportional to the used reference signal, however, control systems apply a calculated output voltage based on system requirements [63]. The switching frequency used for multi-level inverters categorizes modulation schemes into two groups: 1) fundamental switching frequency techniques, which produce switch commutations at output fundamental frequency to cancel particularly low frequency harmonics, include space vector control (SVC), and selective harmonic elimination (SHE), and optimized harmonic stepped waveform (OHSW). 2) High switching frequency techniques, which utilize classic PWM modulations for multi-level topologies and switch at high frequencies, include space vector pulse width modulation (SVPWM), phase shifted pulse width modulation (PSPWM), and level shifted pulse width modulation (LSPWM) which includes three major techniques known as phase Disposition (PD), phase opposition disposition (POD), and alternate opposition disposition (AOD). A family of modulations, known as mixed switching frequency techniques, also exists in which switches in different cells commutate at different frequencies. This family is mostly modulations is mostly suitable for hybrid converters.

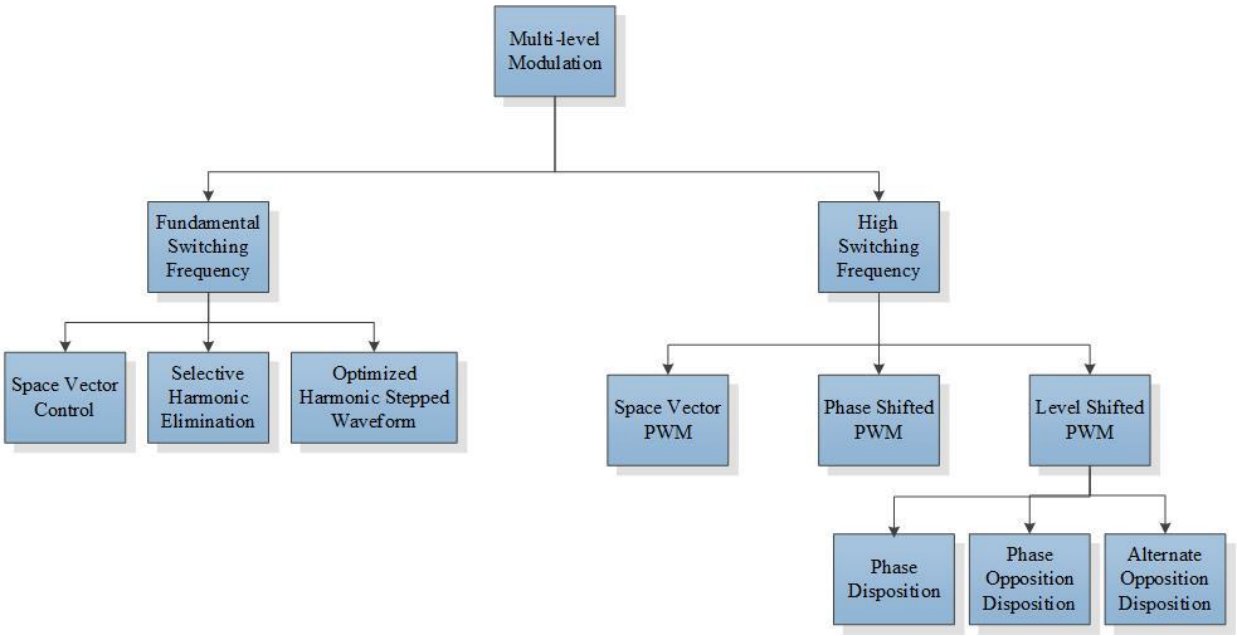


Figure 2.19 Multi-level modulation schemes classification[63]

2.5.1 Fundamental switching frequency modulations

2.5.1.1 Space vector control (SVC)

Space vector control (SVC) is a unique voltage-source modulation technique which differs from the classic space vector modulation (SVM) technique. This modulation technique can be expanded to current source converters if voltage vectors are replaced by current vectors [64]. In this modulation, the switching frequency of each switch is equal to the fundamental, reducing power losses commutation and utilizing it for slow semiconductor devices. Practical implementations of this modulation indicate that it can generate a lower THD than the classic SVM technique [65]. Implementation of the SVC modulation is simple, and making it a suitable choice specially for high-level converters. Operation of this modulation technique is based on the assumption that the inverter can be switched to the vector nearest the commanded voltage vector and held until the next cycle of calculations [61]. The nearest vector to the commanded voltage is determined according to hexagonal regions around each vector. Figure 2.20shows one quadrant of the vector plot of the SVM technique for a 5-level inverter.

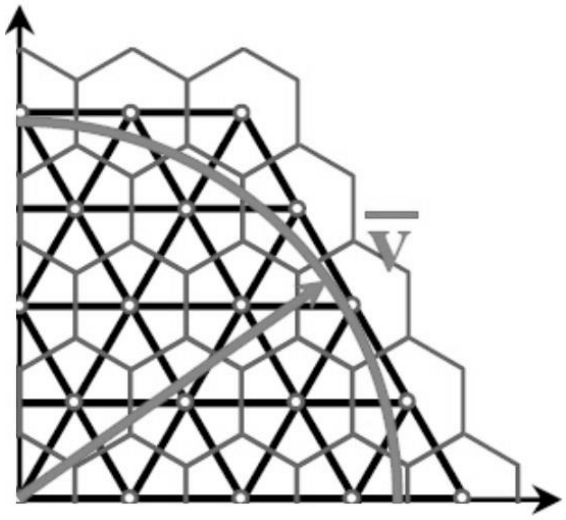


Figure 2.20 5-Level space vector control[63]

Because the commanded voltage vector will lay on the nearest generable vector, SVC cannot produce an output vector exactly equal to the DC value of the reference. Therefore, a small non-compensated error is generated in a PWM cycle. However, the modulation scheme operates in such a way as to minimize this error by selecting the closest generable vector. The generated error becomes smaller as the number of voltage levels goes higher and vice versa. Hence, the

SVC technique does not show a proper performance for conventional 2-level or multi-level inverters with 3levels since output voltage ripples become significant.

2.5.1.2 Selective harmonic elimination (SHE)

The selective harmonic elimination (SHE) method, also known as the fundamental switching frequency method targets the cancellation of various ordered harmonics. The method principle is based on offline calculations of proper switching angles in order to eliminate specific harmonics [66],[67], meaning that, over each switching period, if the integral of a specific harmonic equals zero, the harmonic is completely cancelled.

For an n-level waveform the Fourier series expansion of the output voltage waveform can generally be expressed as:

$$h_m = \frac{4}{m\pi}\sum_{k=1}^{n}[V_k \cos(m\alpha_k)] \quad (2.4)$$

Where V_k is the kthlevel of DC voltage and $\alpha_k$is the kthswitching angle, considering that $\alpha_1 < \alpha_2 < \cdots < \alpha_k < \frac{\pi}{2}$.

where keeping all switching angles lower than $\frac{\pi}{2}$ is a complicated constrain specially as the number of levels increase. To minimize harmonic distortion, theoretically up to $n-1$harmonic contents can be cancelled from the voltage waveform. High frequency harmonics can be easily removed usuing an output filter; therefore, switching angles are typically chosen in such a way as to remove major low-frequency harmonics.

For an 11-level inverter, the Fourier series expansion of the output voltage, shown in Figure 2.21, is depicted as:

$$V(\omega t) = \frac{4E}{\pi}\sum[\cos(m\alpha_1) + \cos(m\alpha_2) + \cdots + \cos(m\alpha_5)]\frac{\sin(m\omega t)}{m} \quad (2.5)$$

Where= 1,3,5,7, … .

Hence, the normalized Fourier series for an 11-level waveform with respect to E is:

$$H(m) = \frac{4}{m\pi}[\cos(m\alpha_1)+\cos(m\alpha_2)+\cdots+\cos(m\alpha_5)] \quad (2.6)$$

where $\alpha_1, \alpha_2, \ldots, \alpha_5$ are the first to fifth firing angles, respectively. These equations can be solved offline and the pre-calculated switching angles are stored as data in memory (look-up table) of a microcontroller in order to generate PWM gate signals. Gained firing angles are used for cancellation of target harmonics including the 5th, 7th, 11th, and 13th harmonics. The above equation, for an 11-level inverter, can be reformatted as:

$$\cos(5\alpha_1) + \cos(5\alpha_2) + \cos(5\alpha_3) + \cos(5\alpha_4) + \cos(5\alpha_5) = 0$$
$$\cos(7\alpha_1) + \cos(7\alpha_2) + \cos(7\alpha_3) + \cos(7\alpha_4) + \cos(7\alpha_5) = 0$$
$$\cos(11\alpha_1) + \cos(11\alpha_2) + \cos(11\alpha_3) + \cos(11\alpha_4) + \cos(11\alpha_5) = 0$$
$$\cos(13\alpha_1) + \cos(13\alpha_2) + \cos(13\alpha_3) + \cos(13\alpha_4) + \cos(13\alpha_5) = 0$$
$$\cos(\alpha_1) + \cos(\alpha_2) + \cos(\alpha_3) + \cos(\alpha_4) + \cos(\alpha_5) = 5m_a \quad (2.7)$$

Where $m_a = \frac{V_L^*}{V_{LMax}}$ is called modulation index and V_L^* is the amplitude command of the inverter for a sine wave output phase voltage[12]. It should be noted that the nonlinear equations previously mentioned govern the amplitude of each harmonic, but the complexity associated with solving the SHE problem for higher level inverters increases greatly. These equations can be solved by an iterative method, such as Newton-Raphson or several other methods, such as genetic algorithms or resultant theory [12]. In [68], detailed explanation of angles calculations for SHE technique is provided. Moreover, [69],[70] demonstrate how to solve SHE equations for five- and seven-level inverters.

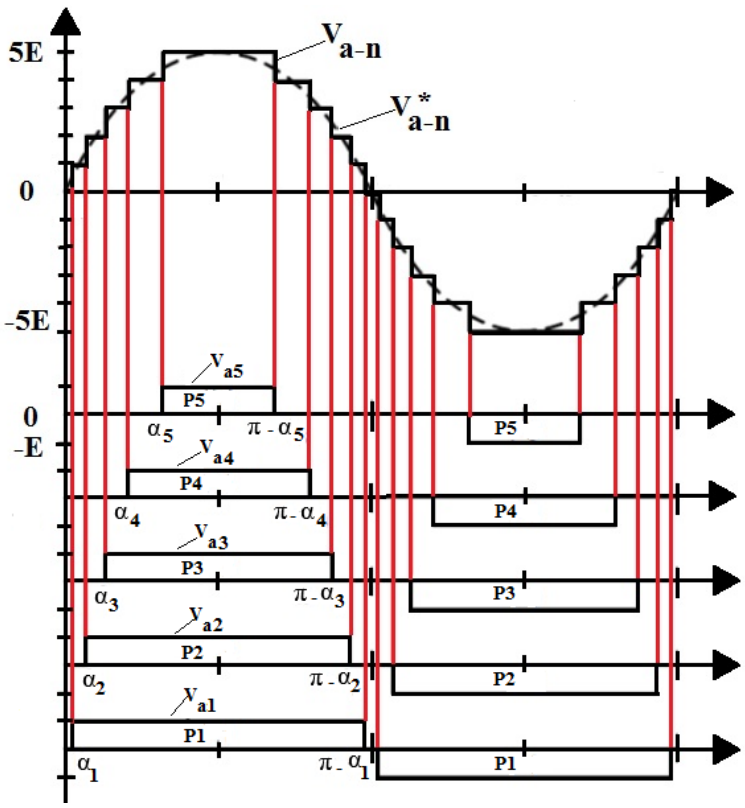


Figure 2.21 An 11-level output voltage waveform [12]

A generalized SHE method was introduced in [67] and [71]in order to achieve a wide range of modulation indexes with minimized THD for synthesized waveforms. In this method, a general stepped waveform with n switching angles can be divided into n modulation index regions. This technique produces minimized harmonics using low switching frequencies, even at low modulation indexes [63].

The primary advantage of this modulation technique is that lower order harmonics are easily cancelled, which consequently lowers the switching frequency. The primary disadvantage of the SHE technique is that the THD of the output voltage waveform remains relatively constant as the number of firing angles increases [60].

2.5.1.3 Optimized harmonic stepped waveform (OHSW)

The optimized harmonic stepped-waveform technique (OHSW) is similar to SHE modulation. However, this modulation is a better choice for higher-level inverters because it can reduce THD without filters. In OHSW, as in the SHE method, the switching angle should be calculated offline in order to minimize specific harmonics. Then, calculated firing angles are stored in a look-up table to be used to generate PWM signals. In general, this technique is able to eliminate $(\frac{n-1}{2} - 1)$

harmonics, where n is the number of voltage levels. Figure 2.22shows the output waveform of an 11-level inverter using OHSW modulation. As shown five firing angles are presented in an 11-level inverter and these angles can be used to eliminate up to four harmonic orders. The OHSW is assumed to be the quarter-wave symmetric. The output voltage level for an 11-level OHSW technique is zero from $wt = 0$ to $wt = \alpha_1$. At $wt = \alpha_1$, the output voltage level is changed from zero to $+V_1$, and from $+V_1$to $+V_2$at $wt = \alpha_2$. This process is repeated until $wt = {}^{\pi}/_{2}$, and the output voltage level becomes $+V_5$. In the second quarter, the output voltage decreases from $+V_5$to $+V_4$ at $wt = \pi - \alpha_5$, and from$+V_4$ to $+V_3$at$wt = \pi - \alpha_4$. This process is similarly repeated until $wt = \pi - \alpha_1$and the output voltage becomes zero. In the second half of the waveform, the process is repeated similarly.

In this method, as with SHE, the main principle is based on the cancellation of individual harmonics areas over one period[60]. Harmonics can be eliminated by three methods: 1) Heights of the firing angles can be changed while the firing angles remain constant, 2) both the firing angle heights and the firing angles can be changed, and 3) the firing angles can be changed while the firing angle height remain constant.

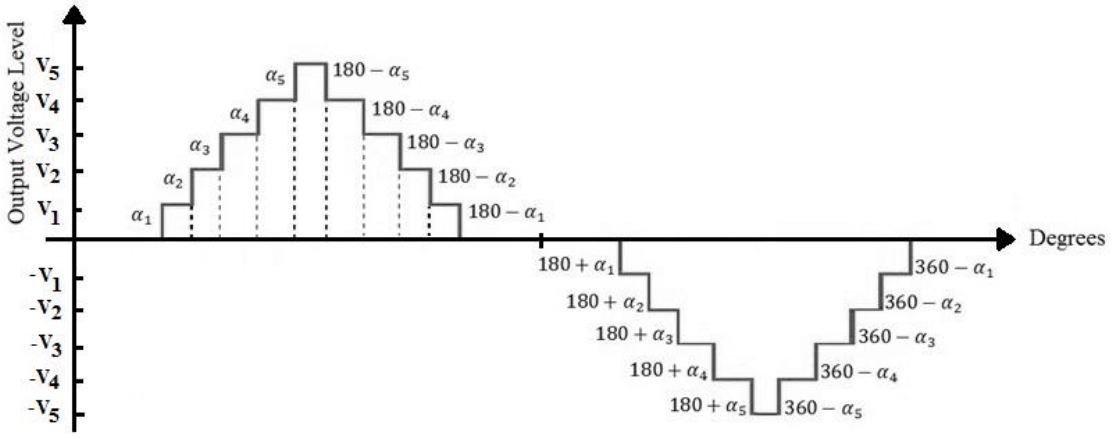


Figure 2.22 Output waveform for an 11-level inverter using OHSW technique

Assuming that the inverter uses identical DC voltage levels, the amplitude of each harmonic can be shown by[72]:

$$H_n(\alpha)=\begin{cases} \frac{4V}{h\pi}\sum_{i=1}^{n-1}\cos(h\alpha_i) & h\ is\ odd \\ 0 & h\ is\ even \end{cases} \quad (2.8)$$

where n is the number of levels, h is the harmonic, $\alpha_i$is the ith switching angle, and V is the DC voltage value.

S with the SHE modulation, a set of non-linear equations must be solved in order to find the desired firing angles in the OHSW technique. This makes complex specifically for higher-level inverter. For an n-level inverter $\frac{n-1}{2}$equations with $\frac{n-1}{2}$ non-linear terms must be solved, by an iterative method such as Newton-Raphson or several other methods, such as genetic algorithms. In [60], particle swarm optimization (PSO) is deployed to solve OHSW non-linear equations for a 5-level inverter using hybrid-clamped topology.

2.5.2 High switching frequency modulations

2.5.2.1 Space vector pulse width modulation (SVPWM)

Space vector pulse width modulation (SVPWM) is one of the most widely used PWM schemes for multilevel inverters. This modulation technique, as with other high frequency modulation techniques, generates output voltage with the same mean value of its reference waveform in a fixed cycle of time. SVPWM was first used in[73]to more than three-levels for the DC topology. SVPWM is an attractive candidate for a multilevel inverter because it directly uses the control variable given by the control system, and identifies each switching vector as a point in complex space [74], it also improves DC link voltage utilization, and reduces commutation losses and THD. In addition, SVPW is suitable for digital signal processing (DSP) implementation and optimization of switching patterns. In SVPWM schemes, a reference space vector is sampled at regular intervals to determine the inverter switching vectors and their time durations, in a sampling interval. In SVPWM, the output waveform generally is generated as the weighted mean of the three vectors adjacent to the reference in the d-q system. A typical space vector diagram for 3, 5, 7, and 9-level inverters are illustrated in Figure 2.27[75].For example, 216 small triangles occur for a 7-level inverter in which the vertex of each triangle represents a space vector. Each space vector is defined by:

$$\bar{V} = V_a e^{j0} + V_b e^{j2\pi/3} + V_c e^{j42\pi/3} \quad (2.9)$$

where V_a , $V_{b,}$ and V_c are phase voltages of the inverter. These vectors can be divided into six major triangular sectors. The first sector is depicted in Figure 2.23, assuming a unity DC supply

source. The coordinates of each vector in the common Cartesian coordinate system can be shown as:

$$V_x = V_a - (V_b + V_c)/2$$
$$V_y = \sqrt{3}(V_b - V_c)/2 \quad (2.10)$$

In order to decrease voltage harmonic distortion, reference voltage V^* can be generated by the three nearest vectors. With V^*lying in triangle ΔEFG, the reference voltage can be shown by:

$$\overline{V_E} = \frac{7}{2} + \frac{j\sqrt{3}}{2},\ \overline{V_F} = 3 + j\sqrt{3},\quad \overline{V_G} = 4 + j\sqrt{3} \quad (2.11)$$

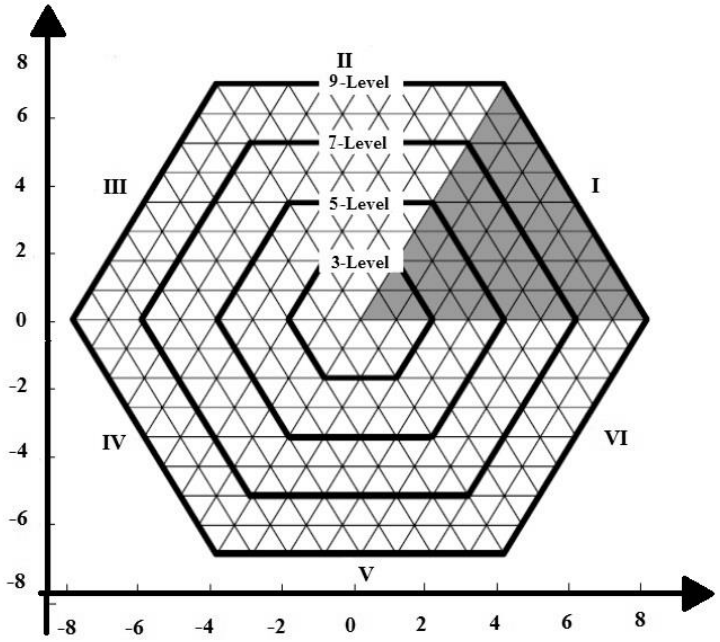


Figure 2.23 Voltage vectors of 3-, 5-, 7-, and 9-level voltage source inverter

The vectors are in Cartesian coordinates, thus causing two complications. 1) Complexity determining the reference vector position, and 2) Specific equations for dwell time calculation particular to each triangle. The solution is to use the 60° coordinate system [75] , instead of the Cartesian coordinate system using equations below:

$$V_\alpha = cos\theta - \frac{Vsin\theta}{\sqrt{3}},\ \ V_\beta = Vcos(60° - \theta) - \frac{Vsin(60°-\theta)}{\sqrt{3}} \quad (2.12)$$

where V_α and V_β are coordinates of a space vector in the 60° coordinate system, and V and θ are the amplitude and phase angle, respectively. This algorithm is very simple and general, meaning that it can be used for inverters independent of the number of voltage levels. Moreover, it has the

advantage of using only two sets of equations for calculating dwell times which makes it simpler for digital implementation.

2.5.2.2 Phase shifted PWM (PSPWM)

Sinusoidal pulse width modulation (SPWM) is one of the most well-known modulation techniques for conventional 2-level inverters. In the simplest configuration, generation of desired output voltage is achieved by comparing the desired reference waveform (modulating signal) with a high-frequency triangular carrier waveform. Depending on whether the reference signal is larger or smaller than the carrier waveform, PWM signals are generated. When the reference signal is greater than the triangular wave, the inverter outputs a positive voltage and when the triangular wave is greater than the control signal, the inverter outputs a negative voltage. Typically, the frequency of the triangular signal is 7–10 times greater than the frequency of the control waveform[60]. Figure 2.25 shows the structure of a conventional 2-level SPWM. For a grid connected inverter, the reference signal frequency, also called control signal, is identical to the 50 or 60 Hz grid frequency. Output voltage of the inverter using SPWM technique is governed by a factor called amplitude modulation, or modulation index (m_a or m). Amplitude modulation is defined as:

$$m_a = \frac{\hat{V}_{control}}{\hat{V}_{tri}} \qquad (0 \leq m_a \leq 1) \tag{2.13}$$

where $\hat{V}_{control}$ and $\hat{V}_{tri}$ are the peak amplitudes of the control and triangle signals, respectively. In PWM generation, another factor is defined as m_f which is the ratio between frequency of the triangle wave and frequency of the sine wave signal:

$$m_f = \frac{f_{tri}}{f_{control}} \tag{2.14}$$

m_f is generally an odd integer. This number significantly determines the frequency of harmonics in the PWM output signal. Significant components of this output are the primary, the harmonic at frequency $m_f * f_c$where f_c is the frequency of the sine wave control (as well as primary output), and the harmonics at $m_f + 2f_c$ and $m_f - 2f_c$. m_f, therefore, determines the harmonic frequency of the output, which affects how easily they can be filtered out. Harmonics

can then be easily filtered out using a low-pass filter containing much smaller components. The disadvantage to this approach is that no harmonics are eliminated, but they are moved to a higher frequency instead. Therefore, the filter loss is also added to the loss of the inverter[60]. Moreover, with increasing switching frequency, switching losses also increases. As a result, the switching frequency should be kept as low as possible.

In order to create a PWM signal which closely follows the desired sine wave output, a multi-level PWM technique should be used. As advantages of higher level PWM generation is that less of a voltage swing exists from the minimum and maximum of each step, resulting in less power loss due to the slope up and down for each step (known as dV/dt losses). This reduced power loss results in higher inverter efficiency. However this increased efficiency includes the expense of additional components and frequency effects which must be filtered out. In a multilevel inverter, the SPWM technique is similar to the 2-level SPWM, with the only difference being that multiple carrier signals are used instead of one carrier signal. Although this modulation technique is unable to improve the total harmonic distortion without filtering circuit responds quickly, because the modulation is not dependent on pre-defined switching angles as with other multi-level modulation techniques, such as selective harmonic elimination or optimized harmonic stepped waveform.

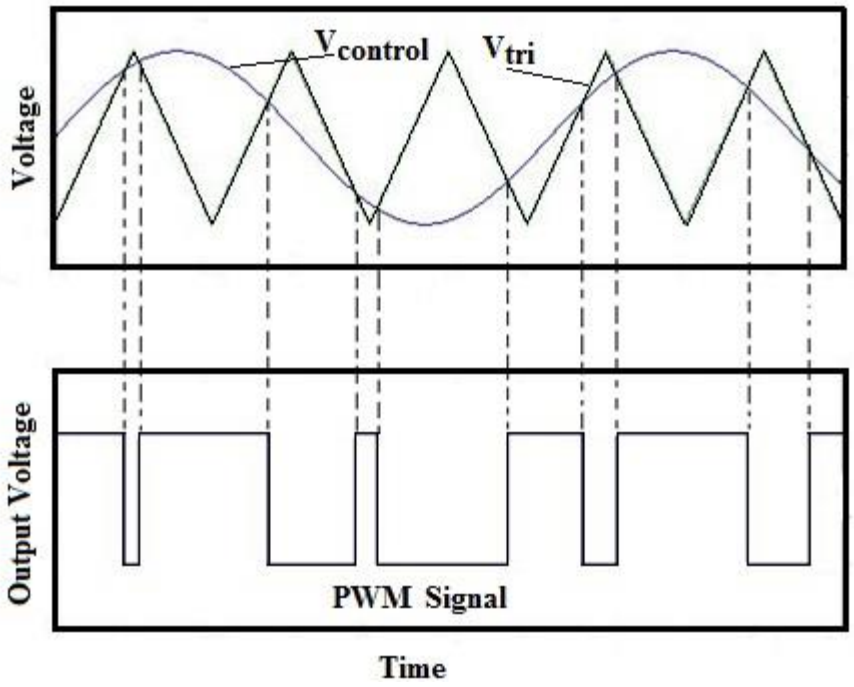


Figure 2.24 Structure of a conventional 2-level SPWM

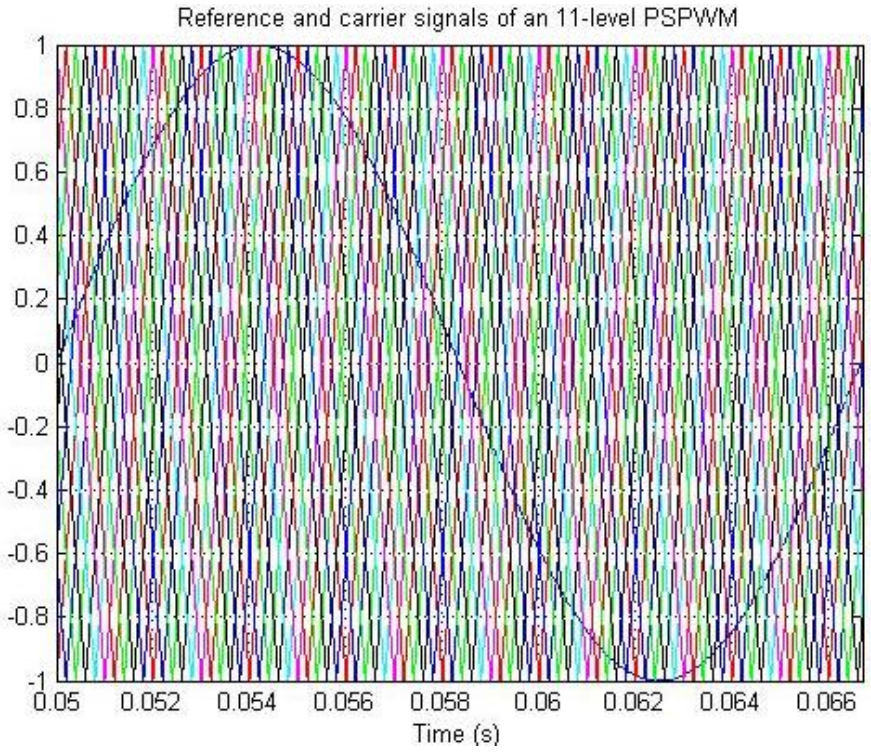
Multi-level SPWM modulations are also referred to multi-carrier PWM techniques. The Phase Shifted PWM (PSPWM) is a standard multi-carrier modulation strategy, but it is not limited, for the cascaded inverter [76]. PSPWM uses multi- carriers which have phase-shifted from each other. In the case of an n-level inverter, $n-1$ carriers with identical amplitude and frequency are needed which are shifted with a delay. For example, a reference modulation signal for an 11-level inverter is compared with ten triangular carrier signals that are phase shifted by a delay. The resulting PWM signals control corresponding switches. To gain optimum harmonic reduction, the desired delay can be expressed by:

$$\Delta = \frac{T_s}{n-1} \tag{2.15}$$

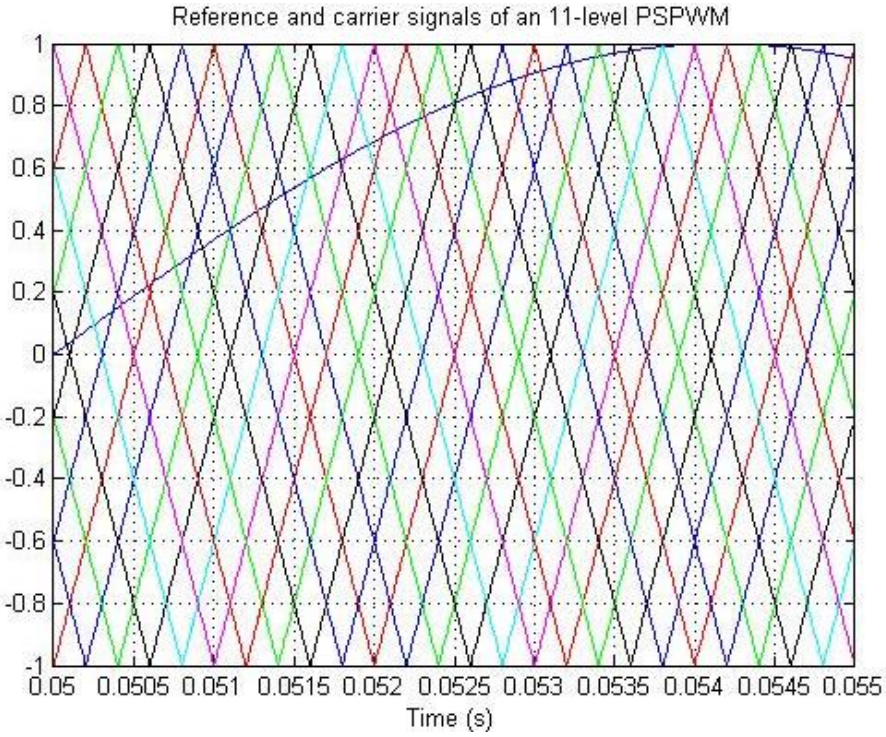
where T_s is the switching period. This strategy cancels all carriers and associated sideband harmonics. Gate signals for the inverter can be directly derived from comparing the carrier with the sinusoidal reference signal. In this modulation technique, variations which use more than one carrier signal can occur[73]. Frequency of the output waveform is higher than the carrier signals. The relationship between output waveform frequency and the carriers is governed by:

$$f_{out} = (n-1)f_c \tag{2.16}$$

Figure 2.26(a) shows reference and carrier signals for an 11-level inverter using PSPWM in which the delay is equal to $Ts/10$. Figure 2.26(b) shows a more-detailed portion of Figure 2.26(a). In Figure 2.27(a), the comparison between the reference and carrier is illustrate in which, the switching frequency is 500 Hz. Using equation (2.16) results in an output switching frequency of 5 kHz. The output waveform of an 11-level inverter using PSPWM is demonstrated in Figure 2.27(b).

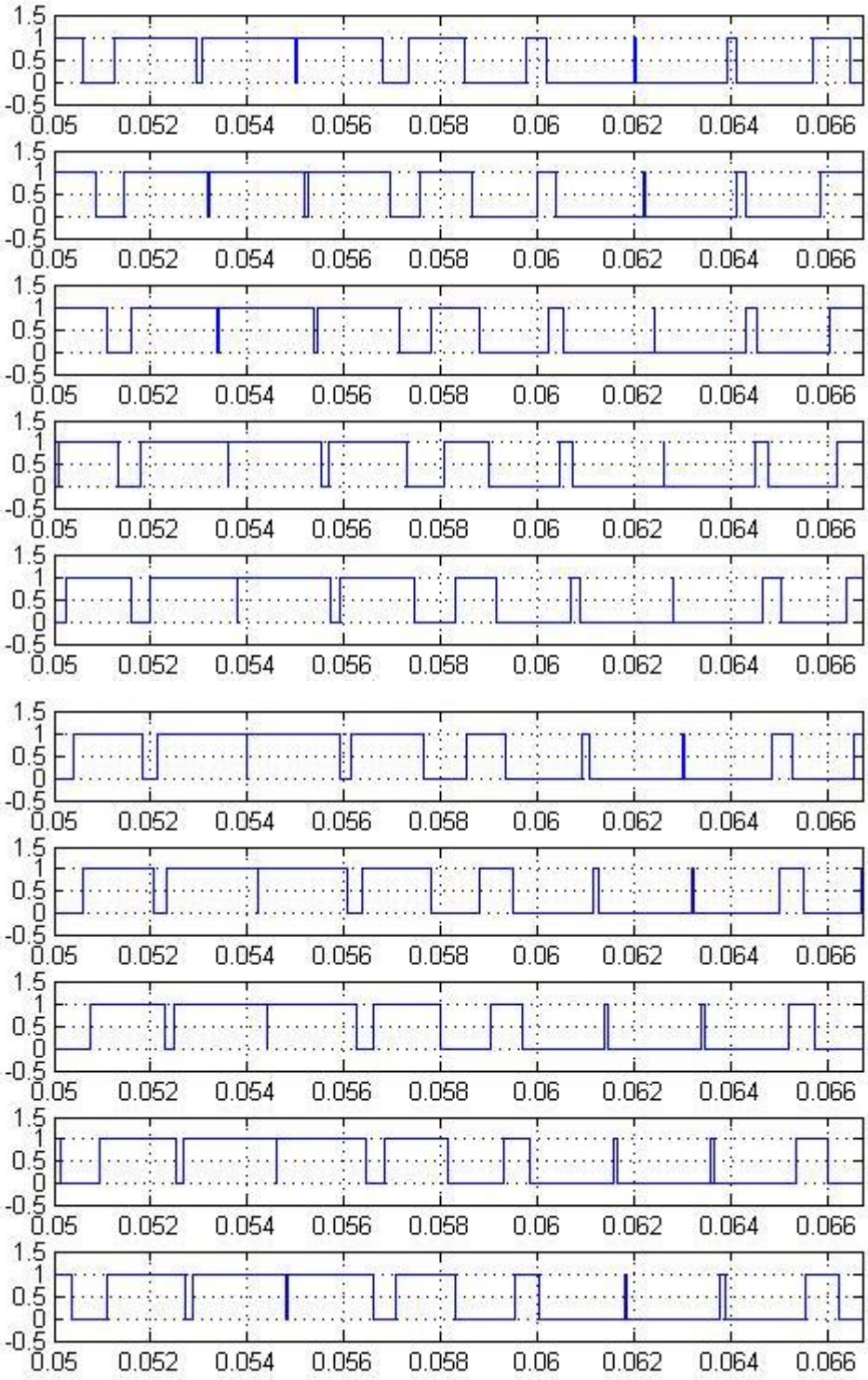


(a)



(b)

Figure 2.25 a) Reference and carrier signals for an 11-level inverter using PSPWM, b) more-detailed portion of part (a)



(a)

(b)

Figure 2.26 a) Comparison between the reference and carrier signals for 11-level PSPWM technique, b) output waveform

2.5.2.3 Level shifted PWM (LSPWM)

Level shifted pulse width modulations can be categorized into three families; phase disposition (PD), phase opposition disposition (POD), and alternative phase opposition disposition (APOD). The basics of all three modulations are the same with small differences. All three modulations possess $(n-1)$carrier signals with the same frequency and amplitude, where n is the number of voltage levels [77],[78]. This modulation technique is generally accepted as the method which generates the lowest harmonic distortion in line-line voltage[79].In this modulation, each carrier signal is connected to a specific output voltage level and every instant of time the modulation signals are compared with the carrier. Depending on which is greater, the definition of switching pulses is generated. In other words, the interval of possible voltage reference values is divided into one zone for every carrier which modulates the output only when the reference belongs to its zone[63]. When the reference does not belong to a zone, associated

carrier comparison output is fixed to a high level, when the reference is above the carrier signal, or low level, when the reference is under the carrier. Figure 2.28 shows the PDPWM technique for an 11-level inverter in which all carrier signals are in phase and arranged on top of each other.

As previously mentioned, for an n–level inverter, $(n-1)$triangle waveforms are used that have a peak-to-peak value of $2/(n-1)$. Hence the most upper triangle magnitude varies from 1 to $(1-2/(n-1))$, second carrier waveform varies from $(1-2/(n-1))$to $(1-4/(n-1))$, etc, for all positive carriers. Similarly, for negative carrier signals, the most upper triangle magnitude varies from 0 to $(-2/(n-1))$, the second carrier varies from $(-2/(n-1))$ to $(-4/(n-1))$. In Figure 2.39(a), comparison between the reference and carrier is shown in which the switching frequency is 3 kHz. The resulting output waveform for an 11-level inverter using PDPWM is shown in Figure 2.39(b).

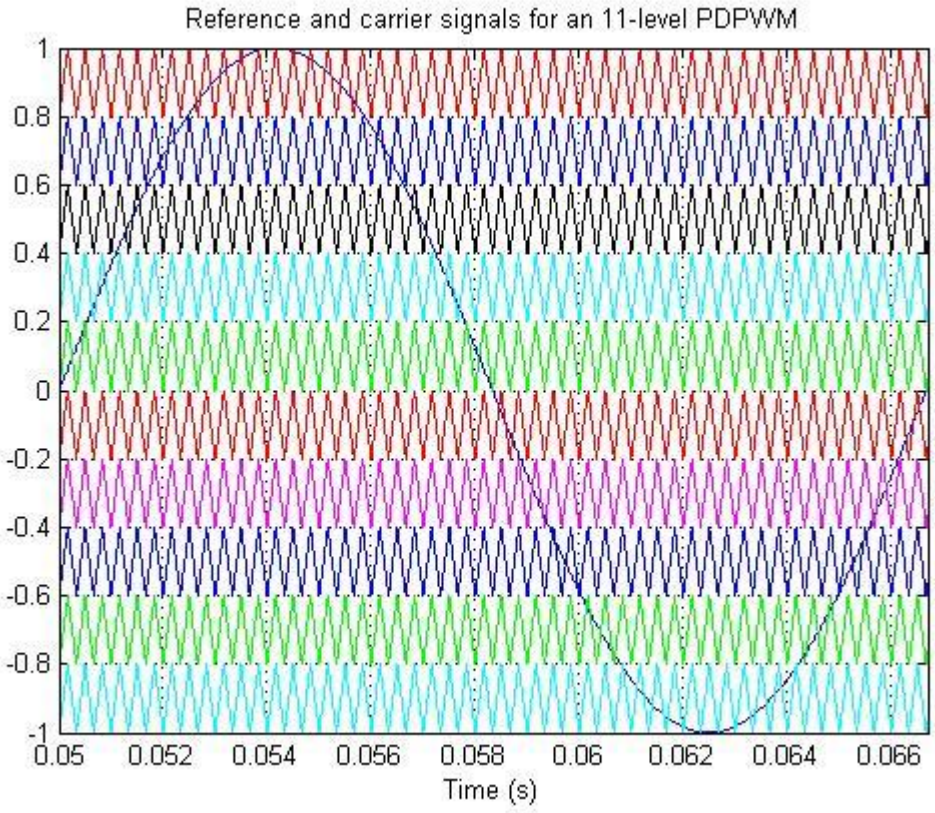
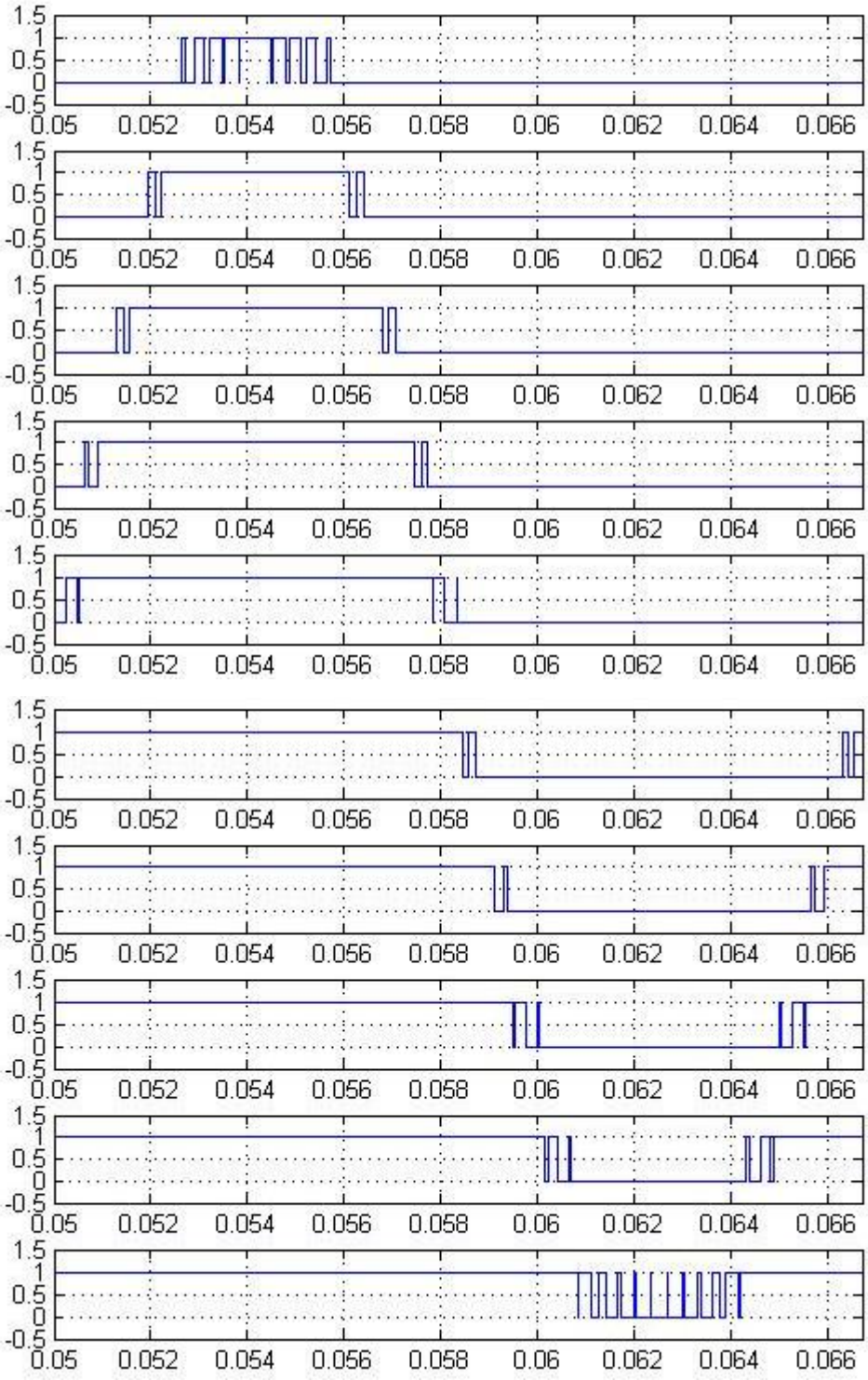
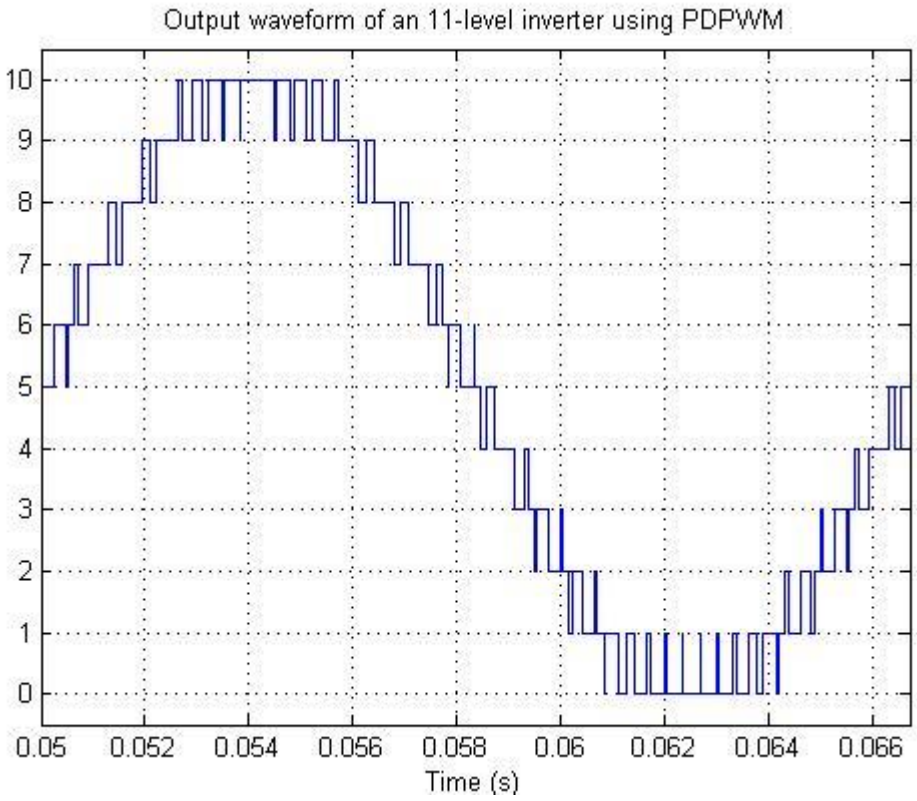


Figure 2.27 PDPWM technique for an 11-level inverter



(a)



(b)

Figure 2.28a) Comparison between the reference and carrier signals for an 11-level PDPWM, b) output voltage

The principle of phase opposition disposition (POD) is similar to PDPWM because, $n-1$ carrier signals with the same amplitude and frequency are used, where n is the number of voltage levels. In this case, carrier waveforms above the zero reference value are in phase. In this case carrier waveforms below are also in phase, but are 180 degrees phase shifted from those above zero[78].Figure 2.30 shows the POD technique for an 11-level inverter. In Figure 2.31(a), comparison between the reference and carrier is shown with a switching frequency of 3 kHz. The resulting output waveform for an 11-level inverter using POD modulation is shown in Figure 2.31(b).

In the alternative phase opposition disposition (APOD) modulation, every carrier waveform is out of phase with its neighbor carrier by 180'. In other words, this technique has carriers in alternative phases or in opposition. Figure 2.32 shows the APOD technique for an 11-level inverter. In Figure 2.33 shows the comparison between the reference and carrier, and the resulting output waveform for an 11-level inverter using APOD technique.

All three PWM techniques have identical structure with a primary difference being the way they generate output the symmetry. PD modulation has even symmetry, meaning that positive half-wave can be mirrored to negative half-wave. Unlikely, POA and APOD modulations have odd symmetry. The switching frequency of inverters using LSPWM modulation techniques is equal to the carrier frequency, while the average switching frequency of each single switch is equal to $(1/(n-1))$ of the carrier frequency.

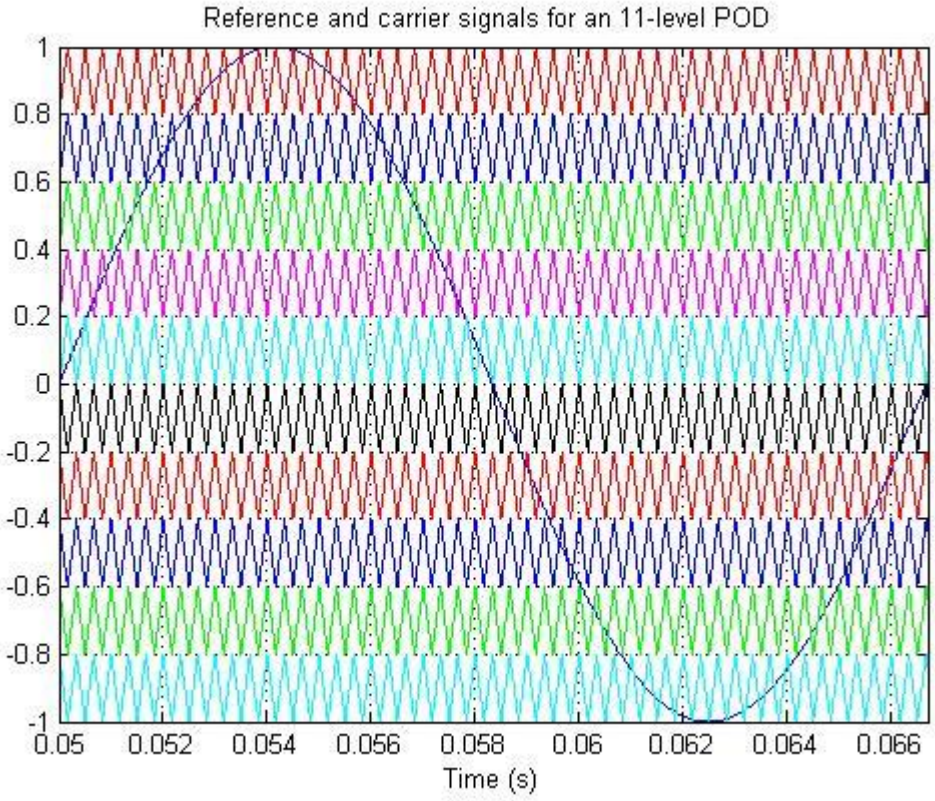
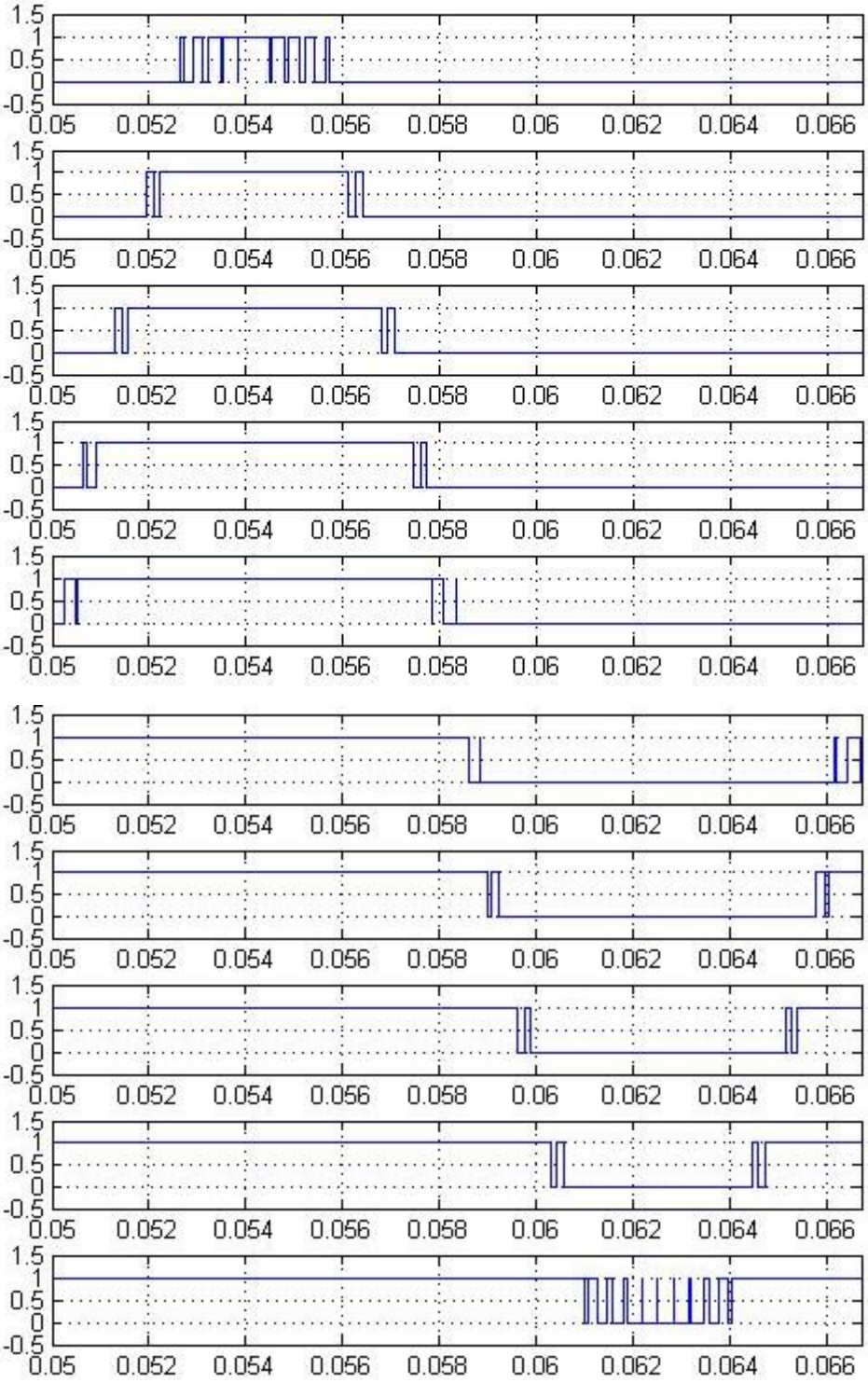
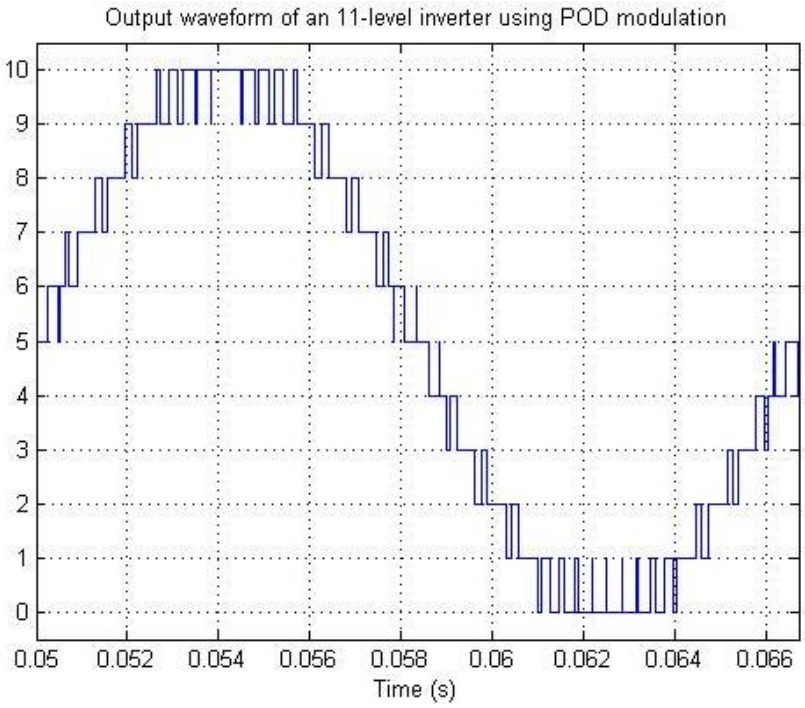


Figure 2.29 POD technique for an 11-level inverter



(a)



(b)

Figure 2.30a) Comparison between the reference and carrier signals for an 11-level POD, b) output voltage

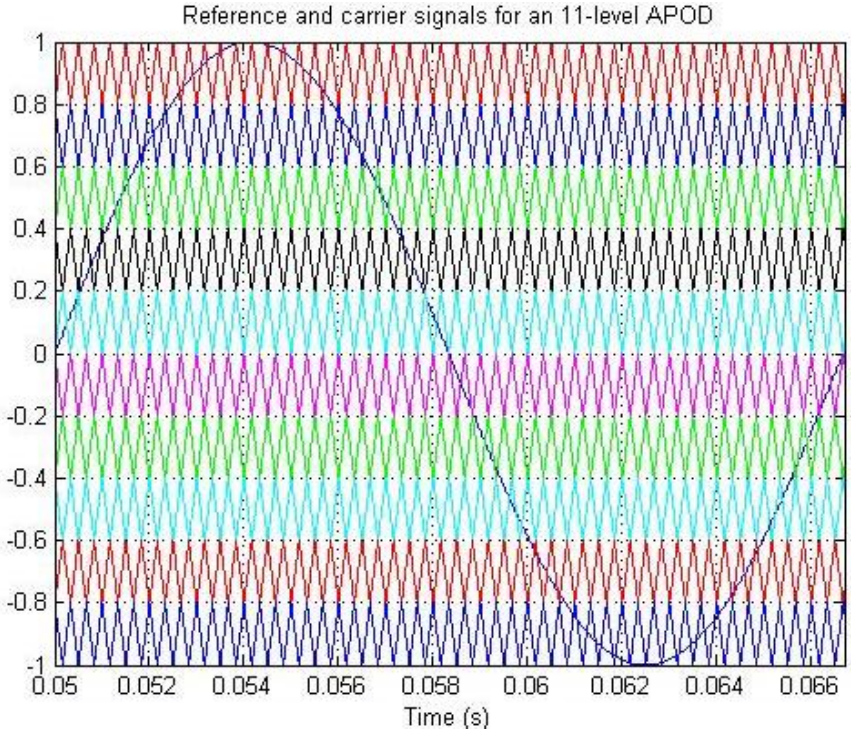
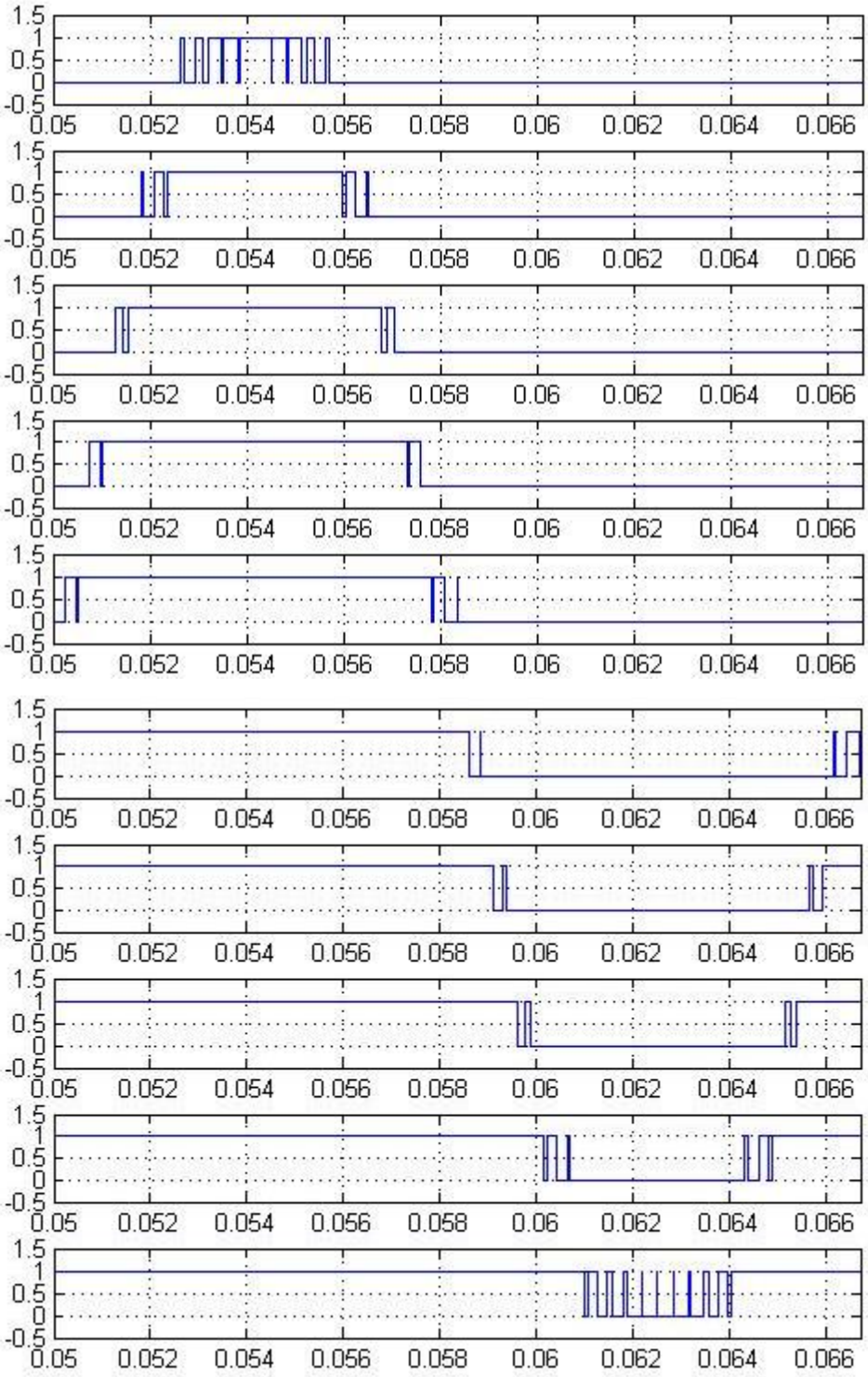
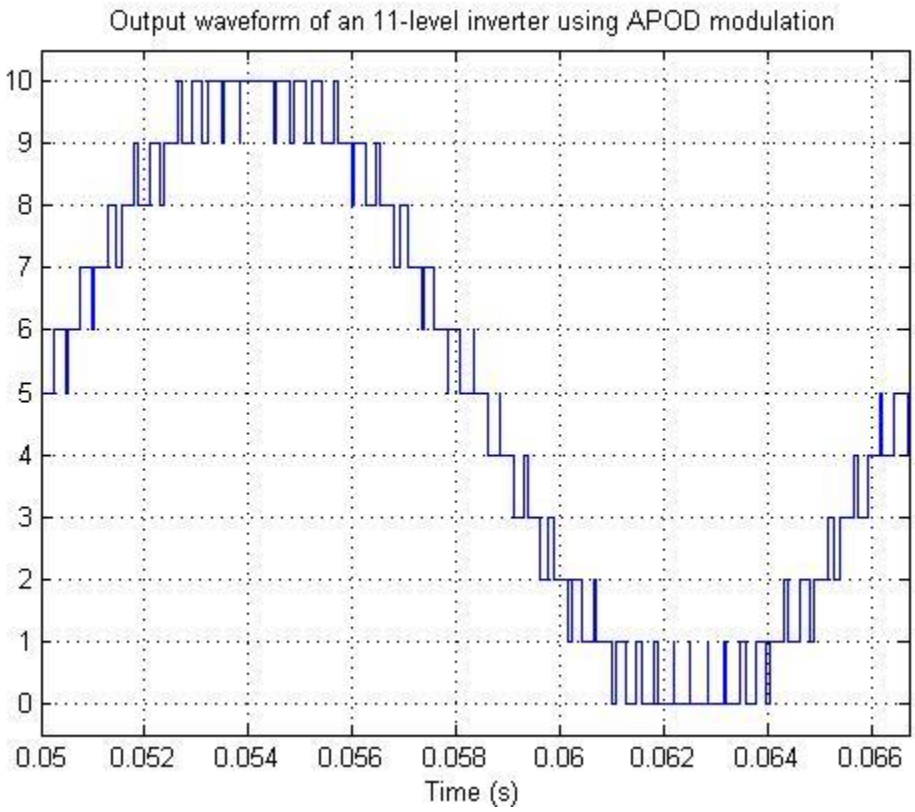


Figure 2.31 APOD technique for an 11-level inverter



(a)



(b)

Figure 2.32 a) Comparison between the reference and carrier signals for an 11-level APOD, b) output voltage

2.6 Summary

Many multi-level inverter topologies and modulation schemes have been developed to generate a stepped switched waveform which represents an arbitrary sinusoidal reference signal with adjustable amplitude, and frequency. The major challenge among all topologies and modulation schemes is to provide high power quality with minimum switching frequency. The PSPWM and LSPWM are derived from the carrier-based SPWM used for multi-cell (CHB and FC), and the NPC inverters, respectively [25].

The PSPWM technique introduces a synchronism in CHB and FC topologies by utilizing phase-shifted carrier signals to different cells of CHB and FC topology, thus generating the stepped waveform. Although, PDPWM has a better output voltage in terms of harmonic content, PSPWM technique is the only method that has found commercial implementation for CHB and FC topologies. Conversely, use of the LSPWM, including the PD, POD, and APOD technique, is

a straightforward way to switch gate signals of NPC converters, and, therefore, is one of two modulations schemes used in the industry. The SHE technique is another modulation scheme that has become commercial. Negative features associated with this scheme have limited it to low-dynamic-performance demanding drive applications. Several similar modulations, such as selective harmonic mitigation (SHM) or synchronized optimum PWM techniques have the same disadvantage as SHE, preventing them from being used for variable-speed applications. However, SHM produces a lower THD in grid-connected applications. Nevertheless, real-time (online) SHE methods have recently been introduced for grid-connections; however, it does not guarantee that grid codes are always met, irrespective of the modulation index and operating condition.

Despite the fact that multi-level topologies have more degrees of freedom than conventional 2-level topologies, such as more voltage levels and switching state redundancies, manufacturers still prefer to use classic PWM-based modulations because of their simplicity and proven performance, leading to less availability of new multi-level modulation schemes in industrial implementations. For instance, despite all positive developments in SVM-based techniques, they still have not been firmly established in industrial applications. Recently simpler way has been found that is able to generate identical voltage waveform of the most common SVM algorithms by using a single-phase modulator. Its advantages include the ability to easily extend to any number of levels with lower complexity than SVM algorithms.

One application of multi-level inverters pertains to power systems. Among all issues associated with power systems, power distribution control and management play a significant role. Flexible AC Transmission Systems (FACTS) devices have been introduced as a solution for improving power transfer in network grids. Static var compensator (STATCOM) is one of the most important members of FACTS devices. CHB and NPC have demonstrated the best performance for STATCOM applications. A comparison between these two topologies demonstrates that CHB has greater efficiency and dynamic performance while requiring a simpler control system; however, NPC topology possesses a higher range of operation. Currently, at least one manufacturer uses 3L-NPC for commercial STATCOMs. As previously mentioned, an MMC-based system called SVC plus has also found commercial implementation for STATCOM applications.

Multilevel converters are also offered in secure power management applications. In this area, a CHB-based converter with ability to interconnect different grids is introduced in[80].Another suitable field for multi-level converters is the train traction power conversion system. These applications require medium-voltage high-power range as well as very high performance over a wide range of frequencies up to high speed. Multi-level converters can generate a high-frequency output without increasing the average switching frequency. Moreover, utilizing multi-level converters eliminates the need for large, and heavy step-down transformers. A 3L-NPC topology has already been used for drive systems in [81]. Several other configurations for CHB and NPC topologies are proposed for this application. In addition, multi-level topologies have gained increasing attention for ship propulsion. NPC topology is a good choice for this purpose due to its improved power quality. Although electric vehicles (EVs) have greatly developed, multi-level topologies have not shown prominence in this area due to the low power range of this application. However, additional power quality and efficiency can lead to the use of multi-level topologies in this field. Nevertheless, NPC and ANPC topologies have been proposed for large electric hybrid EVs. This is a possible area for future development of multilevel converter technology.

Another application of multi-level topologies has been energy generation, conversion, and transmission, such as renewable energy productions. Recent grid codes require large energy conversion systems to control active and reactive power transfer. Because of the high demand for wind energy generation, including high power generation and transmission, multilevel converters offer a promising alternative. For instance, back-to-back 3L-NPC is the most related topology for this application due to its characteristics in working with the MPPT system. Currently, at least two manufacturers offer 3L-NPC back-to-back converters for wind power conversion.

The 5L-ANPC topology has also been proposed in back-to-back configuration for this area. In general, CHB, which requires multiple isolated DC sources, is not a proper choice for this purpose; however, some concepts have been proposed in order to use CHB. The principle of CHB for wind applications is based on the use of rectifiers fed from independent permanent magnet (PM) generators, providing required DC sources for H-bridges of CHB converters. This idea is especially useful for off-shore wind generation. On the other hand, the use of multilevel converters for photovoltaic (PV) grid-connected systems is becoming more important as the number of PV power plants is rapidly increasing. Today, conventional 2-level inverters are not

able to transfer power for megawatt grid-connected PV power plants. Multilevel converters can be used to interconnect PV systems in a more intelligent way in order to reach higher voltages. In this area, NPC- and CHB-based converters have been proposed to interconnect PV plants to primary networks.

Another recent application of multilevel converters is hydro-pumped energy storage. Currently, one manufacturer produces 3L-ANPC, which has been used for a 200-MVA hydro-pumped energy storage system [25]. Moreover, several multi-level converters have also been proposed as feasible solution for HVDC application, such as MMC topology which has recently entered the market and is produced by SIEMENSE. Moreover, this topology has been used for an HVDC-plus transmission system interconnecting two ac grids. In addition to MMC, NPC topology has also been proposed for HVDC transmission. Cascaded topologies, particularly CHB with unequal DC sources, are attractive choices for Class-D digital audio power amplifiers, because they have a low THD which improves audio quality while facilitating high-frequency filtering.

In general, multi-level converter developments have resulted in several commercial and proven technologies; however, several challenges still exist for further development in this area. Typically, manufacturers are eager to offer multilevel converters with lower average switching frequencies. The primary reason is to increase system efficiency, resulting in a simpler cooling system as well. Furthermore, lower order harmonics are produced if the device is working with lower switching frequencies. In other words, matching efficiency with high performance remains challenges for multi-level converter development. This challenge can be alleviated, however, higher-level topologies, which is why most new multi-level topologies utilize additional levels. In addition to this, switching losses can be modified through the modulation scheme for a given topology.

Another source of multi-level converter loss is conduction loss which must be considered. Therefore, multilevel topologies with the lowest components capable of sharing losses among the switches, in order to reach higher ratings, are more attractive. Moreover, generating lower harmonics must also be considered. One possible way to reduce harmonics is to utilize topologies with more voltage levels. Another important challenge for multi-level converters is reliability because the maintenance of a fully reliable, completely functional fault detection–diagnosis–operation system is still not practically feasible.

Some multi-level topologies use a simple structure, such as NPC, ANPC, and H-NPC, but need higher-rated components. Other topologies, such as CHB, FC, and MMC, have more complex structures but need lower rated components. Both configurations have distinct advantages and disadvantages, thus affecting the total cost of the converter, considering the nature of the application. Although semiconductor technology has seen a very fact development, additional research and development is expected to enhance switch performance as well as reducing the expense.

Another important challenge for multi-level converters is reducing the size and weight of the devices. Although many applications currently utilize multi-level converters, these topologies are expected to find more position in many other applications. Therefore, additional research is needed for the full deployment of multi-level converters in various fields such as FACTS, HVDC, and distributed generation systems.

Chapter 3 - Flexible AC Transmission Systems (FACTS)

3.1 Background

Power flow through an AC transmission line is dependent on several parameters, such as line impedance, magnitude of sending- and receiving-end voltages, and the phase angle between the two end voltages. This forces the AC transmission systems to use switched series and shunt reactive compensators, as well as voltage-regulating and phase-shifting transformer tap changers in order to adjust parameters to control the power transmission. In the past, these devices could not be adjusted with adequate speed to control transient or dynamic behavior of the transmission system. As a result, these devices were used only for steady-state control of power flow, requiring power systems to be operated well below their theoretical maximums in order to be able to recover from the transient faults. This forces power systems to forgo use of their full capacities and operate in under-utilized conditions. However, at the present time, power systems are forced to operate at almost full capacity.

A traditional way to reinforce the power grid is to upgrade the electrical transmission system infrastructure by adding new transmission lines, substations, and associated equipment. However, the process to construct new transmission lines is difficult, expensive, and time-consuming. This complication can be resolved if factors influencing power flow are be controlled under dynamic and transient conditions. As a result, power systems could more closely achieve their theoretical limits. This idea dates back to the 1960s but could not establish practical implementation because of lack of proper power switches [82]. Today, developments in semiconductor technology have made it possible to dynamically control the four power flow major parameters using solid-state switching devices. This has replaced mechanically switched devices with efficient, fast, and reliable semiconductor switches. The idea of high-speed controlling the major parameters was first presented in 1988 in order to increase availability, operating flexibility, and system stability. [83] proposed two basic practical methods to control power flow parameters. The first approach was to utilize fast switching devices with the traditional compensation devices, such as series and shunt capacitors, and the second idea was to perform the control by using advanced power electronics-based devices. The second approach has presented the concept of flexible AC transmission systems (FACTS).

In general, FACTS systems include a group of power electronic devices developed to perform the same functions as traditional power system controllers, such as transformer tap changers, passive reactive compensators, synchronous condensers, etc. [84]. These devices control all parameters that influence active and reactive power transmission. Therefore, system performance can be considerably improved by controlling power flows without generation rescheduling or topological changes. Moreover, thermal limits are not violated, losses are minimized, and the stability margin is increased. This technology replaces mechanical switches used in power systems by fast semiconductor switches required for dynamic and transient conditions without limiting number of control actions, allowing faster response times. [85]. The IEEE P1409 has defined the FACTS as "Alternating Current Transmission Systems incorporating power electronics-based and other static controllers to enhance controllability and power transfer capability." FACTS has been increasingly developed throughout the past decades. It is currently a well-known and recognized technology in power systems and widely used as an interesting tool to control and stabilize power transmission systems. However, FACTS technology is much more expensive as compared to the traditionally mechanical technology.

3.2 Overview

The development of FACTS began with the growing capabilities of power electronic components. The overall starting points are power grid components affecting reactive power or the impedance of a part of the power system. Figure 3.1 shows a number of basic devices separated into conventional and the FACTS devices. In the right-side of the Figure, the term "dynamic" is used to state the fast controllability of devices provided by power electronics and the term "static" refers to devices, such as mechanical switches, that have no moving parts with which to perform dynamic controllability. In the left-side of Figure 3.1, conventional devices including fixed or mechanically switchable components such as resistance, inductance, or capacitance are shown. FACTS devices also utilize these elements, but power electronics circuits are used to switch elements in smaller steps. The left side of FACTS devices uses Thyristor valves or converters which have low losses because of low switching frequency or the usage of Thyristors in order to bridge valve impedance [86]. The right column of FACTS devices includes advanced technology of voltage source converters (VSCs). The advantage of using VSCs is that they generate a controllable output voltage in magnitude and phase containing low harmonics.

The primary disadvantage of VSC-based compensators is that, with increasing switching frequency, losses also increase.

In general, FACTS devices can be categorized in three groups including shunt, series, or shunt and series. Shunt devices are for reactive power compensation and therefore voltage control. When compared to mechanically switched devices, the SVC generates a smoother and more precise control which enhances power grid stability. EEE defines static VAR compensator (SVC) as a shunt connected static VAR generator or Absorber. SVC output can be adjusted in such a way as to exchange capacitive or inductive reactive power. SVCs were first developed in the late 1960s to compensate for large fluctuating loads such as electric arc furnaces. SVCs include Thyristor-switched capacitors (TSC), and Thyristor-controlled reactors (TCR) with fixed filters to control capacitive/inductive reactive power and harmonic filtering. One disadvantage of SVCs is that these systems can produce harmonic current issues while compensating reactive power, thus requiring constant shunt filters or special transformer connections. Figure 3.2 shows different types of SVC devices [87].

As compared to SVC, STATCOM has an additional advancement that is capable of improving the power quality even against dips and flickers. On the other hand, series reactive power compensators can affect the stability and power flow of power lines by changing the effective line impedance. Various series compensators are protected with a Thyristor-bridge. In fact, TCSC is used for stability improvement purposes; however, it is capable of affecting power flow. The SSSC is not currently utilized for transmission level since TCSC performs all transmission system requirements with lower cost. VSCs can also be used in series applications in order to improve power quality issues on distribution systems. These series compensators are called dynamic voltage restorer (DVR) or static voltage restorer (SVR). Power flow control devices, such as phase shifting transformers (PSTs), shift power flows from overloaded regions to areas with free transmission capability. In addition to series and shunt FACTS device, another family of devices called hybrid (series and shunt), are present. The unified power flow controller (UPFC) provides power flow control along with independent voltage control. The complex structure of UPFC makes it an expensive device, thus causing major drawback for the use of this application. Interline power flow controller (IPFC) and generalized unified power flow controller (GUPFC) are complex devices derived from UPFC in order to provide power flow controllability in more than one line starting from the same substation. Dynamic power flow controller (DFC) is

a FACTS device with a simpler setup than UPFC and dynamic power flow ability. Finally, HVDCs have full dynamic controllability over transmission systems.

Several other FACTS devices such as series dynamic breaking resistor (SDBR), Thyristor-controlled phase angle controller (TCPAR), etc., exist in such a way that each device greatly contributes to specific applications. Table 3.1 provides an overview of current FACTS devices [60].

Among all FACTS devices, VSC-based compensators are one of the most well-known families. These compensators are the focus of the next section.

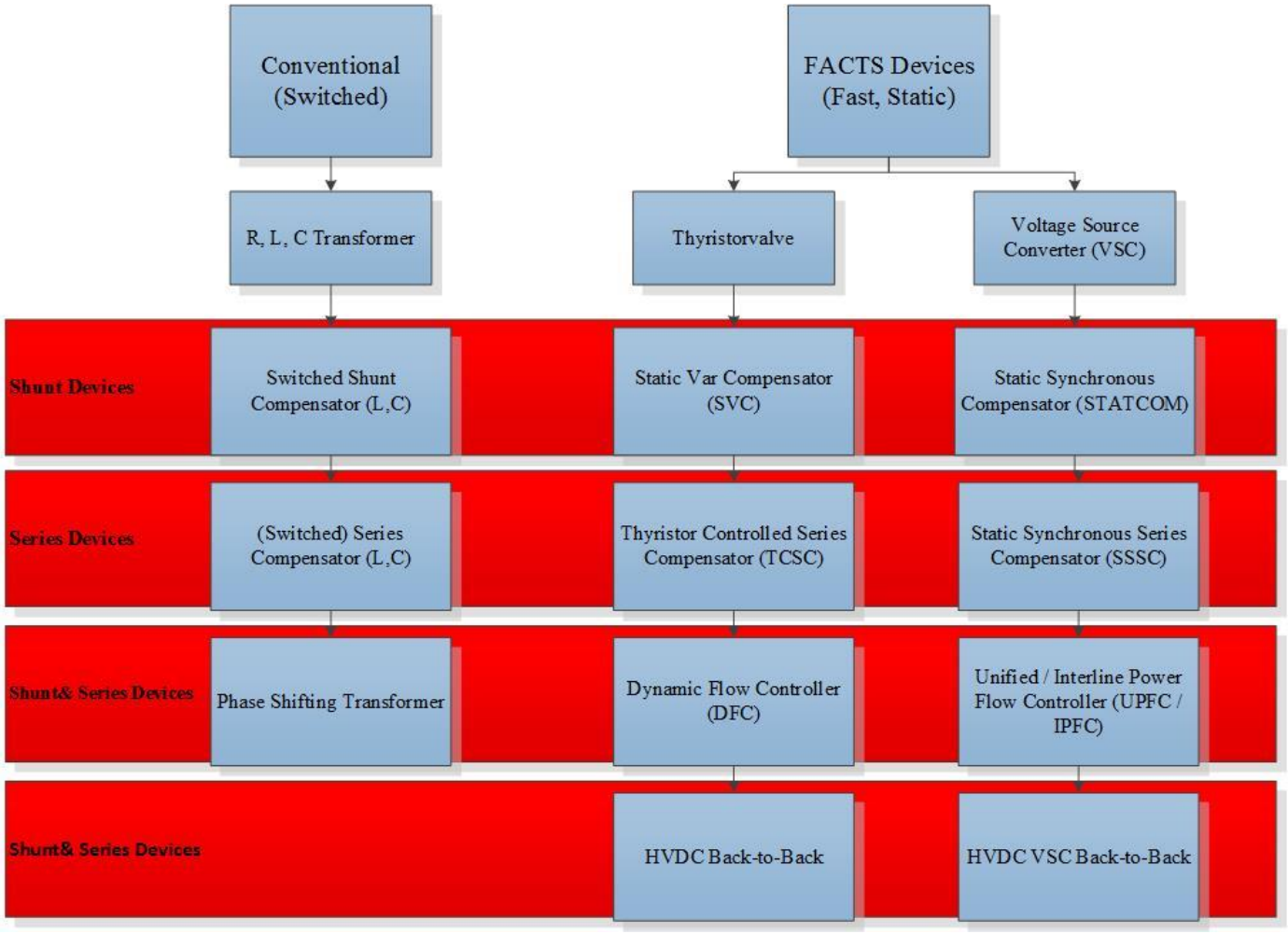


Figure 3.1 Overview of main FACTS devices

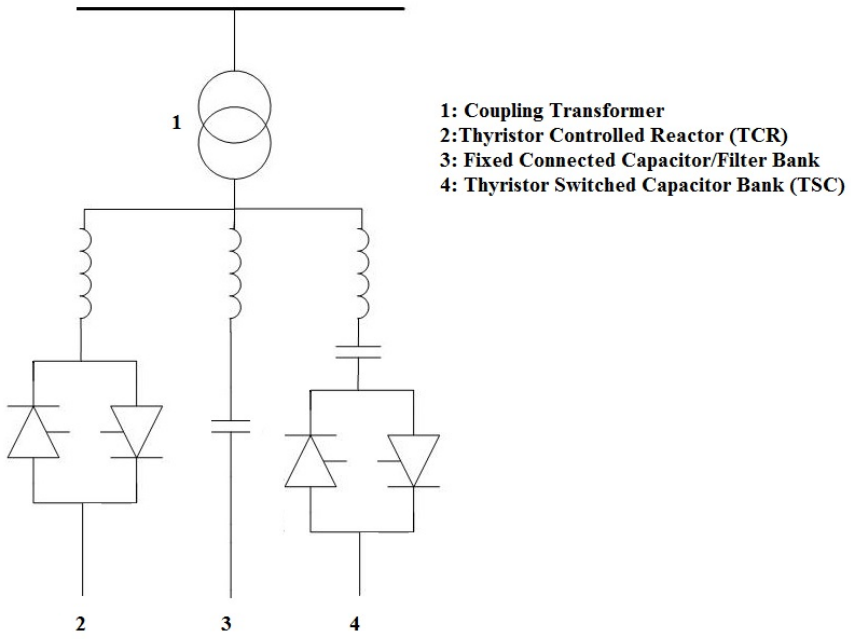


Figure 3.2 Different types of SVC devices

Table 3.1 Overview of major current FACTS device [60]

FACTS	**STATCOM**	**SSSC**	**DVR**	**UPFC/IPFC**	**HVDC**	**TCSC**	**SVC**
Degree of Freedom	1	1	1	3	3	1	1
Shunt	YES	NO	NO	YES	YES	NO	NO
Series	NO	YES	YES	YES	YES	YES	YES
Shunt & Series	NO	NO	NO	YES	YES	NO	NO
VSC	YES	YES	YES	YES	NEW	NO	NO
Thyristor	NO	NO	NO	NO	OLD	YES	YES
Active Power Control	NONE	NONE	NONE	HIGH	HIGH	NONE	NONE
Reactive Power Control	HIGH	HIGH	HIGH	HIGH	HIGH	MED	HIGH
Power Flow Control	LOW	HIGH	HIGH	HIGH	HIGH	NONE	MED
Cost	MED	MED	MED	HIGH	HIGH	LOW	LOW

3.3 VSC-based compensators

This family of FACTS devices utilizes voltage source inverters in order to insert a near-sinusoidal AC voltage waveform into the power systems. Three primary members in this category include the static synchronous series compensator (SSSC), static synchronous compensator (STATCOM) and unified power flow controller (UPFC). The, UPFC is the combination of the first two devices. These devices control several essential factors affecting active and reactive power flow, in a power system.

3.3.1 Static synchronous series compensator (SSSC)

The static synchronous series compensator (SSSC) is an inverter-based series compensator first introduced in [88]. The SSSC applies AC voltage into the transmission line at the synchronous frequency through a series injection transformer. This applied voltage can affect power flow on the line. The device controls the magnitude and angle of the injected voltage, depending on its mode of operation [82]. In this device, a Thyristor protection is necessary due to the low overload capacity of the semiconductors, especially when IGBTs are used. The voltage source converter plus the Thyristor protection makes the device more complex and costly than other series FACTS device. However, this combination does not present better performance of transmission systems. Figure 3.3 shows the SSSC structure. Two modes of operation for the SSSC include line impedance emulation mode and direct voltage injection mode [89].

3.3.1.1 Line impedance emulation mode

In line impedance emulation mode, also referred to as "constant reactance mode" or "X_c-controlled SSSC," the SSSC injects a lagging voltage in series with the transmission line. This emulates a capacitive reactance in which voltage lags the current emulating a capacitive reactive voltage drop. However, in practice, the voltage V_c is not in quadrature with the current which generates a small amount of real power to compensate for inverter losses. The voltage V_c can be shown as:

$$V_c = kIe^{-j\frac{\pi}{2}} \tag{3.1}$$

where I is the line current phasor, and k demonstrates the degree of series compensation [90]. Changing k from zero to k_{max} allows for control of the applied voltage, thus causing the reactive compensation to operate similarly to a conventional series capacitive reactance [91]. k can be written similarly to the ohmic magnitude of a series capacitor as:

$$k = \frac{|V_c|}{|I|} \tag{3.2}$$

This implies that the operation of an SSSC is similar to a classic series capacitive reactance [82] in which capacitive reactance varies by changing the term k. In an SSSC, capacitive reactance can be controlled quickly as the amplitude of the applied voltage, V_q, can vary rapidly.

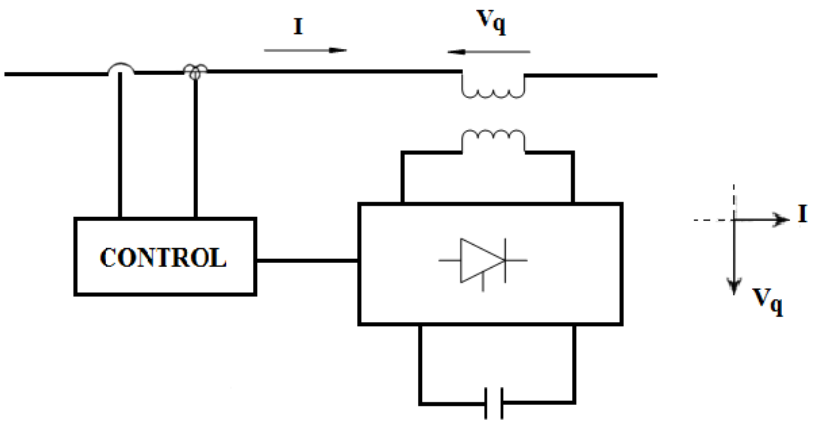


Figure 3.3 Schematic of the SSSC

3.3.1.2 Direct voltage injection mode

This mode of operation, sometimes referred to "constant quadrature voltage mode" or "V_c-controlled SSSC", inserts a series voltage independent of the current. In other words, the applied voltage has no direct magnitude relationship with the line current, implying that the voltage is capacitive in nature. In this mode of operation, unlike the previous mode, the SSSC does not act similarly to a conventional capacitive reactance, but the magnitude of applied voltage is used indirectly, such as the utilization of applied voltage in a closed loop control system.

3.3.2 Static synchronous compensator (STATCOM)

Static synchronous compensator (STATCOM), sometimes referred to advanced static VAR compensator (ASVC) or static condenser (STATCON), is a shunt-type inverter-based compensator possessing similar components to an SSSC [92]. STATCOM provides reactive compensation by injecting a variable magnitude near-sinusoidal current signal at the point of connection. The amount of reactive power transfer can be determined by the voltage difference of the STATCOM and power grid. The inverter output voltage is relative to its DC link voltage. If the DC link voltage is increased, implying an increase in the STATCOM's AC voltage, the reactive power flows from the inverter to the grid and vice versa. When the DC link voltage of the inverter is decreased, translating to a reduction in output AC voltage of the STATCOM, the reactive power transfers from the grid to the inverter. These two operations are similar to the over-excited and under-exited behavior of a synchronous generator, respectively. The amount of active power transfer is also governed by the phase angle between the inverter and the power

grid [91]. Figure 3.4 shows the schematic diagram of an STATCOM. STATCOMs operate in two modes of reactive power compensation: VAR control mode, and Automatic voltage control mode [89]. STATCOM is the primary focus of this.

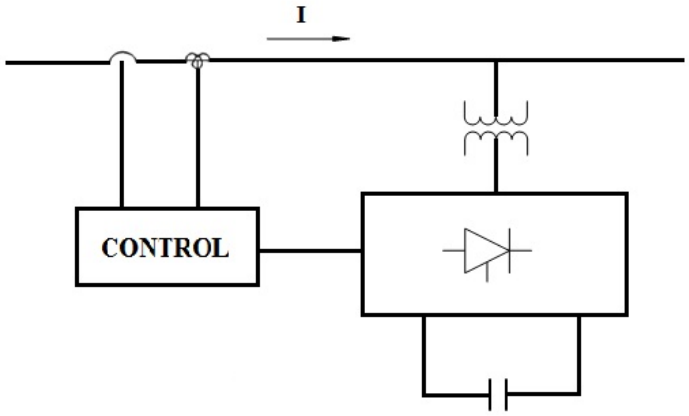


Figure 3.4 Schematic of the STATCOM

3.3.3 Unified power flow controller (UPFC)

An SSSC or STATCOM can only generate reactive power compensation when working in stand-alone mode. In stand-alone mode operation, these two devices cannot exchange active power except the required amount for internal power losses. This problem can be solved by combining these two devices, thus creating a larger device called unified power flow controller (UPFC). Therefore, the SSSC and STATCOM share a common DC link capacitor which can be controlled by the STATCOM. Moreover, the STATCOM enables shunt reactive current exchange with the power line [91]. The SSSC portion of the UPFC can exchange both active and reactive power with the transmission line. The net active power absorbed by the UPFC from the transmission line is equal to internal losses of the series and shunt inverters and corresponding coupling transformers [82]. In this way, the UPFC can act identical to an AC-to-AC converter in which active power flows bi-directionally through the device, and reactive power is controlled independently by the STATCOM or the SSSC [93].

In UPFC, the SSSC portion can operate in three modes of operation. The first two modes are identical to the regular SSSC which are “line impedance emulation mode” and “direct voltage injection mode.” Another operation mode which is “automatic power flow control mode” [89]. In this mode of operation, the SSSC is able to control active and reactive power flow independently. In this case, the UPFC is most advantageous compared to other conventional

compensators because it provides real-time control over all basic power system parameters [82]. Figure 3.5 shows the schematic of a UPFC.

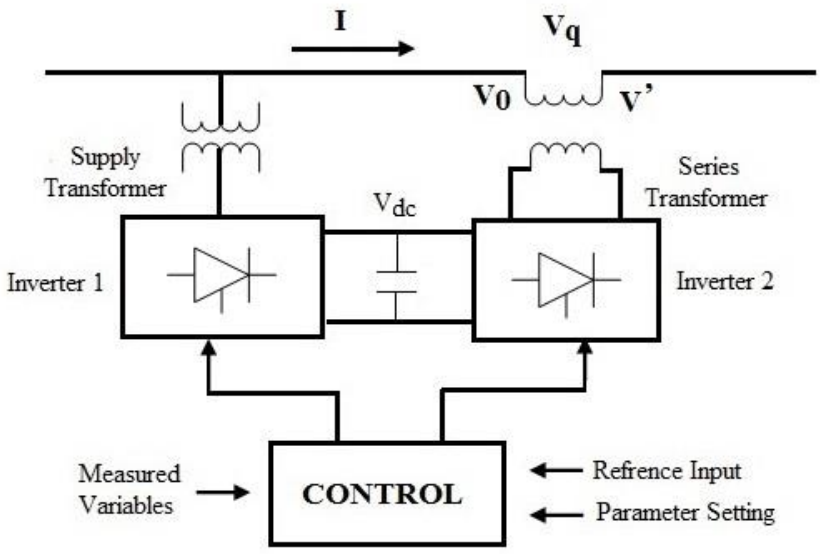


Figure 3.5 Schematic of the UPFC

Typically, in a UPFC, the SSSC operates in the last operation mode, automatic power flow control mode, and the STATCOM operates in the "automatic voltage control mode" [89], which enables power systems with maximum active power transmission as well as minimum reactive power flow.

3.4 STATCOM

The idea of directly generating controllable reactive power by switching power converters, without the use of AC capacitors or reactors dates back to 1976 [87]. The operation of these converters is similar to synchronous condensers. Synchronous condenser is an ideal synchronous machine connected to a power grid and working in no load conditions, in which reactive power is varied by changing field current. However, the use of synchronous condenser cannot guarantee control of reactive power for fast load changes. Switching converters can also transfer active power with the AC system if supplied from a DC source. Their structure, which is similar to a rotating synchronous generator, makes them to be known as static synchronous generator (SSG). If the active energy source is replaced by a DC source which is not able to absorb or inject active power, such as a DC capacitor, SSG becomes a static synchronous compensator (STATCOM) [87]. In other words, STATCOM acts like a source or sink of reactive power by using power electronic converters. These converters compensate the reactive power by producing controllable

voltage and current waveforms at the output terminals instead of using capacitor or reactor banks. However they typically take advantage of output LC filters in order to cancel switching frequency harmonics. In a STATCOM system, reactive power compensation is defined by the switching power converter independent of supply voltage fluctuations, while in traditional compensation systems, reactive power compensation is directly determined by capacitors or reactors. Figure 3.6 shows the V-I characteristic of a STATCOM system [94].

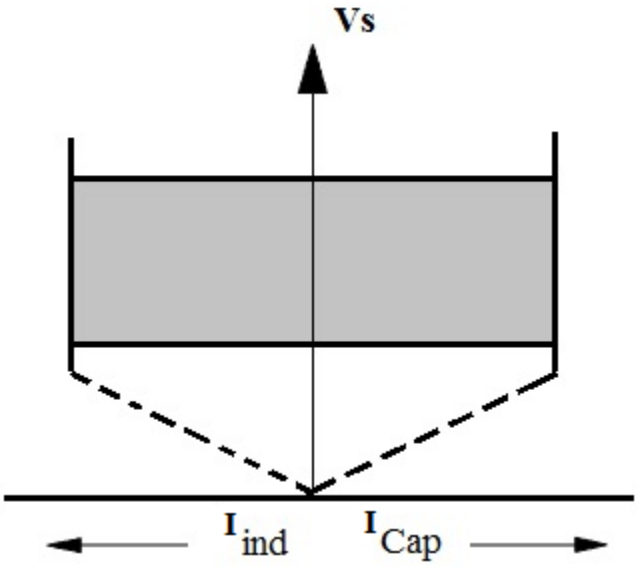


Figure 3.6 V-I characteristic of the STATCOM

STATCOMs can be divided into two types of transmission STATCOMs and distribution STATCOMs (D-STATCOMs). Power ratings of transmission STATCOMs is typically high, such as 20-100MVAR, while switching frequencies are low. Transmission STATCOMs usually utilize high-power low-speed semiconductors such as integrated gate commutated Thyristor (IGCT), gate turn-off Thyristor (GTO), and high voltage insulated-gate bipolar transistor (HV-IGBT). The function of these devices is to perform reactive power compensation as well as supply voltage support to transmission systems. D-STATCOMs (up to 5MVAR) are installed in distribution systems to enhance the system power factor (PF) in addition to voltage regulation. Their switching frequency and response time is shorter than transmission STATCOMs. These devices take advantage of faster IGBTs, or IGCTs. Typical applications of STATCOM are voltage regulation and control, improvement of steady-state power transfer capacity, improvement of transient stability margin, damping of power system oscillations, damping of sub-synchronous power system oscillations, flicker control, power quality improvement, and distribution system applications. STATCOMs have identical capabilities as SVCs but with

higher control bandwidth. The primary advantage of the STATCOM over Thyristor-type SVC is that the compensating current does not depend on the voltage level of the connecting point and thus the compensating current is not lowered as the voltage drops. This is an important aspect because of new standards requiring applications, such as wind turbines, to supply reactive power variably depending on power grid demand and actual voltage level. However, the most relevant feature of the STATCOM is its capability to increase the transient stability margin by injecting a controllable reactive current independent of the grid voltage [95]. The following section presents a brief literature review of transmission and distribution STATCOM applications extracted from [87].

3.4.1History of STATCOMs

The first practical implementation of STATCOM dates back to two decades ago, in which a 100 MVAR system at the TVA Sullivan substation able to perform leading or lagging compensation was installed in order to regulate the bus voltage. Later on, the American Electric Power (AEP) performed a two-part UPFC project at the Inez Kentucky station which with two ±160 MVA inverters. In the first part, the inverter was installed in shunt and in the second part the inverter was installed in series to operate jointly as a UPFC. In 1997, a ±2 MVAR D-STATCOM was developed by EPRI and Westinghouse for BC-Hydro Company to be installed on a 25 kV bus bar. The aim of this project was to mitigate sawmill-generated voltage flicker causing disturbance on the 26 KV feeder. This project was followed by a join project in 1999 by Henan electric power company and Tsinghua University to develop a 20 MVA STATCOM to be installed on a 220 kV system in order to enhance the stability of power transmission system. After this study, the utilization of STATCOMs expanded to Europe. In the UK, Areva developed a ±75 MVAr STATCOM system for UK National Grid to be installed on a 275 kV /400 kV power grid. Toshiba and Mitsubishi Transmission and Distribution (TM T&D), Fuji Electric, Tubitak-Uzay and several other manufacturers also designed and developed transmission and distribution STATCOM systems in order to mitigate voltage flicker problems, improve power quality, and perform reactive power compensation on power transmission and distribution systems. Figure 3.7 shows a commercial STATCOM system, called PCS100 technology, manufactured by ABB. This system consists of six 4.5 MVAR STATCOM units [96].

Figure 3.7 PCS100, a commercial STATCOM system manufactured by ABB [96]

3.4.2 Operating principles of a VSC-based STATCOM system

The static synchronous compensator (STATCOM) is a shunt connected reactive compensator capable of generating or absorbing reactive power. The STATCOM output can be regulated in such a way as to maintain control of specific parameters of the power system. This compensator is based on the voltage source inverter/converter (VSI or VSC) utilizing fast switching semiconductor components, enabling rapid controllability on the magnitude and phase angle of output voltages. A STATCOM system typically consists of a step-down transformer, a GTO- or IGBT-based VSC, and DC capacitors. The VSC (or VSI) is the building block of a STATCOM and many other FACTS devices. The primary goal of a VSC is to generate an AC voltage from a DC voltage, so that it is often referred to as a DC-AC converter or inverter. It must generate a symmetric AC voltage with a desired magnitude and frequency. The voltage difference across the transformer leakage reactance in addition to power line reactance (known as leakage reactance) produces reactive power transfer between the STATCOM and the power system. The STATCOM function is to regulate the AC voltage at the bus bar to improve the voltage profile of the power system. Moreover, it can be used to enhance power system oscillation stability [97]. Figure 3.8 demonstrates a schematic of a one-line diagram of a STATCOM system.

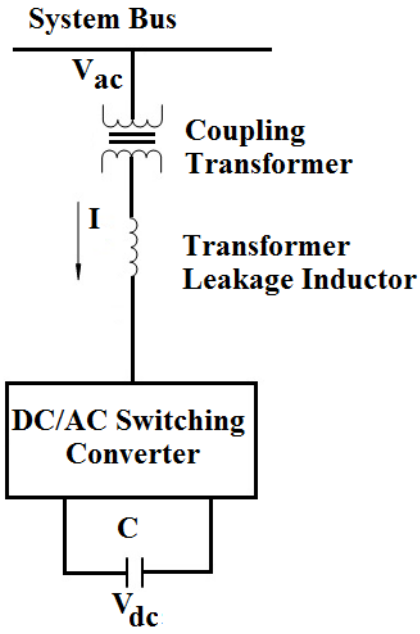


Figure 3.8 One-line diagram of a STATCOM system

The VSC generates a controllable AC voltage before reactance (actually transformer's leakage reactance added to the line reactance). In terms of active power exchange, if the STATCOM has a DC source, such as a DC capacitor, on its DC side, it is able to inject active power to the grid. The active power transfer can be controlled using the phase angle difference between the STATCOM terminals and the power system. When the phase angle of the power grid lags the phase angle of the inverter, the STATCOM injects active power from the grid. Unlikely, if the phase angle of the power system leads the phase angle of the inverter, the STATCOM absorbs active power from the power grid [98],[99]. In terms of reactive power exchange, three operating conditions are: 1) if the grid voltage is lower than the output voltage of the inverter, the grid recognizes the STATCOM as a capacitance connected to its terminals, 2) if the grid voltage is higher than the output voltage of the inverter, the grid recognizes the STATCOM as an inductance connected to its terminal, 3) if these two voltage are equal, there is no reactive power transfer between the two sources.

Static compensators are devices able to generate and absorb reactive and active power, but the most common applications occure in reactive power exchange between the AC power system and the compensator. As previously mentioned, the reactive power exchange between the power grid and the STATCOM is controlled by adjusting the magnitude of the fundamental component of the VSC output voltage higher or lower than the power grid voltage. Moreover, control of the

active power transfer is achieved by small variations in the switching angle of the semiconductor devices. Therefore, the fundamental component of the VSC output voltage is forced to lag or lead the AC system voltage by a few degrees, thus causing active power flow in or out of the inverter and modifying the value of the DC capacitor voltage. Theoretically, active power provided by the DC capacitor is zero, if the compensator exchanges only reactive power. Practically, however, a small amount of active power is required to compensate internal losses of the inverter.

3.4.3 Main components of a VSC-based STATCOM system

Figure 3.9 shows a simplified single phase schematic of a STATCOM system. A VSC-based STATCOM system usually includes a transformer, voltage-source converter, leakage reactance, and DC capacitor.

Typically, the VSC is connected to the power system via a step-down transformer. Usually STATCOMs or D-STATCOMs are connected to high voltage power systems in order to mitigate the undesired aspects of the power systems. Therefore, the primary function of this transformer is to level-down the voltage of the grid to a suitable voltage applicable to the VSC; however, this transformer increases compensating current on the STATCOM-side which can increase power losses associated with leakage reactance (Leakage inductance of the transformer added to the inductance of the power lines).

The voltage-source converter or inverter (VSC or VSI) is the most important block of a STATCOM system. This VSC can utilize a two-level conventional topology or a multi-level topology. The major objective of a VSC is to generate a sinusoidal AC voltage with minimal harmonic distortion from a DC voltage, such as a DC capacitor.

Leakage inductance (simply reactance) is a key component in a VSC to permit continuous and independent control of active and reactive power. The main purposes of the converter reactor are: 1) to provide low-pass filtering of the VSC output waveform in order to cancel out undesired harmonics made by the converter (inverter) switching frequency, 2) to provide active and reactive power control, 3) to limit short-circuit currents.

In addition to leakage inductance, an output filter may minimize the output voltage and current harmonics. This filter can be a single inductor or a second-order LC filter depending on the harmonic content of the output waveform. The rating of output filters depends on

performance requirements and magnitude of the harmonics, but a typical filter for a two-level conventional converter is approximately 10% to 30 % of the rated power. This value can be lower for a multi-level inverter since they produce lower harmonic content [100].

Another significant component of a STATCOM system is the DC capacitors serve as an energy storage device that supports the DC voltage. Another primary function of the DC side capacitor is to provide a low-inductance path for the turned-off current. These capacitors also reduce the harmonics ripple on the direct voltage.

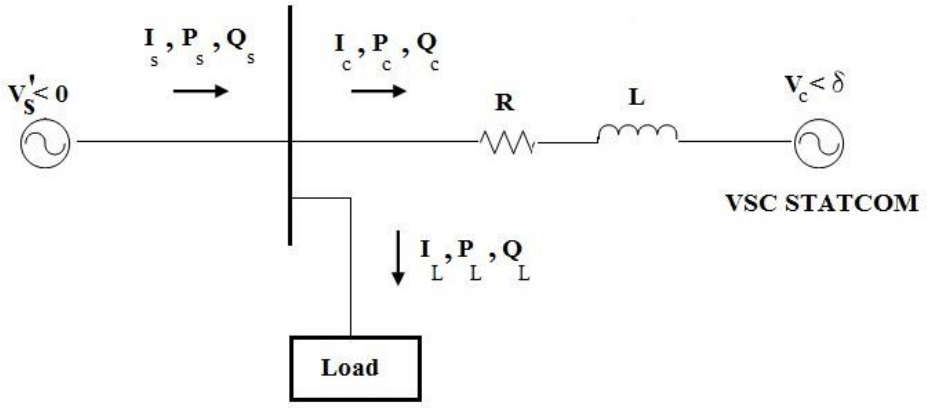


Figure 3.9 Simplified model of the STATCOM

Figure 3.10 illustrates the typical layout of a STATCOM substation used for voltage compensation of AC transmission lines. The numbered boxes in the figure are identified below.

1. *"STATCOM main building: contains converter valves, control and protection systems, and DC capacitors*
2. *Energy storage building (optional)*
3. *Line inductors*
4. *Heat exchanger and cooling system*
5. *Three-phase, step-down transformer*
6. *AC high-voltage equipment"*

[101]

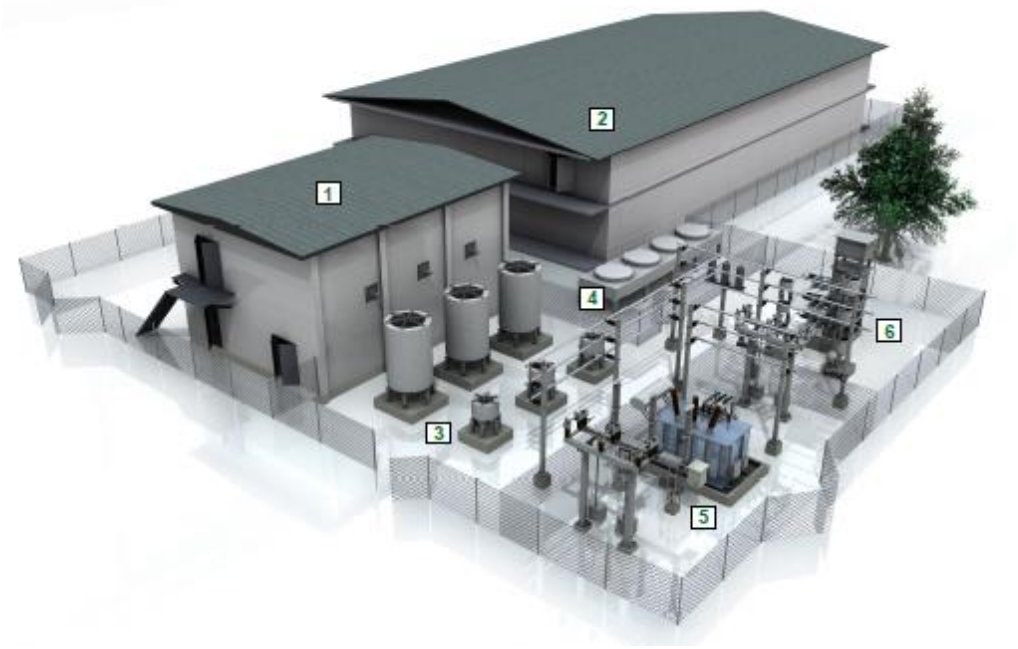


Figure 3.10 Typical layout of a STATCOM substation [101]

3.4.4 Power flow in a VSC-based STATCOM system

This section is extracted from [87] in which a theoretical explanation of STATCOM operation modes is presented. In Figure 3.9, As previously mentioned, a schematic diagram of a STATCOM is presented, where V_s' is the RMS value of the grid voltage with a zero phase angle referred to STATCOM-side, V_c is the RMS value of the STATCOM fundamental voltage, Q_s is the source reactive power, Q_c is the compensator reactive power, Q_L is the load reactive power, δ is the phase angle between the voltage of grid and compensator, R and L are the equivalent total resistance and inductance between the STATCOM and the power grid. The phasor diagram for Figure 3.9 is given below.

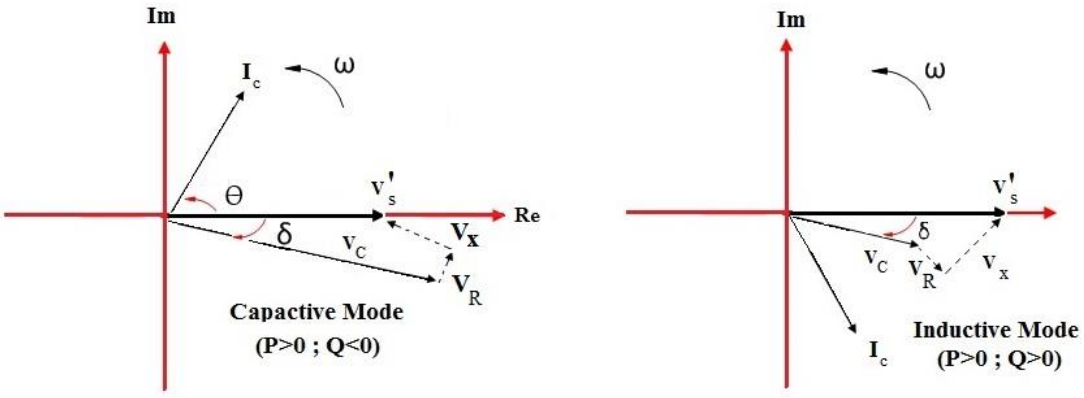


Figure 3.11 Phasor diagram for lossy system

As previously demonstrated in Figure 3.9, active and reactive power consumed by the STATCOM from the AC power grid can be presented by:

$$P_c = V_s' I_c cos\theta$$

$$Q_c = V_s' I_c sin\theta \quad (3.3)$$

The above equations assumes that power flows from the grid to the STATCOM, and the STATCOM input current lags the AC supply voltage by θ. Using Kirchoffs voltage equations for the STATCOM shown in Figure 3.9 results in:

$$\bar{V}_s' = \bar{V}_c + \bar{V}_R + \bar{V}_X \quad (3.4)$$

where:

$$\bar{V}_X = jXI_c$$

$$\bar{V}_R = RI_c$$

$$X = 2\pi fL \quad (3.5)$$

Substituting (3.5) in (3.4) and using Real-Imaginary plane yields:

$$V_s - V_c cos\delta = XI_c sin\theta + RI_c cos\theta = I_c(Xsin\theta + Rcos\theta)$$

$$V_c sin\delta = XI_c cos\theta - RI_c sin\theta = I_c(Xcos\theta - Rsin\theta) \quad (3.6)$$

Solving active and reactive power Equation (3.3) using above equations results in:

$$Q_c = V_s I_s sin\theta = V_s \frac{V_s - V_c cos\delta}{Xsin\theta + Rcos\theta} sin\theta$$

$$P_c = V_s I_c cos\theta = V_s \frac{V_c sin\delta + RI_c sin\theta}{X} \quad (3.7)$$

The above equation can also be expressed as:

$$P_c = \frac{V_s'}{X}\left[\frac{RV_s'sin\theta + XV_csin\theta sin\delta - RV_csin\theta sin\delta + RV_ccos\theta sin\delta}{Rcos\theta + Xsin\theta}\right]$$

$$Q_c = V_s'\frac{V_s' - V_c cos\delta}{Rcos\theta + Xsin\theta}sin\theta \quad (3.8)$$

Theoretically, no power loss occurs in an ideal system, resulting in no active power transfer. As a result, for an ideal STATCOM system, active power should be equal to zero implying that δ is equal to zero. In this case, STATCOM voltage is in phase with the AC power system and the current is purely reactive. Consequently, the above active and reactive power equations for a lossless STATCOM system becomes:

$$P_c = 0$$

$$Q_c \cong V_s\frac{V_s - V_c}{X} \quad (3.9)$$

Figure 3.12 shows phasor diagrams for an ideal lossless STATCOM system.

In an ideal STATCOM system if V_c is lower than V_s', the induced current lags V_X (and also V_s'), and the power grid recognizes the STATCOM as an inductance. In this case, the STATCOM operates in inductive mode, absorbing reactive power from the AC power system. Unlikely, if V_c is higher than V_s', the induced current lags V_X (but leads V_s'), and the power grid recognizes the STATCOM as a capacitance. In this case, the STATCOM operates in capacitive mode, njecting reactive power to the AC power system. In the third condition, if V_c is equal to V_s', there is no reactive power generation. Thus, the statement can be made that, in a stationary state, reactive power only depends on the difference between V_s' and V_c voltages. The amount of reactive power is proportional to this voltage difference. Figure 3.13 shows the voltage and current of the AC power system and the STATCOM for a lossless STATCOM system.

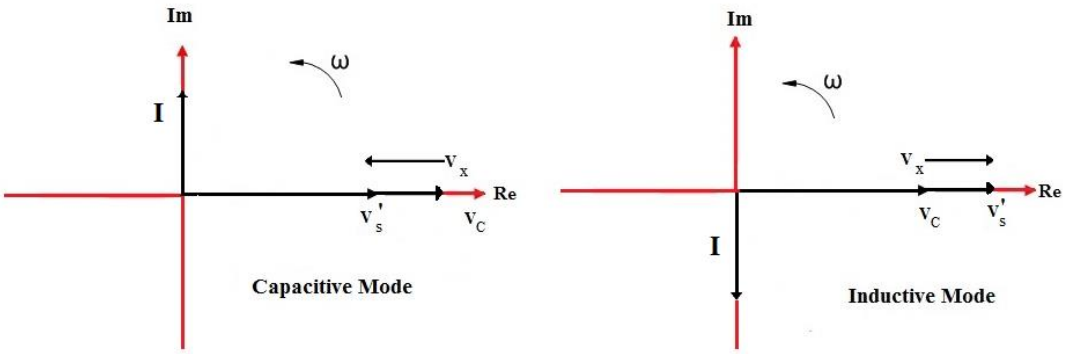


Figure 3.12 Phasor diagrams for an ideally lossless STATCOM system

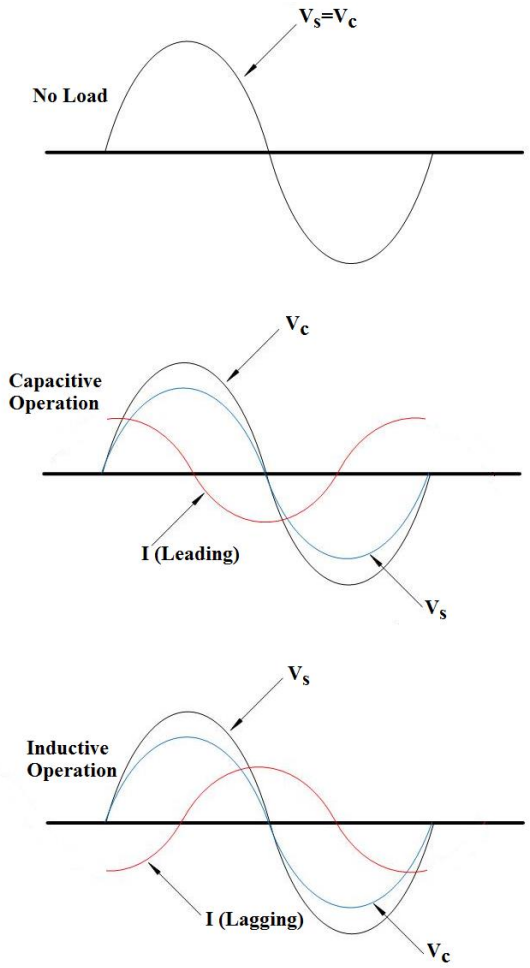


Figure 3.13 Voltage and current of a lossless STATCOM system

During transient operation of the STATCOM, DC capacitors are charged and discharged periodically and active power transfers from the AC power system to the DC link or from the DC link to the AC power system through the converter. In practical, a small amount of internal power loss is associated with the VSC and the output filter, making a small phase angle δ

between the voltage of the converter and the AC power supply. Figure 3.14 shows a practical phasor diagram of the STATCOM system assuming that $R << X$.

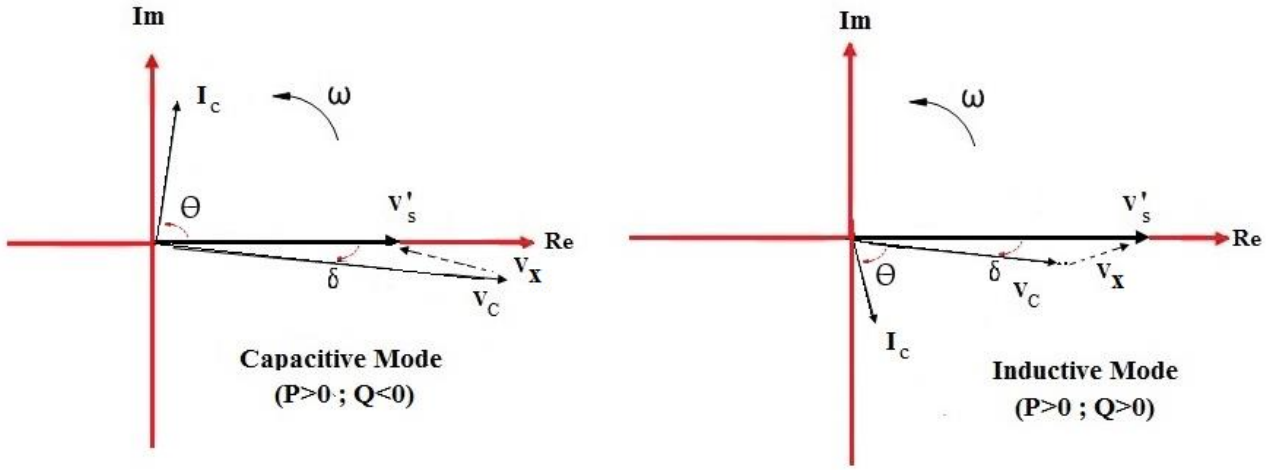


Figure 3.14 Phasor diagram of the STATCOM system for $R << X$

Considering the mentioned assumption in addition to the fact that the power angle δ is typically a small value near zero and θ is near 90 degrees, it can be approximated that:

$$\sin(\delta) \cong \delta$$
$$\sin(\theta) \cong \delta \, , \cos(\theta) \cong 0 \tag{3.10}$$

Therefore:

$$P_c \cong \frac{V_s V_c}{X} sin\delta$$
$$Q_c \cong V_s \frac{V_s - V_c cos\delta}{X} \tag{3.11}$$

The relationship between the output voltage of the STATCOM and the DC link voltage can be written as:

$$V_c = kV_d \tag{3.12}$$

Using the above equation in STATCOM active and reactive power equations previously mentioned yields:

$$P_c \cong \frac{V_s'}{X} kV_d sin\delta$$

$$Q_c \cong \frac{V_s'}{X}(V_s' - kV_d cos\delta) \tag{3.13}$$

The relationship between the input and output voltage of a classic inverter is defined by a factor called modulation index (m) defined as:

$$\hat{V_c} = m_a \frac{V_d}{2} \tag{3.14}$$

where $\hat{V_c}$ is the peak value of fundamental component of the STATCOM output voltage (line-to-neutral) and V_d is the DC link voltage value. Comparing (3.12) and (3.14) results in:

$$k = \frac{m_a}{2\sqrt{2}} \cong 0.35 m_a$$
$$V_c \cong 0.35 m_a V_d \tag{3.15}$$

Therefore, active and reactive power equations of the VSC-STATCOM using classic inverter topologies can be written as:

$$P_c \cong \frac{0.35 V_s'}{X} m_a V_d sin\delta$$
$$Q_c \cong \frac{V_s'}{X}(V_s' - 0.35 m_a V_d cos\delta) \tag{3.16}$$

The above equation demonstrates that the operating condition of the STATCOM can be controlled by the value of $0.35 m_a V_d cos\delta$. If this value is higher than V_s', then reactive power of the compensator becomes negative, causing capacitive operation mode. Unlikely, if this value is lower than V_s', reactive power of the compensator becomes positive, causing inductive operation mode. Considering that δ is a small value, $cos\delta$ can be approximated with 1. In this case, reactive power of the compensator can be controlled by the term $0.35 m_a V_d$ introducing three types of reactive power control: 1) changing DC link voltage while keeping the modulation index constant (phase angle control) [102], 2) changing modulation index while keeping DC link voltage constant (constant DC link voltage scheme) [103], and 3) varying both modulation index and DC link voltage.

3.4.4.1 Phase angle control

In this method the DC link voltage is changed while the modulation index remains constant. The control variable is the phase angle which is related to the DC link capacitors voltages. If the DC link voltage increases (charging DC capacitors), then the phase angle increases and the STATCOM supplies more reactive power to the AC power system, resulting in the STATCOM is operating more deeply in capacitive mode. Unlikely, if the DC link voltage decreases (discharging DC capacitors), then the phase angle decreases and the STATCOM absorbs more reactive power from the AC power system, resulting in the STATCOM operating more deeply in inductive mode. STATCOM voltage lags AC power system voltage ($\delta > 0$) for inductive and capacitive operation modes in steady-state (Figure 3.11).

Equation (3.16) demonstrates that active power can be extracted from the DC link if the phase angle becomes negative. This active power can compensate internal losses of the inverter. If negative active power exceeds inverter losses, the STATCOM begins to deliver active power to the AC power system, decreasing DC link voltage. On the other hand, if the power angle becomes more than the steady-state power angle, the active power absorbed by STATCOM in excess of the losses will be stored in the DC link capacitor, thus increasing DC link voltage. Phasor diagrams of STATCOM in transient state are shown in Figure 3.15.

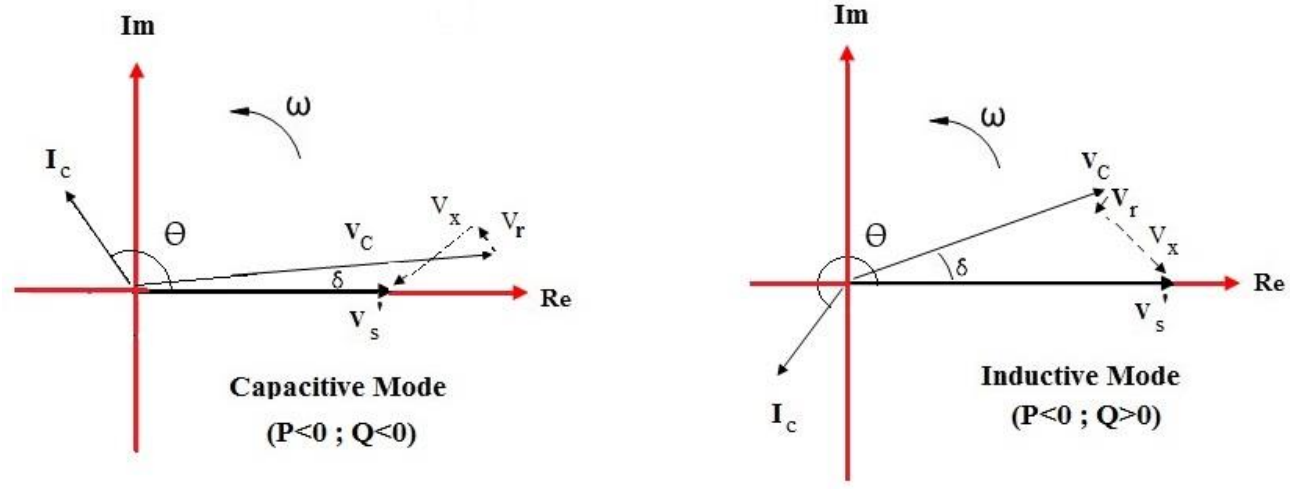


Figure 3.15 Phasor diagrams of the STATCOM in transient state

In this reactive power control method, reactive power is measured and compared to a reference value. The error is processed using a PI controller. Output of the PI controller is called phase angle(δ). The resulting phase angle is then used to shift the reference signal of the PWM in

respect to the AC power source voltage. Figure 3.16 shows a schematic of the phase angle control method.

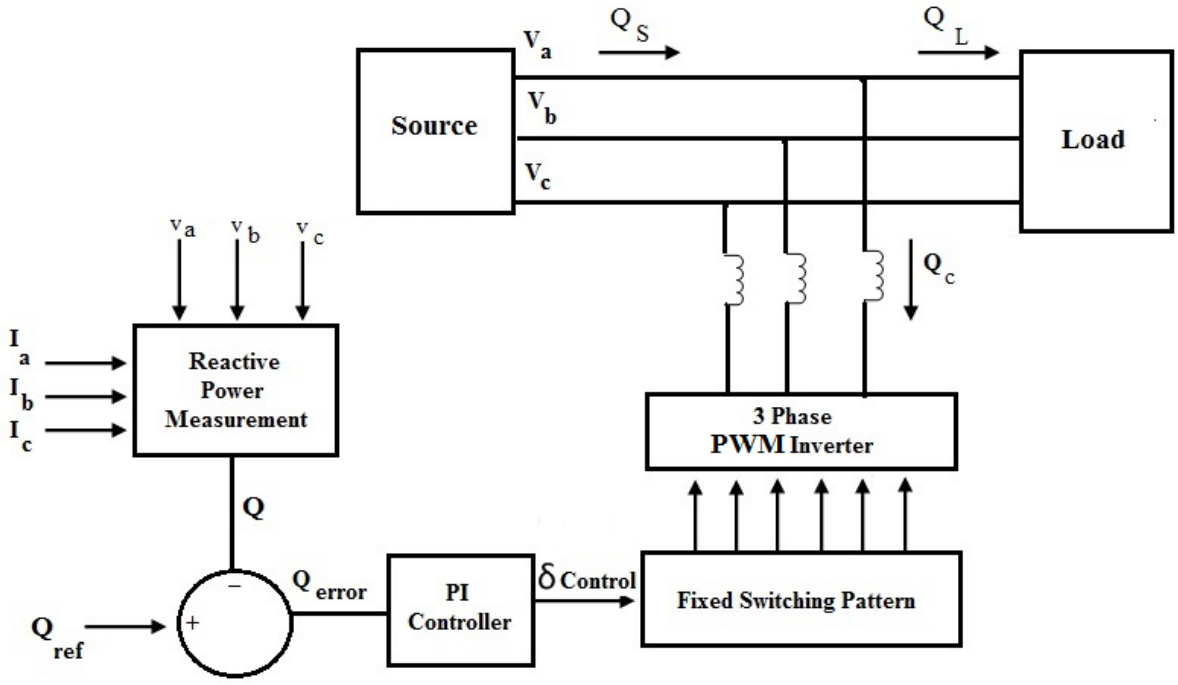


Figure 3.16 Schematic of the phase angle control method

3.4.4.2 Constant DC link voltage scheme

In this reactive control method, the DC link voltage is kept constant by controlling the phase angle and the modulation index varies. The DC link voltage is measured and compared with the reference value. The error is processed by a PI controller to determine the phase angle of the inverter voltage. The resulting phase angle can be used to shift the reference waveform in order to generate PWM signals. This control method is preferred for the STATCOMs with SPWM control methods. On the other hand, reactive power is measured and then compared with the reference value. The error is processed by a PI controller (different from the first one) to determine the modulation index. The resulting modulation index can be used to change the reference signal amplitude of the PWM generation block. In this control method, the DC link voltage control loop has a slow response, while the reactive power loop must be fast in order to rapidly control reactive power. Figure 3.17 shows a schematic of the constant DC link voltage method.

In the phase angle control method, the DC link voltage changes according to reactive power reference, while the DC link voltage remains constant in a constant DC link voltage scheme. The

second control method changes reactive power only by varying the modulation index, consequently eliminating the delay resulting from charging or discharging of DC link capacitors associated with the phase angle control method. Hence, the step response of the constant DC link voltage scheme is faster than the phase angle control method. The step response of the device can be varied depending on passive components such as output filter reactance and DC link capacitors.

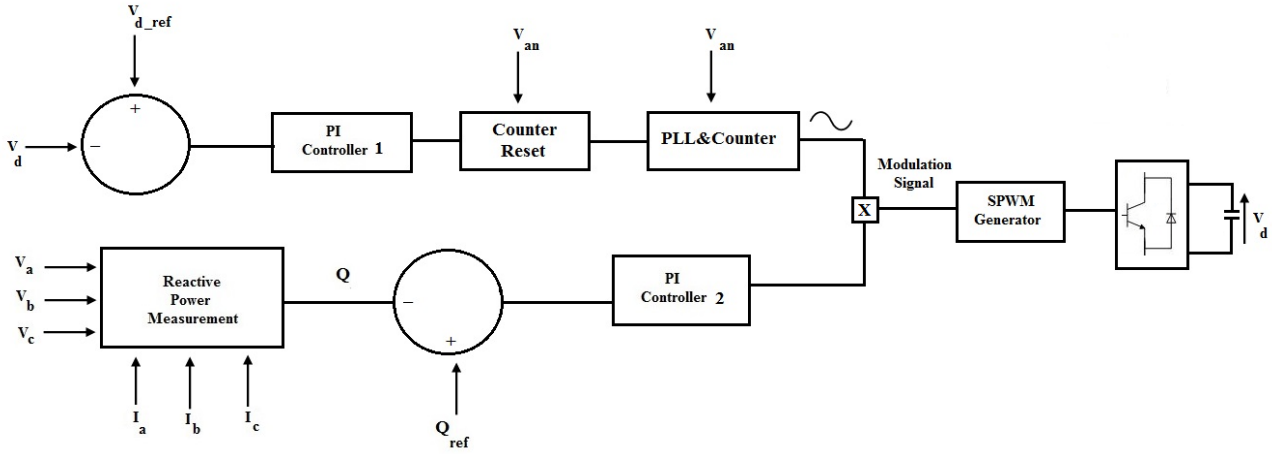


Figure 3.17 Schematic of the constant DC link voltage method

Choosing the proper control algorithm for a STATCOM system depends on the reactive power rating of the converter and the step response required for compensation. Constant DC link voltage scheme has faster response but the expense of higher switching frequencies, thus affecting device efficiency. Typically, lower switching frequencies are utilized for higher-power STATCOMs and high switching frequency PWM techniques are used for lower-power applications.

3.4.5 Integrating STATCOM and energy storage system (ESS)

Typically, STATCOM systems have two possible steady-state operating modes, inductive and capacitive. Although the magnitude and phase angle of the device output voltage can be controlled, they cannot be independently adjusted because of lack of significant STATCOM active power capabilities. In normal operation, STATCOM voltage is in phase with PCC voltage, thus ensuring that only reactive power flows from the STATCOM to the power system. However, internal losses of the STATCOM cause a small phase shift between STATCOM voltage and the AC power system. This small phase shift causes the flow of a small amount of

active power from the power system to the STATCOM. However, the active power capability of the STATCOM is very limited due to the absence of any energy storage.

An energy storage system (ESS) can be integrated within classic STATCOMs and play an important role in power system control [104]. Energy storage device have advantages such as their ability to rapidly damp oscillations, respond to sudden load transients, continually supply the load during transmission or distribution interruptions, and correct load voltage profiles with rapid reactive power control. This integration provides greater improvements over traditional STATCOM. Adding an ESS to the STATCOM system allows for active power transfer control between the STATCOM and PCC. In this way, STATCOM compensates the reactive power as well as store energy in the storage system when the generated power is greater than the power limits [105]. Integrating the ESS with a STATCOM enhances the degree of freedom in compensator operation. Moreover, this combination provides the capability to perform an independent active and reactive power absorption or injection to or from the power system, leading to a more flexible power system controller.

Figure 3.18 shows a typical STATCOM system integrated with an ESS. This system (STATCOM + ESS) offers more flexibility because it possesses four steady-state operation modes, including: inductive mode with DC charge and DC discharge and capacitive mode with DC charge and discharge. The primary disadvantage this system is that the size of the ESS, especially battery energy storage (BESS), can be too large for large-scale transmission power systems. Moreover, large battery systems can lead to voltage instability if a large number of cells are placed in series. However, the possibility of controlling active and reactive power independently makes this structure a suitable choice for improving various issues related to power systems such as controlling reactive and active power flow, enhancing stability, enhancing system security, managing power flow congestion, and integrating renewable energy systems, especially wind generation.

Because of the pulsating nature of wind generation, output power of turbine oscillates that can damage the generator. During severe disturbances such as line sag, the wind turbine supplies lower amounts of active power to the grid. This condition leads to more consumption of reactive power by the generator, causing voltage decrease. In order to solve this problem, reactive power must be supplied from an external device. Using a battery in parallel with the wind turbine has an advantage of storing energy that cannot be transferred to the grid. A STATCOM integrated with

a battery can be utilized to maximize power that can be injected into a weak network in a distributed generator (DG) system [106]. In this case, even a generator more highly rated than the maximum rating can be used since the excessive power can be stored in the battery system. On the other hand, if power consumption exceeds maximum generation, the battery is able to provide necessary power.

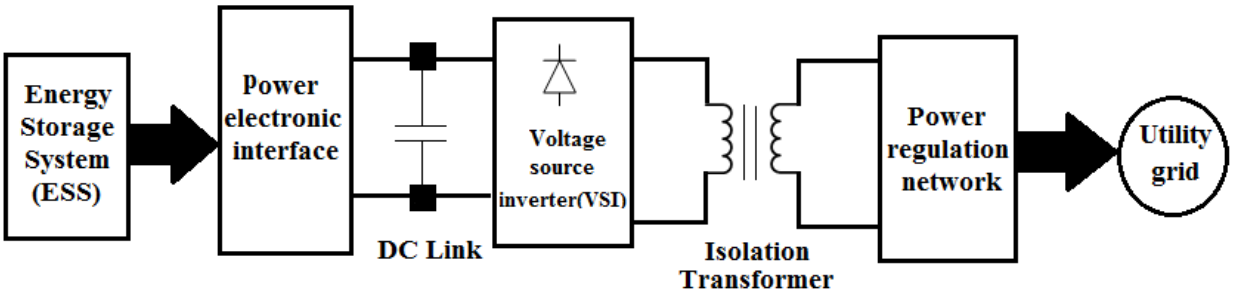


Figure 3.18 A typical STATCOM system integrated with an ESS

The integration of STATCOM with ESS can improve several other stability applications as well [105]. This combination also can improve power system operation, regulation, and control. Use of STATCOM + BESS can reduce DC link capacitor value significantly. For specific applications, only a small-size capacitor is adequate in order to smooth the battery DC current. From an economic standpoint, the cost of this integration can be divided into three main parts: 1) energy storage system, 2) supporting systems, and 3) power conversion system. The amount of energy needing to be stored defines the ESS cost. However, for high-power applications requiring low-energy storage, the configuration and size of the power conversion system determines the cost of the system. Recent developments in battery storage systems have decreased the total cost of these integrated systems. A detailed system modeling and simulation analysis for integration of STATCOM with BESS is presented in [105].

3.4.6 Benefits of using STATCOM

STATCOMs are implemented to provide stability to power systems and are usually placed on weak buses or critical paths. Most voltage instability issues are related to a lack of adequate reactive power, STATCOMs are able to offer support by providing VARs as the load demands. Major applications of STATCOMs in power systems include: decreasing undesired reactive power flows which result in power losses reduction, consumer compensation and improvement of power quality (especially with huge demand fluctuations), improvement of static or transient

stability of power systems including transmission and distribution systems, improvement of transient stability margin by increasing the maximum transmittable power in the transmission line, compensation of loads with poor power factor (PF) in order to obtain near unity power factor, load balancing by cancelling the effect of unbalanced loads, and damping power oscillations. Moreover, a growing area of application includes renewable or distributed energy, such as wind generation. Wind turbines must provide a balanced reactive power level and maintain voltage limitations within the wind farm. STATCOMs can be utilized in wind generation applications in order to mitigate undesirable aspects of power generation. Applications of STATCOM for voltage regulation/control [107],[108] and stability [109],[110] have been discussed in several papers.

Primary benefits of STATCOM compared to conventional Thyristor-switched reactive elements (such as SVC) include the use of a relatively small DC capacitor, occupying a smaller space in a substation (smaller footprint results in lower cost), having faster dynamic response, and producing the rated current at almost any network voltage. These devices are able to respond very rapidly to changes in the system because of power electronic circuits utilizing high-switching components. In addition, one of the most critical times for VAR support occurs after or during a fault when the system may require an injection of VARs to raise the voltage back to stable limits. STATCOMs are better than SVCs because the amount of reactive power compensation they provide is a linear function of grid voltage while the amount of reactive power compensated by a SVC is a quadratic function of the grid voltage. This means that when grid voltage drops and is in most need of VAR support, the SVC can provide the least amount.

STATCOMs have symmetric lead-lag capability and can theoretically go from full lag to full lead in a fraction of cycles [105]. As previously mentioned, combining a STATCOM system with an energy storage system (ESS) achieves significant improvements compared to traditional STATCOM performance. This combination is capable of solving many stability and voltage fluctuation issues in a power system.

3.5 Summary

Flexible AC transmission systems (FACTS) are a group of devices used to improve various aspects of the power system including distribution and transmission systems. These devices can be categorized in different ways. One way is to categorize them as they connect to the AC power

systems in order to mitigate undesirable aspects of the power systems. In this way, three types of devices, including a series device (TCSC and SSSC), shunt devices (SVC and STATCOM), and hybrid devices (UPFC, IPFC, and DFC) are able to be utilized. The other categorical grouping of FACTS devices is based on their structure including Thyristor- and VSC-based systems. Thyristor-based devices use well-known Thyristor-valves or converters. They have low losses due to low switching frequency. SVC, TCSC, and DFC are the primary members of this device family. VSC-based systems take advantage of voltage source converter topologies, including classic or multi-level topologies, while utilizing high switching frequency components such as IGBT or IGCT. These FACTS devices generate lower harmonic contents due to the use of high-frequency modulation techniques. However, this increases power losses of these compensators. This family includes several devices, including STATCOM, SSSC, UPFC, and IPFC. All these devices, independent of their category, are used to improve power systems. A number of their functions are as: compensating reactive power on power systems, enhancing stability problems, improving PF of the grids, and mitigating issues such as flicker, voltage unbalancing, and power fluctuations.

Among all mentioned FACTS devices, STATCOM has gained increasing attention recently because of its structure and advantages in comparison to other compensators. STATCOM is a shunt compensator based on use of a VSC on distribution (up to 5MVAR) and transmission systems (20-100 MVAR) in order to enhance PF of the power systems as well as regulate voltage. The STATCOM has the same capabilities as the SVC, but with a higher response time. In addition, STATCOM provides reactive compensation by injecting a variable magnitude near-sinusoidal current signal at the point of connection. Compensation amount is determined by the voltage difference of the STATCOM and the AC power system. When the DC-link voltage of STATCOM increases, the output AC of the device goes higher, causing the STATCOM to generate reactive power (capacitive mode). Unlikely, when DC link voltage decreases, the output of the STATCOM reduces, causing the STATCOM to absorb reactive power (inductive mode). Conversely, if the STATCOM has a DC source, such as a DC capacitor, it is able to supply active power to the grid. The active power transfer can be adjusted by varying the phase angle between the STATCOM and the power system. If the phase angle of the STATCOM lags the phase angle of the AC power grid, the device absorbs active power. Unlikely, if the phase angle of the STATCOM leads the phase angle of the AC power system, the STATCOM injects active

power to the grid. STATCOMs can also be integrated with energy storage systems (ESSs) in order to enhance their capabilities for several specific applications. In such an integrated system, four operating modes exist for the STATCOM including inductive mode with DC charge and DC discharge, and capacitive mode with DC charge and discharge. This option improves active power controllability of the STATCOM. The primary drawback of this system is that it cannot be used for large-scale transmission systems because the physical size of the ESS becomes too large. Moreover, large battery systems cause instability if a large number of ESSs are connected in series. STATCOM integrated with ESS has the possibility to independently control active and reactive power independently. This option can be very helpful in renewable energy applications with fluctuating active and reactive power, such as wind generation.

Chapter 4 - Proposed inverter and control strategy

4.1 Overview

In this chapter, a new inverter with D-STATCOM capability is proposed. The idea of such an inverter, topology used for the inverter, and the control system are explained in detail. The proposed inverter is categorized as custom power electronics. Custom power electronics is defined by IEEE as "the concept of employing power electronic (static) controllers in 1 kV through 38 kV distribution systems for supplying a compatible level of power quality necessary for adequate performance of selected facilities and processes" [60]. To date, limited research has been conducted on the use of these custom power electronic devices for renewable energy applications, possibly because the IEEE1547 standard declares that "the distributed renewable (DR) shall not actively regulate the voltage at the PCC"[60]. This declaration limits application of these devices. However, research on custom power electronics devices can prove the technology, thus resulting in the development of new standards. As mentioned in Section 3.4.5, D-STATCOMs can be integrated with ESSs in order to develop a device that can regulate reactive power, like a D-STATCOM, as well as control active power independently for short durations. In normal conditions, the operation of these devices is very similar to classic D-STATCOMs. They are designed to be placed on weaker busses or on critical paths of the system. They have also been practically implemented on wind energy applications in which active and, as a result, reactive power fluctuates.

Several other applications of custom power electronics in renewable energy systems exist, including [111] an application of a custom power interface where two modes of operation, including an active power filter and a renewable energy STATCOM. Another application [112] looks at the current-source inverter (CSI) which controls reactive power and regulates voltage at the PCC.

In [113] new commercial wind energy converters with FACTS capabilities are introduced with no detailed information regarding the efficiency or the topology used for the converters. The proposed converters are able to control reactive power while operating as a power converter.

[114],[115],[116],[117],[118] propose an application of PV solar inverter as STATCOM in order to regulate voltage on 3-phase power systems, for improving transient stability and power transfer limit in transmission systems. The authors called their proposed system "PV-

STATCOM". Similar to wind farms when there is no wind, solar farms are idle during nights. All mentioned papers are from the same authors which demonstrate the completion of the same system. The authors have proposed a control strategy that makes the solar farms act as STATCOMs during the night when they are not able to produce active power. The main purpose of the "PV-STATCOM" system is to improve voltage control and power factor correction on 3-phase transmission systems. As previously mentioned, the main focus of the papers is on developing a control system for a 3-phase system. The authors have tested and verified the proposed control strategy on a ready-to-use conventional six-pulse PV inverter. The controller system uses the benefit of dq-transform which makes controlling active and reactive power more convenient than in single-phase systems, where the dq-model cannot be used. The authors have done the simulations in EMTDC/PSCAD environment and the proposed system was supposed to be showcased for the first time in Canada in 2012 on two 10 kW PV-solar systems. Furthermore, the authors have presented the real-time digital simulation of the PV-STATCOM controller in a real-time digital simulator (RTDS). Also, they have seen that the controller system is able to sense the system faults and switch to regular STATCOM mode. In [114-118], the authors did not mention the efficiency of their system. However they believe that using the entire capacity of their system may have negative effect on the efficiency.

The last significant research on application of custom power electronics in renewable energy systems is [60] in which a new D-STATCOM inverter is proposed. In this research, the author proposes a 5-level hybrid-clamped inverter with the ability to regulate the active and reactive power of the grid in renewable energy applications. The primary drawback of this research is that the author states that the STATCOM output current is not compatible with IEEE standards. A problem with snubber circuit design has been mentioned as a possible reason for oscillations in output current of the D-STATCOM inverter.

The main idea behind this dissertation originated from the last study mentioned, [60]. The primary focus of the present research is to demonstrate the application of custom power electronics in renewable energy systems. Because of recent developments in wind energy, the utilization of smarter wind energy inverters (WEIs) has become an important issue. Many single-phase lines take power to multiple small farms or remote houses in the United States. Such customers are able to produce energy by using a small- to medium-sized wind turbine. Increasing the number of small to medium wind turbines can lead to several issues, such as harmonics or

power factor (PF) problems, for local utilities. Traditionally, utilities must use capacitor banks to solve PF issues, thus increasing the total cost of the system. Currently, PF of the power lines is controlled by using small distribution static synchronous compensators (D-STATCOMs). D-STATCOMs are typically placed in parallel with distributed generation (DG) systems and power systems to operate as a source or sink of reactive power in order to improve power quality on the distribution lines. Using regular STATCOMs for small- or medium-size single-phase wind applications is not economical, because the cost of the system increases significantly, thus creating opportunity to use smarter WEIs with FACTS capabilities in order to be cost-effective and compatible with IEEE standards. The proposed inverter in this research is equipped with a D-STATCOM option to regulate reactive power of local distribution lines. As with a regular WEI, this inverter can be placed between the wind turbine and the grid at no additional cost. The function of the proposed inverter is to convert DC power coming from the DC link to a suitable AC power for the main grid, and to fix the PF of the local grid at a target PF by injecting enough reactive power to the grid. In the proposed control strategy, concepts of WEI and D-STATCOM are combined to create a new inverter which possesses D-STATCOM capability at no additional cost. The proposed control strategy also allows the inverter to act as an "inverter with D-STATCOM option" when enough wind is present to produce active power, and to act as a "D-STATCOM" when no wind is present. Active power is controlled by adjusting the power angle (δ), or the angle between voltages of the inverter and the grid, and reactive power is regulated by the modulation index (m).

The proposed inverter, presented in this dissertation, utilizes modular multi-level converter (MMC) topology. Replacing conventional inverters with this inverter eliminates the need to use a separate capacitor bank or STATCOM device in order to fix the PF of local distribution grids. Depending on the size of the power system, multiple inverters may be used in order to reach the desired PF. The unique work in this dissertation is the use of MMC topology for a single-phase voltage source inverter (VSI) for wind applications, which meets the IEEE519 standard requirements, and is able to control the PF of the grid regardless of the wind speed. As previously mentioned, controlling active and reactive power in a single-phase system is more complicated than in 3-phase systems in which dq-transform can be used to control power transfer more conveniently. Figure 4.1 shows the complete grid-connected configuration of the proposed inverter. The DC link of the inverter is connected to the wind turbine through a rectifier using

MPPT and its output terminal is connected to the utility grid through a series-connected second-order filter and a distribution transformer.

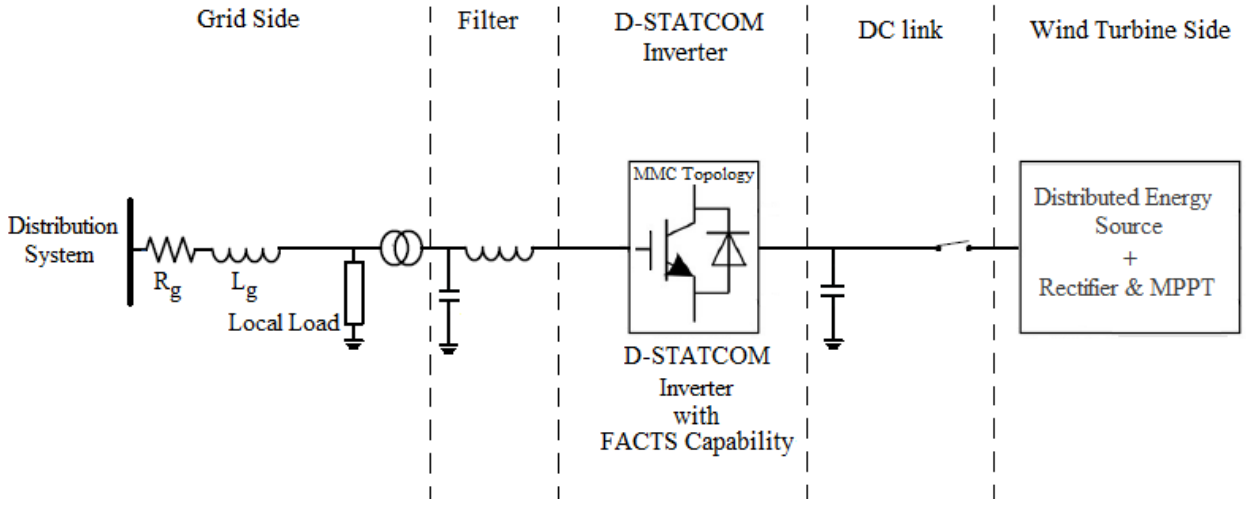


Figure 4.1 Complete configuration of the proposed inverter with FACTS capability

4.2 Design objectives

In the design of the proposed inverter with D-STATCOM capability, several issues were considered which are as: 1) the inverter should be able to operate with minimum switching frequency in order to minimize the losses and increase the efficiency of the inverter, 2) the inverter output should be completely compatible with IEEE standards in terms of total harmonic distortion and power in each harmonic, 3) the inverter should be cost-effective for use in medium or even small applications (50 kW and less).

The goal of the proposed inverter is to replace the regular inverter of a wind turbine with one that possesses a D-STATCOM option to give the utilities additional control on power factor. The basic design criteria of the proposed inverter are: 1) the inverter should be connected between the wind turbine and a single-phase feeder line, 2) the proposed inverter should be able to support turbines rated from 10–20 kW, 3) the proposed inverter should be able to compensate up to 20 kVARs of capacitive compensation regardless of the wind speed and incoming active power, 4) the inverter must be able to fix the PF of the feeder line at a target value set by the user (utility), if the required compensation is within the range of inverter ratings. These design criteria were considered for utilizing the inverter for small businesses and farms. These customers are normally able to use up to 20 kW wind turbines as this is a good level of generation and is financially feasible for them. The amount of reactive power compensation (20 kVARS) is also

selected based on the rating of the corresponding wind turbine as it is a realistic amount of reactive power compensation for a small- to mid-sized wind turbine.

In this dissertation 5-level and 11-level inverter using modular multi-level converter (MMC) topology are designed. The simulations are done in MATLAB/Simulink environment and to validate the simulation results, a scaled version of the inverters is built and tested. The simulation and experimental results are explained in chapters 5 and 7, respectively. This chapter proceeds by going through the proposed architecture, proposed control strategy, and design steps of this inverter.

4.3 Modular multi-level converter (MMC)

Modular multi-level converter (MMC) has previously been introduced in order to avoid the drawbacks of conventional VSC in high-voltage applications. Recently, MMC has gained increasing attention. Many papers on MMC have suggested the use of this topology for "inverter+D-STATCOM" application. MMC is a converter system comprised of arbitrary numbers of identical half-bridge (HB) sub-modules (SMs). In this topology, additional "central" components are avoided in order to make a stringent modular and scalable realization. Each SM is a two-terminal device, considered a controllable voltage source, consisting of two switches working in a complementary manner and a local DC-storage capacitor. For the full four-quadrant operation of this topology, no more additional connection is necessary. Figure 4.2 illustrate the structure of a single-phase MMC inverter and each SM. Generally, an n-level single-phase MMC inverter consists of a series connection of $2(n-1)$ basic SMs, two buffer inductors, and two DC capacitors which translates to $4(n-1)$ switches and $2(n-1)$ SM capacitors, in addition to two inductors and two DC link capacitors. Buffer inductors must provide current control in each phase arm and limit the fault currents. These protection chokes do not disturb operation or generate overvoltage for the semiconductors. The output voltage of each SM (v_o) is either equal to its capacitor voltage (v_c) or zero, depending on the switching states. The voltage of each SM can easily be controlled by software. Individual voltages of the SMs can even be chosen unequal in order to increase the number of output voltage levels. In addition, a defective SM can be replaced by a redundant SM by control action without mechanical switches, thus improving device safety and availability of the device. If i_c is the current flowing through the switches, failure-free switching states for each SM are shown in Table 1.1. When S_m is switched *On,*

output voltage of the SM is equal to zero. Similarly, when S_c is switched *On*, output voltage of each SM equals its capacitor voltage (V_c). When both S_m and S_c are switched off, impressed voltage to the power devices is limited by the capacitor voltage V_c. In order to describe the operation of MMC, each SM can be considered as a two-pole switch. If S_{ui}, defined as the status of the i_{th} sub-module in the upper arm is equal to unity, then the output of the i_{th} SM is equal to the corresponding capacitor voltage; otherwise it is zero. Likewise, if S_{li}, defined as the status of the i_{th} sub-module in the lower arm is equal to unity, then the output of the i_{th} lower SM is equal to the corresponding capacitor voltage; otherwise it is zero. In general, when S_{ui} or S_{li} is equal to unity, the i_{th}upper or lower S_m is *On*; otherwise it is *Off*. Therefore, upper and lower arm voltages of the MMC are as follows:

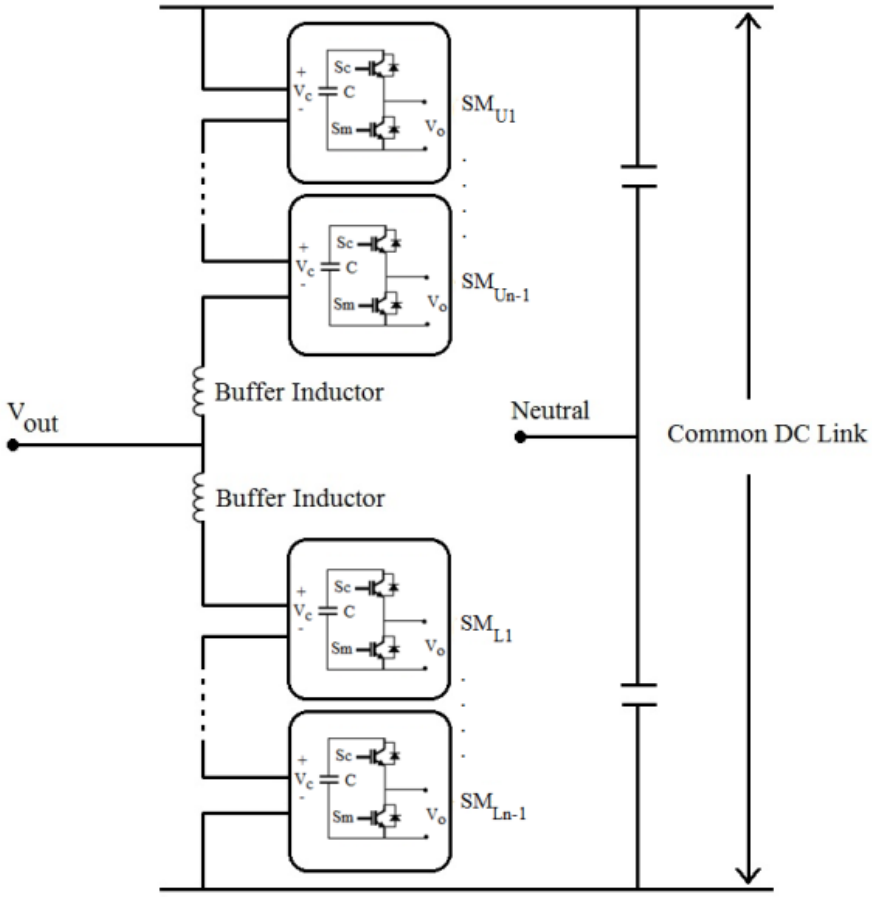


Figure 4.2 Structure of a single-phase MMC inverter

Table 4.1 Failure-free switching states for each SM of MMC topology

Mode	Sm	Sc	Vo
1	Off	On	Vc
2	On	Off	0

$$v_{upperArm} = \sum_{i=1}^{n-1}(S_{ui}v_{ci}) + v_{l1} \quad (4.1)$$

$$v_{lowerArm} = \sum_{i=1}^{n-1}(S_{li}v_{ci}) + v_{l2} \quad (4.2)$$

where v_{l1} and v_{l2} are the voltages of upper and lower buffer inductors, n is the number of voltage levels, and v_{ci} is the voltage of the i_{th} SM capacitor in upper arm or lower arm. For instance, a single-phase 11-level MMC inverter consists of 20 SMs which translates to 40 power switches, 20 capacitors, and two buffer inductors. The DC and AC voltages of the 11-level MMC are described by:

$$v_{dc} = v_{upperArm} + v_{lowerArm} = \sum_{i=1}^{10}(S_{ui}v_{ci}) + \sum_{i=1}^{10}(S_{li}v_{ci}) + (v_{l1+}\, v_{l2}) \quad (4.3)$$

$$v_{out} = {}^{v_{dc}}/_{2} - v_{upperArm} = -{}^{v_{dc}}/_{2} + v_{lowerArm} \quad (4.4)$$

The upper arm current in an MMC is determined by the voltage difference across the upper arm inductor as:

$$i_{upperArm} = {}^{1}/_{l_1} \int (v_{l1}) \quad (4.5)$$

Substituting (4.1) and left part of the (4.4) in (4.5) yields:

$$i_{upperArm} = {}^{1}/_{l_1} \int \left(v_{upperArm} - \sum_{i=1}^{n-1}(S_{ui}v_{ci})\right) = {}^{1}/_{l_1} \int \left(({}^{v_{dc}}/_{2} - v_{out}) - \sum_{i=1}^{n-1}(S_{ui}v_{ci})\right) \quad (4.6)$$

where v_{ci} can be defined as:

$$v_{ci} = {}^{1}/_{c_i} \int (i_{upperArm} * S_{ui}) \quad (4.7)$$

In a similar way, the lower arm current of the MMC can be defined by:

$$i_{lowerArm} = {}^{1}/_{l_2} \int (v_{lowerArm} - \sum_{i=1}^{n-1}(S_{li}v_{ci})) = {}^{1}/_{l_2} \int \left((v_{out} + {}^{v_{dc}}/_{2}) - \sum_{i=1}^{n-1}(S_{li}v_{ci})\right) \quad (4.8)$$

where v_{ci} can be defined as:

$$v_{ci} = {}^{1}/_{c_i} \int (i_{lowerArm} * S_{li}) \quad (4.9)$$

The above equations demonstrate the differential equation for MMC voltage and current. The conclusion can be made that the MMC controller uses the upper (lower) SM gating signals ($S_{u/l\,i}$) to regulate the upper (lower) arm current and SM capacitor voltages. Therefore, a positive change on $S_{u/l\,i}$ results in a negative change on arm current if capacitor voltages are considered constant, and vice versa.

The primary benefits of MMC topology include modular design based on identical converter cells, simple voltage scaling by a series connection of cells, simple realization of redundancy, possibility of a common DC bus, low PWM carrier frequency, and DC link short circuit protection. In the MMC topology, arm currents can be controlled by the converter control system. Unlike the two-level converters, in this topology the internal arm currents flow continuously and are not chopped. Furthermore, SM voltage balancing is not critical with respect to the timing of pulses or switching times because it is assured by the converter control on a non-critical, larger time scale. Moreover, for three-phase HVDC applications, MMC needs no separate DC link capacitor and uses a common DC link. MMC can be scaled to different voltage levels only by varying the number of SMs. Hence, the same hardware with identical mechanical construction can be used for a wide range of applications. Initially, the high number of components needed for this topology can be considered a disadvantage. However, this enables new degrees of freedom for control. Power losses of this topology can be compared to classic converters since switching losses of the semiconductors are very low. In general, the exclusive structure of MMC makes it an ideal candidate for medium- to high-voltage applications such as wind energy applications. Moreover, this topology needs only one DC source, which is a key point for wind applications. MMC requires large capacitors which may increase the system cost; however, this complication is offset by the lack of need for any snubber circuit.

The MMC system offers many advantages over conventional two-level or multi-level topologies and, therefore, can be used in a wide range of applications, including renewable energy systems, DC power transmission, or micro grid. While MMC's distinctive structure introduces many new features, it also requires a sophisticated controller to deal with extra control requirements. The MMC controller needs to balance SM capacitor voltages. In the following section, the MMC control scheme is presented in detail.

4.4 Proposed controller system

In order to synthesize a multi-level output voltage with the fundamental component equal to the sinusoidal reference, the phase disposition pulse width modulation (PDPWM), introduced in Section 2.5.2.3, is used for the proposed controller system. As shown in (4.6) and (4.8), coupling of the arm current and SM capacitor voltage makes the control system complicated. As previously mentioned, a positive variation applied by the controller to SM gating signals ($S_{u/l\,i}$) by the controller and a consequently negative variation on arm current could complicate the SM capacitor voltage balancing. In addition to this, the proposed inverter must act as a regular inverter which is equipped with a D-STATCOM option. The aim of the inverter is to control the PF of the local distribution grid at a target value set by the user (utility grid). This application requires the independently control of active and reactive power transferred between the inverter and the grid. Hence, the proposed controller consists of three major functions. The first function is to control the active and reactive power transferred between the inverter and the power line, the second function is to keep the voltages of the SMs capacitors balanced, and the third function is to generate desired PWM signals. Figure 4.3 shows the complete proposed controller system. The aim of the designed inverter is to transfer active power coming from the wind turbine as well as to provide utilities with distributive control of VAR compensation and power factor correction of feeder lines. Application of the proposed inverter requires active and reactive power to be independently controlled, so that if wind is blowing, the device should operate as a normal inverter in addition to being able to fix the PF of the local grid at a target PF. If no wind is present, the device should only operate as a D-STATCOM (or capacitor bank) to regulate PF of the local grid. This translates to two modes of operation: 1) when wind is blowing and active power is coming from the wind turbine: the "inverter plus D-STATCOM" mode. In this mode, the device operates as a regular inverter to transfer active power from the renewable energy source to the grid as well as performing as a normal D-STATCOM to regulate the reactive power of the grid in order to control the grid PF. 2) When wind speed is zero or too low to generate active power: the "D-STATCOM" mode. In this case, the inverter is acting only as a source of reactive power to control the PF of the grid, as a D-STATCOM. This option eliminates the use of additional capacitor banks or external STATCOMs to regulate the PF of the distribution feeder lines. The device is capable of outputting up to its rated maximum real power and/or reactive power and always outputs all real power generated by the wind turbine to the grid. The amount

of reactive power, up to the design maximum, is dependent only on what the utility asks the device to produce. Three parts of the controller system are described in the following sections.

4.4.1 Active and reactive power control

The primary goal of the designed inverter is to provide utilities with distributive control of VAR compensation and power factor (PF) on feeder lines. To enhance reactive power control of the proposed inverter, it is equipped with the additional D-STATCOM option which permits the inverter to deliver reactive power independently from wind speed. The inverter is able to control the active and reactive power regardless of the input active power from the renewable energy source.

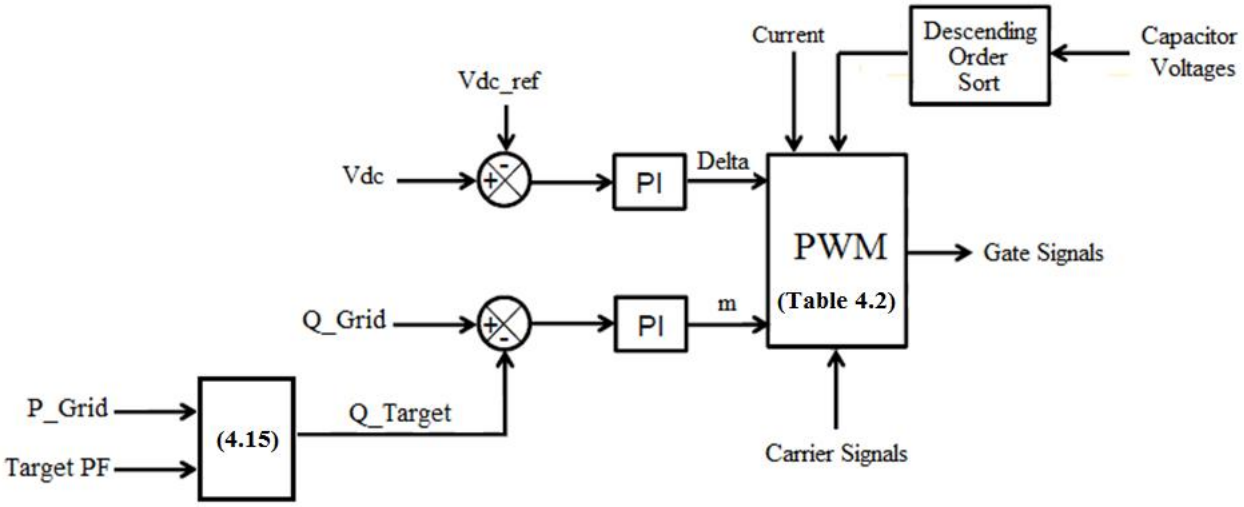


Figure 4.3 Complete schematic of the proposed controller system

The use of this inverter eliminates the need for additional capacitor banks or external STATCOMs in order to regulate PF on the feeder lines. The proposed controller system depends on several assumptions. The first assumption is that the load on the feeder line can be considered fixed for a small window of time: assuming the load does not vary within one cycle of the grid frequency. Second, the feeder line can be accurately modeled as a constant P, Q load, meaning that power produced by a wind turbine displaces other power on the feeder line and does not add to it. Third, a change in the modulation index predominantly affects Q, while a change in delta predominantly affects P. Any effect on Q from a small change in delta is thus ignored, assuming that P and Q are independently controlled.

As described in Section 3.4.4, the power flow between a STATCOM and a line is governed by the equations below that describe the power flow between two active sources separated by an inductive reactance. For normal transmission lines this inductive reactance is the inductance of a transmission line. For a STATCOM, the modeled inductance denoted X is the summation of the inductance of the power lines and the transformer that connects STATCOM to the line. The RMS voltage of the STATCOM is given as E_C and considered to be out of phase by an angle of δ to the RMS line voltage E_S. Active power transferred from the STATCOM to the line is given by (4.10) and reactive power transferred from the STATCOM to the line is given by (4.11).

$$P_S = \frac{E_C E_S}{X} \sin \delta \tag{4.10}$$

$$Q_s = \frac{E_S^2 - E_C E_S \cos \delta}{X} \tag{4.11}$$

Reactive power control of the STATCOM can be performed by varying the voltage level of the STATCOM, and active power transfer can be controlled by the angle between the two voltages. In general, the relationship between the STATCOM output voltage and the DC link voltage can be written as $V_{out} = mE_{DC}$. Therefore, active and reactive power of the STATCOM can be shown as:

$$P_S = \frac{mE_{DC} E_S}{X} \sin \delta \tag{4.12}$$

$$Q_s = \frac{E_S^2 - mE_{DC} E_L \cos \delta}{X} \tag{4.13}$$

The above equations govern the operation of the STATCOM compensator. In the proposed controller, the active and reactive power transfer between the inverter and the power grid is controlled by adjusting the power angle and modulation index, respectively. The modulation index of a STATCOM is the primary governor of provided reactive power compensation, and its primary task is to make the power factor of the grid equal to the target power factor. In order to keep the PF of the grid constant at a target value, the controller requires equations which relate the active and reactive power of the inverter to the target PF. The target PF can be shown as:

$$PF_T = \frac{P_G}{\sqrt{P_G^2 + Q_T^2}} \tag{4.14}$$

In the above equation, $\mathrm{Q_T}$ is the target reactive power, PF_T is the target PF desired by the utility, and P_G is the grid reactive power. Hence, the target reactive power can be calculated as:

$$Q_T = \sqrt{\left(\frac{P_G}{PF_T}\right)^2 - P_G^2} \tag{4.15}$$

Therefore, the reactive power transfer between the STATCOM and the power grid is determined indirectly by controlling the reactive power needed to make the target PF for the utility. In the next step, the amount of target reactive power is compared with reactive power on the grid. The resulting error is called Q_{error}. In order to keep the controller within the acceptable operation range of the inverter, the controller uses (4.16) as:

$$PI_{Input} = min\begin{cases}|Q_{Max} - Q_C| \\ |Q_{error}|\end{cases} \tag{4.16}$$

where Q_{Max} is the maximum allowable reactive power that the STATCOM can compensate. In other words, if the amount of reactive power demanded from the inverter is less than its limits, the inverter injects the calculated amount to the grid in order to keep the PF at the target value. If the demanded amount is more than the maximum value of the inverter, the inverter injects the maximum value in order not to damage the device and keep the modulation index in its defined range. In the second case, the PF of the grid falls from its target value, because the inverter is not able to provide the required reactive power to keep the PF at the target value. In this condition, multiple devices may be needed to compensate the entire amount of reactive power in order to reach the target PF. After determining the amount of reactive power compensation by the inverter, the resulting value is processed by a PI controller. The PI controller output is called modulation index (m), which is used to change the amplitude of the sinusoidal reference signal in the PWM generator block. Figure 4.4 shows the schematic of this portion of the controller, also called reactive power control.

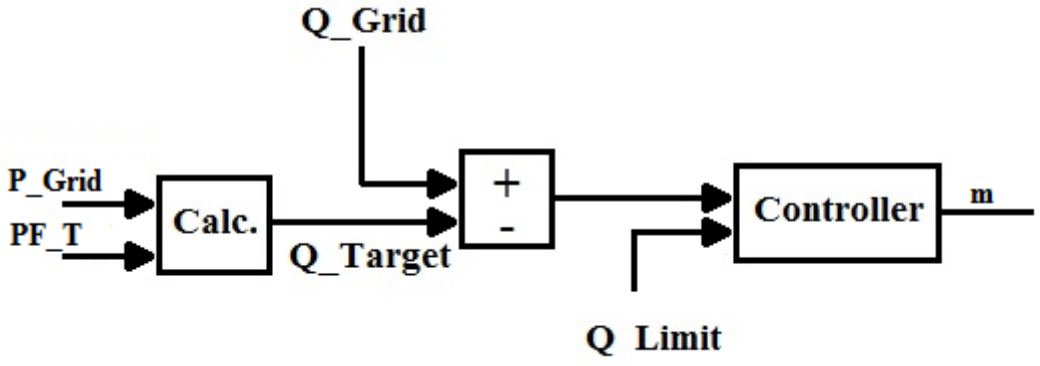


Figure 4.4 Schematic of the reactive power control

In order to control the active power transfer between the compensator and the grid, the power angle is used. The function of the power angle controller is to keep the DC link voltage constant at the reference value. In this way, active power transferred between the inverter and the power

grid can be controlled. In other words, the DC link voltage is kept constant by maintaining proper charge on the DC link capacitors. Proper selection of the angle delta secures the correct active power transfer between the inverter and the power grid, thus maintaining the proper charge across the DC link capacitors. Hence, when active power from the wind turbine increases (wind blows faster), the controller increases the power angle in order to inject more active power out of the inverter to decrease DC link voltage. Similarly, when input power from the wind turbine decreases, the controller attempts to increase DC link voltage by decreasing the power angle. In fact, the actual DC link voltage of the inverter is compared with a reference value. The resulting error is then processed by a PI controller. The controller output, delta, is used to shift the sinusoidal reference signal in the PWM generator block. Figure 4.5 shows the schematic of the power angle controller.

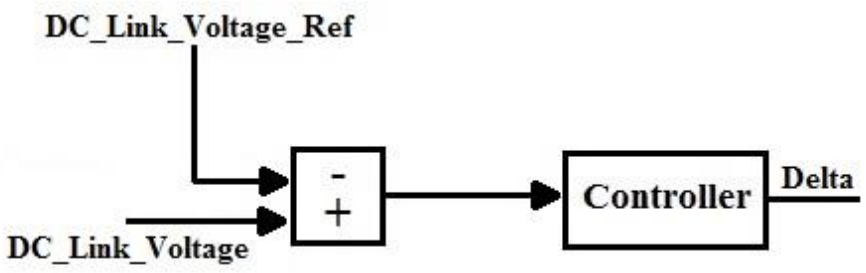


Figure 4.5 Schematic of the power angle controller

4.4.2 Capacitor voltage balancing

The second function of the controller systems is to keep capacitor voltages balanced. In order to achieve this balance, a PDPWM method is used as explained in Section 2.5.2.3. To simplify the explanation of the voltage balancing controller here, an 11-level inverter is assumed. The top graph in Figure 4.6 shows the reference signal and the carrier waveforms for an 11-level MMC inverter using the PDPWM technique. The bottom graph of Figure 4.6 shows output voltage levels generated based on Table 4.2.

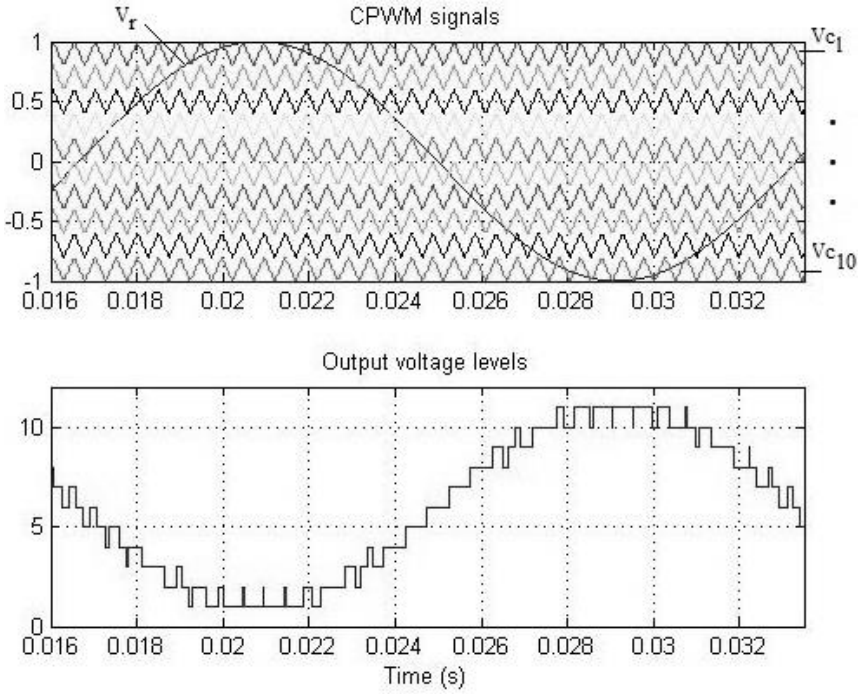


Figure 4.6 CPWM waveforms for an 11-level MMC inverter, and the generated output voltage levels

In an 11-level CPWM technique, 10 carrier signals are compared with a reference sinusoidal signal. Based on the phase of the reference signal (v_r), 11 operating regions exist in which each region defines a voltage level in the output, as shown in Figure 4.6.

Table 4.2 Operating regions for an 11-level MMC inverter

Voltage level	Status	$n_{UpperArm}$	$n_{lowerArm}$	V_{out}
1	$v_r \geq v_{c1}, v_{c2}, v_{c3}, v_{c4}, v_{c5}, v_{c6}, v_{c7}, v_{c8}, v_{c9}, v_{c10}$	0	10	$5v_{dc}/10$
2	$v_r < v_{c1}$ $v_r \geq v_{c2}, v_{c3}, v_{c4}, v_{c6}, v_{c7}, v_{c8}, v_{c9}, v_{c10}$	1	9	$4v_{dc}/10$
3	$v_r < v_{c1}, v_{c2}$ $v_r \geq v_{c3}, v_{c4}, v_{c5}, v_{c6}, v_{c7}, v_{c8}, v_{c9}, v_{c10}$	2	8	$3v_{dc}/10$
4	$v_r < v_{c1}, v_{c2}, v_{c3}$ $v_r \geq v_{c4}, v_{c5}, v_{c6}, v_{c7}, v_{c8}, v_{c9}, v_{c10}$	3	7	$2v_{dc}/10$
5	$v_r < v_{c1}, v_{c2}, v_{c3}, v_{c4}$ $v_r \geq v_{c5}, v_{c6}, v_{c7}, v_{c8}, v_{c9}, v_{c10}$	4	6	$v_{dc}/10$
6	$v_r < v_{c1}, v_{c2}, v_{c3}, v_{c4}, v_{c5}$ $v_r \geq v_{c6}, v_{c7}, v_{c8}, v_{c9}, v_{c10}$	5	5	0
7	$v_r < v_{c1}, v_{c2}, v_{c3}, v_{c4}, v_{c5}, v_{c6}$ $v_r \geq v_{c7}, v_{c8}, v_{c9}, v_{c10}$	6	4	$-v_{dc}/10$
8	$v_r < v_{c1}, v_{c2}, v_{c3}, v_{c4}, v_{c5}, v_{c6}, v_{c7}$ $v_r \geq v_{c8}, v_{c9}, v_{c10}$	7	3	$-2v_{dc}/10$
9	$v_r < v_{c1}, v_{c2}, v_{c3}, v_{c4}, v_{c5}, v_{c6}, v_{c7}, v_{c8}$ $v_r \geq v_{c9}, v_{c10}$	8	2	$-3v_{dc}/10$
10	$v_r < v_{c1}, v_{c2}, v_{c3}, v_{c4}, v_{c5}, v_{c6}, v_{c7}, v_{c8}, v_{c9}$ $v_r \geq v_{c10}$	9	1	$-4v_{dc}/10$
11	$v_r < v_{c1}, v_{c2}, v_{c3}, v_{c4}, v_{c5}, v_{c6}, v_{c7}, v_{c8}, v_{c9}, v_{c10}$	10	0	$-5v_{dc}/10$

In Table 4.2, $n_{upperArm}$ and $n_{lowerArm}$ are the numbers of SMs which are *On* (S_c is *On* and S_m is *Off* in Figure 4.2) in the upper arm or lower arm, respectively. In an 11-level MMC inverter the total number of SMs with the status of *On* is:

$$n_{upperArm} + n_{lowerArm} = 10 \quad (4.17)$$

In an 11-level MMC inverter, ten upper and ten lower SMs are present, in which each SM has a capacitor. For instance, in voltage level 1 of Table 4.2, all upper SMs should be *Off* and all lower SMs should be *On*, which means that the main switches (S_m) of all upper SMs and the auxiliary switches (S_c) of all lower SMs must be *On* and all other switches must be *Off*. In this case, the input DC voltage is applied only to ten lower capacitors, so that the output voltage is $^{V_{dc}}/_{2}$. Figure 4.7 illustrates the selection of capacitors for various voltage levels shown in Table 4.2.

The most critical issue in controlling MMC is to maintain voltage balance across all capacitors. Therefore, the SM voltages are measured and sorted in descending order during each cycle. If the current flowing through the switches is positive, so that capacitors are being charged, $n_{upperArm}$ and $n_{lowerArm}$ of the SMs in the upper arm and lower arm with the lowest voltages are selected, respectively. As a result, 10 capacitors with lowest voltages are chosen to be charged. Likewise, if the current flowing through the switches is negative, so that capacitors are being discharged, $n_{upperArm}$ and $n_{lowerArm}$ of the SMs in the upper arm and lower arm with highest voltages are selected, respectively. As a result, 10 capacitors with highest voltages are chosen to be discharged. Consequently, voltages of SM capacitors maintain balanced. Considering Table 4.2 and based on the direction of current flowing through the switches, the proper algorithm is selected to maintain capacitor balance.

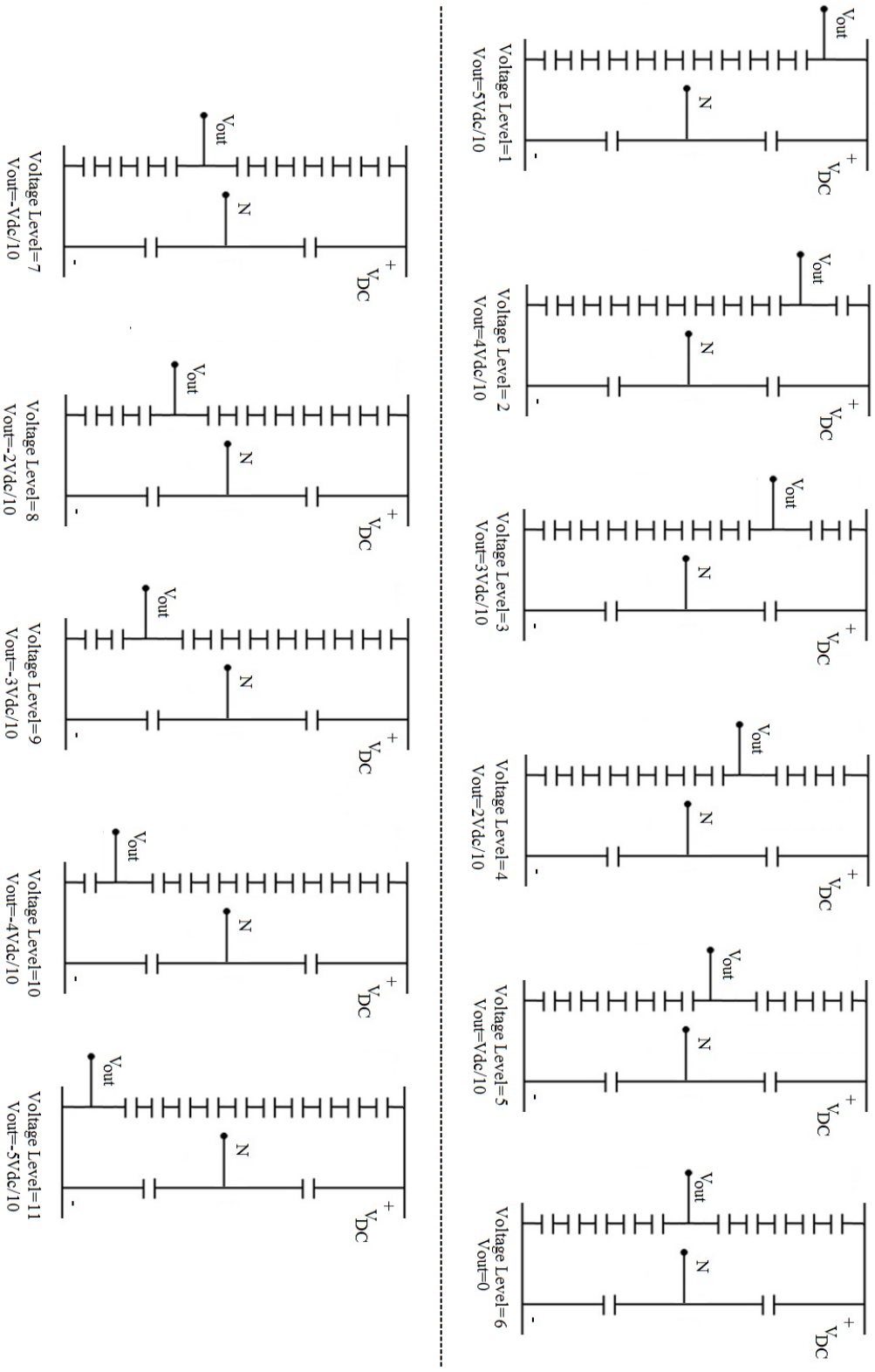


Figure 4.7 Selection of SMs' capacitors for different voltage steps

4.3.3 PWM generator

The third function of the controller system is the PWM generation block. In this block, based on the desired modulation index, power angle, capacitor voltages, direction of current flowing through switches, and using Table 4.2, the controller generates the PWM signals in order to meet all system requirements. The algorithm used in the PWM generator block is:

UNTIL (1)

GENERATE A 60 HTZ SINUSOIDAL REFERENCE SIGNAL WITH UNIT AMPLITUDE

GET MODULATION INDEX, AND POWER ANGLE FROM PI CONTROLLERS

SHIFT THE PHASE OF THE REFERENCE SIGNAL WITH THE VALUE OF POWER ANGLE AND MODIFY ITS AMPLITUDE BY MULTIPLYING THE MODULATION INDEX

GENERATE THE TRIANGLE CARRIER WAVEFORM SIGNALS USING PDPWM TECHNIQUE

COMPARE THE REFERENCE SIGNAL WITH THE TRIANGLE CARRIER WAVEFORMS

USE TABLE 4.2 AND Figure 4.7 TO DEFINE THE VOLTAGE LEVEL AND NUMBER OF REQUIRED CAPACITORS IN UPPER AND LOWER ARM

MEASURE THE CURRENT FLOWING THROUGH THE SWITCHES

IF CURRENT IS POSITIVE, SELECT THE REQUIRED CAPACITORS WITH LOWEST VOLTAGE. APPLY PROPER GATE SIGNALS TO TURN ON AND OFF THE CORRESPONDING SWITCHES

IF CURRENT IS NEGATIVE, SELECT THE REQUIRED CAPACITORS WITH HIGHEST VOLTAGE, APPLY PROPER GATE SIGNALS TO TURN ON AND OFF THE CORRESPONDING SWITCHES

PAUSE FOR ONE MACHINE CYCLE

ENDUNTIL

The above algorithm shows the processes inside the PWM generator block. In fact, this block uses all information from PI controllers, considering the PDPWM method and voltage balancing concept in order to generate the desired gate signals. The generated PWM signals are applied directly to the switches to turn them on and off in order to meet application requirements.

4.5 Design of the proposed inverter in Simulink

The design of the proposed inverter was carried out in MATLAB/Simulink environment using the SimPowerSystems toolbox. Basic design concepts for the 5-level and 11-level are similar, with the only differences of inverter structure (number of switches and capacitors) and the expansion of the PDPWM method used to generate PWM signals. Figure 4.8 shows an overview of various parts of the inverter system.

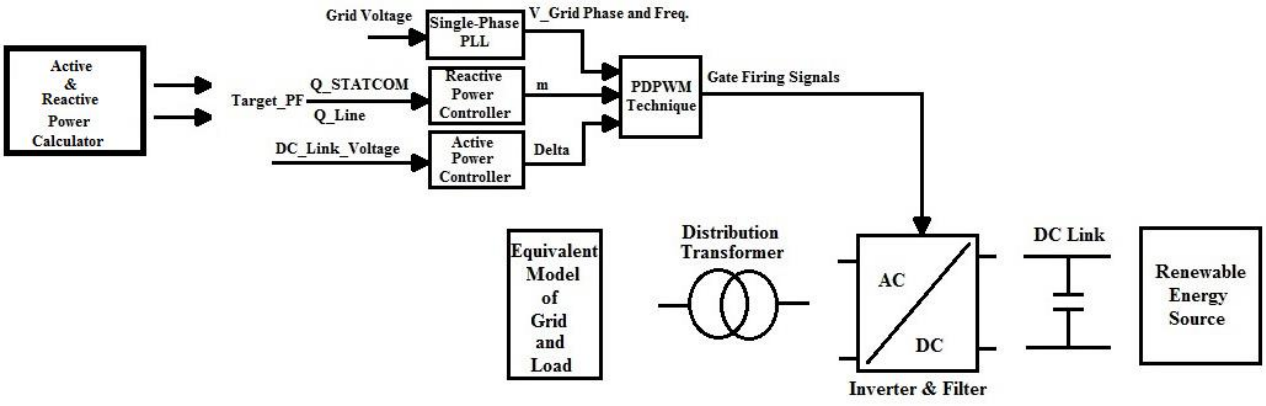


Figure 4.8 Overview of the proposed inverter design

The design of the inverter consists of six distinct parts including the wind turbine model, the inverter model, the power grid model, the controller model, the load model, and the PQ calculator model. The complete configuration of the system in MATLAB/Simulink is shown in Figure. 4.9.

4.5.1 The wind turbine model

Two controlled-current sources are used to model power generated by a wind turbine. These current sources generate varying wind turbine output power by varying the current while the voltage is fixed. A timer component, which is a component generating a signal change at specified times, varies the input of current sources. This timer is used to simulate wind speed changes. The generated power is then rectified by a 3-phase AC-DC rectifier using diodes. The output voltage and current of the rectifier is then measured making the instantaneous and average power feeding the DC link of the inverter. A 1 mH inductance is used between the rectifier and the DC link voltage in order to limit the current change.

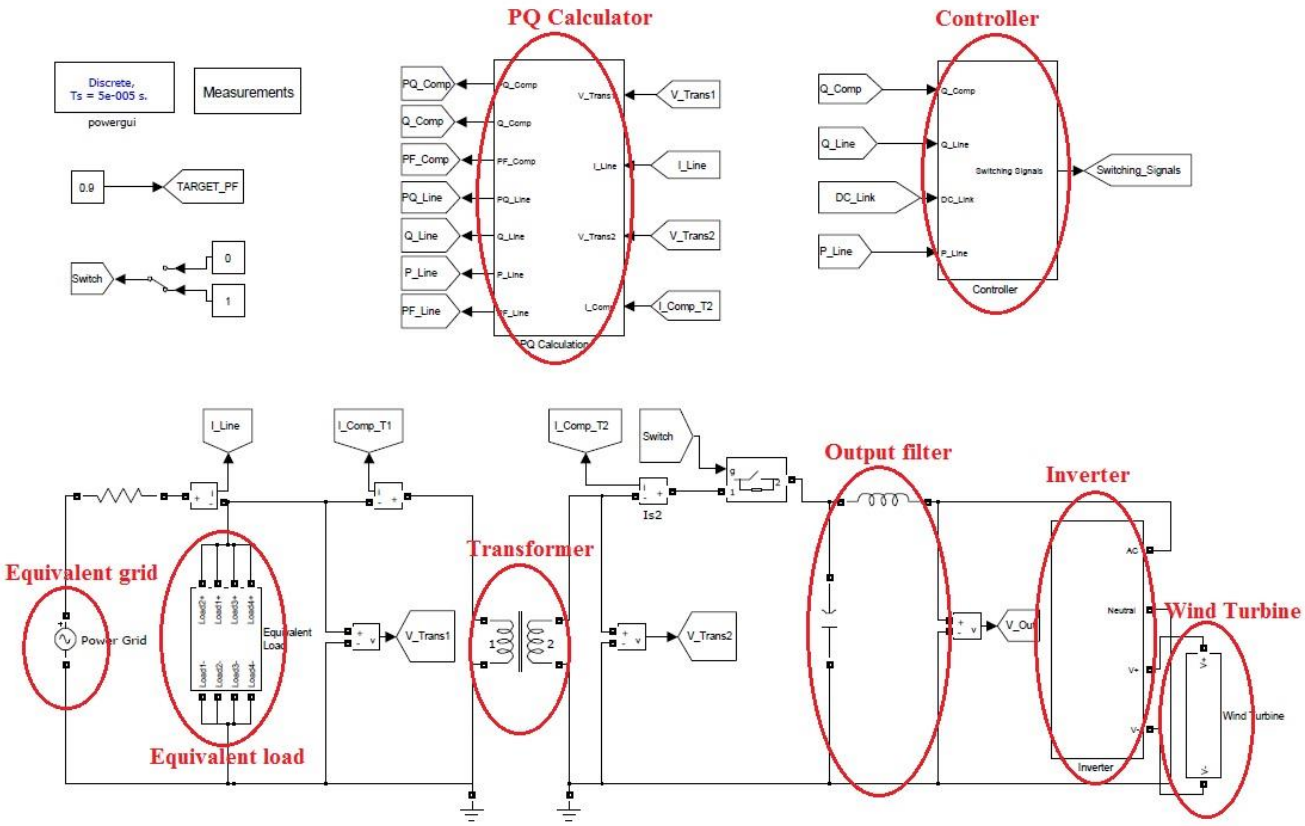


Figure 4.9 Complete configuration of the proposed inverter system in Simulink

The disadvantage of this wind turbine model is that the generated power is a function of the DC link voltage and the amplitude of the current, meaning that the current sources can affect DC link voltage stability. Another wind turbine model is to use a variable-speed three-phase permanent magnet (PM) generator connected to a three-phase rectifier. The rectified output can be delivered to the DC link of the inverter. In this simulation, the first model is used. Figure 4.10 shows the block diagram of the wind turbine model used for the simulation.

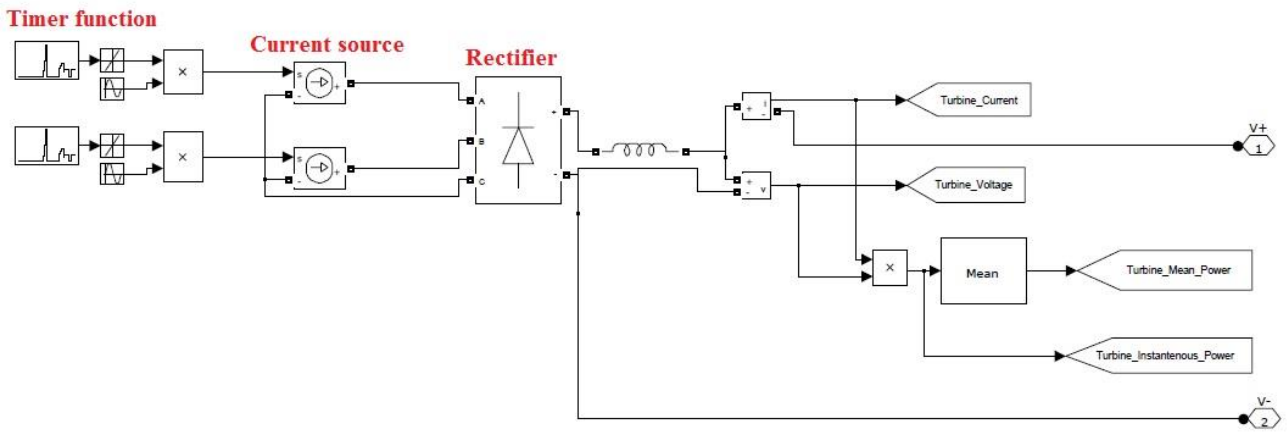


Figure 4.10 Block diagram of the wind turbine

4.5.2 The inverter model

Figure 4.11 shows the block diagram of the single-phase 5-level inverter using MMC topology. As shown, there are 4 upper and 4 lower SMs where each SM has two switches and a capacitor. The DC link consists of two DC capacitors which define the neutral point of the inverter. There is one inductance in each arm which provides current control and protection. The DC link voltage and the voltage of each SM capacitor are measured and then processed by the controller system in order to control the DC link voltage as well as performing voltage balancing among all SM capacitors. The only difference for the 11-level model, shown in Figure 4.12, is the number of SMs which is increased to 10 upper and 10 lower SMs. The 11-level model possesses 40 switches and 20 SM capacitors.

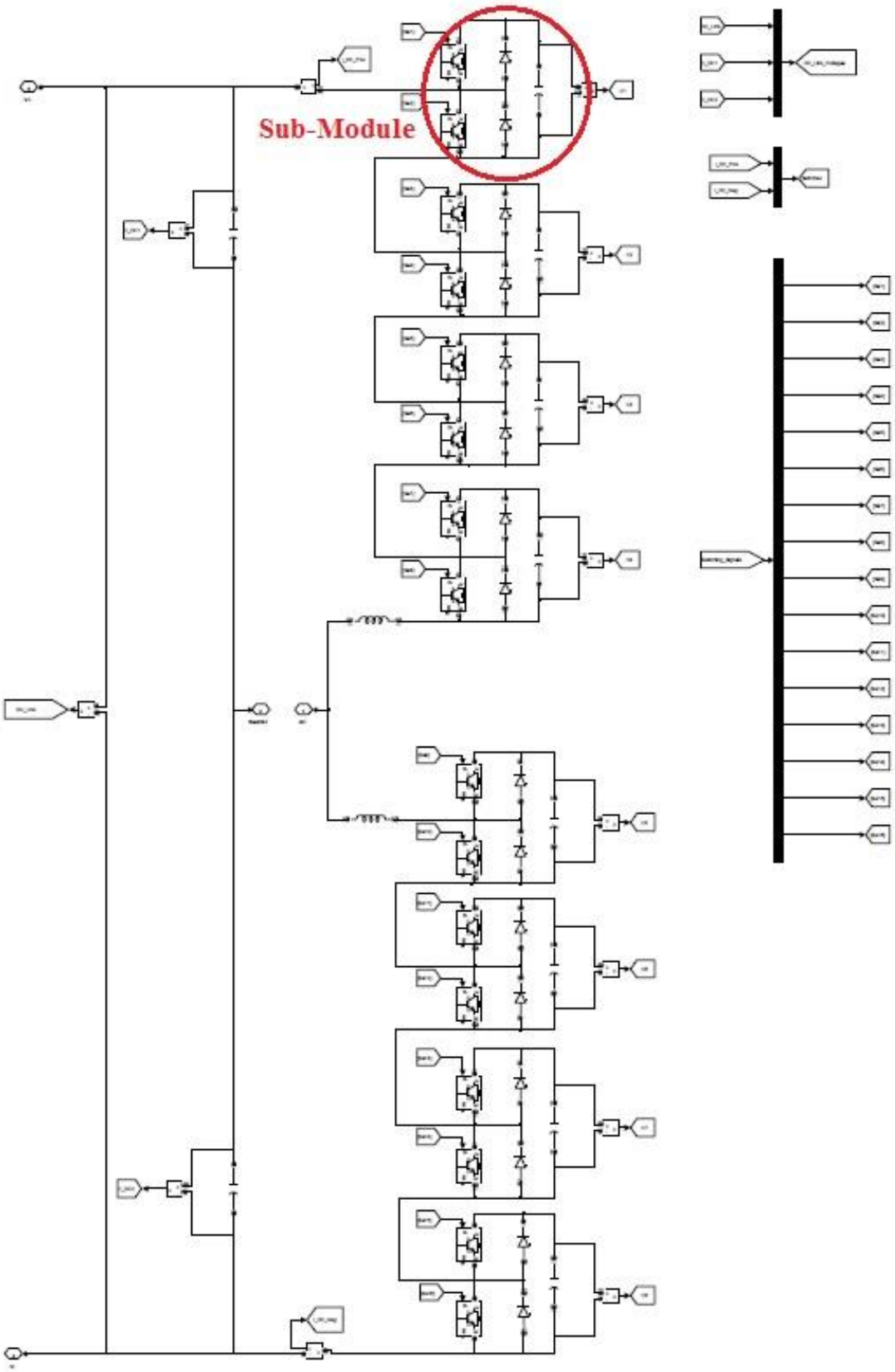


Figure 4.11 Structure of the 5-level inverter using MMC topology in Simulink

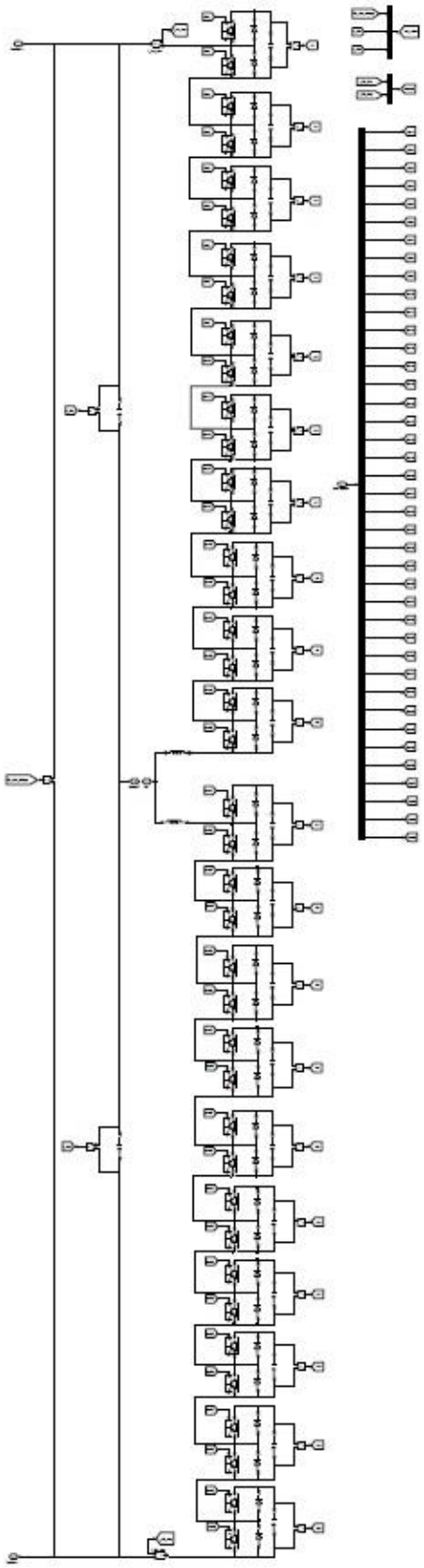


Figure 4.12 Structure of the 11-level inverter using MMC topology in Simulink

4.5.3 The local distribution grid and load model

The Thevenin equivalent model of the local distribution grid is created using an AC voltage source in series with a resistor and inductance. The frequency of the AC source is set to 60 Hz, the RMS value of the AC source voltage is equal to 12000 V, and the value of the equivalent resistor is set to 5 ohms. Figure 4.13 shows the block diagram used for the equivalent power grid.

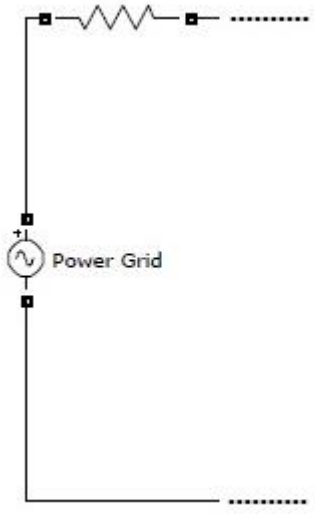


Figure 4.13 Model of the equivalent distribution grid in Simulink

4.5.4 The controller model

The controller of the proposed inverter consists of several parts including the modulation index controller, the delta controller, and the PWM controller. The main function of the controller is to generate the proper gate signals to turn switches on and off in order to meet application requirements. Each part of the controller was previously explained in Section 4.4. Implementation of the controller in the Simulink environment is shown in Figure 4.14. Figures 4.15 and 4.16 show the interior of the modulation index controller and power angle controller blocks, respectively. The function of the modulation index controller is to determine the modulation index to be used by the reference signal generator. This parameter is the primary governor of reactive power compensation and its major function is to make the PF of the grid equal to the desired PF set by the utility. This block calculates the desired change in reactive power on the feeder line, compares it to the inverter operating limits, and finally delivers the signal into a PI controller to generate the modulation index. In order to reduce oscillations of the modulation index, a “Mean block” is placed before the PI controller to stabilize controller input.

The function of the power angle controller is to maintain the DC link voltage at a constant reference value. Therefore, the amount of active power transferred between the STATCOM and the grid can be controlled. The DC link voltage is kept constant by maintaining proper charge on the DC link capacitors. In order to reduce the oscillations of the power angle, a “Mean block” is placed before the PI controller to stabilize the input of the controller. Figures 4.17 (a) and 4.17 (b) show the block diagrams of the PWM controller block for the 5-level and 11-level inverter using MMC topology. The left part of Figure 4.17(a) shows the reference signal generator. A phase-locked loop (PLL) is used in this portion to provide the controller with the frequency and phase of the grid in order to generate the reference sinusoidal signal (The PLL is responsible for acquiring the grid frequency and providing that signal for the rest of the controller). In this design, the Simulink 1-phase PLL block is used. The middle part of the figure shows the carrier signals generator for PDPWM technique. The right portion of the Figure shows two MATLAB function blocks which perform voltage balancing and PWM signals generation. This part is the major part of the controller system which defines the output voltage level based on Table 4.2. Therefore, based on current direction and SM capacitor voltages, this part generates proper switching signals. The complete code for the Embedded Functions blocks (1 & 2) is provided in Appendix A and B, respectively (for the 11-level inverter). For the 5-level inverter, this code is much simpler than the 11-level inverter.

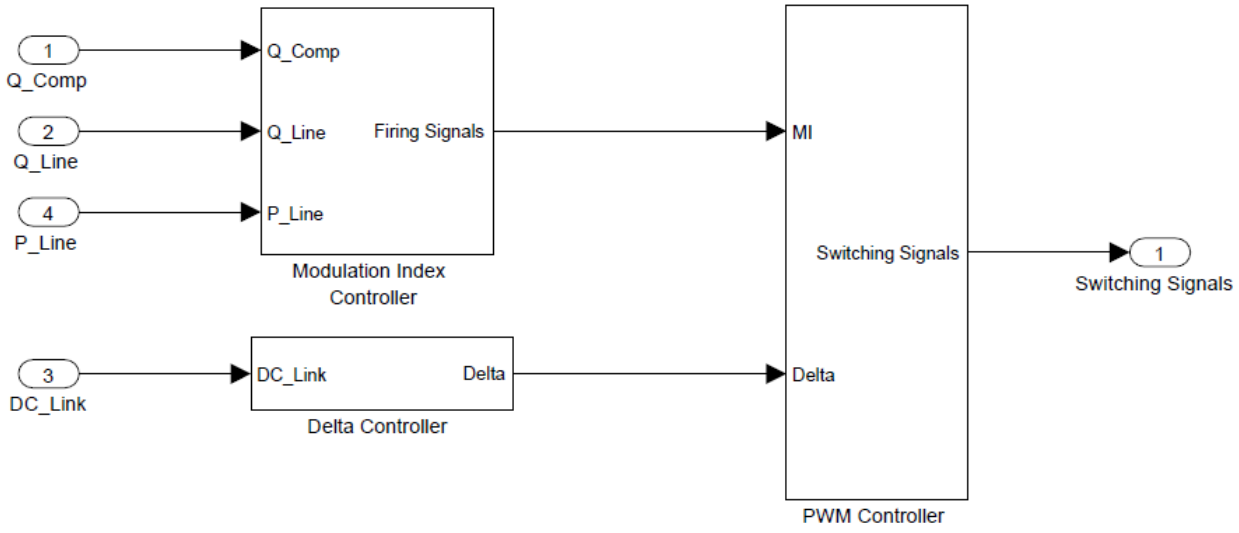


Figure 4.14 Block diagram of the controller in Simulink

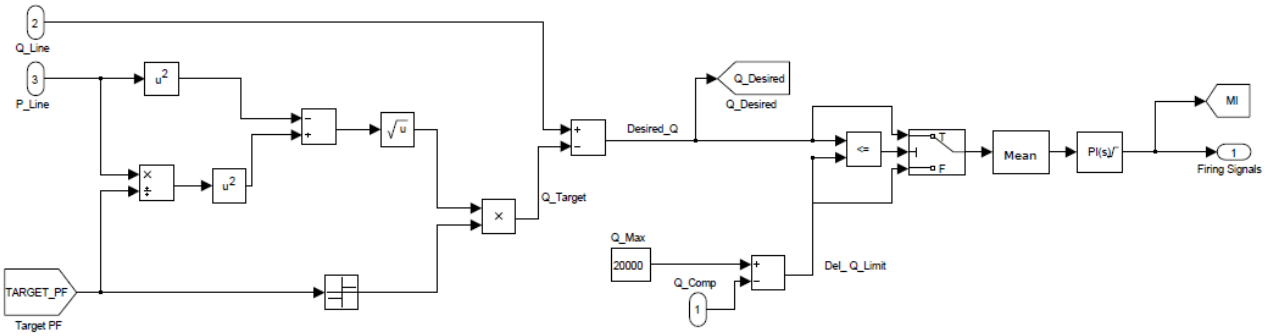


Figure 4.15 Block diagram of the modulation index controller in Simulink

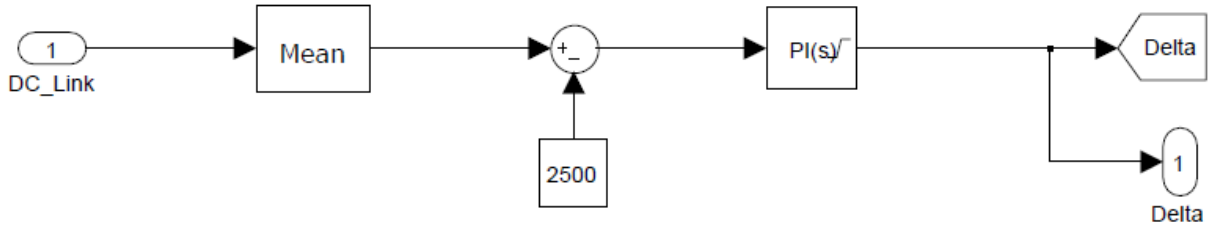
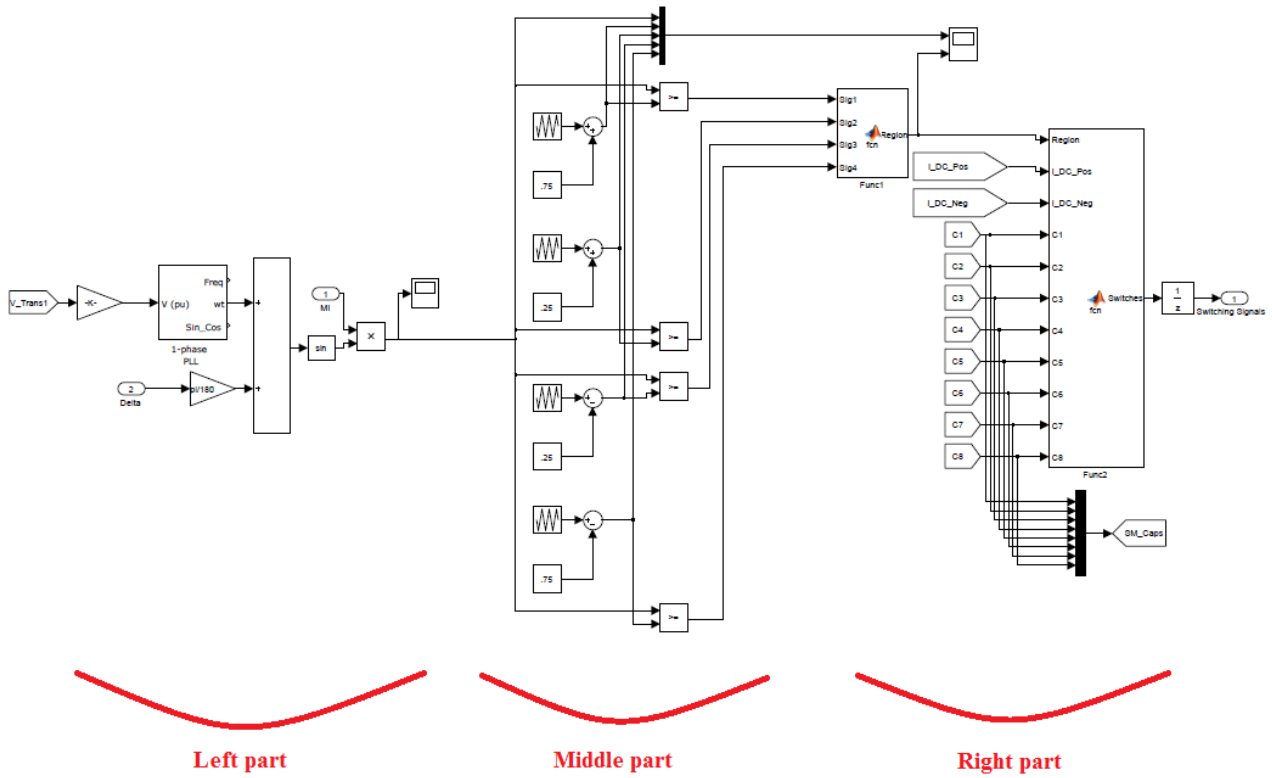
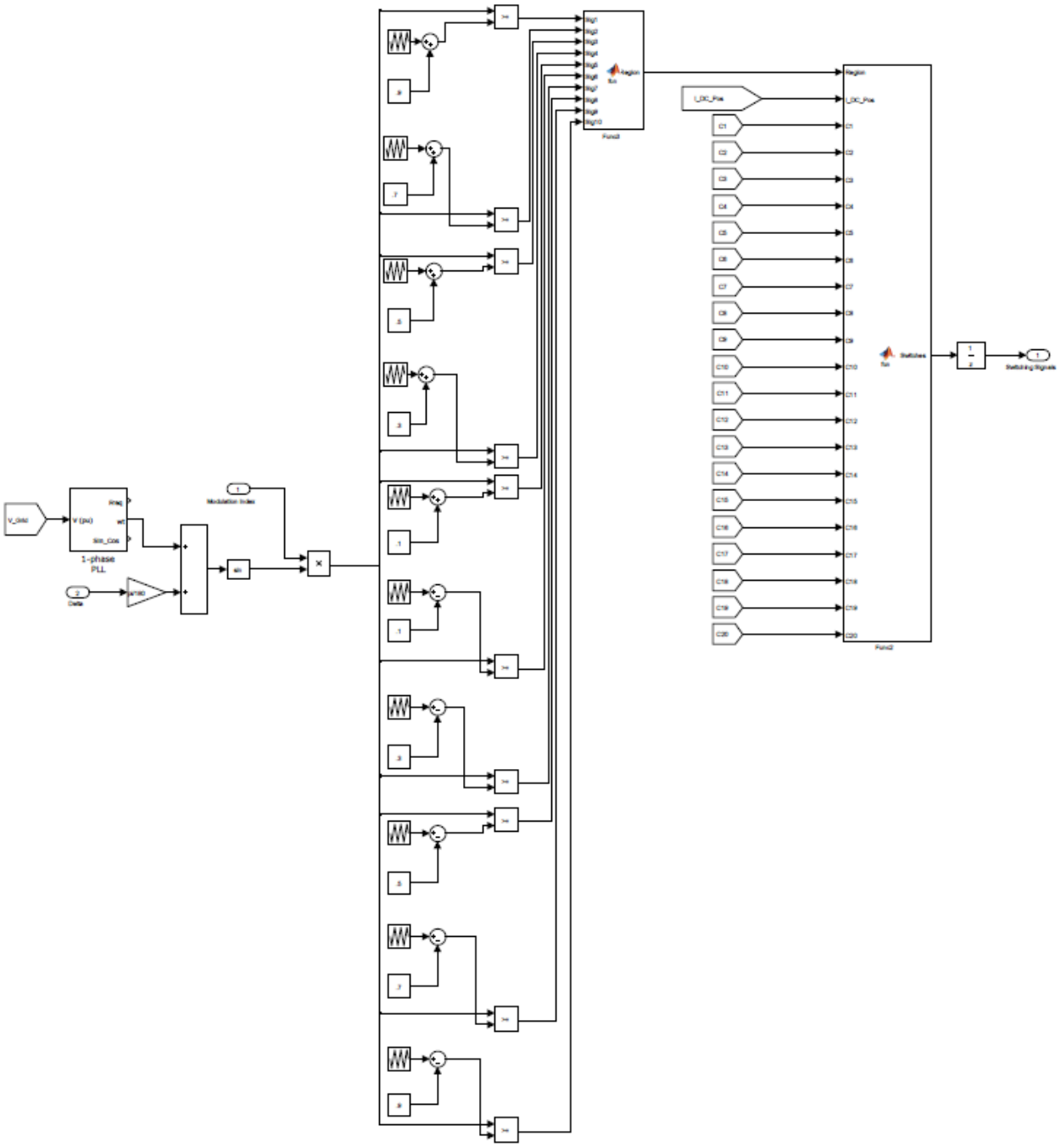


Figure 4.16 Block diagram of the power angle controller in Simulink



(a)



(b)

Figure 4.17 Block diagram of the PWM controller in Simulink for (a) 5-level, (b) 11-level

4.5.5 The load model

The equivalent model of the distribution load is defined by this sub-system in the Simulink model. The load is created using four SimPowerSystems parallel load branches. Load values are:

1) load1: 50 kW active power and 35 kVAR inductive reactive power, 2) load2: 50 kW active power and 28 kVAR inductive reactive power, 3) load3: 10 kW active power and 3 kVAR inductive reactive power, and 4) load4: 5 kW active power and 11 kVAR inductive reactive power. By selecting various combinations of these loads, different PFs can be achieved. These values are selected to exaggerate inverter effects on a real distribution system. The active and reactive loads of the distribution grid are much larger and a single inverter of the proposed size can have a small effect on the overall system. Therefore, multiples of this inverter should be used in order to reach the desired compensation. Figure 4.18 shows the equivalent load model in Simulink.

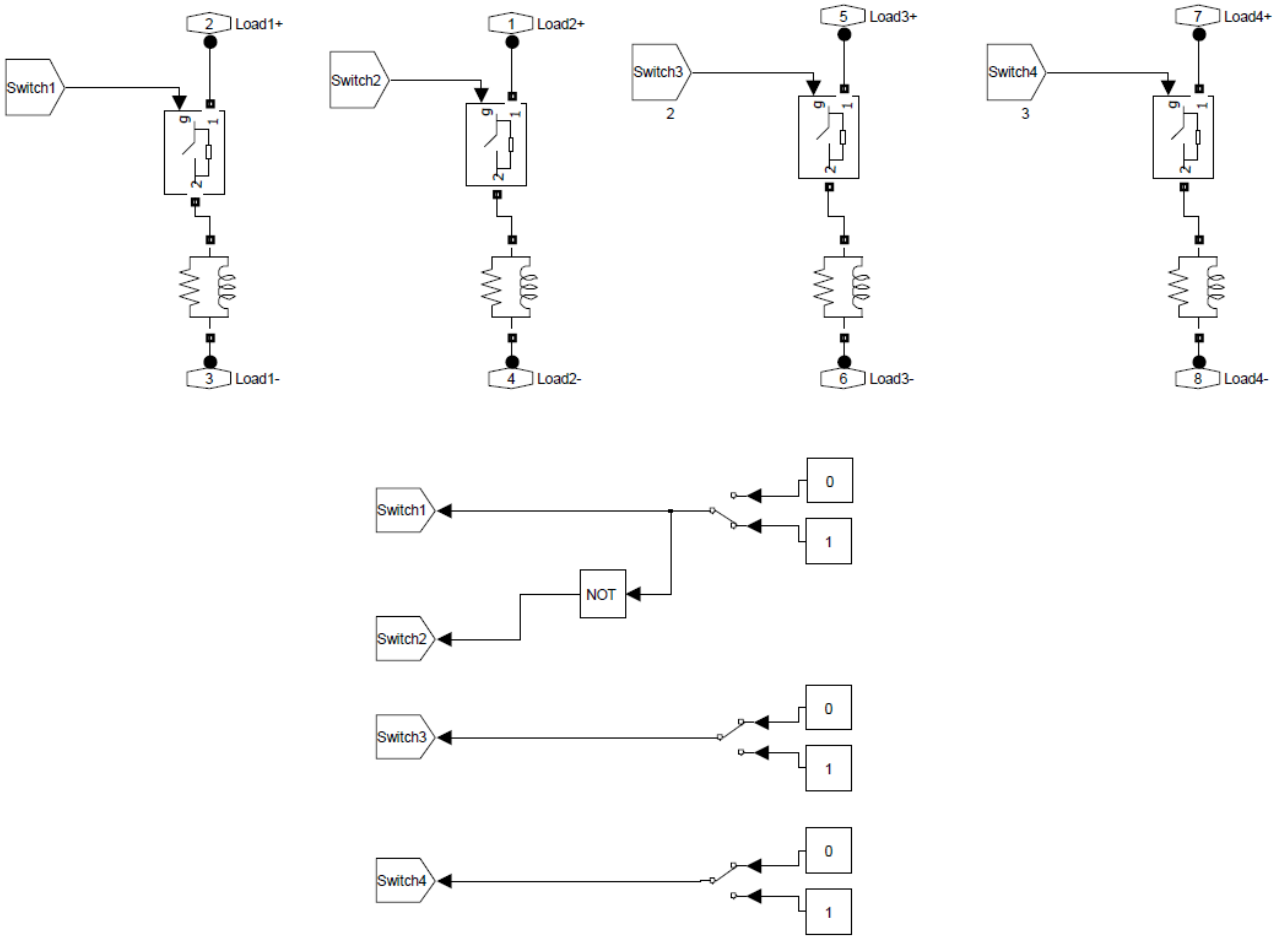


Figure 4.18 Model of the equivalent distribution load in Simulink

4.5.6 The PQ calculator model

The function of the PQ calculator block is to calculate the required signals for the controller. This block calculates the active and reactive power of the grid, the active and reactive power

provided by the inverter, and the grid power factor by using the four primary signals, which are voltage and current of the grid and voltage and current of the inverter. In practice, acquiring real-time measurements of the voltage and current on the grid requires current and voltage sensors (transducers) to be placed on the grid lines. Figure 4.19 shows the PQ calculator model in Simulink.

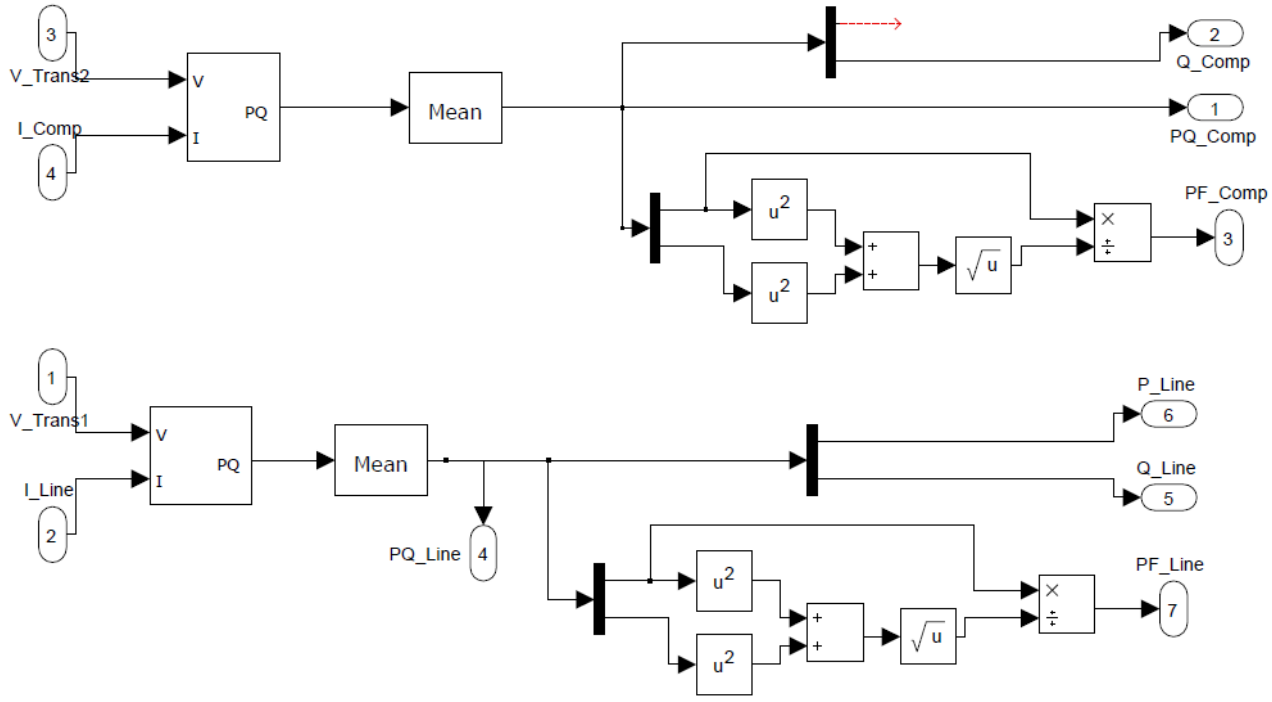


Figure 4.19 Model of the PQ calculator in Simulink

Simulation results for the proposed 5- and 11-level inverter are described in Chapter 5.

4.6 Summary

In this chapter, an inverter with D-STATCOM capability was proposed and modeled in MATLAB/Simulink. As previously mentioned, the proposed inverter is categorized as custom power electronics, as it is a combination of two different devices (inverter and STATCOM). The primary focus of the present research is to demonstrate the application of custom power electronics in renewable energy systems.

Using regular STATCOMs for small- or medium-size single-phase wind applications does not make economic sense because the cost of the system increases significantly, thus creating opportunity to use smarter inverters with FACTS capabilities in order to be cost-effective and compatible with IEEE standards. The proposed inverter in this research is equipped with a D-

STATCOM option to regulate reactive power of local distribution lines. The function of the proposed inverter is to convert DC power coming from the DC link to a suitable AC power for the main grid and, to fix the PF of the local grid at a target PF by injecting sufficient reactive power to the grid.

In the design of the proposed inverter with D-STATCOM capability, several issues were considered: 1) efficiency, 2) standards compatibility, and 3) cost. Between all multi-level inverter topologies, modular multi-level converter (MMC) is seen to be a proper candidate for this application.

MMC is a converter system comprised of arbitrary numbers of identical half-bridge (HB) sub-modules (SMs). Generally, an n-level single-phase MMC inverter consists of a series connection of $2(n-1)$ basic SMs, two buffer inductors, and two DC capacitor, which translates to $4(n-1)$ switches and $2(n-1)$SM capacitors. This topology offers many advantages over conventional two-level or multi-level topologies and, therefore, can be used in a wide range of applications, including renewable energy systems, DC power transmission, or micro grid.

To proposed control strategy uses the phase disposition pulse width modulation (PDPWM) technique. The aim of the inverter is to control the PF of the local distribution grid at a target value set by the user (utility grid). This application requires the independent control of active and reactive power transferred between the inverter and the grid. Hence, the proposed controller consists of three major functions. The first function is to control the active and reactive power transferred between the inverter and the power line, the second function is to keep the voltages of the SM capacitors balanced, and the third function is to generate desired PWM signals. Application of the proposed inverter requires independent control of both active and reactive power, so that if wind is blowing, the device should operate as a normal inverter in addition to being able to fix the PF of the local grid at a target PF. If no wind is present, the device should only operate as a D-STATCOM to regulate PF of the local grid. This makes two modes of operation: 1) when wind is blowing and active power is coming from the wind turbine: the "inverter plus D-STATCOM" mode and 2) when wind speed is zero or too low to generate active power: the "D-STATCOM" mode. In this case, the inverter is acting only as a source of reactive power to control the PF of the grid, as a D-STATCOM. This option eliminates the use of additional capacitor banks or external STATCOMs to regulate the PF of the distribution feeder lines.

Active power transfer between the inverter and grid is controlled by adjusting the power angle (δ), or the angle between voltages of the inverter and the grid, and reactive power is regulated by the modulation index (m).

One important function of the controller is to maintain SM capacitor voltages balanced. Therefore, the SM voltages are measured and sorted in descending order during each cycle. Based on the current direction flowing through the switches, the proper switching algorithm is selected and applied.

In the PWM generation block of the controller, based on the desired modulation index, power angle, capacitor voltages, and direction of current flowing through switches, the controller generates the PWM signals in order to meet all system requirements.

Finally, the design of the proposed inverter was carried out in MATLAB/Simulink environment using the SimPowerSystems toolbox. Basic design concepts for the 5-level and 11-level are similar to each other. Implementing the inverter model, controller system, wind turbine, grid, and equivalent loads used for the simulations have been explained in detail.

Chapter 5 - Simulation results

5.1 Overview

Simulations for the 5- and 11-level model are performed in MATLAB/Simulink environment. This environment is chosen because of its simplicity in modeling the inverters and the controller system. Simulink offers an embedded set of tools (such as SimPowerSystems) for the simulation of electrical systems which is used to build the entire inverter and grid system. Simulink standard blocks can be used to implement the control algorithm and they can be easily connected to SimPowerSystems blocks. Simulation results of Simulink are not as accurate as the results of pSpice. However, implementing the inverter structure and the controller system in pSpice is very difficult as it is a specific environment designed only for circuit simulation.

The S-Function is an interesting block in the Simulink environment used specifically for implementing continuous and discrete systems in the input-state-output form. This block can be deployed to produce systems not present in the Simulink library. These blocks can be used to write code in M-code, which is high-level programming language similar to the C-code. The use of M-code and S-Function structure simplifies the simulation. In the 5- and 11-level inverter simulation, the S-Function block (PWM generator block) performs the function of the DSP or any other type of Microcontroller in real systems. In other words, this block must generate the switching gate signals, in the same way a DSP generates signals. Therefore, the block must change outputs every time a new switching state is required based on inputs. Figure 5.1 shows the structure of a typical S-Function.

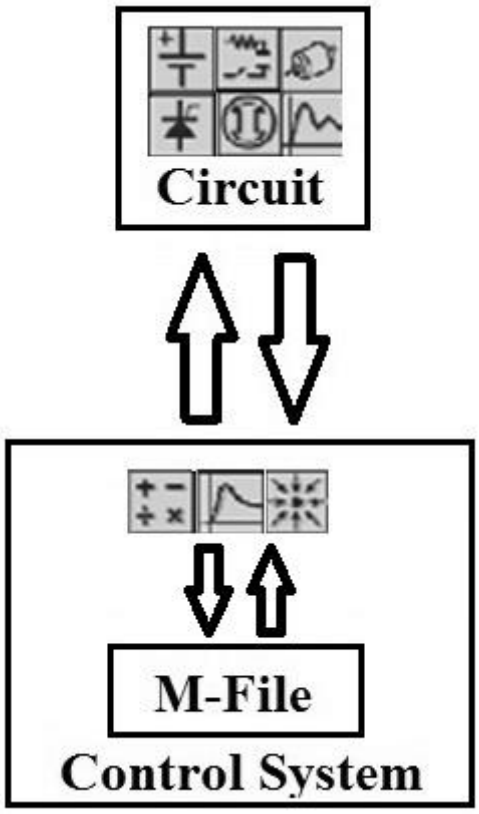


Figure 5.1 Structure of a typical S-Function

5.2 5-Level inverter (20 kW/kVAR)

The simulation of the proposed 5-level inverter is 45 seconds long and contains two parts. The first part demonstrates the performance of the proposed inverter for various load combinations making different PFs. In the second portion of the simulation, severe ramping and de-ramping of input active power of the inverter from the wind turbine is applied. The function of the inverter in all cases is to transfer active power from the wind turbine to the distribution grid as well as to compensate the PF of the local distribution grid at the target PF of 0.90. In other words, the inverter must function as a regular wind energy inverter which possesses a D-STATCOM option in order to fix the PF of the grid at the target value set by the utility (target PF in this simulation equals 0.90), regardless of load changes or input active power from the wind turbine due to wind speed variation. Table 5.1 shows the parameter values used for the simulations.

Table 5.1 Parameter values used for the 5-level inverter simulation

Parameter	Value
L_{line}	1 mH
R_{line}	1 Ohm
L_{filter}	25 mH
C_{filter}	90 uF
Transformer power rating	25 kVA
Transformer primary voltage	12000 V
Transformer secondary voltage	600 V
Switching frequency	4 kHz
Target PF	0.90
DC link reference value	2500 V
Initial voltages of DC link capacitors	1250 V
Initial voltages of SM capacitors	625 V
Transformer inductance	$R_1 = 0.001\ p.u.$, $L_1 = 0.001\ p.u.$ $R_2 = 0.001$ p.u., $L_2 = 0.002\ p.u.$

As mentioned in Section 4.5.1, in order to simulate the wind turbine two timer functions that handle two current sources in conjunction with a rectifier are used. Discrete intervals for the amplitudes of the current controlled sources are given in Table 5.2. The output active power provided by the controlled current source of the wind turbine model is calculated by multiplying the amplitude of the current by the DC link voltage. Before t=19 s, the input active power from the wind turbine is zero, implying that the wind speed is zero or too low to produce active power. At the 19th second of the simulation, power provided by the wind turbine ramps up to 18.5 kW in four seconds and then ramps down to zero in seven seconds.

Table 5.2 Discrete intervals for amplitudes of current sources used in turbine model

Time (s)	Current source amplitude (A)	Time (s)	Current source amplitude (A)
0	0	23	0
1	0	24	0
2	0	25	0
3	0	26	0
4	0	27	0
5	0	28	0
6	0	29	0
7	0	30	0
8	0	31	0
9	0	32	4
10	0	33	5
11	0	34	6
12	0	35	6
13	0	36	2
14	0	37	3
15	0	38	3
16	0	39	3
17	0	40	0
18	0	41	0
19	2.5	42	3
20	7.5	43	3
21	15	44	3
22	7.5	45	3

Starting at 30 s, there is no wind production for two seconds, and then at t=32 s, the wind turbine power ramps up again to 15 kW in three seconds and then ramps down again to 2 kW in seven seconds, subsequently rising to 7.5 kW. These variations show a severe condition and are only used to assess controller system performance since real situations would not have such an

extreme change in power production of a wind turbine. Output active power from the wind turbine (input power to the inverter) is shown in Figure 5.2.

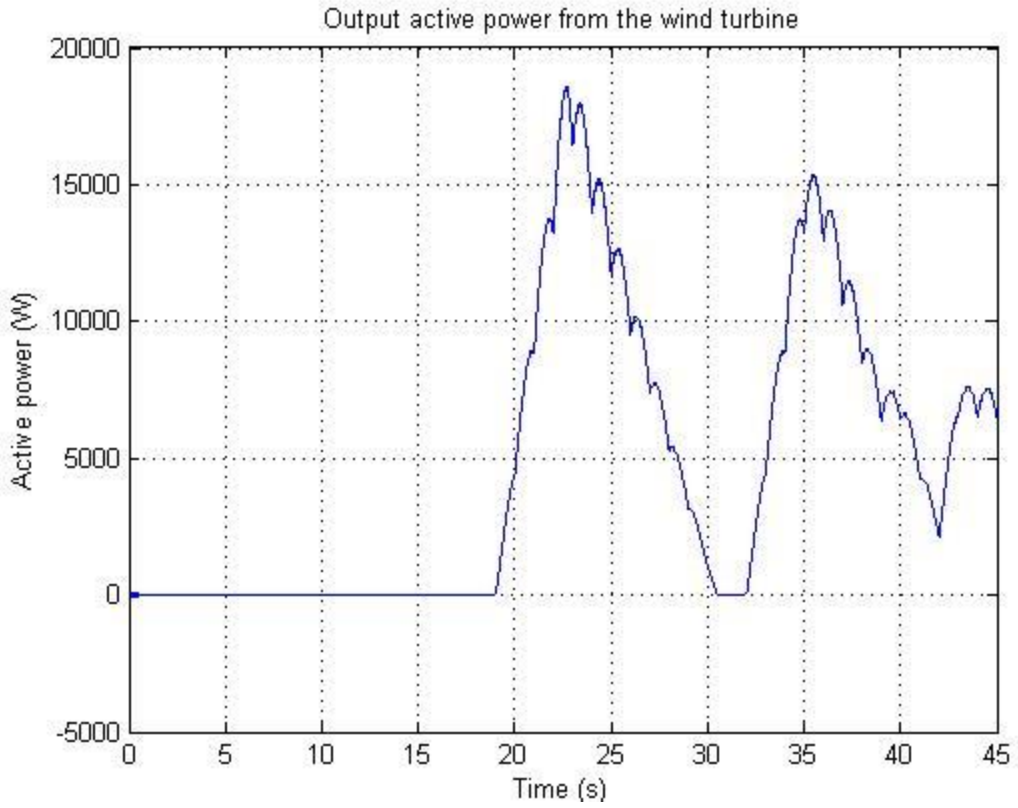


Figure 5.2 Output active power from the wind turbine

To demonstrate the performance of the proposed controller in various conditions, the PF of the load varies by selecting different combinations of the loads. The simulation begins with the selection of only load1 making the PF 0.82. At t=3 s, the PF of the load is changed to 0.87 by selecting load2 instead of load1. After three seconds, load3 is added to load2 making the PF 0.89. At t=8 s, load4 is also added to load2 and load3 making the PF 0.84. At t=10 s, load3 is removed, resulting in load2 and load4 again making the PF 0.81. After two seconds, load4 is also removed, resulting in having only load2, which makes the PF 0.87. Subsequently, at t=14 s, load1 is replaced by load2 making the PF 0.82 again. After this time, no load changes occur and, as a result, no PF variation. The process of load variation in respect to time is shown in Table 5.3. This is to show the performance of the system in subject to different load combinations. After t=14, the load PF is fixed at 0.82. The function of the proposed inverter is to fix the PF of the local distribution grid at the target PF, which is 0.90 in this case, regardless of load or wind speed changes.

Table 5.3 Equivalent distribution load variations in respect to time

Time (s)	Loads combination	Resulted load's P & Q	Resulted load PF	Target PF
0	1	50 kW, 35 kVAR	0.82	0.90
1	1	50 kW, 35 kVAR	0.82	0.90
2	1	50 kW, 35 kVAR	0.82	0.90
3	2	50 kW, 28 kVAR	0.87	0.90
4	2	50 kW, 28 kVAR	0.87	0.90
5	2	50 kW, 28 kVAR	0.87	0.90
6	2+3	60 kW, 31 kVAR	0.89	0.90
7	2+3	60 kW, 31 kVAR	0.89	0.90
8	2+3+4	65 kW, 42 kVAR	0.84	0.90
9	2+3+4	65 kW, 42 kVAR	0.84	0.90
10	2+4	55 kW, 39 kVAR	0.81	0.90
11	2+4	55 kW, 39 kVAR	0.81	0.90
12	2	50 kW, 28 kVAR	0.87	0.90
13	2	50 kW, 28 kVAR	0.87	0.90
14	1	50 kW, 35 kVAR	0.82	0.90
15	1	50 kW, 35 kVAR	0.82	0.90
16	1	50 kW, 35 kVAR	0.82	0.90
17	1	50 kW, 35 kVAR	0.82	0.90
18	1	50 kW, 35 kVAR	0.82	0.90
19	1	50 kW, 35 kVAR	0.82	0.90
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
43	1	50 kW, 35 kVAR	0.82	0.90
44	1	50 kW, 35 kVAR	0.82	0.90

After the simulation begins, the inverter provides enough compensation to raise the PF to its target value of 0.90 regardless of equivalent load variations. As soon as the inverter provides

reactive power compensation, the amount of reactive power provided by the feeder line to the load decreases. After t=19 s, output power of the wind turbine increases and, consequently, the level of active power provided by the feeder line decreases by the same amount. The PI controller coefficients used for the 5-level simulation, obtained by trial and error method, are listed in Table 5.4.

Table 5.4 Coefficients used for PI controllers

PI Controller	Coefficient
Power angle controller	$K_p = 0.05$ $K_I = 0.2$
Modulation index controller	$K_p = .00001$ $K_I = .0001$

5.2.1 Output voltage and current of the inverter

The simulated output voltage of the proposed 5-level inverter before and after the filter is shown in Figure 5.3.

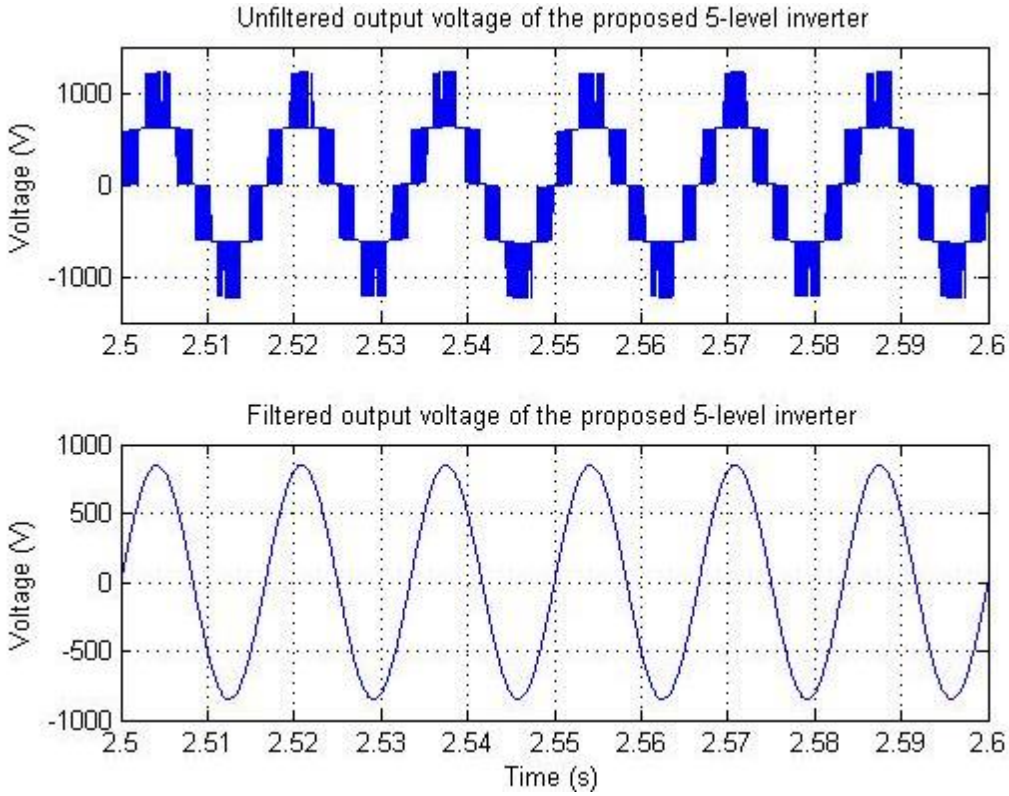


Figure 5.3 Simulated output voltage before and after the filter

In the above Figure, the output voltage RMS value of the inverter before the filter is 650 V representing the filter voltage drop of 7% which is more than the standard value. The total harmonic distortion (THD) of the output voltage of the inverter after the filter is 0.24%. Figures 5.4 and 5.5 show the Fast Fourier Transform (FFT) of the unfiltered and filtered output voltage of the 5-level inverter, respectively.

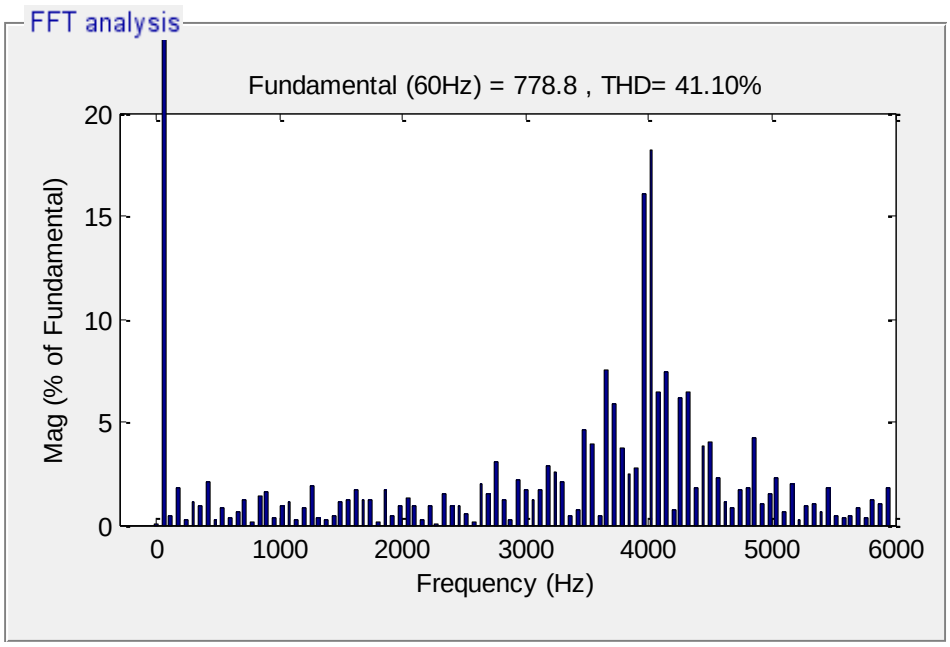


Figure 5.4 FFT of the unfiltered output voltage of the 5-level inverter

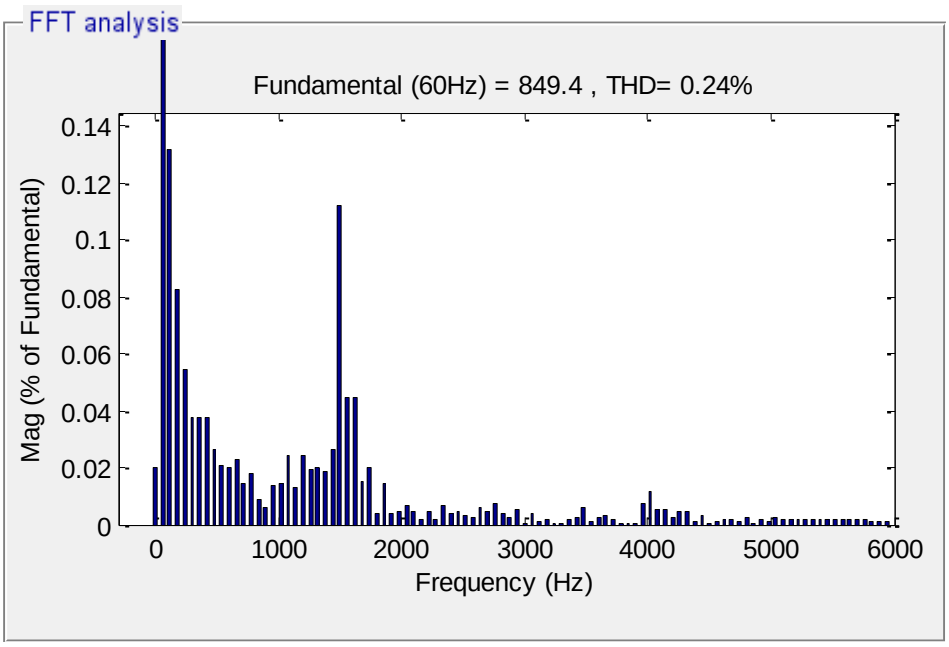


Figure 5.5 FFT of the filtered output voltage of the 5-level inverter

In PWM methods, individual harmonics of the output waveform typically are shifted to a higher frequency. The amount of shift depends on the ratio of carrier frequency to frequency of the fundamental component. In other words, frequencies of the harmonics are increased by the frequency of the carrier waveform. Figure 5.4 shows the THD of the output voltage of the inverter before the output filter. As expected, the most significant harmonic orders are near $n * f_s$ frequencies where f_s is the switching frequency of the inverter, in this case $f_s = 4\,kHz$. In addition, sub-harmonic orders are present below and above these frequencies, as shown in Figure 5.4. Figure 5.5 shows the output voltage of the inverter after the output filter in which the amplitude of the redundant harmonics is decreased significantly. It should be noted that the output filter for the 5-level is a second-order LC filter, which significantly decreases amplitude of the redundant harmonics. Figure 5.5 demonstrates that a number of harmonics with very little amplitude still exist. These harmonics have no effect on waveform quality. Considering voltage values of the primary and secondary side of the transformer, the output current of the inverter-side is significantly greater than the current on the grid-side. Figure 5.6 shows the current on both sides of the distribution transformer. A minor variation is in the output current of the inverter, which may cause problems for the output power of the inverter. One possible reason of this variation could be the operation of the controller system in balancing SM capacitors.

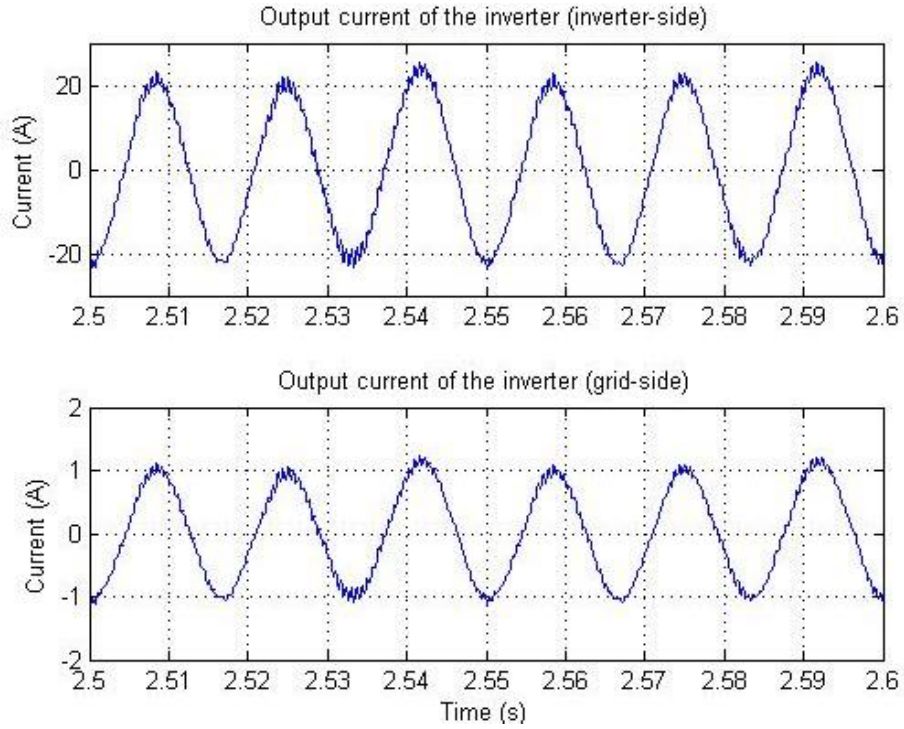


Figure 5.6 Output current on both sides of the distribution transformer

The THD of the output current on the inverter-side of the distribution transformer is 5.83%. Figure 5.7 shows the FFT of the inverter-side output current.

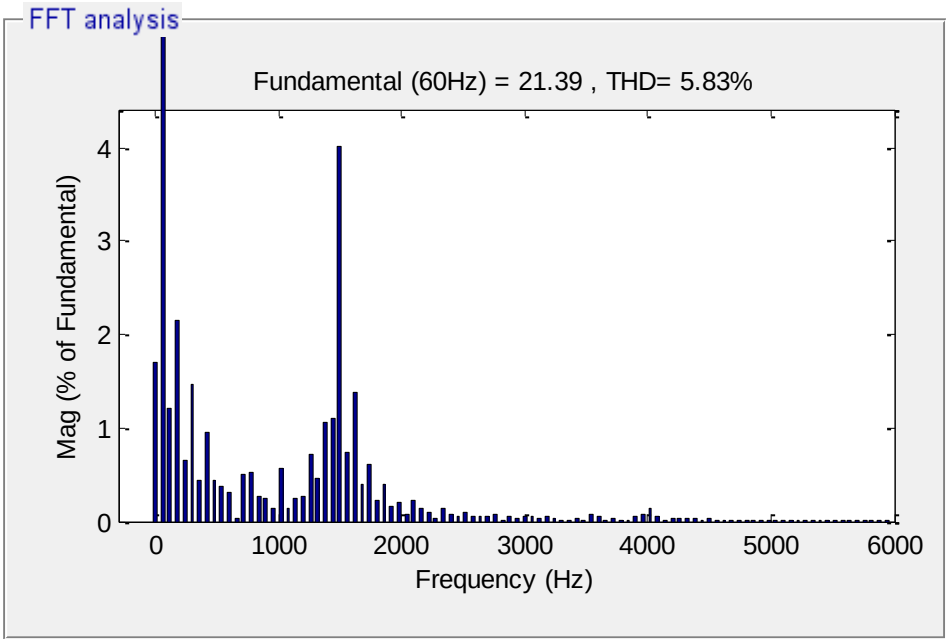


Figure 5.7 FFT of the inverter-side current

Figures 5.7 illustrates that the THD of the output current of the proposed inverter is not completely compliant with IEEE 519 standard since the amplitude of each single harmonic should be less than 3% of the fundamental frequency and the THD should be less than 5%. As shown, the output filter could eliminate the harmonics with frequencies of $n * f_s$, but other harmonics such as the 25^{th} order (1500 Hz), which is approximately 4% of the fundamental value of the output current, have been generated by the filter. However, the use of larger filters would eliminate more of the undesired harmonics.

5.2.2 Power factor of the local distribution grid

The target power factor on the grid is set to 0.90 while the loads demand various PF. The function of the inverter is to fix the PF of the local grid at the target value regardless of the load changes or wind speed variations. The inverter must compensate the reactive power on the grid by injecting reactive power while operating as a regular inverter in order to transfer active power to the grid. Figure 5.8 shows the PF of the local distribution grid.

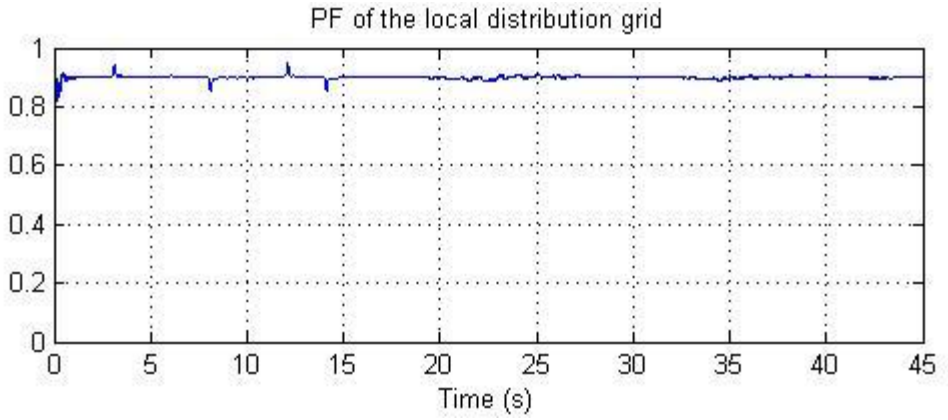


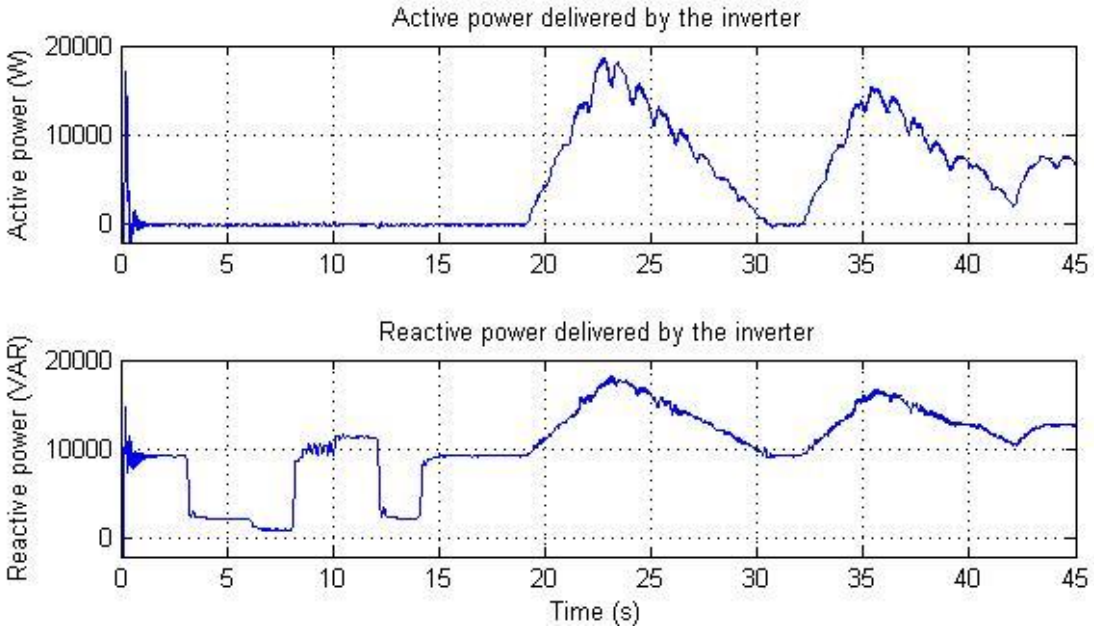
Figure 5.8 PF of the local distribution grid

Beginning at the 0th second, the PF of the line is 0.82 lagging as it is defined entirely by the load. As soon as the simulation initiates, the inverter provides compensation and the PF is adjusted to the target value. As shown, the PF of the grid is constant at the target PF (target PF=0.90) for the entire simulation time, regardless of the load variation and input active power changes from the wind turbine. However, some variations occur during rapid changes in loads or large active power changes from the wind turbine. Simulation values for load changes or input active power variations are exaggerated in this simulation in order to assess inverter performance in worst conditions, while real conditions would not exhibit such rapid changes in these parameters.

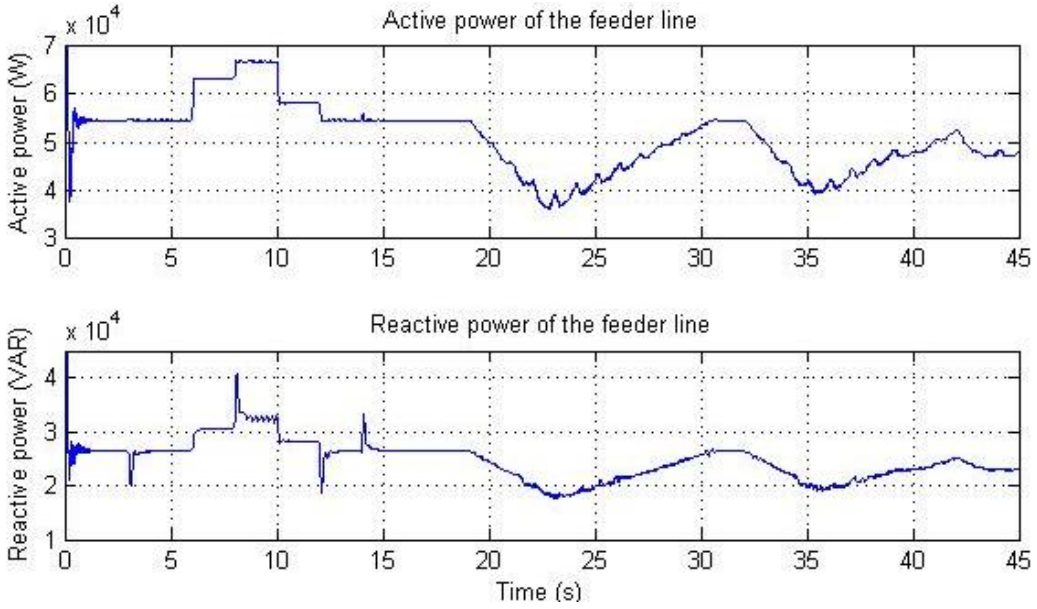
5.2.3 Active and reactive power of the inverter and feeder line

Active and reactive power delivered by the inverter and active and reactive power of the feeder line are shown in Figures 5.9(a) and 5.9(b), respectively. As previously mentioned, no wind and, consequently no active power from the wind turbine are present before the 19th second of the simulation. Therefore the feeder line initially supplies the entire load of 50 kW and 35 kVAR in addition to losses of the feeder line and the distribution transformer. As soon as the simulation starts, the inverter begins to generate capacitive VAR compensation. Therefore, the amount of active and reactive power provided by the feeder line to the load become 54 kW and 26 kVAR, and the inverter generates 9 kVAR in order to meet the target PF requirements. At t=3 s, the total load of the system changes to 50 kW and 28 kVAR in addition to the transformer and line losses. In this condition, PF of the load becomes equal to 0.87 requiring lower reactive power compensation. Hence, the active and reactive power of the feeder lines is kept constant and reactive power delivered by the inverter decreases to 2 kVAR. At t=6 s, the total load

requires 60 kW and 31 kVAR making the PF 0.89. At this time, the inverter must inject less reactive power to the grid. Active and reactive power from the feeder line increase to 64 kW and 31 KVAR, and reactive power delivered by the inverter decreases to 1 kVAR.



(a)



(b)

Figure 5.9 Active and reactive power delivered by the inverter, Active and reactive power of the feeder line

At t=8 s, the load demands 65 kW and 42 kVAR making the PF 0.84. Active and reactive power from the feeder line increase to 68 kW and 32 kVAR and reactive power from the compensator becomes 10 kVAR in order to increase the PF of the grid from 0.84 to 0.90. At t=10 s, the load is changed to 55 kW and 39 kVAR representing the PF of 0.81. In this condition, active and reactive power from the feeder line decrease to 58 kW and 28 kVAR while the reactive power of the compensator is increased to 11 kVAR. After t=12 s, the load returns to 50 kW and 28 kVAR in order to make the PF 0.87. Hence, the active and reactive power of the feeder lines change to 54 kW and 26 kVAR and reactive power delivered by the inverter decreases to 2 kVAR. Subsequently, after t=14 s, load conditions become similar to the start of the simulation and active and reactive power are kept constant while the reactive power of the compensator becomes equal to 9 kVAR. After t=19 s, as the output of the wind turbine increases, the amount of active power provided by the feeder line to the load decreases by the same amount. At t=23 s, the active power of the inverter is equal to 18.5 kW while the active power from the feeder line is equal to 35.5 kW. The reactive power of the inverter is calculated by the controller system in order to fix the PF at its target value. Figure 5.10 shows the output PF provided by the inverter.

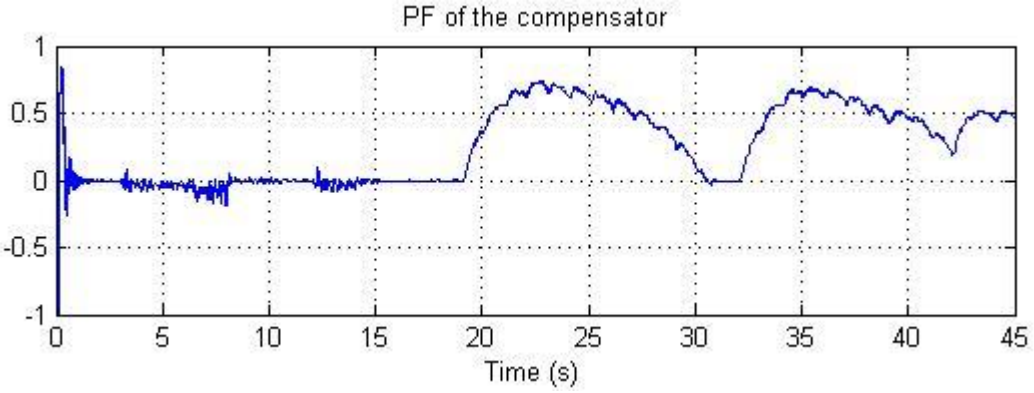


Figure 5.10 Output PF of the compensator

5.2.4 Power angle and modulation index of the inverter

Delta and modulation index figures are shown in Figure 5.11. The power angle controller varies the delta in order to control the active power transfer between the inverter and the grid. When no active power is coming from the wind turbine (before t=19 s), delta is constant. After this time, when active power from the wind turbine increases, the controller increases the power angle in order to inject more active power to the grid to decrease DC link voltage. Conversely,

when active power from the wind turbine decreases, the controller reduces the power angle in order to keep the DC link voltage at its reference value. The reactive power is controlled by varying the modulation index. When less reactive power compensation is required, the PI controller decreases the modulation index, and when more reactive power is required, the controller increases the modulation index to inject more reactive power to the grid.

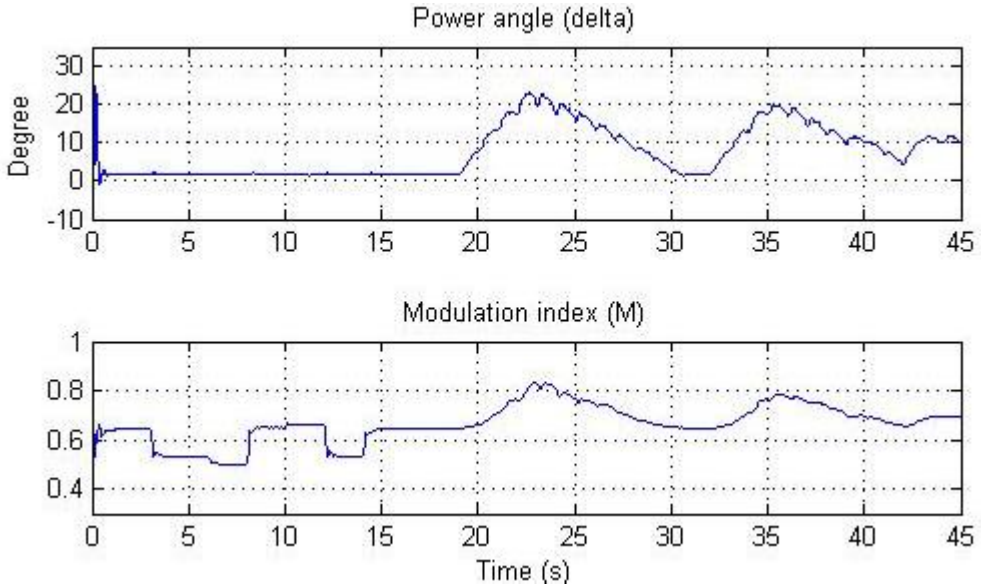


Figure 5.11 Power angle (delta) and modulation index (MI) of the inverter

For classic PWM inverters, the modulation index must be within the range of 0 and 1. However, for the 5-level inverter using PDPWM method, this range is more limited to 0.5 to 1, as lowering the modulation index more than 0.5 can result in loss of voltage levels. Carrier signals for a 5-level PDPWM technique are between -1 and 1 with peak-to-peak amplitudes of 0.5.

5.2.5 DC link voltages

Figure 5.12 shows voltage of the DC link as well as individual voltages across each DC link capacitor.

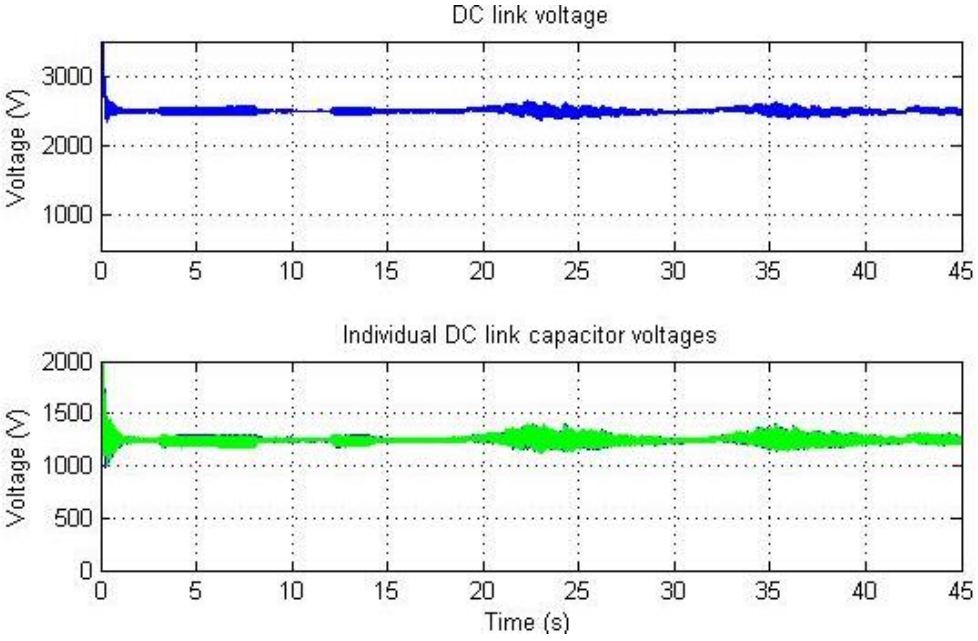
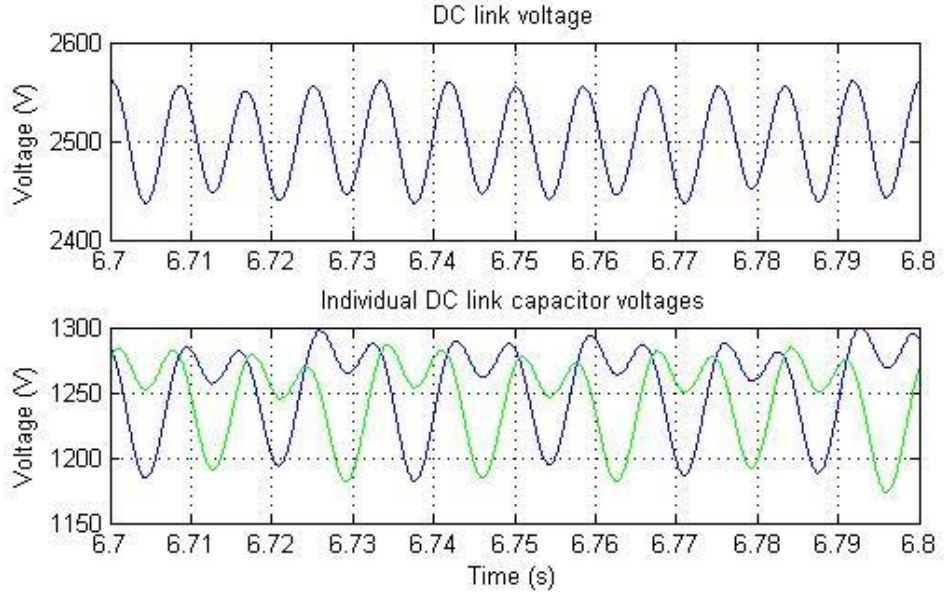
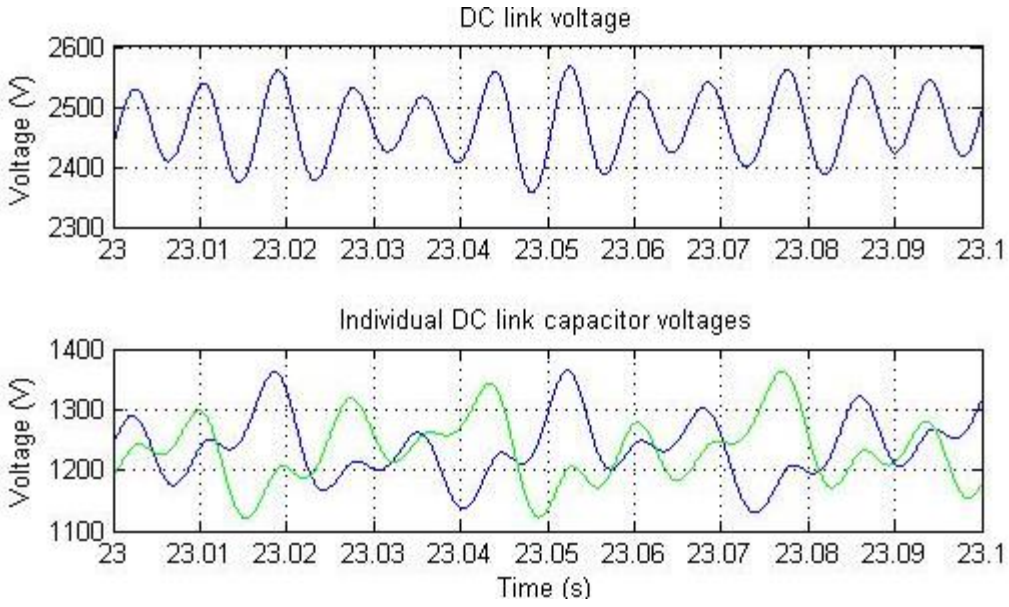


Figure 5.12 Voltages of the DC link and its capacitors

The function of the power angle PI controller is to stabilize the DC link voltage at the reference value of 2500 V. Before t=19 s, at the worst condition the DC link voltage variation is approximately 50 V below or above 2500 V representing a 2% variation. After t=19 s, the worst variation occurs at the most-input-power time, which is approximately 200 V within the reference value meaning an 8% variation. Figure 5.13 fully illustrates the DC link voltage and individual voltages across each DC link capacitor.



(a)



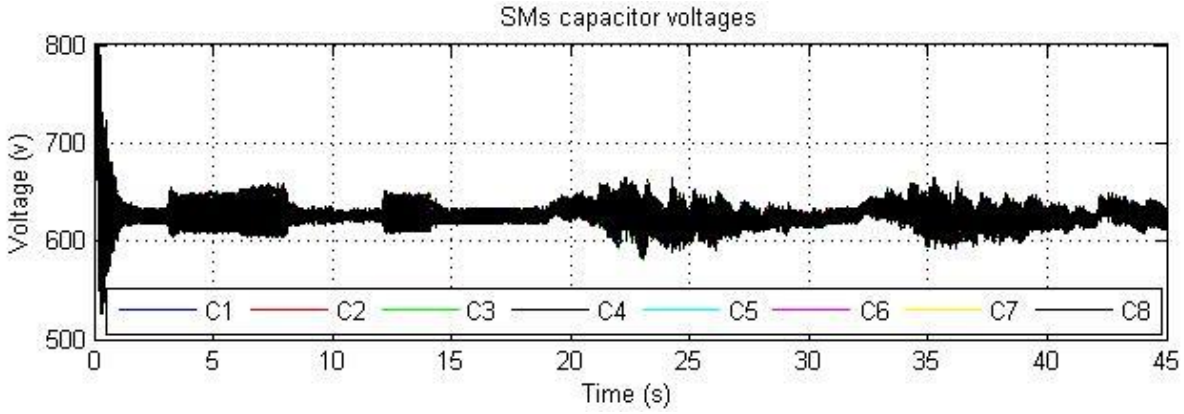
(b)

Figure 5.13 Variations of the DC link and its capacitors' voltages in worst conditions (a) before wind, (b) during wind

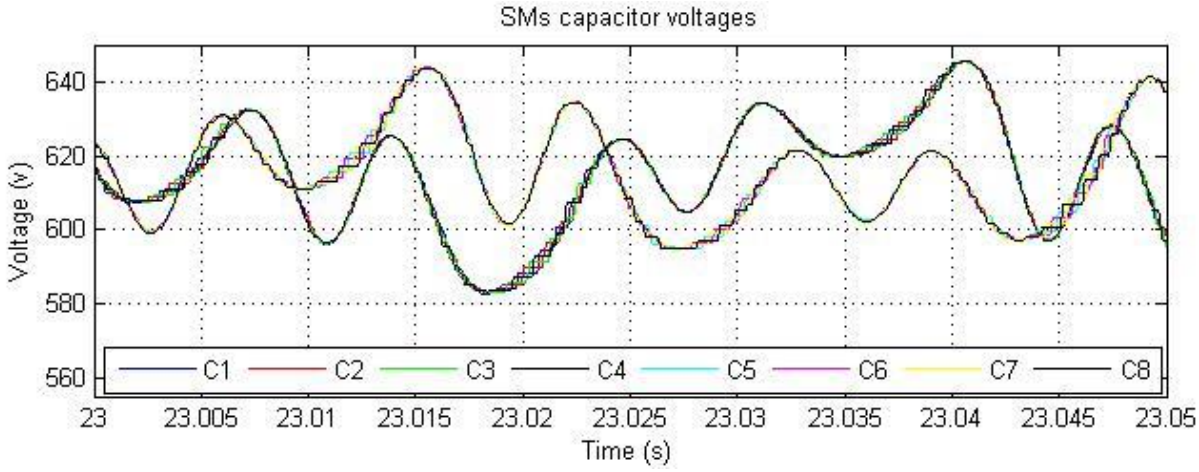
As shown, before t=19 s, the voltage across each DC link capacitor settles to within 50 V of 1250 V and after t=19 s, the voltage is within 200 V of 1250 in the worst conditions.

5.2.6 SMs capacitor voltages

Figure 5.14(a) shows the voltages of eight SM capacitors in a 5-level inverter using MMC topology. One of the primary functions of the controller system is to maintain these voltages balanced by measuring the voltages of these capacitors and sorting them in descending order. Then, based on the direction of the current flowing through the capacitors, the proper switching algorithm is selected to maintain voltage balance. In a 5-level inverter, the four upper SM capacitors have the same voltage at each instance. Similarly, the four lower SM capacitors have equal voltages, which differ from the upper SM capacitors.



(a)



(b)

Figure 5.14 SMs capacitor voltages

As described in Section 4.4.2, in a 5-level inverter, a combination of four SM capacitors should be selected in each instance. Since the DC link reference voltage is 2500, the voltage of each SM capacitor is equal to (2500/4) V or 625 V plus some variation. Figure 5.14(b) shows SM capacitor voltages in detail. The worst SM capacitor voltage variation before t=19 s is approximately 30 V representing a 4% variation, while it is approximately 40 V, showing a 6% variation after t=19 s.

5.2.7 PQ diagrams

The P-Q diagram of the proposed inverter shows the operating range of power transfer between the inverter and the grid. Since the proposed device is a combination of inverter and STATCOM, its correlating P-Q diagram is different from conventional well-known diagrams. The P-Q diagram of this inverter can be shown in two different aspects. The first aspect is device

capability: shown in Figure 5.15. The proposed D-STATCOM inverter can provide active and reactive power independently. The STATCOM option allows control of reactive power completely independent from the active power. If the power from the wind is too low to provide active power, the inverter can still provide reactive power to the power system, as an auxiliary option. The reactive power can be provided from the SM capacitors. In other words, the amount of reactive power injected from the inverter is a function of switching patterns. Based on the switching algorithm, an equivalent capacitance is generated at each instant. The equivalent capacitor can provide the required amount of reactive power to the grid.

The user can set two reference values for active and reactive power, which are controlled independently. This enables the inverter to provide whatever reactive power is demanded (within the inverter's ratings) even if its active power is zero. Similarly, the inverter is able to provide whatever active power its wind turbine can capture even if its reactive power is zero. In this case, all points within the square ABCD, shown in Figure 5.15, are feasibly capable points of the device.

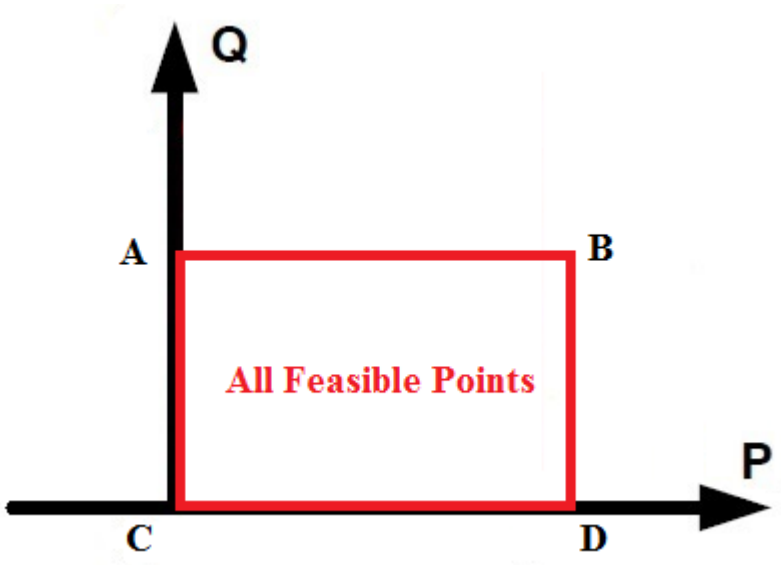


Figure 5.15 P-Q diagrm of the proposed inverter in terms of device capability

The P-Q diagram of this inverter can also be shown in terms of device operation. The operation regions of the device are more restricted than the capability regions. The controller system is responsible for fixing the PF of the local distribution grid regardless of load variations or wind speed changes. This negates various points of operation although the device is capable of operating within them. The proposed inverter can operate on specific lines for each target PF,

because the amount of active power of the inverter is governed by the input active power from the wind turbine, and the reactive power of the inverter is dictated by the grid target PF.

Figure 5.16 shows the active and reactive power transfer between the inverter, grid, and local load. In this case, given that equivalent load of the grid is constant, for each target PF, specific amounts of active and reactive power are required, which must be provided by the grid as well as the inverter. When there is no wind, active power from the inverter is zero. Hence, the entire active power of the load is drawn from the grid. On the other hand, when wind is blowing, active power of the wind turbine is entirely transferred to the load. Hence, active power drawn from the grid is decreased by the same amount. In order to fix the PF of the grid at the target value, reactive power from the grid must be reduced. Therefore, the remaining reactive power demanded by the load must be provided by the inverter. This increases the reactive power provided by the inverter. Figure 5.17 demonstrates the above statement graphically.

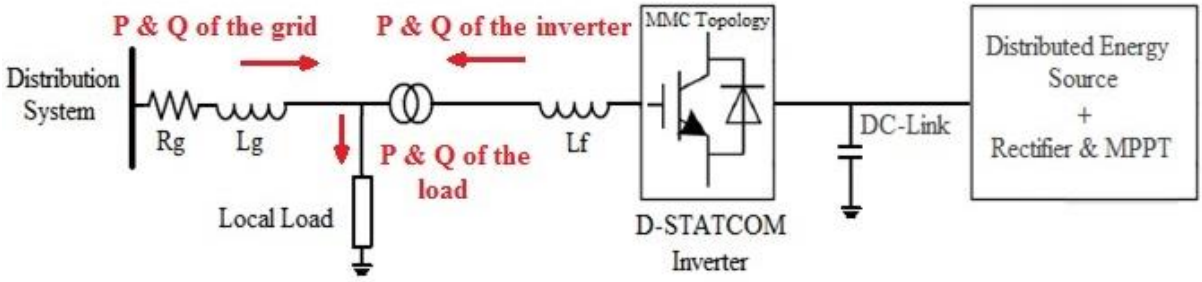


Figure 5.16 Active and reactive power transfer between the inverter, grid and load

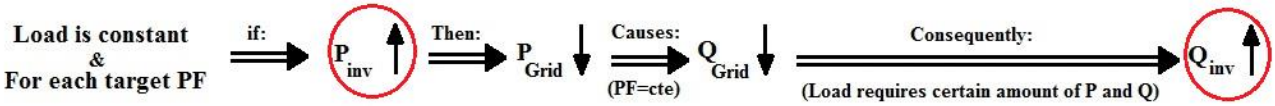


Figure 5.17 Graphical explanation of the system active and reactive power variations

The above paragraph can be mathematically shown as:

$$P_G + P_I = P_L + P_{Loss}$$

$$Q_G + Q_I = Q_L \quad (5.1)$$

where P_G, P_I, P_L, and P_{Loss} are active power of the grid, active power of the inverter, active power of the load, and power loss of the entire system, respectively, and Q_G, Q_I, and Q_L are reactive power of the grid, inverter, and load, respectively. Equation (5.1) demonstrates that

active power provided by the inverter and the grid is consumed by the load and the total power loss of the system including internal power loss of the inverter, distribution transformer, output filter and power lines. Similarly, reactive power demanded by the load is supplied by the grid and the inverter. (5.2) shows the grid PF equation:

$$PF_{Target} = \frac{P_G}{\sqrt{{P_G}^2 + {Q_G}^2}} \tag{5.2}$$

substituting (5.1) into (5.2) yields:

$$PF_{Target} = \frac{P_L + P_{Loss} - P_I}{\sqrt{(P_L + P_{Loss} - P_I)^2 + (Q_L - Q_I)^2}} \tag{5.3}$$

In (5.3), if load is assumed to be constant, for each specific target PF, the active and reactive power of the inverter (P_I and Q_I) can be adjusted to meet the target PF. The relationship between these variables is shown in Figure 5.18.

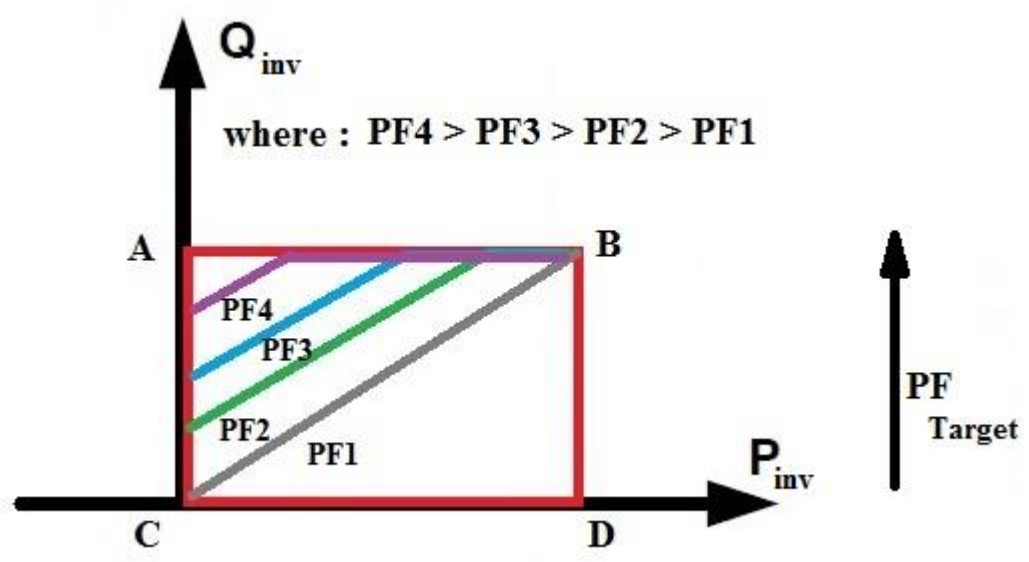


Figure 5.18 P-Q diagram of the proposed inverter in terms of device operation

Figure 5.18 demonstrates that the operating points for each specific target PF are located on a straight line. In other words, for each target PF, when active power of the inverter is zero (no wind), the inverter provides enough reactive power to the grid in order to decrease the reactive power drawn from the grid to fix the grid PF at its target value. Obviously, for higher grid PFs, less reactive power from the grid is required, which results in more reactive power from the inverter. As shown, the inverter can support active and reactive power up to its ratings. For higher grid target PFs, the inverter needs to provide more reactive power, so it reaches its limits

sooner. However, the inverter is able to transfer whatever active power (less than its rating) it gains from the wind turbine even if it hits the reactive power limit.

To make above P-Q diagram more understandable, numeric examples drawn by MATLAB are provided. For the first example, it is assumed that a constant load of 50 kW and 35 kVAR is connected to the primary (high-side) of the distribution transformer. In addition, the entire system has power loss of 3 kW generated by the power lines, distribution transformer, inverter and its output LC filter. The PF of the load is 0.82 and the grid target PF is 0.90. Figure 5.19 drawn in MATLAB, demonstrates the P-Q diagram of the inverter for the mentioned conditions. Before connecting the inverter to the grid, all active and reactive power required by the load is drawn from the grid. At t=0 s, the inverter is connected to the system. To start, it is assumed that there is no wind. Therefore, the active power from the grid is 53 kW (load+loss) and from the inverter is zero. In this case, in order to improve the grid PF, the inverter provides approximately 9 kVAR to the grid. Hence, the reactive power from the grid decreases to 26 kVAR. Therefore, the PF of the grid is improved to 0.90: this situation corresponds to point [A] on the graph in Fig. 5.19.

By increasing the amount of active power from the inverter (when wind blows), the inverter helps the grid to provide required load active power. Consequently, the grid provides less active power to the load, because the load needs a constant amount of active power. Therefore, the amount of active power from the grid is decreased. This causes a reduction in reactive power of the grid in order to hold the grid PF constant (equation 5.2). This forces the inverter to inject more reactive power to the load. As a result, when the inverter active power increases, its reactive power also increases. For instance, when active power of the inverter is 10 kW, the active power drawn from the grid is 43 kW. Because the grid PF is constant at 0.90, it can provide only 21.5 kVAR to the load and the remaining reactive power must be provided by the inverter. Therefore, the reactive power from the inverter increases to 13.5 kVAR (point [B] in Figure 5.19). The active and reactive power of the inverter can also be calculated using equation (5.3).

As the wind increases, the inverter climbs to another operating point, when the active power from the inverter is 14 kW (for example). In this case, the total active power from the grid is 39 kW. In order to maintain the grid PF constant at 0.90, the amount of reactive power drawn from the grid is decreased to 19 kVAR. Therefore, the remaining reactive power required by the load

is drawn from the inverter. This results in increasing the inverter reactive power to 16 kVAR (point [C] in Figure 5.19). The inverter power can be increased until the active or reactive power of the inverter reaches its limit.

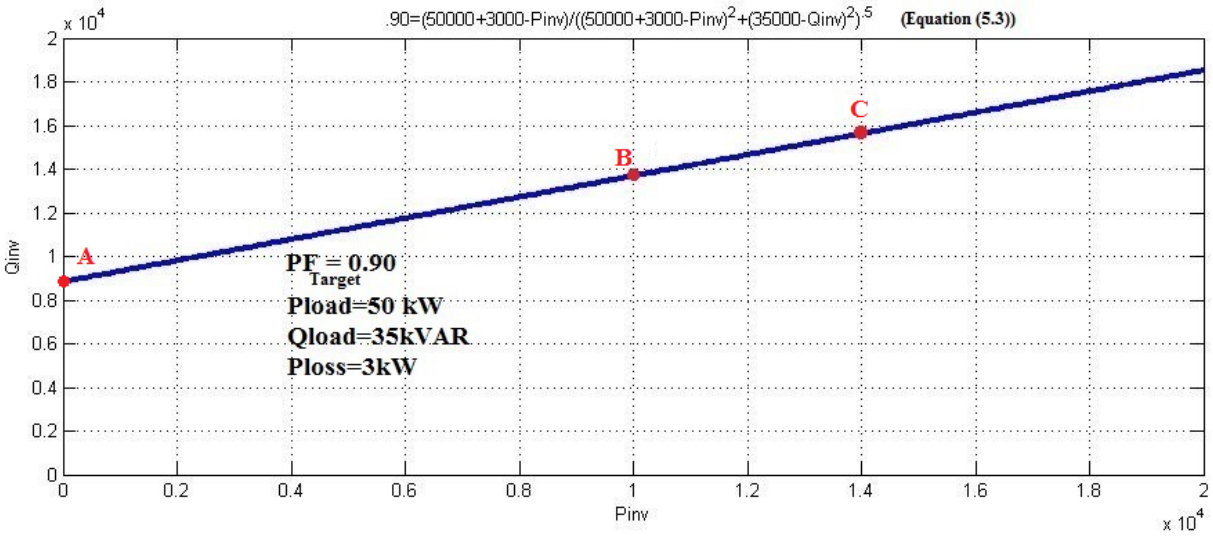


Figure 5.19 P-Q diagram of the inverter for constant load of 50 kW and 35 kVAR and grid target PF of 0.90

In another numeric example, it is assumed that the target PF is 0.92 while the load is 50 kW and 35 kVAR (PF = 0.82); refer to Figure 5.20. In this case, when input active power from the inverter is zero, the entire active power required by the load and losses is supplied by the grid (53 kW). Therefore, the inverter must provide 12 KVAR to improve the grid PF to 0.92 (point [A] in Fig. 5.20). When input active power from the inverter increases to 10 kW, the total active power from the grid decreases to 43 kW. If the grid PF is to be constant at 0.92, it may only provide 18.5 KVAR to the load. As a result, the load forces the inverter to provide 16.5 kVAR, because it requires 35 kVAR (point [B] in Figure 5.20).

Similarly, when the active power of the inverter increases to 14 kW, the grid active power becomes 39kW. Therefore in order to maintain the PF constant at 0.92, 17 kVAR must be drawn from the grid. Therefore the remaining reactive power required by the load is drawn from the inverter which is approximately 18kVAR (point [C] in Figure 5.20).

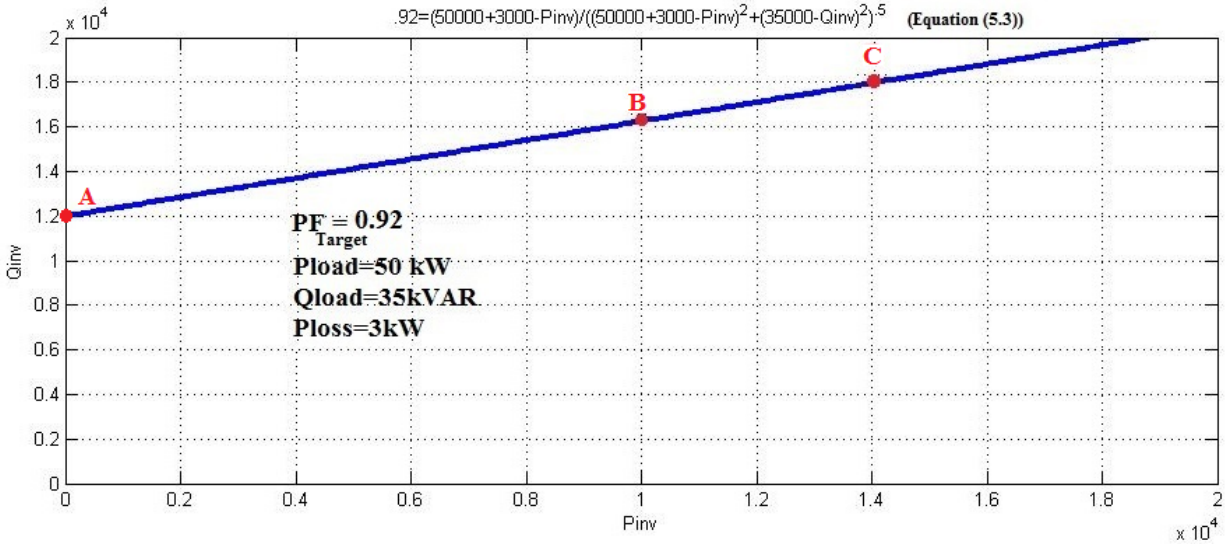


Figure 5.20 P-Q diagram of the inverter for constant load of 50 kW and 35 kVAR and grid target PF of 0.92

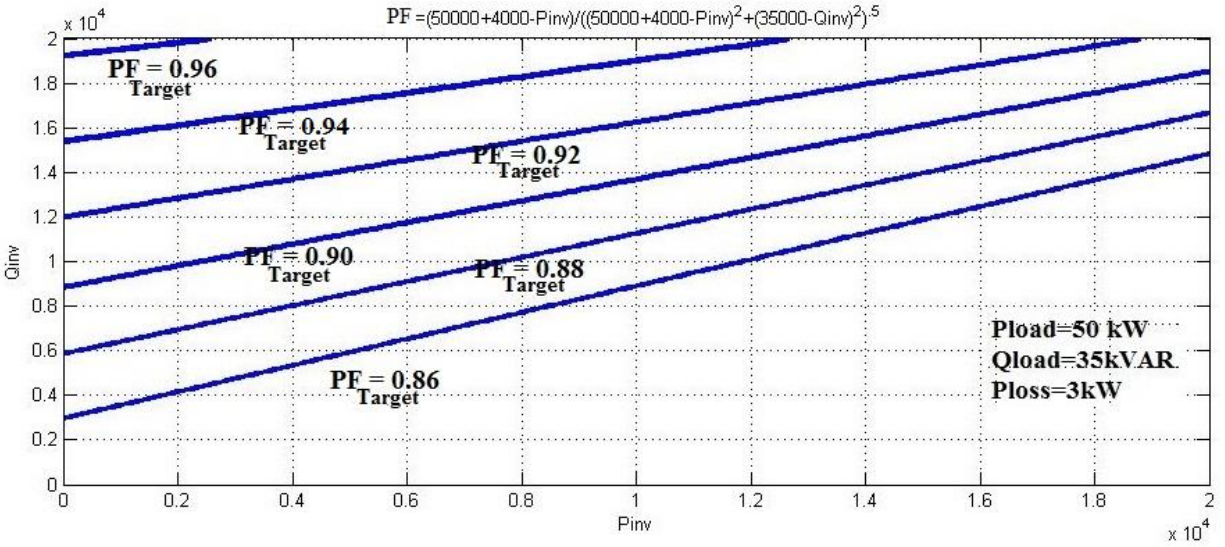


Figure 5.21 P-Q diagram of the inverter for different target PFs

Figure 5.21 shows the P-Q diagram of the system meeting application requirements for a constant load with PF of 0.82. In this case, the load is constant and feasible operating points of the inverter are shown for various target PFs. Results show that, for a constant load, the inverter can only operate on specified lines. When the target PF increases, the inverter must compensate with more reactive power to the system which causes the inverter to reach its reactive power limit sooner. The inverter is able to transfer any active power it obtains from the wind turbine until it reaches a limit of 20 kW. However, the reactive power can be supported by 20 kVAR,

meaning that if the system condition requires more than this amount of reactive power, the inverter is unable to meet the target PF and, therefore, the PF of the system drops. In these conditions, multiple inverters (on multiple wind turbines on the same feeder line) can be utilized in order to compensate more reactive power to meet target PF requirements.

5.3 5-Level inverter (250 W/VAR)

As previously shown, Section 5.2 demonstrated the simulation results for a 5-level inverter with rating of 20 kW/kVAR. To validate the simulations, an experimental setup with actual rating (20kW/kVAR) is required. However, providing such a system is usually impossible in university laboratories, because it needs well-equipped high voltage test facilities. As it is shown in Chapter 6 and 7, to validate the simulation results for the 5-level inverter, a scaled prototype model of 250W/VAR has been built and tested to show the proof of concept. Therefore, to compare the experimental results (shown in Chapter 7) with the simulation results (Section 5.2), a low-rating simulation is performed, which uses the actual (or as close as possible) parameters that experiments use. The simulation is 45 seconds long and demonstrates the performance of the proposed inverter for various conditions. The function of the inverter in all situations is to transfer active power from the wind turbine to the distribution grid as well as improving the PF of the local distribution grid from 0.65 to 0.80. In other words, the inverter must function as a regular wind energy inverter which possesses D-STATCOM option in order to fix the PF of the grid at the target value set by the utility, regardless of variations of input active power from the wind turbine. Table 5.5 shows the simulation parameters used for the low-power (250W/VAR) 5-level model. In this simulation, the goal is to compare the results with the experimental results shown in Chapter 7. Therefore, the simulation conditions are as similar to the experimental tests as possible. In order to do so, several harmonics have been added to the grid representing the line harmonics, because the actual grid in the lab contains small amounts of low order harmonics including the 3^{rd} and 5^{th}. Harmonics have been added based on their order and value shown in Figure 7.2. The value of the 3^{rd}, 5^{th}, and 7^{th} harmonics added to the fundamental frequency are .5%, 1.25%, and .25%, respectively. Before connecting the inverter to the grid, the grid THD is approximately 1.6%, which is close to the actual THD of the grid where experimental tests have been done. Moreover, important component specifications, especially the switches, have been extracted from datasheets and used to make the simulations more similar to the experiments.

Table 5.5 Parameter values used for the 5-level inverter (250W/VAR) simulation

Parameter	Value
L_{line}	1 mH
R_{line}	1 Ohm
L_{filter}	10 mH
C_{filter}	25 uF
Transformer power rating	5 kVA
Transformer primary voltage	120 V
Transformer secondary voltage	24 V
Switching frequency	3 kHz
Target PF	0.80
DC link reference value	90 V
Initial voltages of DC link capacitors	45 V
Initial voltages of SM capacitors	22.5 V
Transformer inductance	$R_1 = 0.0005\ p.u.$, $L_1 = 0.0005\ p.u.$ $R_2 = 0.0005$ p.u., $L_2 = 0.0005\ p.u.$

Discrete intervals for the amplitudes of the current controlled sources are given in Table 5.6. Before t=19 s, the input active power from the wind turbine is zero, implying that the wind speed is zero or too low to produce active power. At the 19th second of the simulation, power provided by the wind turbine ramps up to 90 W in four seconds and then ramps down to zero in seven seconds.

Table 5.6 Discrete intervals for amplitudes of current sources used in turbine model

Time (s)	Current source amplitude (A)	Time (s)	Current source amplitude (A)
0	0	23	0
1	0	24	0
2	0	25	0
3	0	26	0
4	0	27	0
5	0	28	0
6	0	29	0
7	0	30	0
8	0	31	0
9	0	32	2
10	0	33	3
11	0	34	4
12	0	35	4
13	0	36	1
14	0	37	2
15	0	38	2
16	0	39	2
17	0	40	0
18	0	41	0
19	1.5	42	2
20	4.5	43	2
21	0	44	2
22	.5	45	2

During this portion of the simulation, there is no wind production for two seconds, and then at t=32 s, the wind turbine power ramps up again to 75 W in three seconds and then ramps down again to 20 W in seven seconds, subsequently fixing at 35 W. Output active power from the wind turbine is shown in Figure 5.22.

Figure 5.22 Output active power from the wind turbine

The simulation begins with the selection of only load1 making the PF 0.65. At t=3 s, the PF of the load is changed to 0.68 by selecting load2 instead of load1. After three seconds, load3 is added to load2 making the PF 0.70. At t=8 s, load4 is also added to load2 and load3 making the PF 0.66. At t=10 s, load3 is removed, resulting in load2 and load4 again making the PF 0.62. After two seconds, load4 is also removed, resulting in having only load2, which makes the PF 0.68. Consequently, at t=14, load1 is replaced by load2 making the PF 0.65 again. After this time, no load changes occur and, as a result, no PF variation. The process of load variation in respect to time is shown in Table 5.7. After t=14, the load PF is fixed at 0.65. The function of the proposed inverter is to fix the PF of the local distribution grid at the target PF, which is 0.80 in this case, regardless of load or wind speed changes.

Table 5.7 Equivalent distribution load variations in respect to time

Time (s)	Load combination	Resulting load's P & Q	Resulting load PF	Target PF
0	1	102 W, 120 VAR	0.65	0.80
1	1	102 W, 120 VAR	0.65	0.80
2	1	102 W, 120 VAR	0.65	0.80
3	2	102 W, 110 VAR	0.68	0.80
4	2	102 W, 110 VAR	0.68	0.80
5	2	102 W, 110 VAR	0.68	0.80
6	2+3	112 W, 115 VAR	0.70	0.80
7	2+3	112 W, 115 VAR	0.70	0.80
8	2+3+4	115 W, 130 VAR	0.66	0.80
9	2+3+4	115 W, 130 VAR	0.66	0.80
10	2+4	95 W, 118 VAR	0.62	0.80
11	2+4	95 W, 118 VAR	0.62	0.80
12	2	102 W, 110 VAR	0.68	0.80
13	2	102 W, 110 VAR	0.68	0.80
14	1	102 W, 120 VAR	0.65	0.80
15	1	102 W, 120 VAR	0.65	0.80
16	1	102 W, 120 VAR	0.65	0.80
17	1	102 W, 120 VAR	0.65	0.80
18	1	102 W, 120 VAR	0.65	0.80
19 . . . 43	1 . . . 1	102 W, 120 VAR	0.65 . . . 0.65	0.80 . . . 0.80
44	1	102 W, 120 VAR	0.65	0.80

After the simulation begins, the inverter provides enough compensation to raise the PF to its target value of 0.80 regardless of equivalent load variations. As soon as the inverter provides

reactive power compensation, the amount of reactive power provided by the feeder line to the load decreases. After t=19 s, output power of the wind turbine increases and, consequently, the level of active power provided by the feeder line decreases by the same amount.

5.3.1 Output voltage and current of the inverter

Simulated output voltage of the proposed 5-level inverter (250 W/VAR) before and after the filter is shown in Figure 5.23.

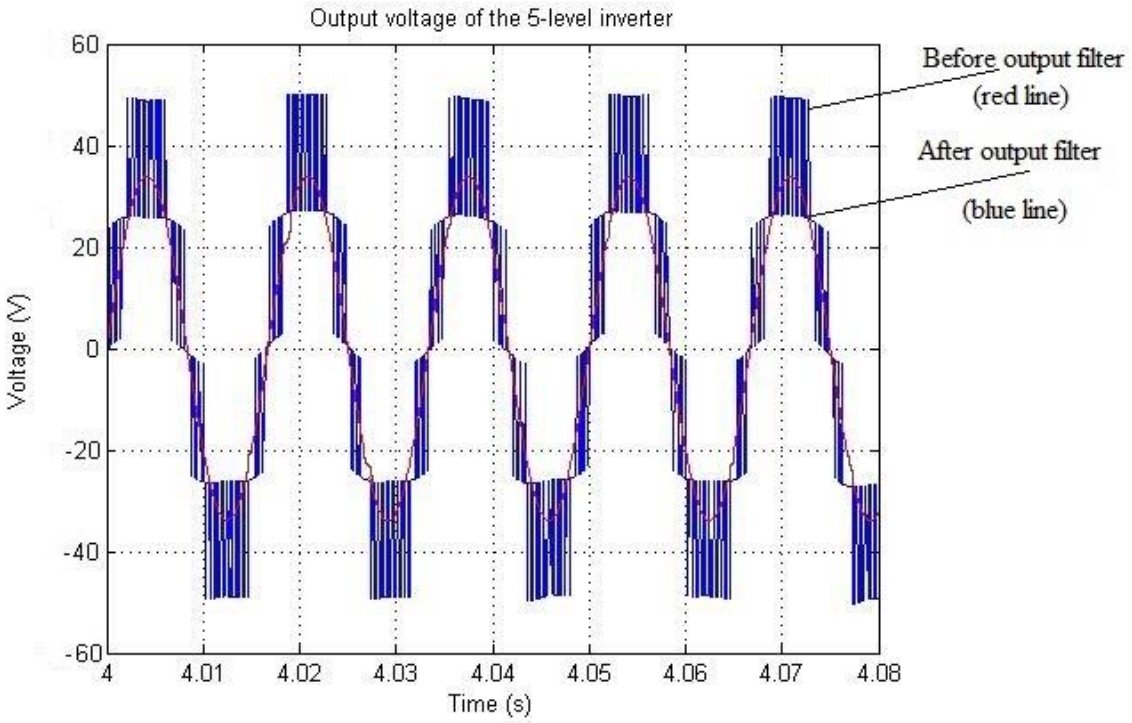


Figure 5.23 Simulated output voltage before and after the filter

The total harmonic distortion (THD) of the output voltage of the inverter after the filter is approximately 2.02%. Figure 5.24 shows the Fast Fourier Transform (FFT) of the filtered output voltage of the 5-level inverter. Figure 5.25 shows the current on both sides of the distribution transformer.

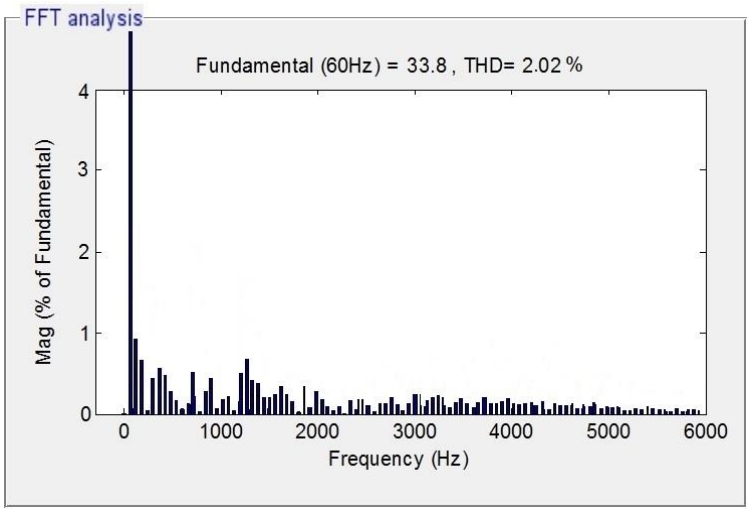


Figure 5.24 FFT of the filtered output voltage

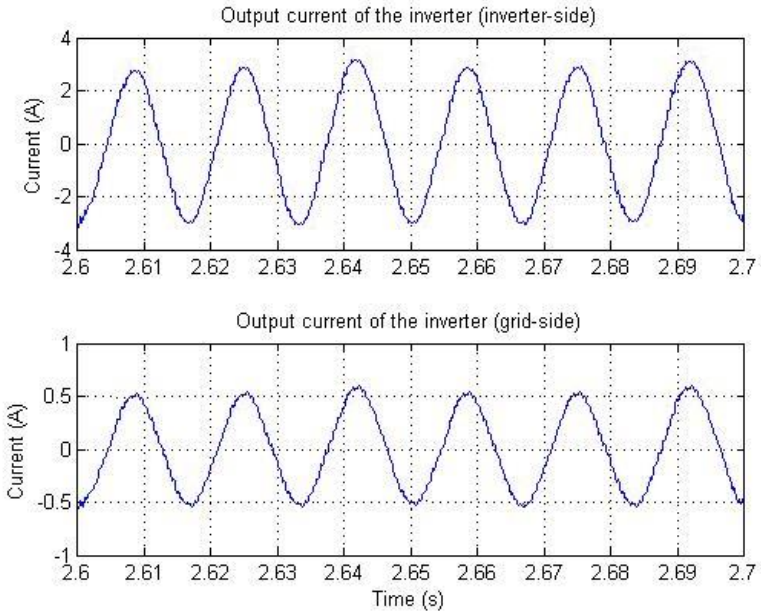


Figure 5.25 Output current on both sides of the distribution transformer

The THD of the output current on the inverter-side of the distribution transformer is 4.19%. Figure 5.26 shows the FFT of the inverter-side output current.

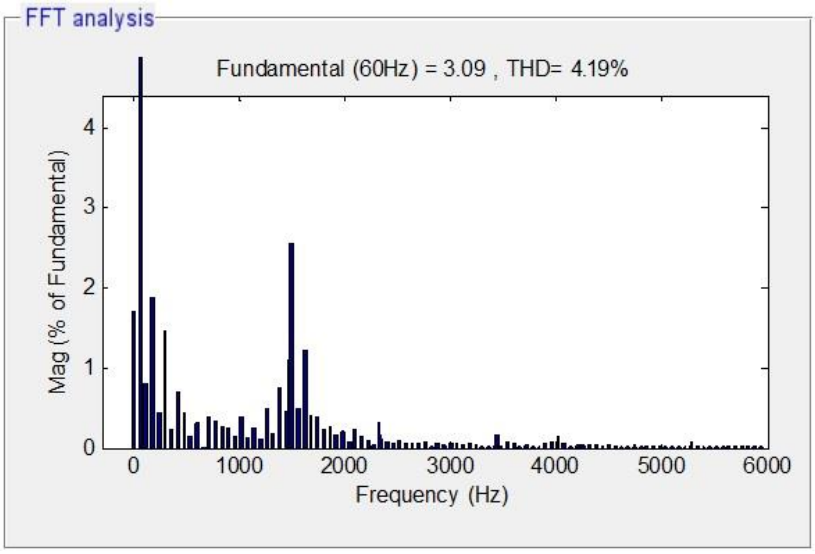


Figure 5.26 FFT of the inverter-side current

As Figures 5.27 shows, THD of the output current of the inverter is compliant with IEEE 519 standard since the amplitude of each single harmonic is less than 3% of the fundamental frequency and the THD is less than 5%. The output current THD can be reduced by using larger output LC filters. However, this may affect the total cost of the system.

5.3.2 Power factor of the local distribution grid

The target power factor on the grid is set to 0.80 while the loads demand various PF. The inverter must compensate the reactive power on the grid by injecting reactive power while operating as a regular inverter in order to transfer active power to the grid. Figure 5.27 shows the PF of the local distribution grid.

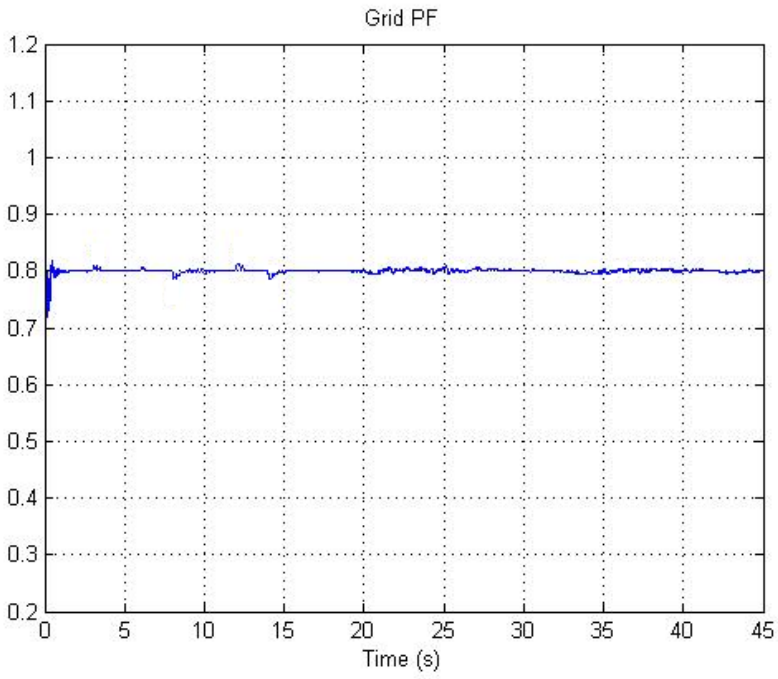
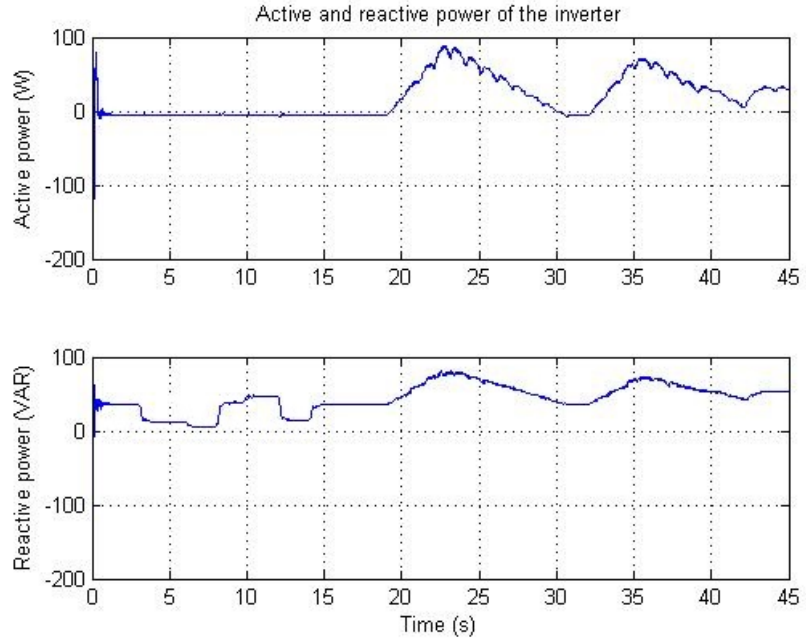


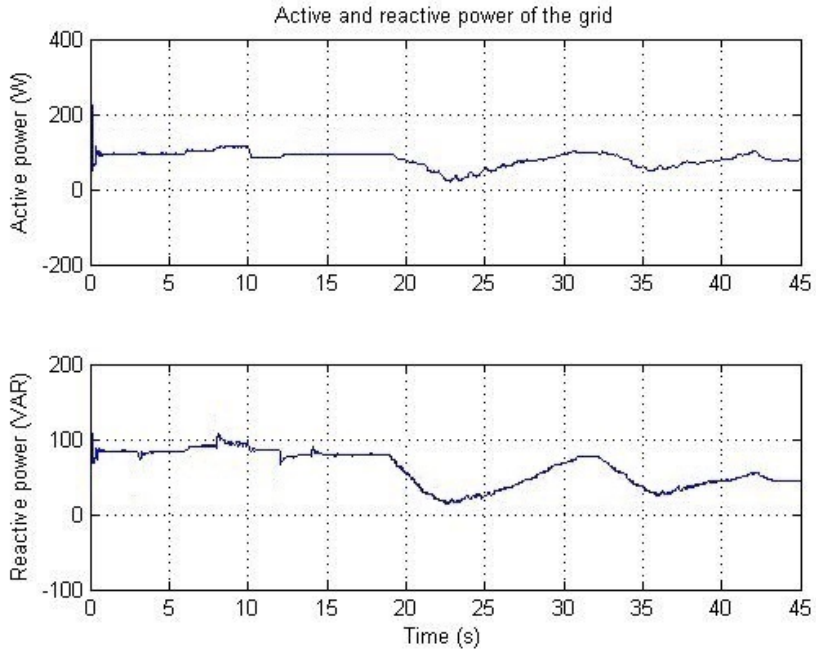
Figure 5.27 PF of the local distribution grid

5.3.3 Active and reactive power of the inverter and feeder line

Active and reactive power delivered by the inverter and active and reactive power of the feeder line are shown in Figures 5.28(a) and 5.28(b), respectively. The basic operation of the inverter and power transfer between the load, inverter, and grid are similar to Section 5.2.3, and the only difference is that all parameters have been scaled down from 20kW/kVAR to 250W/VAR.



(a)



(b)

Figure 5.28 (a) Active and reactive power delivered by the inverter, (b) Active and reactive power of the feeder line

5.3.4 Power angle and modulation index of the inverter

Delta and modulation index figures are shown in Figure 5.29. The power angle controller varies the delta in order to control the active power transfer between the inverter and the grid. As previously mentioned, the reactive power is controlled by varying the modulation index.

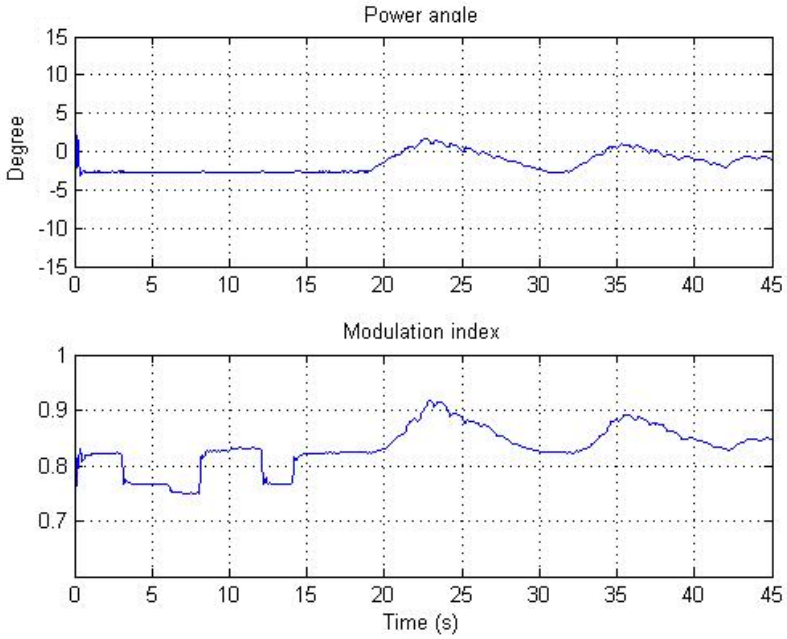


Figure 5.29 Power angle and modulation index

5.4 11-Level inverter (20 kW/kVAR)

Simulation of the proposed 11-level inverter is similar to the 5-level model with a simulation time of 45 seconds and two parts. In the first part, various load combinations, making different PF, are chosen. In the second part, severe variations in the input active power from the wind turbine are considered. The inverter function in all cases involves transferring active power from the wind turbine to the distribution grid as well as compensating the PF of the local distribution grid at the target PF of 0.90. Table 5.8 shows parameter values used for the simulations.

Table 5.8 Parameter values used for the 11-level inverter simulation

Parameter	Value
L_{line}	1 mH
R_{line}	1 Ohm
L_{filter}	20 mH
C_{filter}	70 uF
Transformer power rating	25 kVA
Transformer primary voltage	12000 V
Transformer secondary voltage	600 V
Switching frequency	3 kHz
Target PF	0.90
DC link reference value	2000 V
Initial voltages of DC link capacitors	1000 V
Initial voltages of SM capacitors	200 V
Transformer inductance	$R_1 = 0.001\ p.u.$, $L_1 = 0.001\ p.u.$ $R_2 = 0.001$ p.u., $L_2 = 0.002\ p.u.$

In the 11-level simulation, discrete intervals used as the amplitudes of the current controlled current sources are identical to values used for the 5-level model shown in Table 5.1. However, the output active power of the wind turbine differs because the DC link voltage is different in this case (2000 V in the 11-level model versus 2500 V in the 5-level model). Therefore, before t=19 s, the output active power of the wind turbine is zero, representing wind speed of zero or too low to produce active power. After t=19 s, the power provided by the wind turbine ramps up to approximately 15 kW in four seconds and then ramps down to zero in seven seconds, followed by no wind power production for two seconds. At t=32 s, the wind turbine power ramps up again to 12 kW in three seconds and then ramps down to 2 kW in seven seconds and consequently becomes constant at 6 kW. Similar to the 5-level model, these variations represent severe variations, and are only used to assess the controller system performance. Typically, real situations would not demonstrate such extreme change in wind turbine power production. Figure 5.30 demonstrates output active power from the wind turbine.

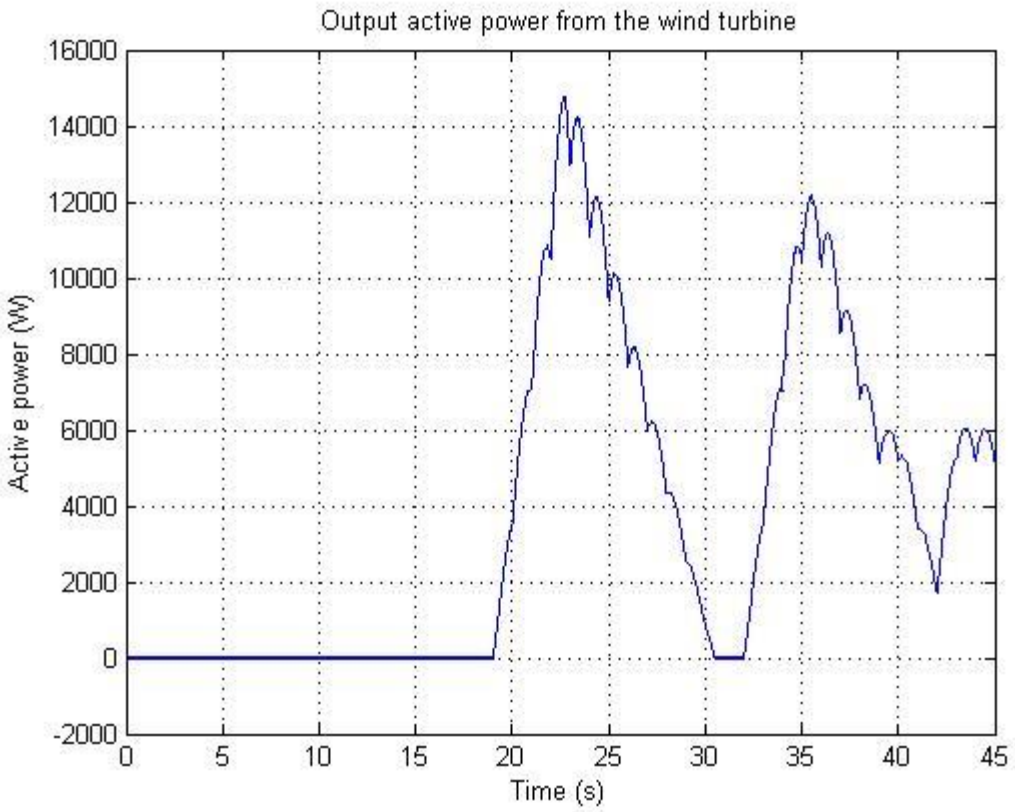


Figure 5.30 Output active power from the wind turbine

In this simulation, similar to the 5-level model, the PF of the load varies by selecting different combinations of the loads. The load selected for the 11-level simulation is identical to the 5-level model shown in Table 5.9. In summary, the load PFs are: 0.82 at t=0 s, 0.87 at t=3 s, 0.89 at t=6 s, 0.84 at t=8 s, 0.81 at t=10 s, 0.87 at t=12 s, and 0.82 for at t=14 s. After t=14, the load PF is fixed at 0.82. The function of the 11-level inverter is to make the PF of the local distribution grid constant at 0.90, regardless of load changes or wind speed changes.

After the simulation begins, the inverter provides reactive power to compensate the PF of the local distribution grid, and the amount of reactive power provided by the feeder line to the load decreases. Coefficients used for the power angle and modulation index controllers, obtained with trial and error method, are listed in Table 5.9.

Table 5.9 Coefficients used for PI controllers

PI Controller	Coefficient
Power angle controller	$K_p = 0.05$ $K_I = 0.1$
Modulation index controller	$K_p = .00001$ $K_I = .00008$

5.4.1 Output voltage and current of the inverter

The simulated output voltage of the proposed 11-level inverter before and after the filter is shown in Figure 5.31.

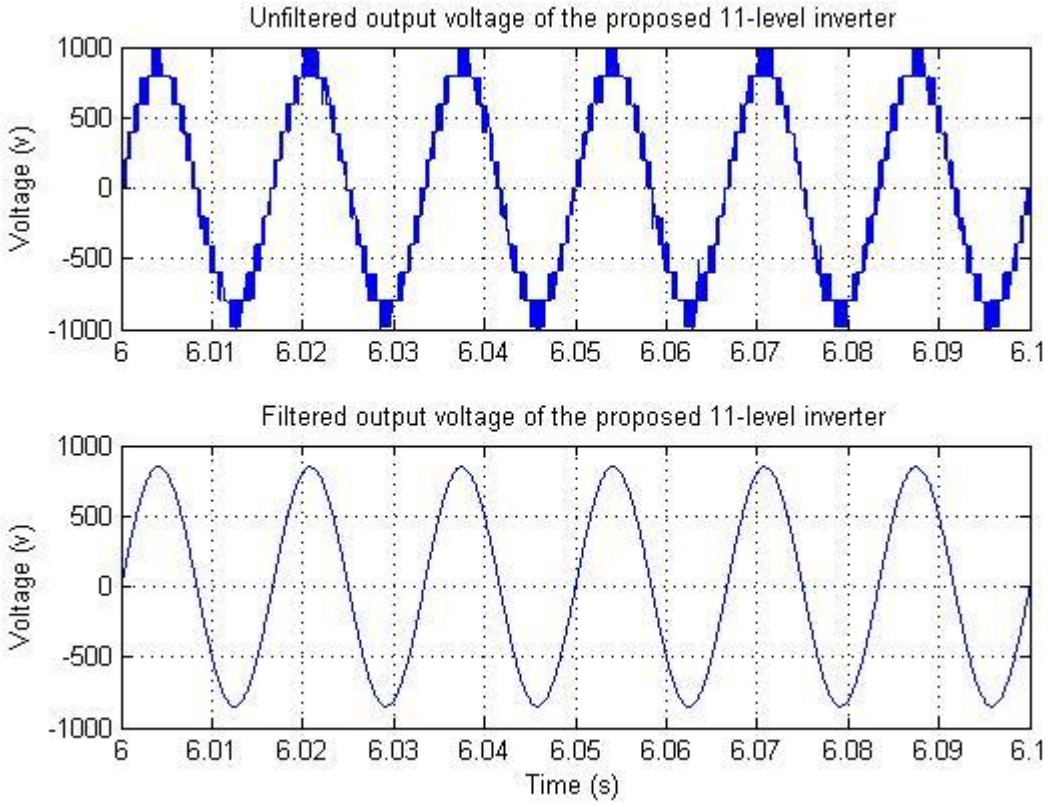


Figure 5.31 Simulated output voltage before and after the filter

In the above Figure, the RMS value of the output voltage before and after the filter are 630 V and 600V, respectively. Therefore, the voltage drop associated with the filter is less than 5% which is compliant with the standard value. The THD of the output voltage of the inverter after the filter is 0.23%. Figures 5.32 and 5.33 show the FFT of the unfiltered and filtered output voltage of the 11-level inverter, respectively.

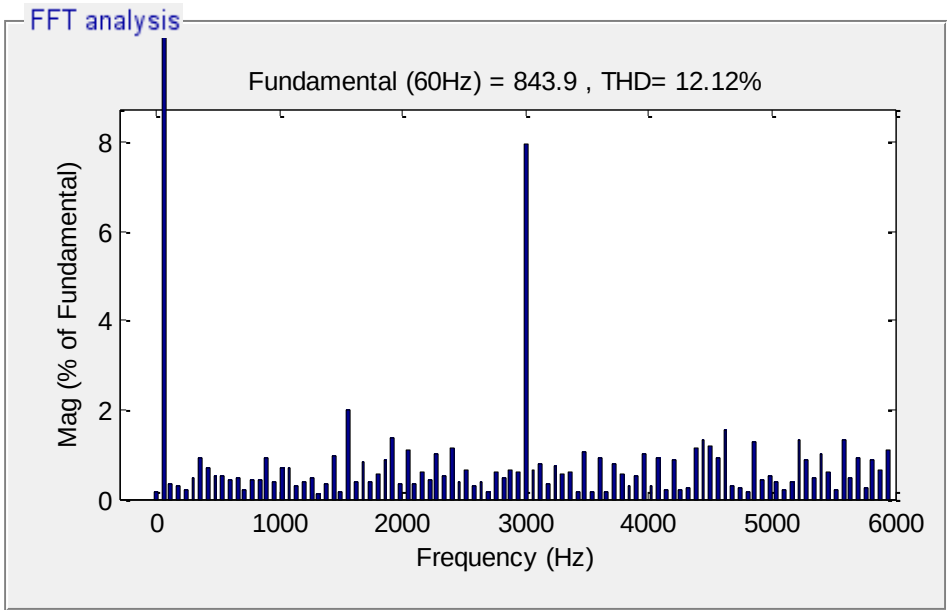


Figure 5.32 FFT of the unfiltered output voltage of the 11-level inverter

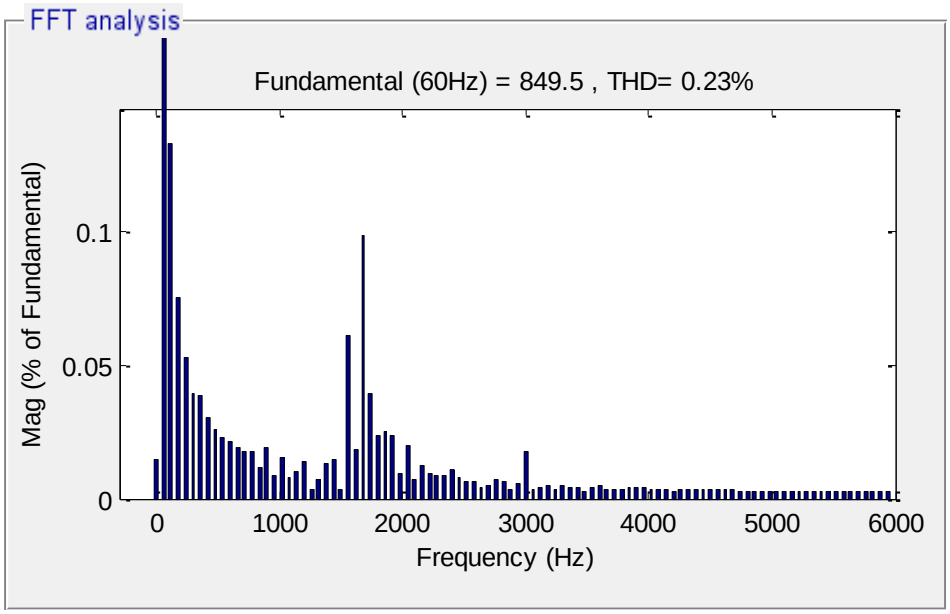


Figure 5.33 FFT of the filtered output voltage of the 11-level inverter

In Figure 5.32, as with the 5-level model, the most significant harmonic orders are near $n * f_s$ frequencies where f_s is the switching frequency of the inverter, in this case $f_s = 3\,kHz$. Figure 5.33 shows output voltage of the inverter after the second-order LC output.

Because of a distribution transformer with turns-ratio of 12000:600, the output current of the inverter-side is 20 times greater than the current on the grid-side. Unlike the 5-level model, output current oscillations have been decreased significantly in the 11-level model. Therefore,

the 11-level model does not contain output power oscillations seen in the 5-level model. Figure 5.34 demonstrates the current on both sides of the distribution transformer.

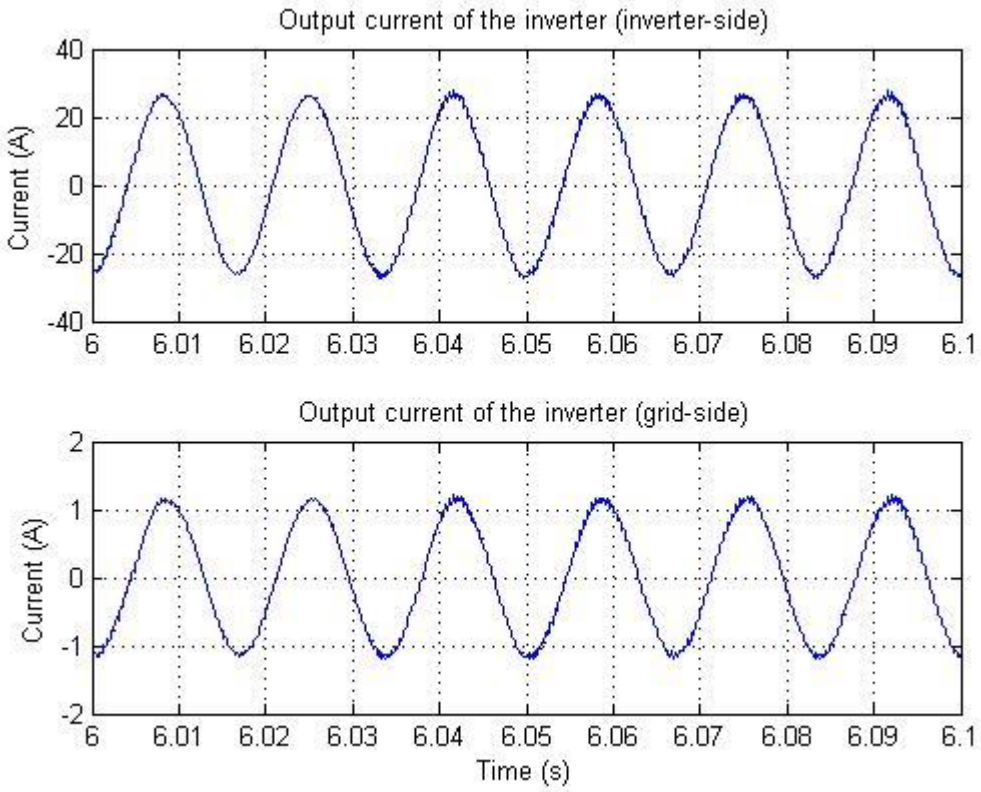


Figure 5.34 Output current on both sides of the distribution transformer

Figure 5.35 shows the FFT of the inverter-side output current. As shown, the THD of the output current on the inverter-side of the distribution transformer is 3.46%.

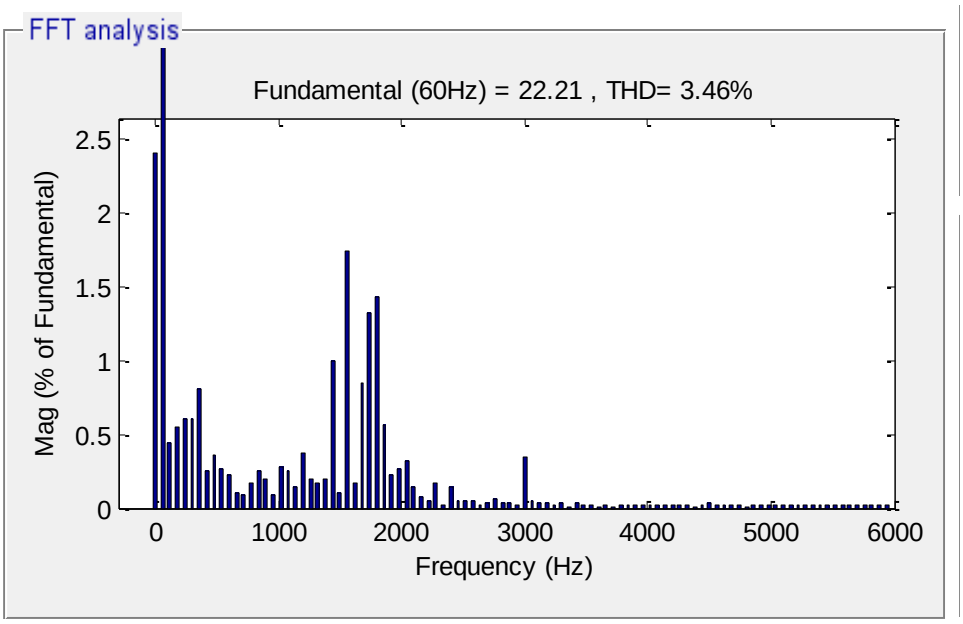


Figure 5.35 FFT of the inverter-side current

As demonstrated in the above figures, the output voltage and current of the proposed inverter are completely compliant with IEEE 519 standard meaning that the amplitude of each single harmonic is less than 3% of the fundamental frequency and the THD is less than 5%. The current and voltage THDs of the 11-level inverter are better than the 5-level model. This is in conjunction with the use of a smaller output filter. Clearly, using a larger filter eliminates more harmonics of the output waveforms.

5.4.2 Power factor of the local distribution grid

The PF of the distribution grid must be constant at the target PF set by the user. Figure 5.36 shows the PF of the local distribution grid, which is fixed at 0.90 with small variations during rapid load variations or severe wind speed changes. The inverter is able to compensate the reactive power on the grid by injecting enough reactive power to the grid. As shown, the PF of the grid is constant at 0.90 for the entire simulation time regardless of the load variation and input active power changes from the wind turbine. As with the 5-level model, in this simulation, the load changes or input active power variations are exaggerated in order to assess inverter performance in the worst conditions.

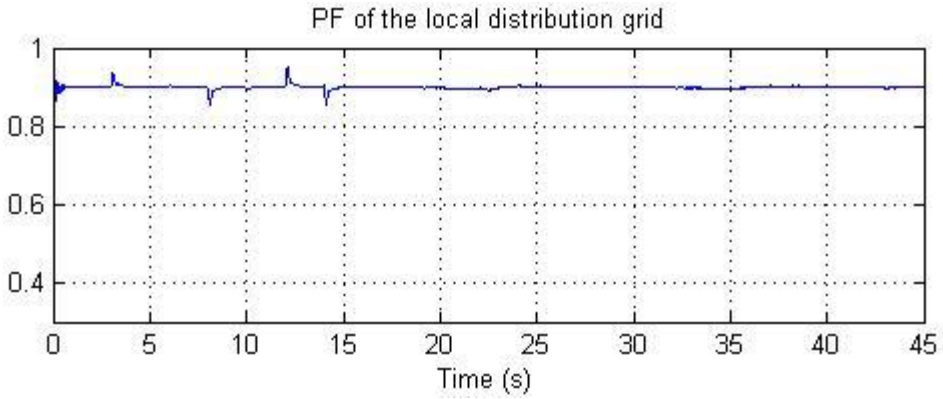
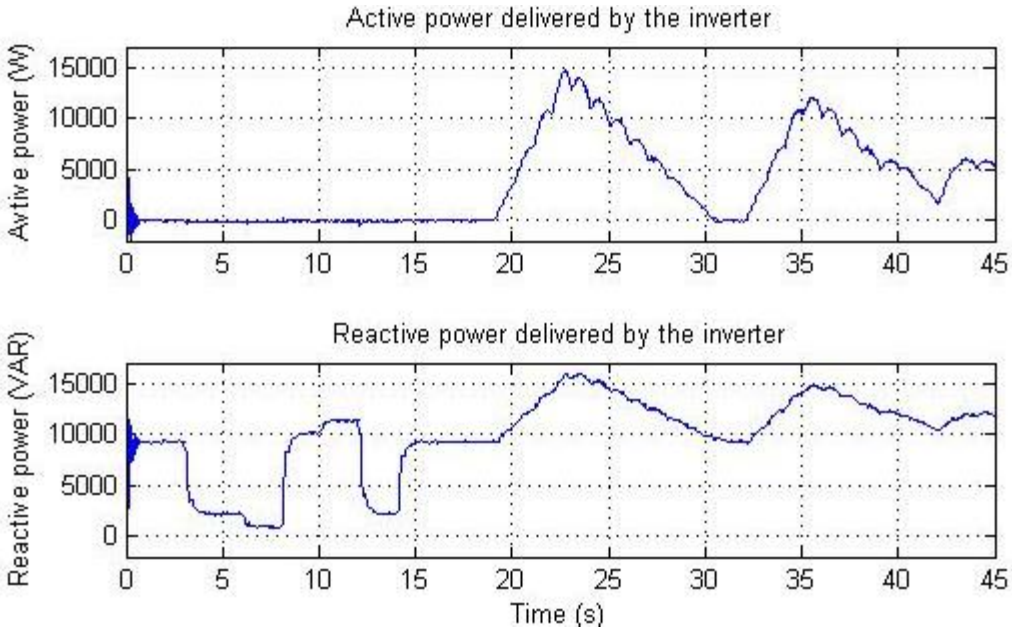


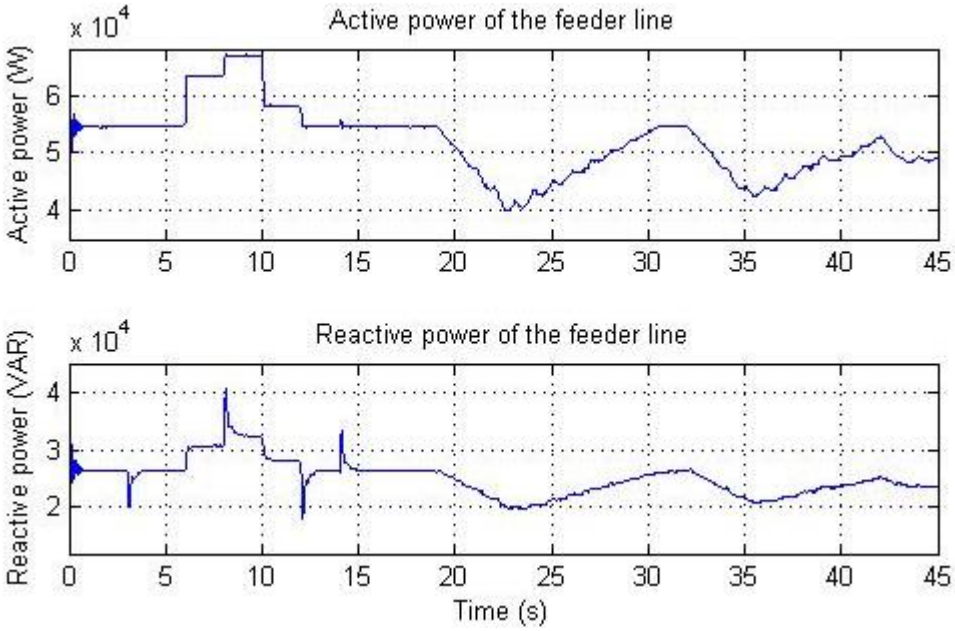
Figure 5.36 PF of the local distribution grid

5.4.3 Active and reactive power of the inverter and feeder line

Active and reactive power delivered by the inverter and active and reactive power of the feeder line are shown in Figure 5.37. These values are similar to the 5-level model simulation. As soon as the simulation starts, the inverter begins to provide compensation and generates capacitive VAR compensation. Therefore, the amount of active and reactive power provided by the feeder line to the load become 54 kW and 26 kVAR. Therefore, the inverter generates 9 kVAR in order to meet target PF requirements. At t=3 s, the total load of the system changes to 50 kW and 28 kVAR in addition to transformer and line losses. In this condition, the PF of the load becomes equal to 0.87 requiring lower reactive power compensation. Hence, the active and reactive power of the feeder lines remain constant and reactive power delivered by the inverter decreases to 2 kVAR. At t=6 s, the total load requires 60 kW and 31 kVAR making the PF 0.89 and requiring the inverter to inject less reactive power to the grid. Active and reactive power from the feeder line increase to 64 kW and 31 KVAR and reactive power delivered by the inverter also decreases to 1 kVAR. At t=8 s, the load demands 65 kW and 42 kVAR, making the PF 0.84.



(a)



(b)

Figure 5.37 (a) Active and reactive power delivered by the inverter, (b) active and reactive power of the feeder line

At this time, active and reactive power from the feeder line increase to approximately 68 kW and 32 kVAR and reactive power from the compensator becomes 10 kVAR in order to increase the PF of the grid from 0.84 to 0.90. At t=10 s, the load changes to 55 kW and 39 kVAR representing the PF of 0.81. In this condition, active and reactive power from the feeder line

decrease to 58 kW and 28 kVAR while reactive power from the inverter increases to 11 kVAR. At t=12, the load returns to 50 kW and 28 kVAR, making the PF 0.87. Hence, the active and reactive power of the feeder lines decrease to 54 kW and 26 kVAR and reactive power delivered by the inverter decreases to 2 kVAR. Consequently, after t=14, load conditions become identical to the beginning of the simulation, and active and reactive power remain constant while the reactive power of the compensator becomes equal to 9 kVAR. After t=19 s, as the output of the wind turbine increases, the amount of active power provided by the feeder line to the load decreases by the same amount. At t=23 s, active power of the inverter is equal to 14.5 kW, while active power from the feeder line is equal to 39.5 kW. The reactive power of the inverter is calculated by the controller system in order to fix the PF at its target value. Figure 5.38 shows the output PF provided by the inverter.

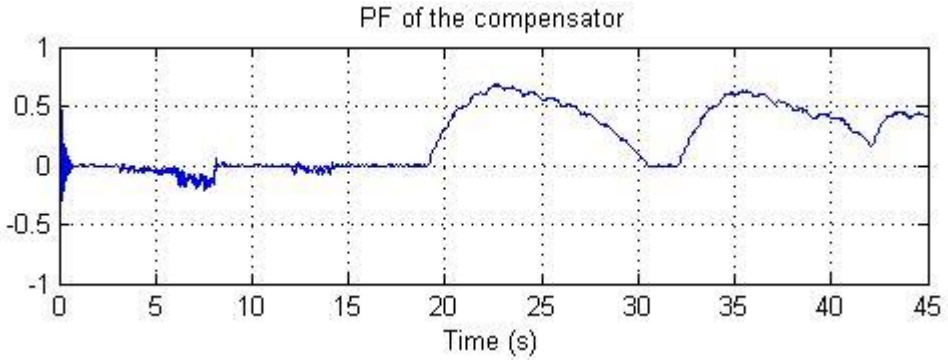


Figure 5.38 Output PF of the compensator

5.4.4 Power angle and modulation index of the inverter

Variations in power angle and modulation index, shown in Figure 5.39, are similar to the 5-level simulation. Before t=19, the power angle has slight variation due to load changes. After t=19 s, the controller increases the power angle in order to inject more active power to the grid to decrease the DC link voltage. The modulation index controller is responsible for reactive power transfer between the inverter and the grid, meaning that when additional reactive power is required, the controller increases the modulation index to inject more reactive power to the grid. For the 11-level inverter using PDPWM method, the feasible range of modulation index is limited to 0.8 to 1, since lowering the modulation index less than 0.8 can result in loss of voltage levels. In an 11-level PDPWM, 10 carrier signals are placed between -1 to 1 where each carrier amplitude is 0.2 V (peak-to-peak).

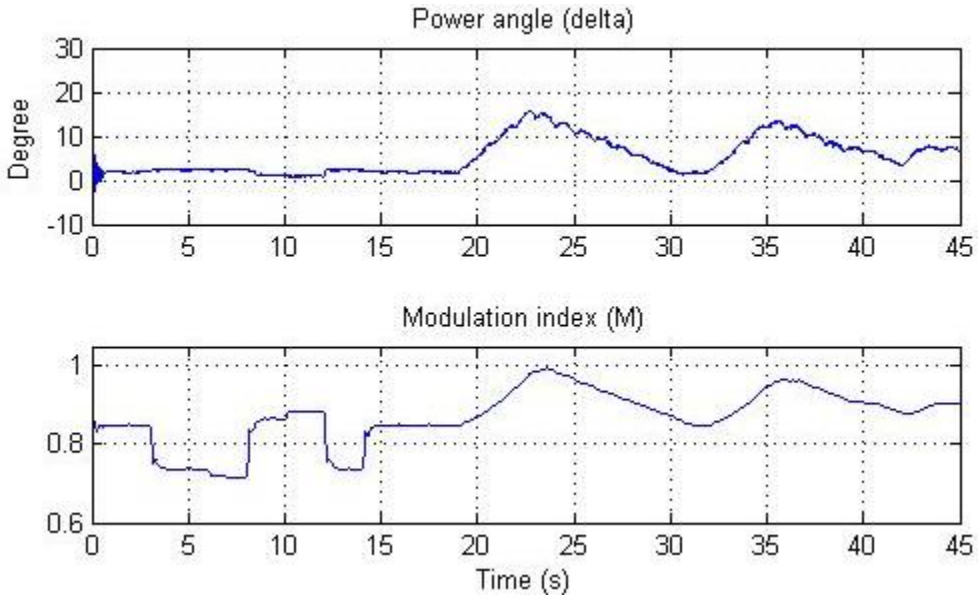


Figure 5.39 Power angle (delta) and modulation index (MI) of the inverter

5.4.5 DC link voltages

In this simulation, the reference value for the DC link voltage is 2000 V. Figure 5.40 shows the voltage of the DC link along with individual voltages across each DC link capacitors.

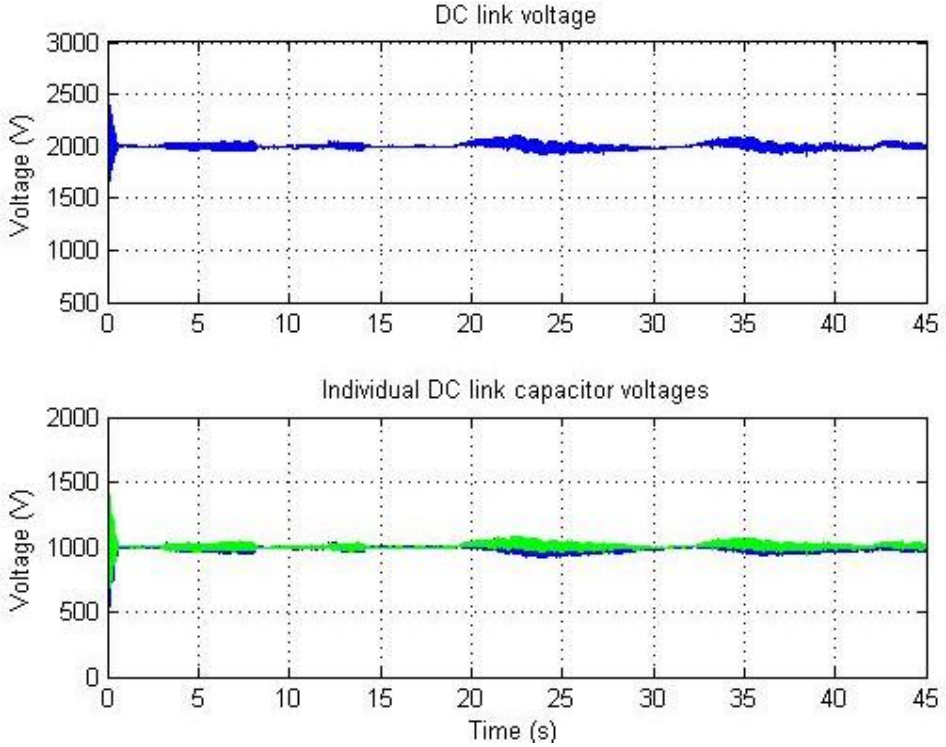
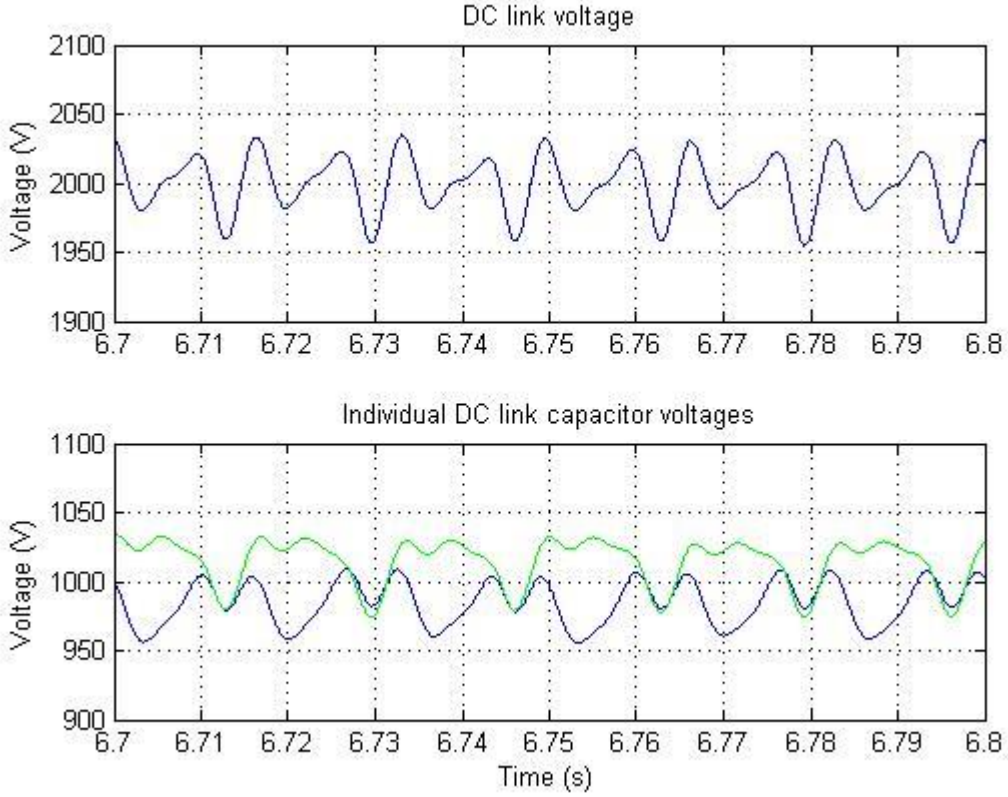
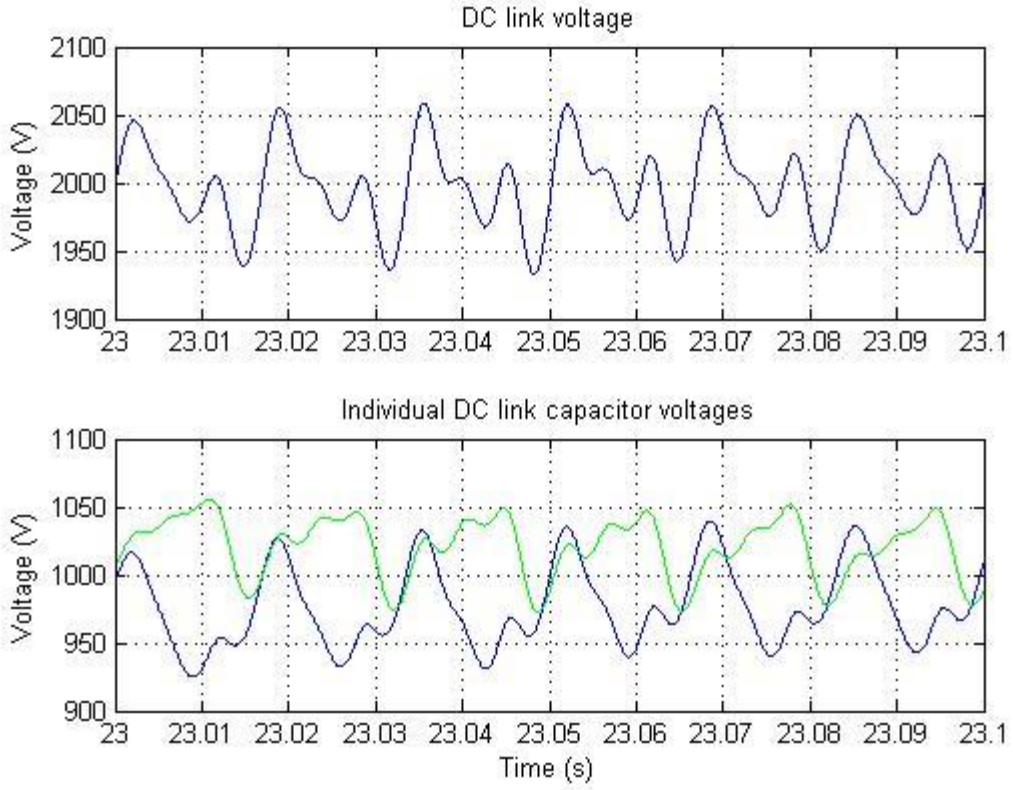


Figure 5.40 Voltages of the DC link and its capacitors

Figure 5.41 shows the DC link voltage and individual voltages across each DC link capacitor. Before t=19 s, in the worst condition the DC link voltage variation is within 50 V of 2000 V, representing a 2.5% variation. After t=19 s, the worst variation occurs at the most-input-power time, which is approximately 120 V below or above the reference value meaning a 6% variation. As demonstrated, before t=19 s, the voltage across each DC link capacitor settles to within 50 V of 1000 V and, after t=19 s, the voltage is within 100 V of 1000 V in the worst conditions.



(a)



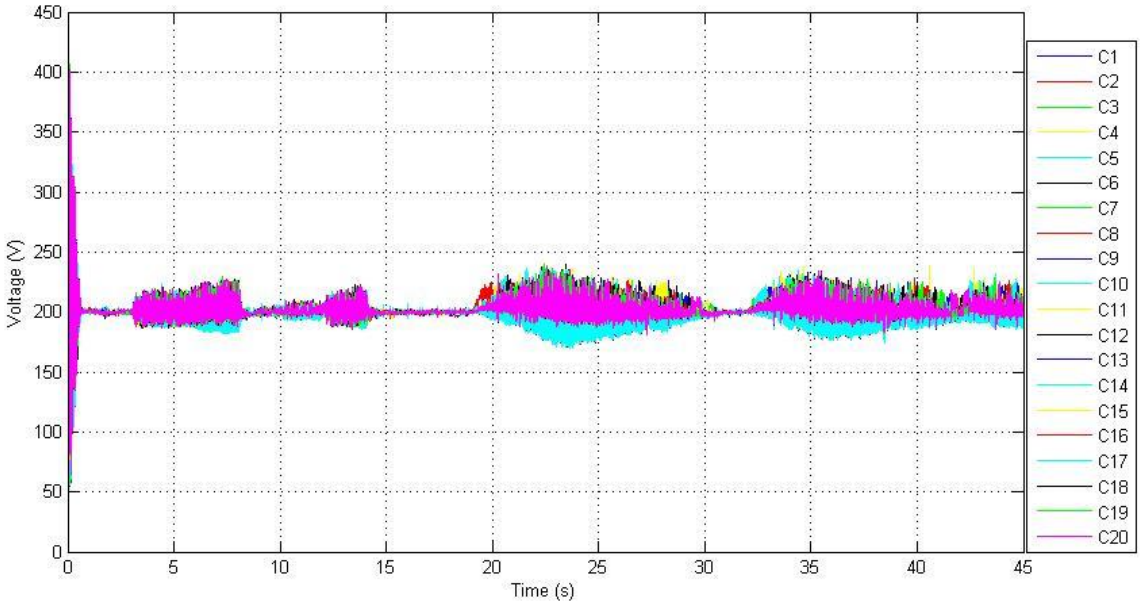
(b)

Figure 5.41 Variations of the DC link and its capacitors' voltages in worst conditions (a) before wind, (b) after wind

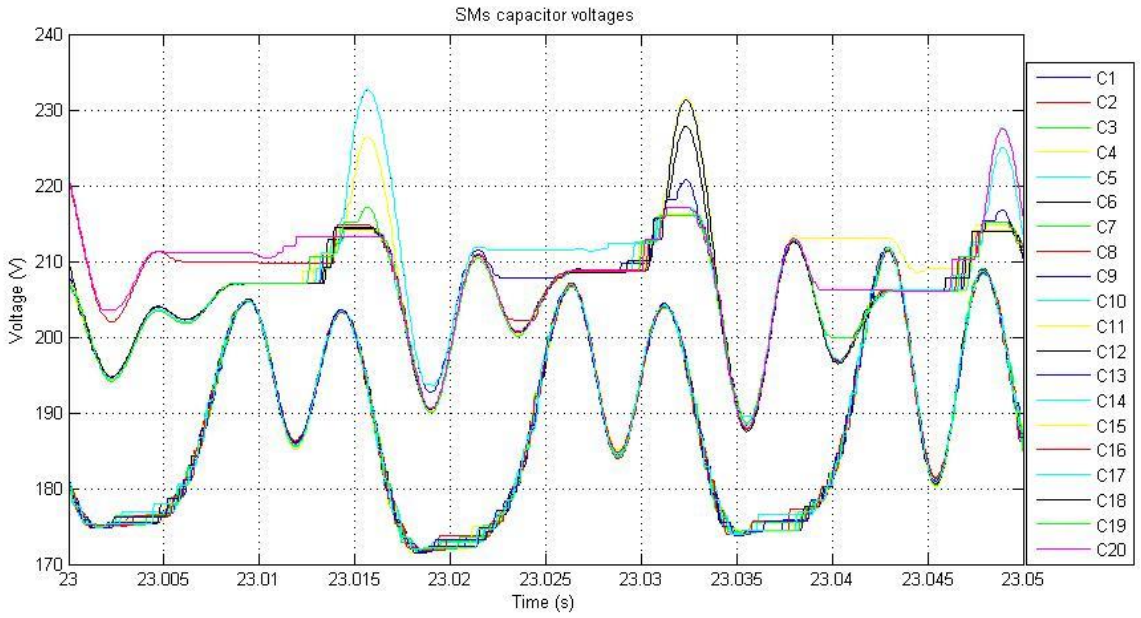
5.4.6 SMs capacitor voltages

Figure 5.42(a) shows voltages of 20 SM capacitors in an 11-level inverter using MMC topology. The ten upper SM capacitors have identical voltage at each instance, and the ten lower SM capacitors have equal voltages which differ from the upper SMs. Unlike the upper SMs, the lower SM capacitor voltages occasionally do not have the exact value. Lower SM capacitor voltages lose voltage equality because the controller system detects only the direction of the upper arm current and applies it for both upper and lower SMs. Therefore, in some instances, the lower SM capacitor voltages deviate from their reference. This issue has no significant effect on the overall performance of the system because it can be solved if both the upper arm current and lower arm current are taken into consideration in the PWM generation block. In other words, for the 5-level inverter, explained in Section 5.2.6, both the upper and lower arm currents are used to

detect the accurate current direction flowing in the upper and lower arm of the inverter. For the 11-level simulations, the lower arm current is neglected and only the upper arm current is used.



(a)



(b)

Figure 5.42 SM capacitor voltages

In this case, the voltage of each SM capacitor is equal to (2000/10) V, which equals 200 V with some variations. Figure 5.42 (b) details SM capacitor voltages.

5.5 11-Level inverter (250 W/VAR)

Section 5.4 demonstrated the simulation results for an 11-level inverter with a rating of 20kW/kVAR. Similar to the simulations for the 5-level reduced model (Section 5.3), to validate the 11-level inverter simulation results, another simulation with actual parameters used for the experimental tests has been done. An effort has been made to become the simulation conditions similar to the experiments. Hence, the data required for the components, such as switches, inductors, capacitors, switching frequency, and other important factors have been extracted from datasheets and used in this simulation. The simulation is 45 seconds long and demonstrates the performance of the proposed inverter for various wind speeds, producing various input active power levels to the inverter. The function of the inverter in all cases is to transfer active power from the wind turbine to the distribution grid as well as to compensate the PF of the local distribution grid at the target PF of 0.80. Table 5.10 shows the parameter values used for the low power (250W/VAR) simulation. In this simulation, the goal is to compare the results with the experimental results shown in Chapter 7.

Table 5.10 Parameter values used for the 11-level inverter (250W/VAR) simulation

Parameter	Value
L_{line}	1 mH
R_{line}	1 Ohm
L_{filter}	2.5 mH
C_{filter}	12 uF
Transformer power rating	5 kVA
Transformer primary voltage	120 V
Transformer secondary voltage	24 V
Switching frequency	2 kHz
Target PF	0.80
DC link reference value	80 V
Initial voltages of DC link capacitors	40 V
Initial voltages of SM capacitors	8 V
Transformer inductance	$R_1 = 0.0005\ p.u.$, $L_1 = 0.0005\ p.u.$ $R_2 = 0.0005$ p.u., $L_2 = 0.0005\ p.u.$

Discrete intervals for the amplitudes of the current controlled sources are similar to the values used in Section 5.3 (Table 5.6). Similarly, before t=19 s the input active power from the wind turbine is zero. At the 19th second of the simulation, power provided by the wind turbine ramps up to 75 W in four seconds and then ramps down to zero in seven seconds. During this part of simulation, there is no wind production for two seconds, and then at t=32 s, the wind turbine power ramps up again to 60 W in three seconds and then ramps down again to 10 W in seven seconds, consequently fixing at 30 W. Output active power from the wind turbine is shown in Figure 5.43.

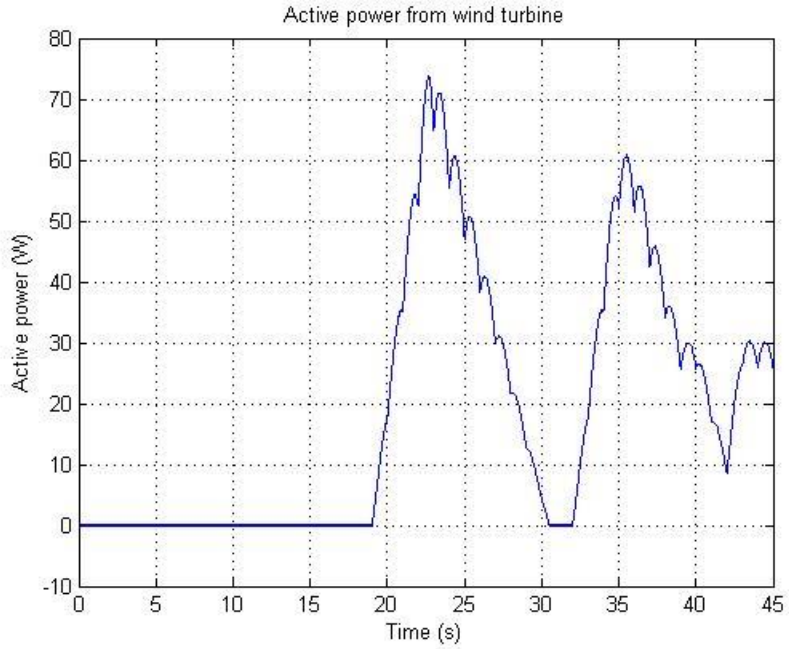


Figure 5.43 Output active power from the wind turbine

Similar to Section 5.3, the simulation begins with the selection of only load1 making the PF 0.65. At t=3 s, the PF of the load is changed to 0.68 by selecting load2 instead of load1. After three seconds, load3 is added to load2 making the PF 0.70. At t=8 s, load4 is also added to load2 and load3 making the PF 0.66. At t=10 s, load3 is removed, resulting in load2 and load4 again making the PF 0.62. After two seconds, load4 is also removed, resulting in having only load2, which makes the PF 0.68. Subsequently, at t=14, load1 is replaced by load2 making the PF 0.65 again. After this time, no load changes occur and, as a result, no PF variation. The process of load variation in respect to time is shown in Section 5.3 (Table 5.7). After t=14, the load PF is fixed at 0.65. The function of the proposed inverter is to fix the PF of the local distribution grid at the target PF, which is 0.80.

5.5.1 Output voltage and current of the inverter

Simulated output voltage of the proposed 11-level inverter (250 W/VAR) before and after the filter is shown in Figure 5.44.

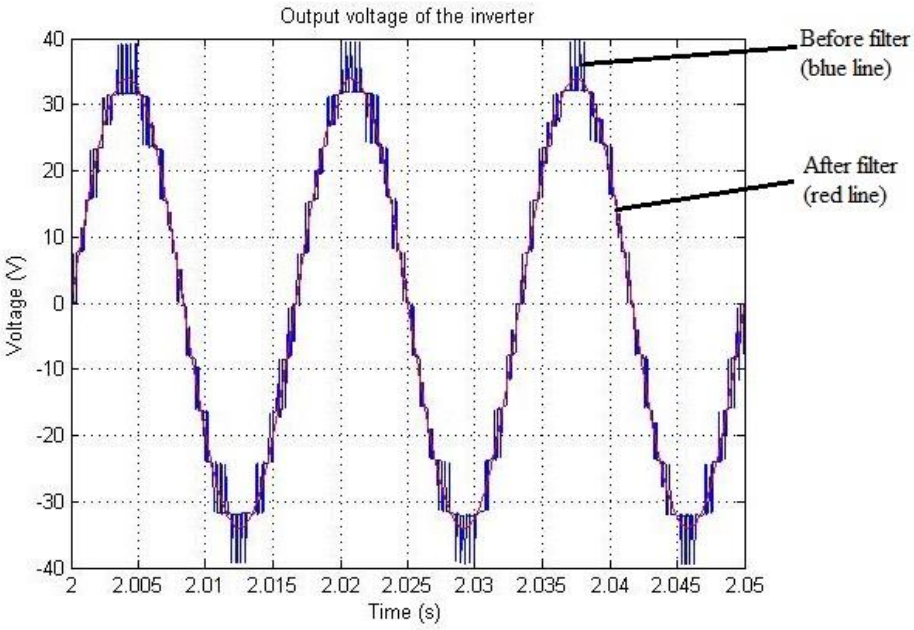


Figure 5.44 Simulated output voltage before and after the filter

The total harmonic distortion (THD) of the output voltage of the inverter after the filter is approximately 2.05%. Figure 5.45 shows the Fast Fourier Transform (FFT) of the filtered output voltage of the 11-level inverter. Figure 5.46 shows the current on both sides of the distribution transformer.

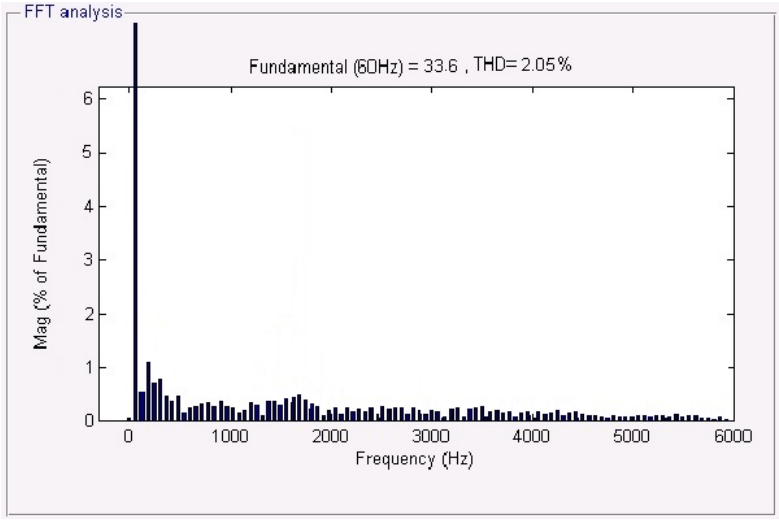


Figure 5.45 FFT of the filtered output voltage

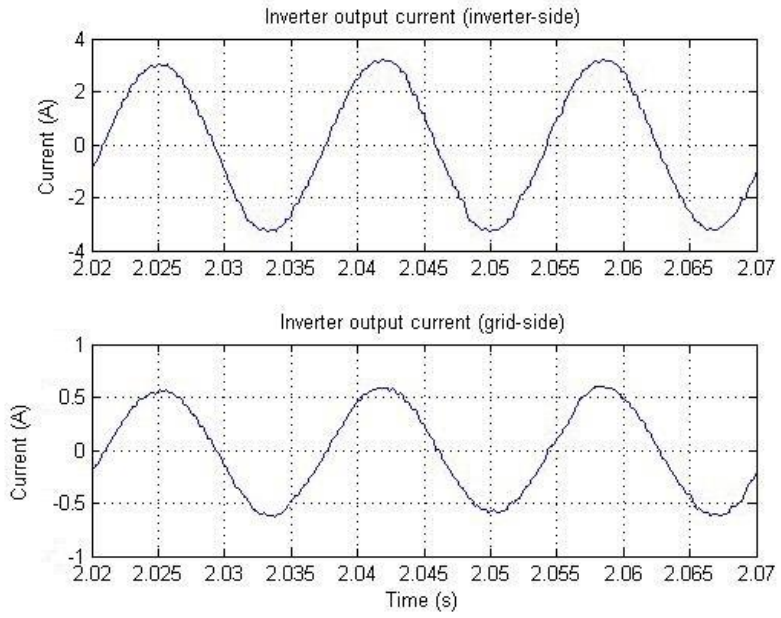


Figure 5.46 Output current on both sides of the distribution transformer

The THD of the output current on the inverter-side of the distribution transformer is 2.63%. Figure 5.47 shows the FFT of the inverter-side output current.

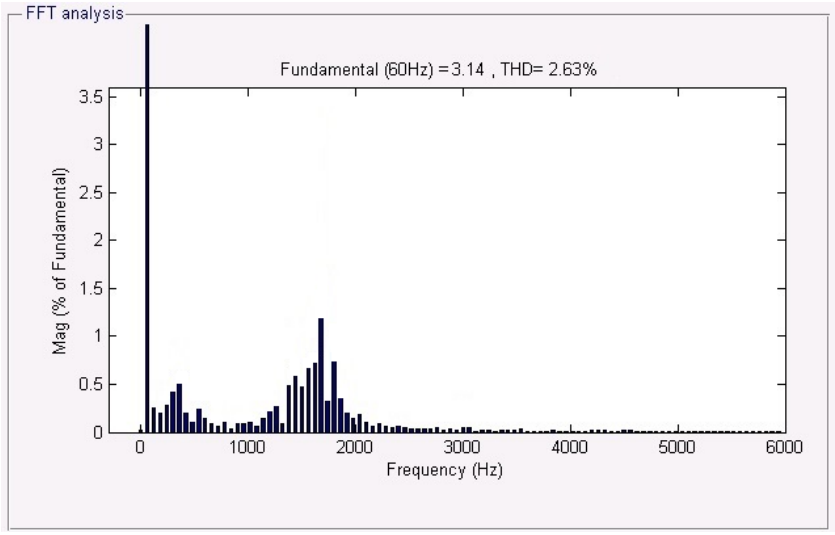


Figure 5.47 FFT of the inverter-side current

As Figure 5.47 shows, THD of the output current of the inverter is compliant with IEEE Standard 519 since the amplitude of each single harmonic is less than 3% of the fundamental frequency and the THD is less than 5%.

5.5.2 Power factor of the local distribution grid

Figure 5.48 shows the PF of the local distribution grid.

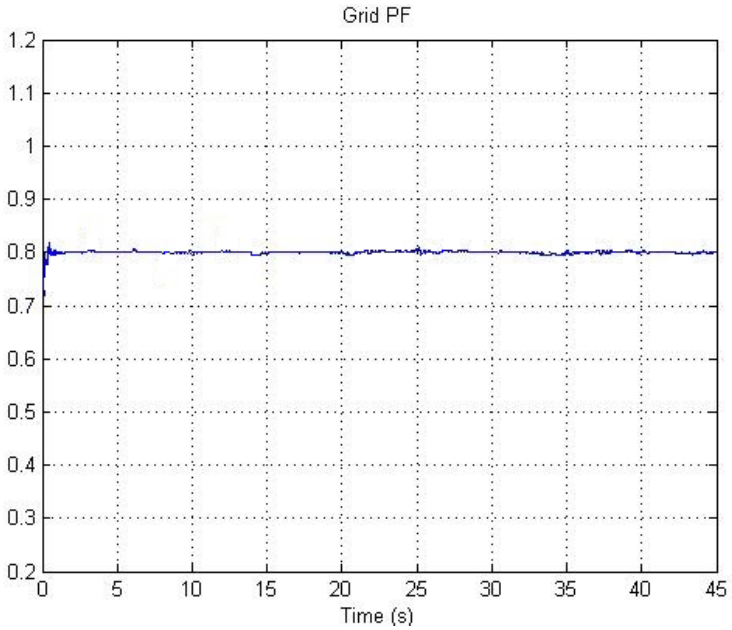


Figure 5.48 PF of the local distribution grid

Active and reactive power transferred between the wind turbine, grid and inverter are very similar to those shown in Section 5.3.3. Hence, in order to avoid duplication, the corresponding figures are not shown in this section. When active power from the wind turbine increases, active power gained from the grid decreases by the same amount. Grid active power reduction causes a decrement in reactive power provided by the grid, because the grid target PF is assumed to be constant. Therefore, by decreasing the reactive power provided by the grid, inverter reactive power is increased to support the load. In other words, by increasing the active power of the inverter, its reactive power increases as well.

Modulation index and power angle variations of the above simulation are also similar to those shown in Section 5.3.4. When active power of the inverter increases, power angle increases as well. Similarly, when the inverter is supposed to produce more reactive power, its modulation index is also increased, and vice versa.

5.6 Summary

Simulation results for the proposed 5- and 11-level inverter using MMC topology were presented in the previous sections. Modulation techniques used for both models are identical (PDPWM). The comparison between the two models can be explained in terms of several aspects. The first aspect is the number of elements used for both simulations. Table 5.11 demonstrates the number of components used for the single-phase 5- and 11-level models.

Table 5.11 Number of components used for all models

Component	5-level model	11-level model
SMs capacitor	8	20
Switch	16	40
Diode	16	40
DC link capacitor	2	2
Arm inductance	2	2
Total	44	104

Initially, Table 5.11 shows that the number of components used for an 11-level single-phase inverter is twice that of a 5-level inverter. However, voltage and current ratings of the components used for 11-level model are smaller, thus significantly reducing the total cost of the system. One important parameter in energy conversion systems is system reliability. System reliability is decreased when the number of elements in a system increases. Therefore, a simple comparison shows that overall reliability of a 5-level inverter is better than an 11-level inverter. However, the modular structure of MMC topology enables the use of several spare SMs for special applications in which the controller system can temporarily replace the impaired SM with a spare.

Table 5.12 shows the THD of the output voltage and current of the simulated 5- and 11-level systems.

Table 5.12 Output voltage and current THD for all models

Parameter	5-level (20 kW/kVAR)	11-level (20 kW/kVAR)	5-level (250 W/VAR)	11-level (250 W/VAR)
Filtered voltage	0.24%	0.23%	2.02%	2.05%
Current	5.8%	3.46%	4.19%	2.63%

As shown, the filtered output voltage of the 5-level inverter contains more harmonics than the 11-level inverter because as the number of voltage levels increases, the output staircase voltage becomes increasingly similar to a sinusoidal signal and, therefore, fewer harmonics are seen in the output waveform. The difference between the THDs of the two 5-level models is that in the second system (250 W/VAR), some harmonics have been added to the grid in order to make the simulations more similar to the experiments shown in Chapter 6 and 7. The output current of the

inverter in an 11-level inverter contains fewer harmonics as compared to the 5-level model. However, the output current of the large-scaled 5-level model (20kW/kVAR) is not completely compatible with IEEE 519 standard requirements because all individual harmonics are not less than 3% of the fundamental frequency and the THD is not less than 5%. The output waveforms of this model can be improved by using larger output filters which may increase the total cost of the system. In the 11-level simulation, the output voltage and current are completely compatible with standards (both systems) because each harmonic is less than 3% of the fundamental and the current THD is lower than 5%. This result has been achieved using a smaller filter than the 5-level model filter (for similar systems). Table 5.13 compares the values used for the output filter in both models for both systems (20kW/VAR and 250 W/VAR).

Table 5.13 Output filter used for all models

Parameter	5-level (20 kW/kVAR)	11-level (20 kW/kVAR)	5-level (250 W/VAR)	11-level (250 W/VAR)
L_{filter}	25 mH	20 mH	10 mH	2.5 mH
C_{filter}	90 uF	70 uF	25 uF	12 uF

Since the output of the 11-level model contains fewer harmonics than the 5-level model, a smaller output filter is required (for systems with similar rating) in order to reduce redundant harmonics, thus decreasing the total cost of the 11-level system.

Table 5.14 summarizes output filter values and resulting THDs for all simulations, including two 5-level models and two 11-level models.

Table 5.14 Comparison between output filter values used for all four simulations and resulting THDs

Parameter	5-level (20 kW/kVAR)	11-level (20 kW/kVAR)	5-level (250 W/VAR)	11-level (250 W/VAR)
L_{filter}	25 mH	20 mH	10 mH	2.5 mH
C_{filter}	90 uF	70 uF	25 uF	12 uF
THD of filtered voltage	0.24.%	0.23%	2.02%	2.05%
THD of current	5.8%	3.46%	4.19%	2.63%

Both the 5-level and 11-level systems have similar performance in terms of controlling the PF of the grid. Active and reactive power transfer between the compensator and the grid are similar in both simulations. The 11-level model seems to be more stable in conditions of rapid load

variations or wind speed changes, but the DC link voltage in the 11-level model experiences more oscillation than the 5-level model.

One important feature of the proposed inverter is system efficiency. The 11-level inverter uses 40 switches while the 5-level model uses 16 switches. This may increase power losses of the 11-level inverter. However, the switching frequency used for the 11-level inverter is lower than that of the 5-level inverter. Therefore, operating with a lower switching frequency enables a total power loss reduction and, as a result, increases inverter efficiency. Moreover, using a smaller filter reduces power losses associated with the output filter. A complete power loss analysis for both models, which is out of the scope of this dissertation, should be performed to determine the exact power losses in each inverter.

One of the primary design objectives of this inverter is minimal total cost since this inverter is intended to be used for small farms or businesses. The total cost of the 11-level system is greater than the 5-level model because the number of components increases for higher voltage levels. However, the 5-level model is unable to satisfy all standard requirements. Moreover, using a smaller output filter reduces the total cost of the system. In fact, a compromise exists between output quality and total cost of the system. In addition, the proposed inverter is a combination of two separate power electronic devices: an inverter and a D-STATCOM. A detailed cost comparison of the proposed inverter is presented in Chapter 8.

Chapter 6 - Setup implementation

In order to validate simulation results, reduced scale prototypes of the single-phase 5- and 11-level inverters were built and tested in the laboratory. The rating of the prototype inverters was below 250 W/VAR. Because the proposed inverter is a combination of inverter and STATCOM, its rating is declared in both W and VAR. These reduced scale inverters were used specifically to show proof of concept, and their rating was limited only by voltage and current ratings of the utilized components, such as switches and capacitors. Therefore, in order to reduce the costs of experimental setups, small-rated power MOSFETs (IRF 510) switches were used. Table 6.1 shows the ratings of these MOSFETs.

Table 6.1 Product summary of IRF 510

IRF 510 Summary	
V_{DS}	100 V
I_d	V_{GS}=10 V : 5.6 A
$R_{DS(on)}$	V_{GS}=10 V : 0.54 Ohm
$Q_{g(Max)}$	8.3 nC
Q_{gs}	2.3 nC
Q_{gd}	3.8 nC

As shown, voltage and current ratings of these semiconductor devices are low which consequently limits the inverter ratings. In fact, the ratings of prototype inverter models can be expanded easily only by replacing the components with larger-rated elements such as higher-rated MOSFETs or IGBTs. The controller system is able to expand to higher ratings with minor modifications. Figure 6.1 shows the schematic of the experimental implementation comprised of the PC with MATLAB program, dSPACE, inverter board, isolation board, distribution load, distribution transformer, DC motor, PM generator setup, and current and voltage sensors. Figure 6.2 shows the experimental setup used for testing the proposed inverters.

In the experimental tests for the 5- and 11-level models, only wind speed variations have been considered and the equivalent load remains constant for the entire test, unlike the simulations. In the following sections, all parts of the 5- and 11-level inverter are fully described. At the end of the chapter, results of the two models are compared.

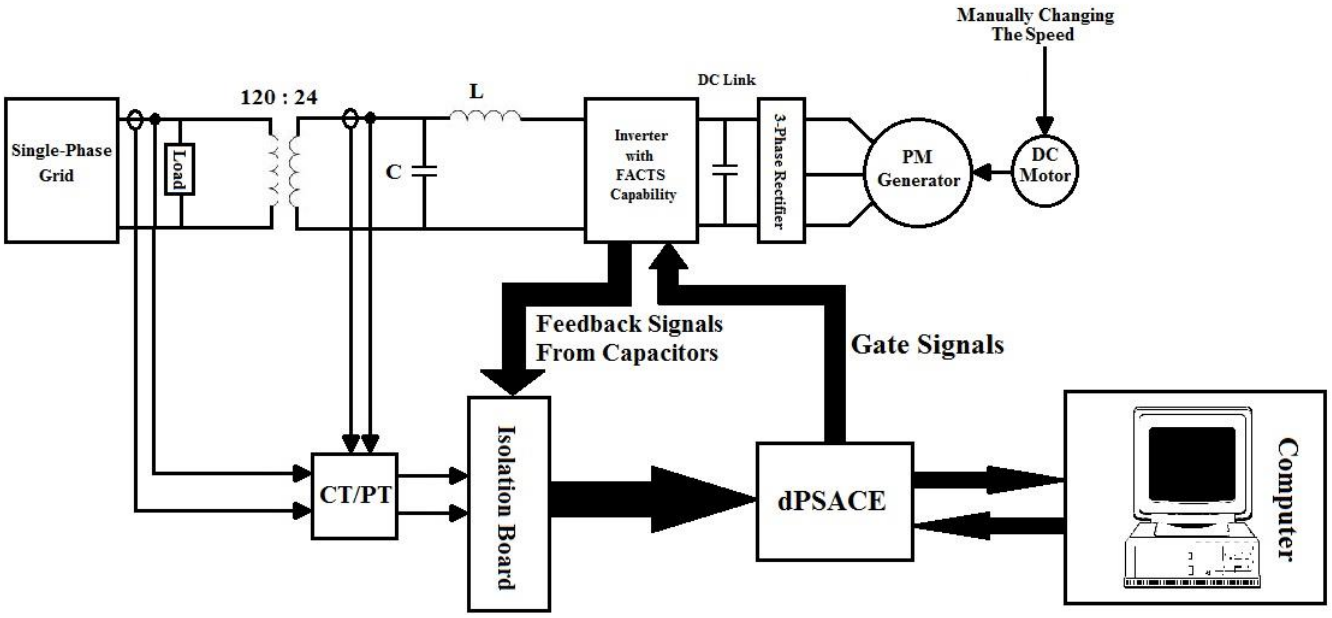


Figure 6.1 Schematic of the experimental setup

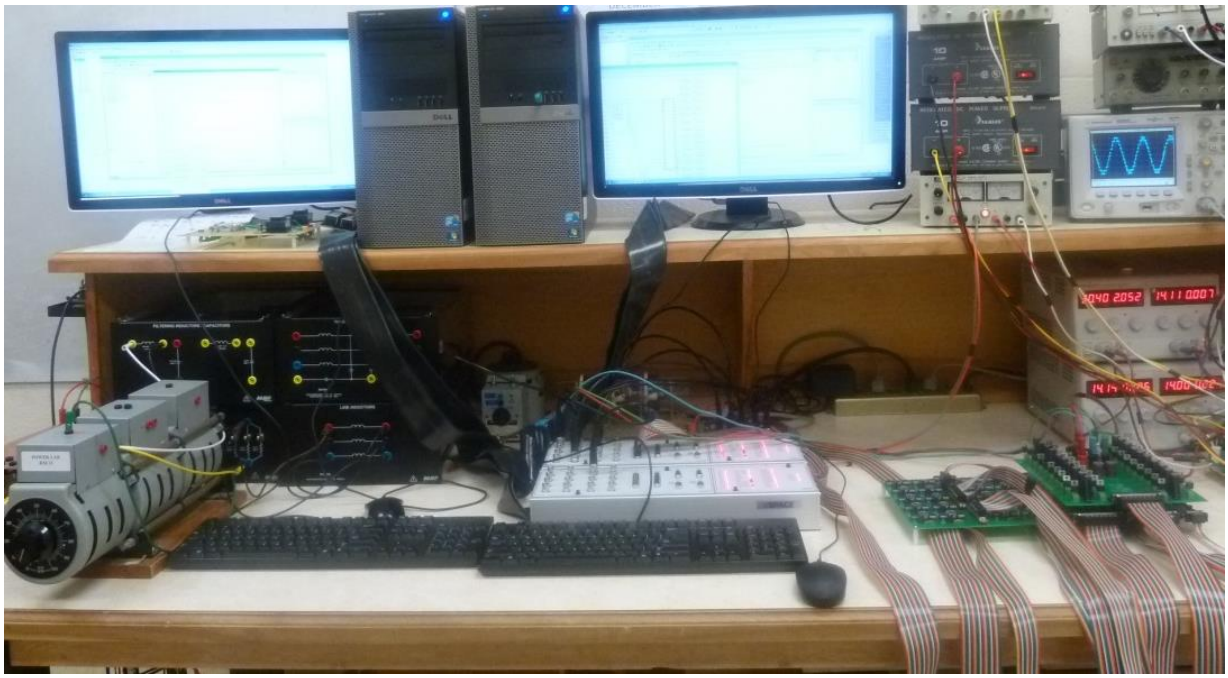


Figure 6.2 Bench setup used for experimental tests

6.1 5-Level inverter

6.1.1 Wind turbine model

One of the most effective ways to emulate wind speed variations is to use a programmable drive system operated with real wind data. In this application, the goal was to emulate wind speeds in order to assess the performance of the proposed inverter; therefore, a simpler system was utilized. In experimental tests, wind speed variations were emulated by using a 3-phase wound-rotor synchronous generator driven by a permanent magnet DC motor. Figure 6.3 shows the wind turbine emulator used to emulate wind speed changes. In this case, the input voltage of the DC motor was changed manually to increase or decrease the speed of the motor linked to the PM generator. The field current of the synchronous generator remained constant and only the shaft speed varied by the DC motor.

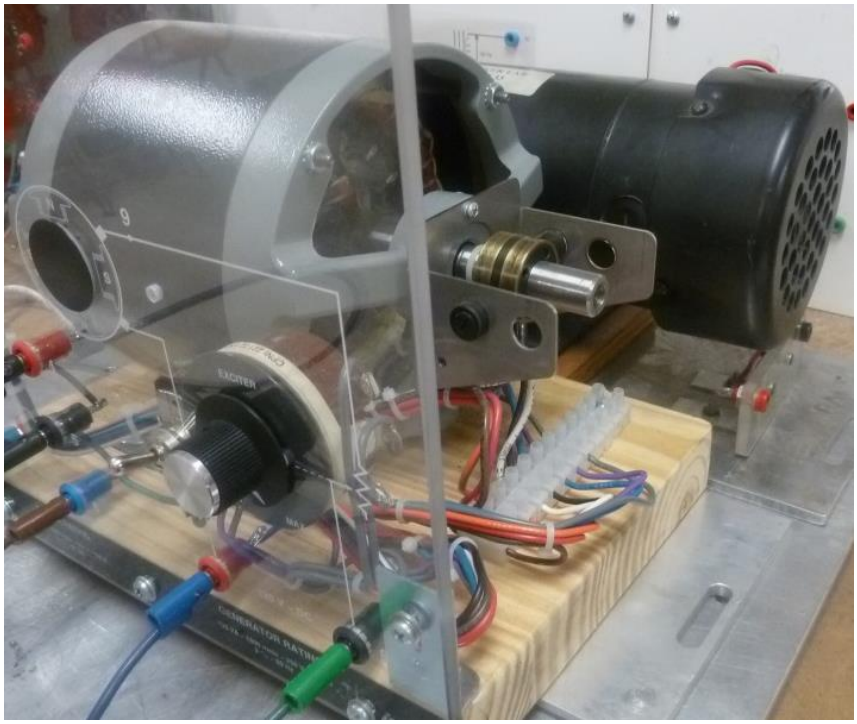


Figure 6.3 Experimental setup used for wind speed variations

When the DC motor is supplied with a higher voltage, it rotates faster and consequently the output voltage of the 3-phase generator increases and vice versa. In other words, the output voltage of the 3-phase PM generator is proportional to the DC motor shaft speed. The output of the PM generator is rectified through a 3-phase rectifier and connected to the DC link of the

inverter, such as a regular wind turbine inverter. Table 6.2 shows specifications of the DC motor and PM generator used to emulate wind speed variations.

Table 6.2 Specification of the motor and generator used for wind turbine emulation

Device	Specification
PM DC motor	HP: ½ RPM: 1225 Armature voltage: 90 VDC Armature current: 5.5 A
Wound-rotor synchronous generator	120 VA 208 V-0.33 A RPM: 1800

6.1.2 Inverter board

To validate simulation results, a reduced scale 5-level model of the system was built and tested. Figure 6.3 shows the 5-level scaled model consisting of power MOSFETs (IRF510), SM capacitors, DC link capacitors, hex logic inverter ICs (74LS04), opto-couplers (HCPL3120), BNC connectors and power terminals. Table 6.2 shows the number of major components used for the 5-level prototype model. Table 6.2 only includes major components.

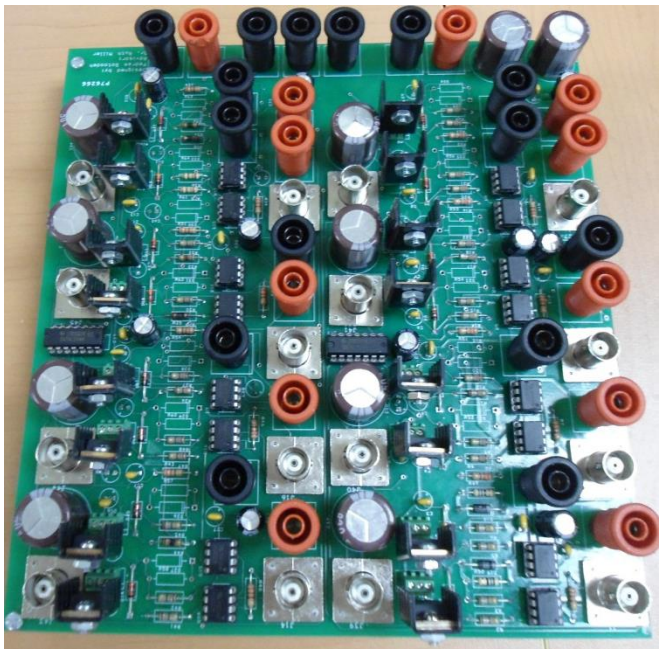


Figure 6.4 The 5-level reduced scale model

Other elements, such as noise reduction capacitors (decoupling capacitors), connectors, resistors, Zener diodes, and Schotky diodes are primarily used for the control (signal) circuit or gate-drive circuits of the power switches. As previously mentioned, the rating of the scaled 5-

level inverter is limited to 250 W/VAR, which is defined by the rating of the used components, specifically power switches. This rating can be increased to a higher value only by replacing the current components by ones with a higher rating.

Table 6.3 Major components used for the 5-level scaled model

Components	Specification	Number
IRF 510 (power MOSFET)	V_{DS}=100 V , $I_D \cong$ 5 A	16
SMs capacitor	820 uF-50 V (Electrolyte)	8
DC link capacitor	820 uF- 50 V (Electrolyte)	2
Gate drive opto-couplers (HCPL3120)	2.5 A output current	16
Hex logic inverter IC (74LS04)	PDIP	2

The single-phase 5-level inverter contains two parts, the control board and power board, which are combined in a two-layer 8" * 7.5" printed circuit board (PCB). In PCB design process, concentrated effort was made to obey electro-magnetic interference (EMI) rules to the extent allowed by the board space in order to reduce EMI issues such as noise on PWM signals. The control board consists of gate-drive ICs (HCPL3120), and the main application of HCPL3120 typically is for driving IGBTs; however, they are used to run power MOSFETs (IRF 510) in this application. The 5-level inverter possesses eight SMs, which translates to 16 switches and eight SM capacitors. Therefore, 16 gate-drive circuits were used to run the power switches. The specific structure of 5-level MMC topology requires the use of 10 power supplies for the single-phase inverter. In fact, power switches with common "Source" pins can use common power supplies, otherwise, each switch needs a separate power supply in order to avoid making short-circuits. Figure 6.5 shows the schematic of power supply arrangement used for the experimental 5-level inverter.

As previously mentioned, the 5-level inverter consists of 16 switches operating in a complementary manner, while the dSPACE (Section 6.1.3) used to generate PWM signals contains only eight digital-to-analog (DAC) outputs. Therefore, in order to convert the eight output signals from the dSPACE to 16 PWM signals, two hex logic inverter ICs (74LS04) were used, where each 74LS04 contains six logic "NOT" gates. As a result, a total of eight "NOT" gates were used.

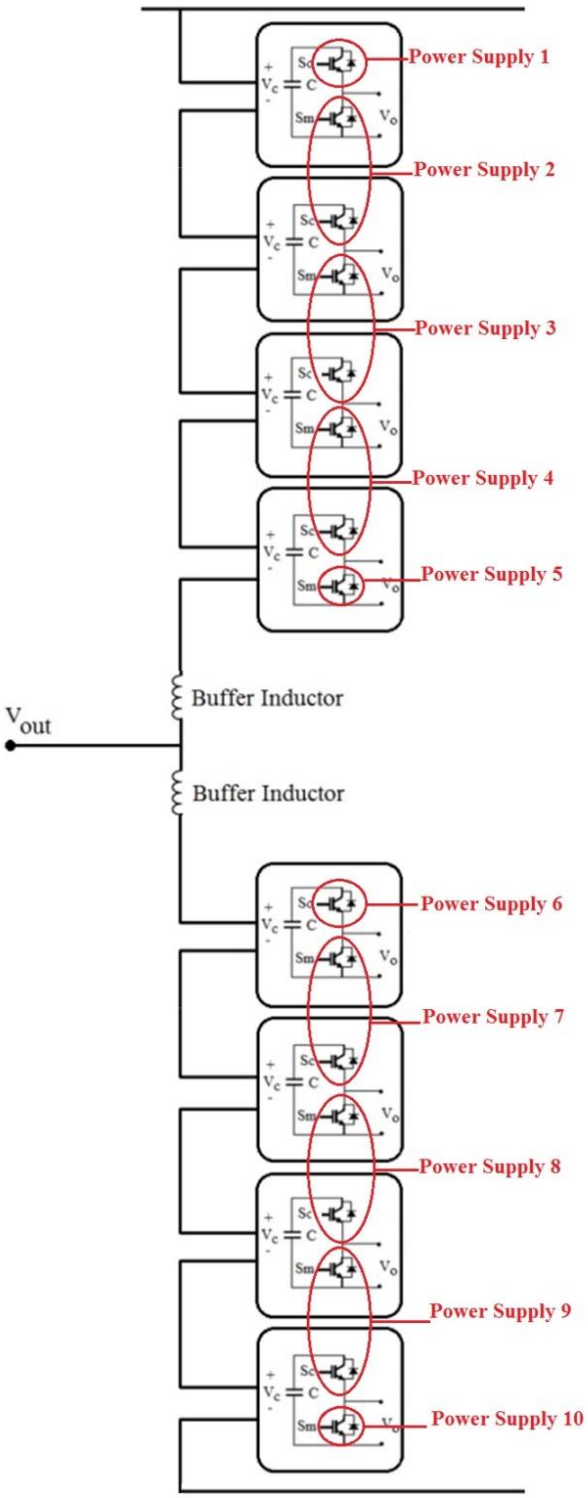


Figure 6.5 Schematic of power supply arrangement used for the 5-level system

6.1.3 dSPACE

The dSPACE 1104 R&D Controller Board (DS1104), shown in Figure 6.6, is a standard board designed for the implementation of high-speed digital controllers and real-time simulations in various fields. This board can be plugged into a PCI slot of a PC to be linked to MATLAB/Simulink. In other words, the DS1104 is a new hardware that can upgrade the PC to a powerful development system for rapid control prototyping. The DS1104 has the following specifications:

- Four multiplexed inputs to 16-bit analog to digital converter (ADC), four inputs with independent 12-bit ADCs, and an 8-output digital to analog converter (DAC).
- Two incremental encoders
- Onboard independent 64-bit floating point processor
- Onboard Slave DSP
- Onboard memory
- Other digital I/O capabilities

The real-time interface (RTI) provides Simulink blocks for graphical I/O configuration. In addition to the controller board, another piece of hardware called a connector panel, shown in Figure 6.7, provides easy access to all input and output signals of the controller board. The control program can be written in the Simulink environment combined with the real-time interface of the DS1104 board. In fact, the control system is designed in the Simulink environment and executed in real time using the dSPACE. After compiling the written code in Simulink, the codes are run on the DSP processor (TMS320F240 DSP) of the controller board.

Figure 6.6 dSPACE 1104 controller board (DS1104)

Controller parameters can be changed online while the experiment is running (real-time). In fact, the use of a dSPACE system can eliminate the need to write code for DPSs (or other types of controllers) in order to save time. This interface is a powerful tool for laboratory-scale experiments, identical to DSP (or other microcontrollers). dSPACEs can operate in regular mode or in specific applications in Master/Slave mode.

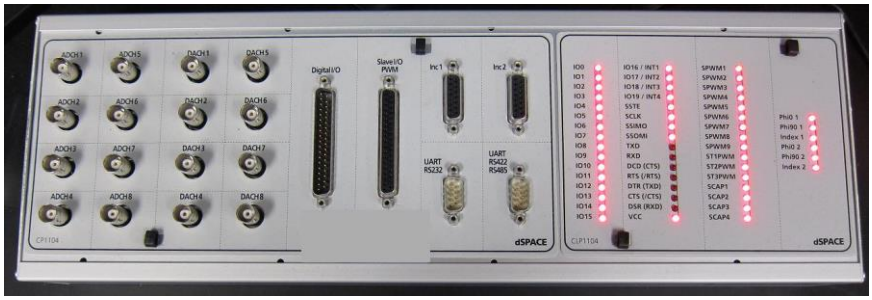


Figure 6.7 The connector panel of the DS1104

The dSPACE experiment software, called ControlDesk developer, is able to provide all functions to control and monitor experiments using graphical user interfaces in order to more effectively develop the controllers. In other words, ControlDesk enables users to generate simple graphical user interfaces, or layouts, with various control elements such as push-buttons, displays, radio buttons, complex plotters and photorealistic graphics. Use of this environment not only allows real-time control or monitoring of control parameters, but also access to I/O signals connected to hardware components.

For the 5-level experiment, one DS1104 operating in normal mode runs the written code in Simulink. This controller manages all outputs which are PWM gate signals to turn *On* and *Off* switches as well as all the inputs' feedback signals originating from various parts of the circuit. Input feedback signals include: 1) SM capacitor voltages, 2) direction of current flowing through the switches, 3) DC link voltage, 4) output voltage and current of the inverter, and 5) voltage and current of the grid. The output PWM generation signals are a combination of 0 and 1, thus determining the status of the switch to be *On* or *Off*. These logic values are converted to actual voltage values (15 V) through gate drive circuits. The other task of gate-drive circuits is to electrically isolate the power electronic device (inverter) from the dSPACE in order to protect the DS1104 board. All system I/O signals are connected to the DS1104 through the connector panel, as shown in Figure 6.7.

6.1.4 Isolation board

One important issue associated with the dSPACE is the commonality of the ground for all I/O signals. This problem shows itself when the dSPACE is required to measure several DC voltages. As previously mentioned, the voltages of all SM capacitors should be measured and sorted in descending order. Therefore, all voltage from the DC link voltage and SM capacitor should be connected to the dSPACE in order to be measured. Because all I/O signals of the dSPACE have a common ground, it is impossible to connect the feedback signals directly to the dSPACE because of short circuits caused among various parts of the circuit. Since capacitor signals are DC in nature, application of potential/voltage transformer (PT/VT) to isolate the signals is not possible. One means to solve this issue is to use DC voltage transducers in order to isolate feedback signals. Using DC voltage transducers increases the total cost of the system because the transducers take advantage of various isolation techniques such as galvanic isolation, etc. The other possible way is to use isolator circuits, such as instrumentation amplifier (INA) circuits or opto-coupler (OC) circuits. The right side of Figure 6.8 shows the schematic of using an isolation board between the inverter and the dSPACE.

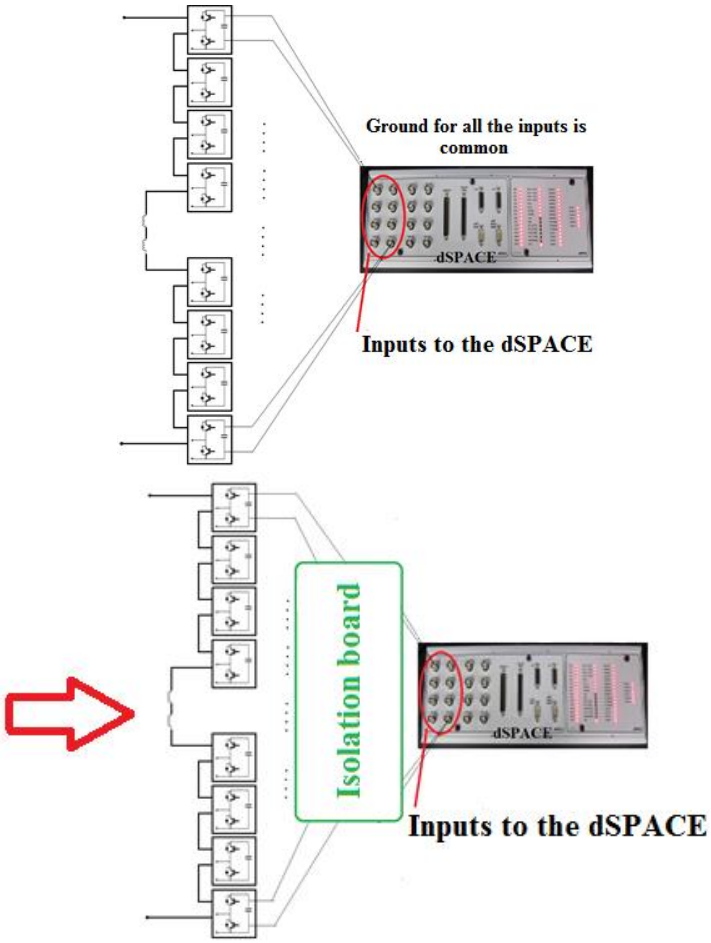


Figure 6.8 Schematic of using an isolation board

For the 5-level experiments, two different isolation boards were designed and tested. The first board uses instrumentation amplifiers. Figure 6.9 shows the designed INA isolation board in which "INA128" is used as the isolator component.

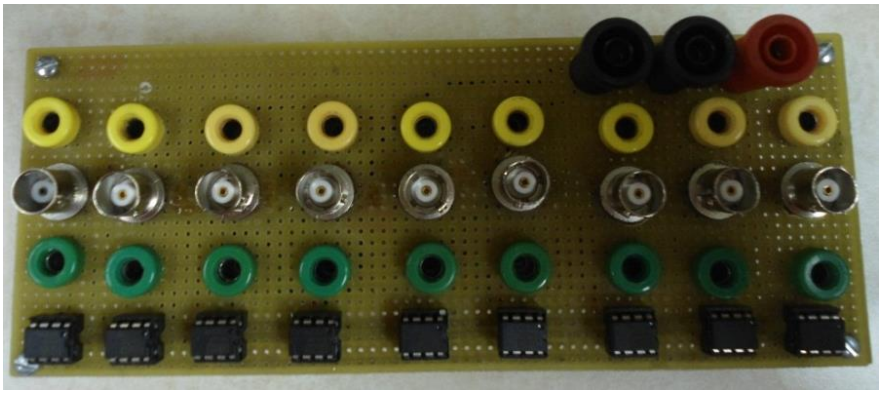


Figure 6.9 The instrumentation amplifier isolation board designed for the 5-level system

The INA128 isolates the inputs (feedback signals-voltages of SM capacitors) and the outputs (the inputs to the dSPACE). This isolation board performs correctly in terms of isolating the 5-level system. The only disadvantage of the INA board is that INA output voltages become significantly noisy for higher voltages, which might cause malfunction of the controller system. Another alternative to the isolation board is to use opto-coupler (OC) circuits. The OC isolation board, as shown in Figure 6.10, was designed and tested as an alternative to the INA board for the 5-level model. The OC isolation board uses "LOC110" chips and has effective isolation between its input and output signals. Use of the OC board isolates the voltages of the capacitors from the dSPACE.

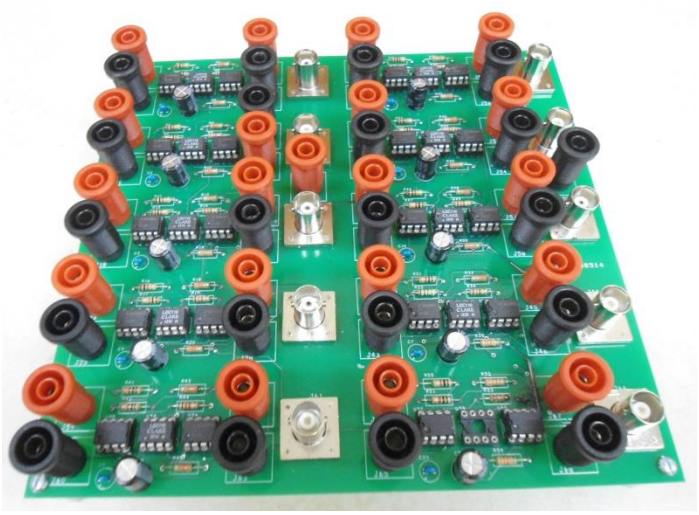


Figure 6.10 The opto-coupler isolation board designed for the 5-level system

6.1.5 Other hardware

In addition to the wind turbine model, inverter, dSPACE, and the isolation board explained in previous sections, other hardware was also used for the 5-level experiment. To connect the inverter to the grid a single-phase variable autotransformer was utilized. Moreover, the distribution equivalent load was made by a combination of power resistors and inductances. To measure voltages of the grid and the output voltage of the inverter, two potential transformers (signal transformer 14A-2.5R12) and two current transformers (13/10TALEMA) were used in order to decrease amplitude of the signals to the suitable range for the dSPACE. Figure 6.11 shows the power loads and the PTs and CTs used for the 5-level experiment.

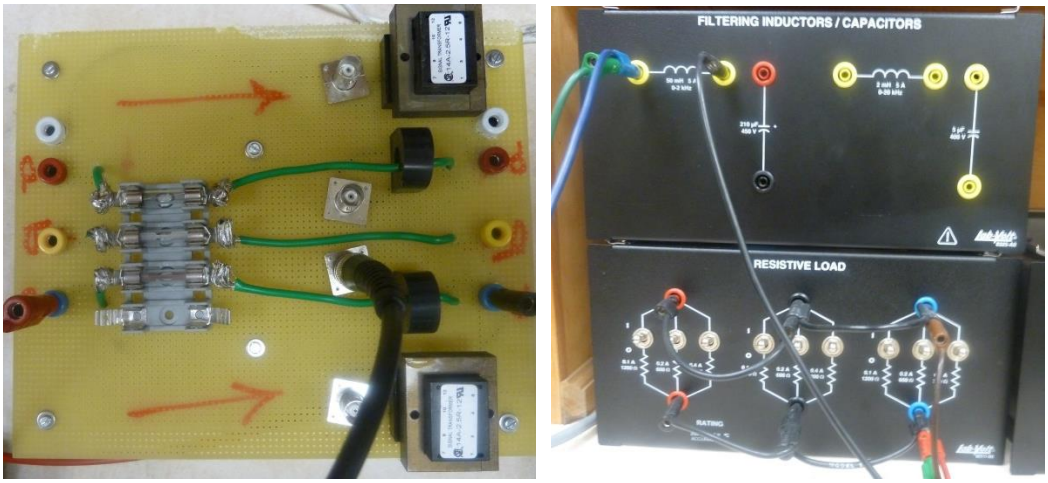


Figure 6.11 Equivalent load and the current and voltage sensors used for the 5-level system

In addition, several power supplies (Sorensen XPL 30-2D Dual DC power supply) were used for the gate-drive opto-couplers and the isolation board. An oscilloscope (Agilent MSO6032A-300 MHz) is used to measure system output waveforms, and to measure the THD of the output signals, a power quality analyzer (AEMC-PowerPad Jr. 8230) is utilized.

6.2 11-level inverter

6.2.1 Wind turbine model

The experimental setup used for the 11-level system is similar to the 5-level model (Section 6.1). The wind turbine model used for the 11-level experiments was identical to the one used for the 5-level system (Section 6.1.1).

6.2.2 Inverter board

The primary difference between the 5- and 11-level experimental setup is the inverter board. The 11-level reduced-scale inverter is shown in Figure 6.12. The 11-level inverter consists of two separate boards. The bottom board is the control (signal) board, containing gate-drive circuits and noise reduction circuits. The top board is the power board, containing SMs comprised of power switches and SM capacitors.

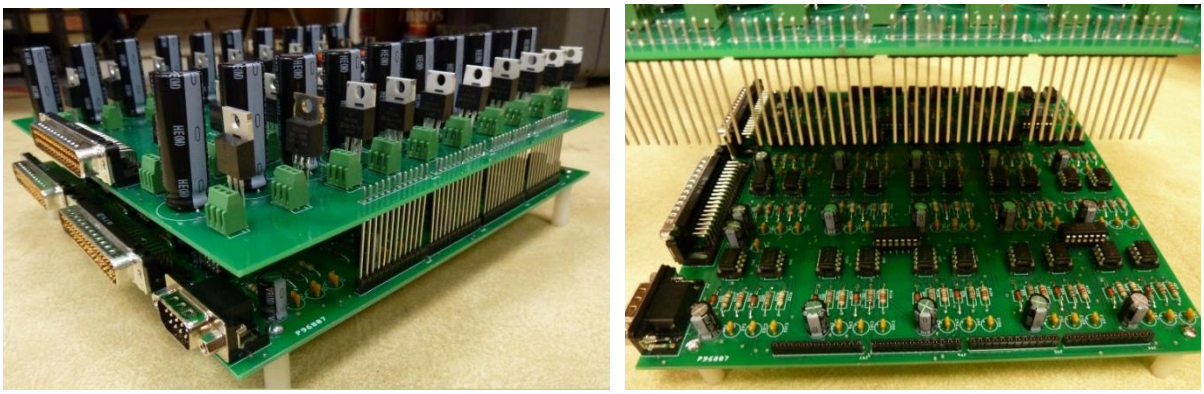


Figure 6.12 The 11-level reduced scale model

As with the 5-level model, power switches used for the 11-level inverter were "IRF 510," which have small voltage and current ratings. Therefore, the rating of the 11-level inverter is 250 W/VAR, identical to the 5-level model. The reduced scale 11-level inverter was developed as proof of concept. The rating of the inverter can be expanded to higher values simply by replacing the components (specifically the power switches) with higher-rated components. As with the 5-level model, other elements such as noise reduction capacitors (decoupling capacitors), connectors, resistors, Zener diodes, and Schotky diodes are primarily used for the control (signal) circuit or gate-drive circuits of the power switches.

The 11-level inverter possesses 20 SMs, which translates to 40 switches and 20 SM capacitors. Therefore, 40 gate-drive circuits were used to run the power switches. The specific structure of the 11-level MMC topology requires the use of 22 power supplies for the single-phase inverter. In fact, power switches with common "Source" pins can use common power supplies; otherwise, each switch needs a separate power supply in order to avoid creating short-circuits. In the 11-level experiment, a power board consisting of several transformers with diode bridge rectifiers was built to generate 22 DC supplies from a single AC input. In a commercial inverter, a similar board is needed to generate various voltages in order to supply different parts of the circuit. As mentioned, the 11-level inverter consists of 40 switches operating in a complementary manner. In the 11-level implements, two dSPACES were used (Section 6.2.3). The first dSPACE was configured to generate PWM signals using its Digital I/O ports. In order to convert the 20 PWM signals generated by the digital I/O ports of the first dSPACE to 40 PWM signals (required for the 11-level inverter switches), four hex logic inverter ICs (74LS04) were used. Each IC contains six logic "NOT" gates. A total of twenty "NOT" gates were used to feed all 40 switches of the 11-level inverter.

6.2.3 dSPACE

As mentioned in Section 6.2.3, for the 11-level system, two dSPACES were used to implement the controller system. Using two dSPACEs achieves better controller performance because voltage balancing of the 11-level inverter is very sophisticated. Figure 6.13 shows the connection of two dSPACEs for the implementation of the controller system. The function of the first dSPACE is to generate PWM signals for 40 switches. The dSPACE contains a digital I/O unit with 20 digital I/O pins. The direction of each pin can be selected by software to operate as input or output. Therefore, the first dSPACE only generates 20 PWM signals for the switches.

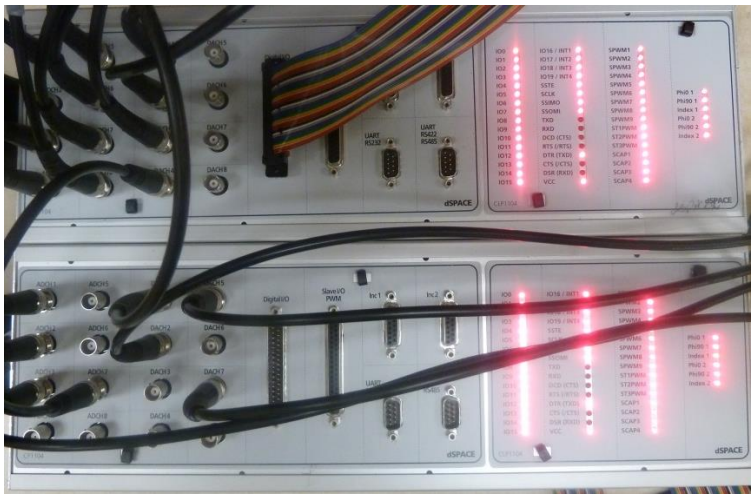


Figure 6.13 Connecting two dSPACEs to implement the 11-level controller system

The signals are then converted to 40 signals using hex logic inverter ICs (74LS04). The function of the second dSPACE used for the 11-level system is to measure and process a number of feedback signals. In this way, all application requirements are met. Because calculations for voltage balancing of the 11-level inverter are complicated, two dSPACES were used to divide the control algorithm in order to obtain better results since using only one dSPACE may lead to undesired controller performance. Moreover, the voltage of the 20 SM capacitors should be measured by the first dSPACE, while each dSPACE has only eight analog to digital converters (ADCs). Therefore, an interface is needed between the isolation board and the first dSPACE to convert eight ADC channels to 20. For this purpose, a multiplexer circuit is used. In the multiplexer board, three 8-channel analog multiplexer ICs (HCF4051BE) are used. This multiplexer possesses 8 input channels, one output channel, and three selector pins. The output signal is equal to one input signal, depending on the status of its selecting pins. Figure 6.14 and Table 6.4 show the schematic and truth table of the HCF4051BE, respectively.

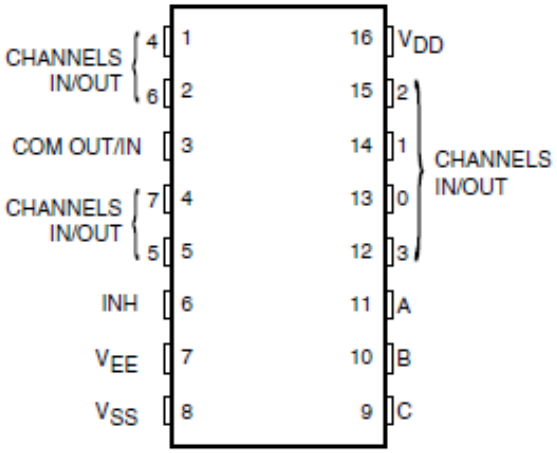


Figure 6.14 Schematic of the analog multiplexer IC (HCF4051BE) used for the 11-level system

Table 6.4 Truth table for the analog multiplexer used for the 11-level system

Input States				**"ON" Channel**
Inhibit	C	B	A	-
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	X	X	X	None

Based on the status of selector pins, the output channel of the multiplexer becomes equal to one input channel. In the 11-level implementation, each input channel of the multiplexers (outputs of the isolation board) are periodically selected each 500 ms and then read by the controller system. Therefore, the dSPACE with only eight ADC channels is able to read 20 analog signals (SM voltage capacitors) using three analog multiplexers. Consequently, for the 11-level experiment, two DS1104 controllers, operating in synchronized mode, run the written code in Simulink.

6.2.4 Isolation board

The purpose of the isolation boards was described in Section 6.1.4. In the 11-level implementation, an isolation board must be placed between the inverter board and the dSPACE. In fact, a multiplexer board is located between the isolation board and the dSPACE in the 11-level system. Because the ground of all inputs of the dSPACE is common, the function of the isolation board, as with the 5-level model, is to cause isolation between feedback signals originating from the SM capacitors. Figure 6.15 shows the isolation board used for the 11-level system utilizing opto-coupler circuits. Figure 6.16 shows the connection between the inverter board and the isolation board in the 11-level configuration.

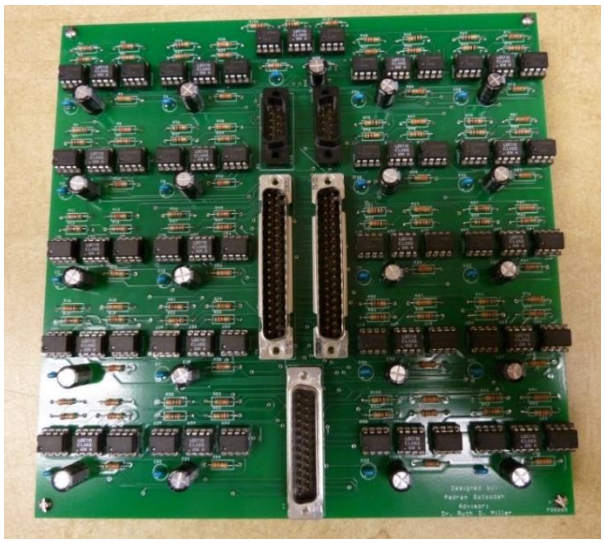


Figure 6.15 The opto-coupler isolation board designed for the 11-level system

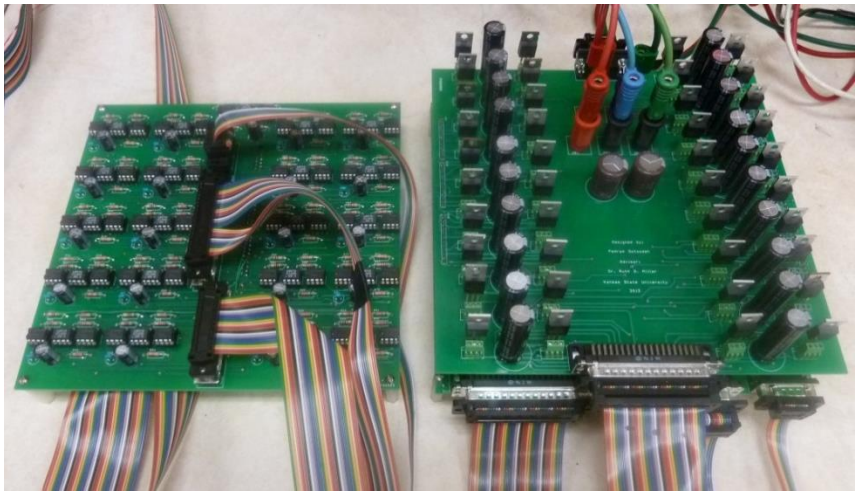


Figure 6.16 Connecting the inverter board to the OC isolation board in the 11-level configuration

6.2.5 Other hardware

In the 11-level system, as with the 5-level model, in addition to the wind turbine model, inverter, dSPACE, and isolation board, other hardware is necessary, such as a single-phase variable auto-transformer to connect the inverter to the grid, a distribution equivalent load made by a combination of power resistors and inductances, voltage and current sensors (signal transformer 14A-2.5R12 and 13/10TALEMA) to measure the voltage and current of the inverter and the grid, power supplies (Sorensen XPL 30-2D Dual DC power supply), oscilloscope (Agilent MSO6032A-300 MHz), and power quality analyzer (AEMC-PowerPad Jr. 8230).

6.3 Summary

In order to validate simulation results, a reduced scale prototype of the single-phase 5- and 11-level inverters were built and tested in the laboratory. The rating of the prototype inverters was below 250 W/VAR. Because the proposed inverter is a combination of inverter and STATCOM, so its rating is declared in W and VAR. These reduced scale inverters were used specifically to show proof of concept, and their rating was limited only by voltage and current ratings of the utilized components, such as switches and capacitors.

In the experimental tests for the 5- and 11-level models, only wind speed variations have been considered and the equivalent load remains constant for the entire test, unlike the simulations.

In order to emulate the wind turbine, a 3-phase synchronous generator driven by a permanent magnet DC motor is used. The input voltage of the DC motor was changed manually to increase or decrease the speed of the motor linked to the generator. The field current of the generator remained constant to emulate a permanent magnet generator, and only the shaft speed was varied by the DC motor.

In order to implement the controller system, a dSPACE 1104 is used. This device is a hardware interface between the PC and inverter which is linked to MATLAB and implements the written code (in MATLAB) to generate real signals utilized by the inverter.

One important issue associated with the dSPACE is the commonality of the ground for all I/O signals. This prevents connecting of all the feedback signals directly to the dSPACE. In order to solve this problem, an isolation board is needed between the inverter and dSPACE. Therefore, two isolation circuits using instrumentation amplifiers (INAs), and opto-couplers (OCs) were built and tested.

Chapter 7 - Experimental results

7.1 Overview

To validate simulation results, the 5- and 11-level experiments were performed separately. The aim of the experiments is to recognize the performance of the proposed inverter and its control strategy in various wind speed conditions. As explained in Chapter 6, the power rating of the scaled prototype model is 250 W and/or VAR, which is limited by the rating of the semiconductor devices. Experimental results serve only as a proof-of-concept. In both 5- and 11-level experiments, the load is constant and only wind speed is changed. Before the compensation, the PF of the load which is a combination of power resistors and inductors is 0.65. In this case the inverter is disconnected from the grid by a power switch. In this chapter, experimental results have been obtained using the ControlDesk program, described in Section 6.1.3, in addition to the power quality analyzer (Section 6.1.5). Figure 7.1 shows the grid voltage and current waveforms before compensation. Figure 7.2 shows the FFT of the grid voltage. Figure 7.3 provides the active power, reactive power, and the PF of the grid before compensation, captured by the power quality analyzer. The voltage and current THD of the grid before compensation are 1.5% and 1.8%, respectively.

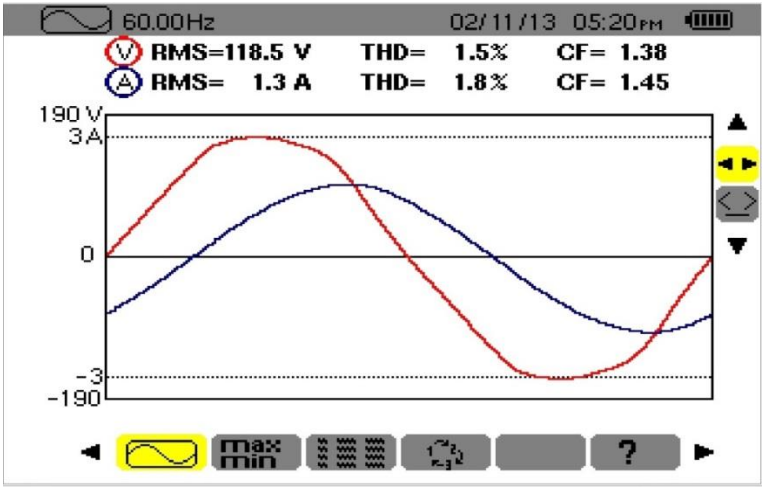


Figure 7.1 Voltage and current waveforms of the grid before compensation

The following sections show the experimental results when the inverter is connected to the grid (grid-connected mode) in order to compensate the PF of the grid as well as operate as a regular wind inverter.

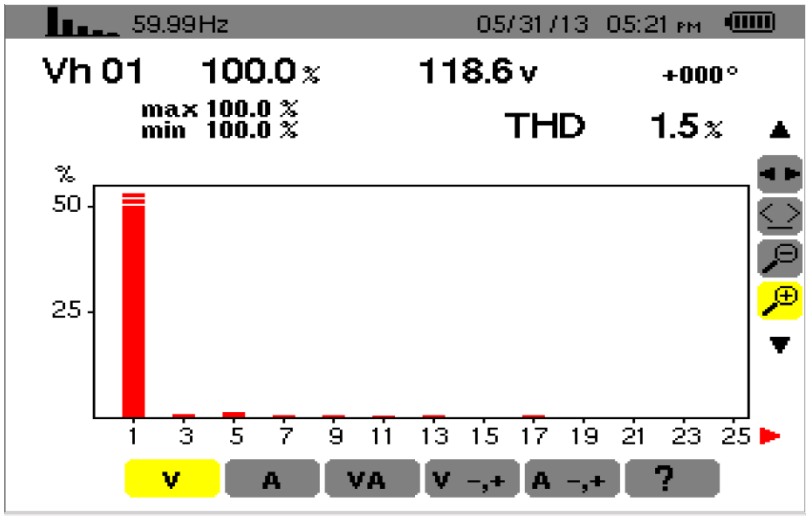


Figure 7.2 FFT of the grid voltage before compensation

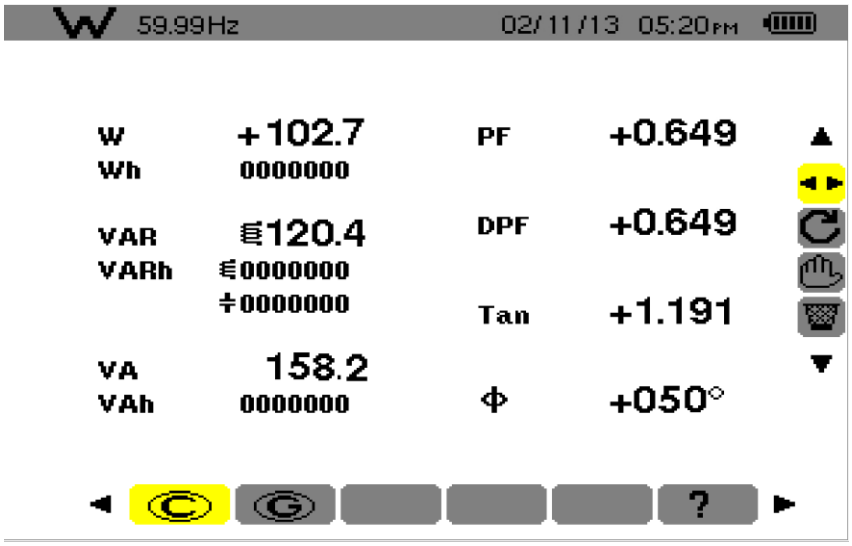


Figure 7.3 Active power, reactive power, and PF of the grid before compensation

7.2 5-Level inverter

7.2.1 After compensation: Target PF=0.80

In this case, the inverter is connected to the grid through a second-order LC filter with values of 10 uH and 25 uF. The target PF is set to 0.80. Therefore, the function of the inverter is to compensate the PF of the local grid from 0.65 to 0.80 by injecting enough reactive power to the grid regardless of the input active power from the wind turbine emulator. Figure 7.4 illustrates

the unfiltered output voltage of the 5-level inverter. Figure 7.5 shows the filtered output voltage and current of the inverter.

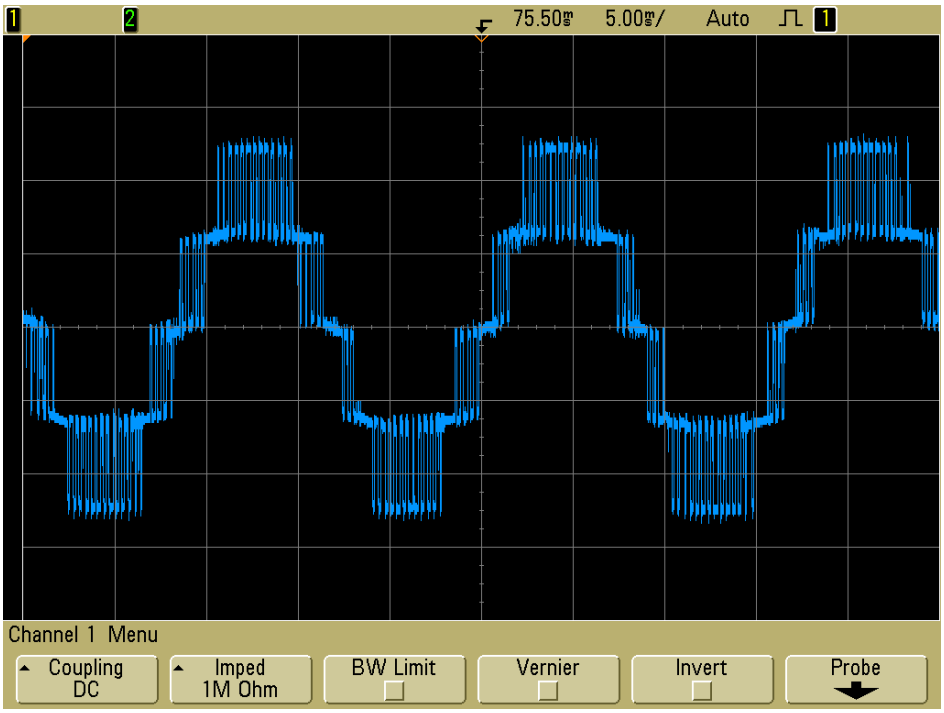


Figure 7.4 Unfiltered output voltage of the 5-level inverter

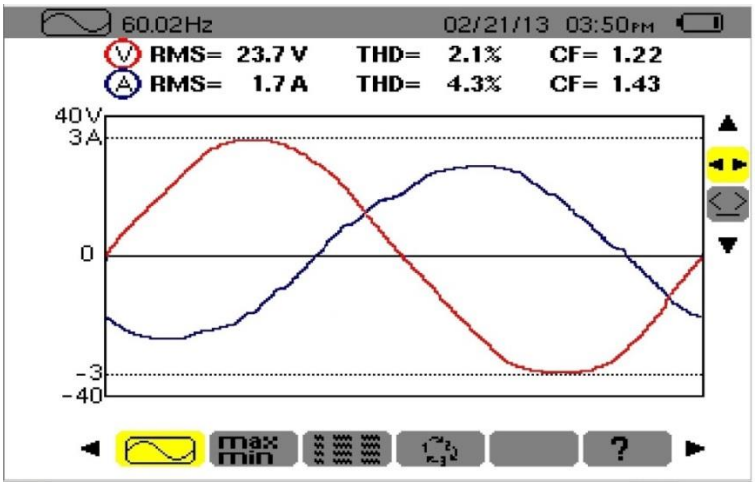


Figure 7.5 Filtered output voltage and current of the 5-level inverter

The output voltage and current THD of the inverter are 2.1% and 4.3%, respectively. Unlike simulation results of Section 5.2.1, the output current THD is compatible with IEEE standards. Although filter values are not the same as the simulations, the 5-level experimental results are

better than the simulation results. Figure 7.6 shows the filtered output voltage and current THD of the inverter. The use of a larger filter improves the THDs while increasing the cost of the system.

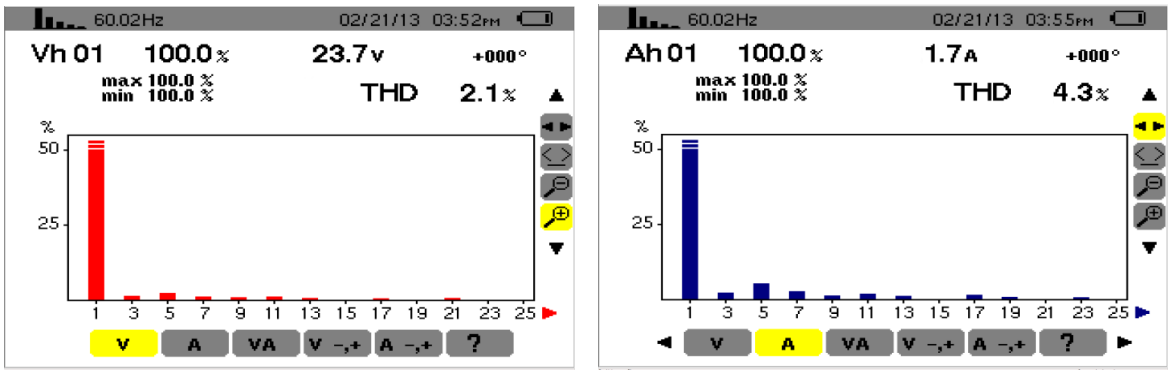


Figure 7.6 Filtered output voltage and current THD of the 5-level inverter

Figure 7.7 provides a complete overview of active powers, reactive powers, PF of the grid, modulation index, and power angle of the inverter after compensation conditions (Target PF=0.80). In this situation, the wind speed is zero and, therefore, no input active power is present from the wind turbine emulator.

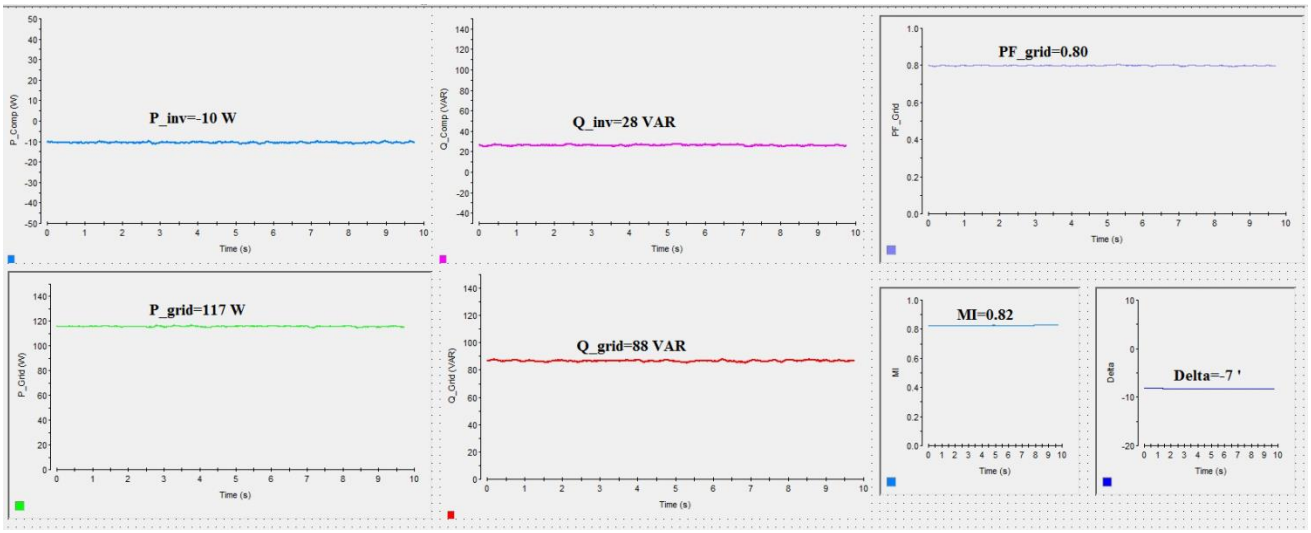


Figure 7.7 System parameters after compensation when wind speed is zero (Target PF=0.80)

In the above condition, the wind speed is zero; therefore no active power transfer is expected between the inverter and the grid. As shown Figure 7.7, the active power transferred between the inverter and the grid is -10 W. Ideally, no active power transfer should occur between the two sources, however due to the fact that the components are non-ideal, 10 W was drawn from the

grid. As shown, the compensated PF of the local grid is constant at 0.80; the inverter acts the same as a D-STATCOM to improve the PF. In other words, the compensator increases the PF of the grid (defined by the load) from 0.65 to 0.80 (target PF set by user) by injecting 28 VARs to the grid. The modulation index and power angle of the inverter are 0.82 and -7 degrees, respectively, demonstrating that the 5-level inverter compensates the PF of the grid. In this case, the inverter is connected to the grid through a transformer with the ratio of 120:24, and the switching frequency of the inverter is 3 kHz. Efficiency of the inverter (without the filter) is approximately 94% in the mentioned conditions. Figure 7.8 shows the active power, reactive power, and PF of the grid after compensation captured by the power analyzer. Results are similar to those captured by the ControlDesk (Figure 7.7), with minor variations. The error between these two measurements is approximately 2%. Also, the PF of the grid is 0.80, which is identical to the PF shown in Figure 6.7.

Figure 7.9 shows system parameters after compensation when active power is present from the wind emulator. In this case, the inverter is serving as an inverter with PF correction capability. The PF of the local grid is fixed at 0.80 with minimal oscillations. In this figure, the graphs were generated by changing the DC motor input to the synchronous generator in random steps. In other words, no particular pattern was used and the changes were made only to demonstrate the capability of the inverter.

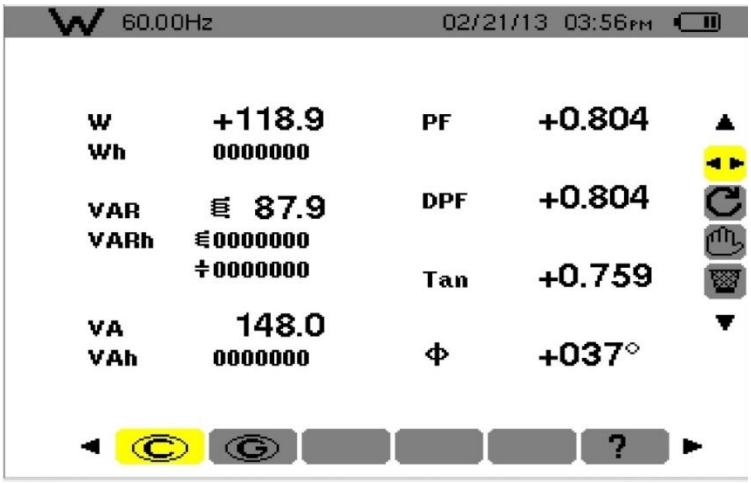


Figure 7.8 P, Q, and PF of the grid after compensation (Target PF=0.80)

Figures 7.7 and 7.9 illustrate that, before compensation, the grid PF is 0.65 and after compensation is constant at the target PF of 0.80 regardless of input active power from the wind emulator. The amount of active power drawn from the grid varies based on the amount of input

active power from the wind emulator. In fact, when output power of the wind turbine increases, the level of active power provided by the feeder line decreases by the same amount.

The inverter transfers the entire active power of the wind, excluding losses, to the grid. The amount of reactive power is dictated by the target PF. When the active power from the wind turbine increases, the controller increases the power angle δ in order to output more active power to the grid in order to decrease the DC link voltage.

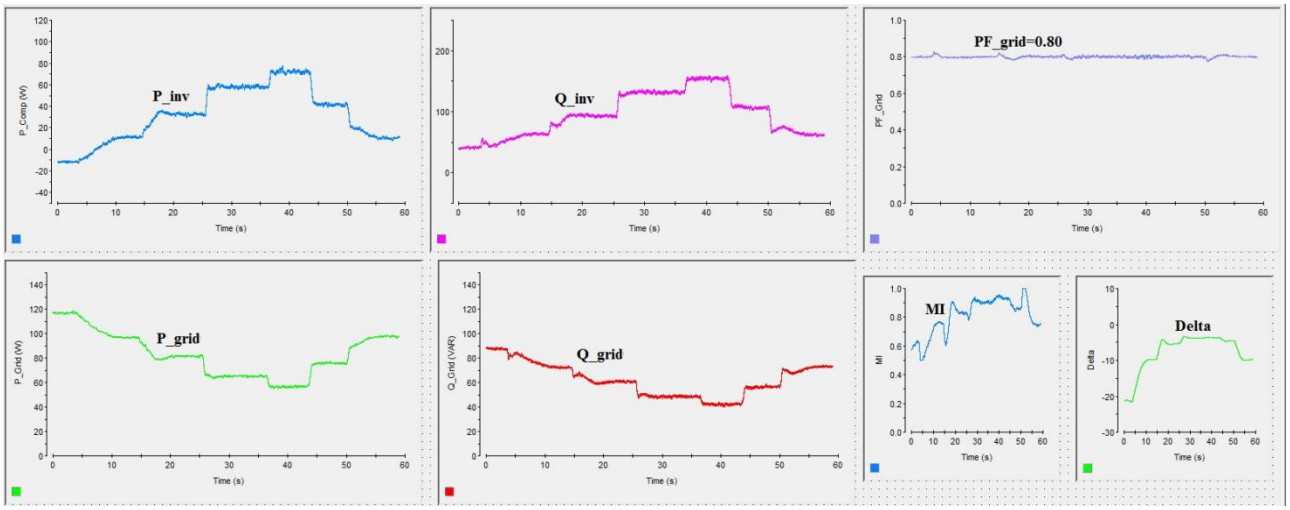


Figure 7.9 System parameters after compensation when wind is blowing (Target PF=0.80)

The modulation index (m) also increases when the inverter is supposed to inject more reactive power to the grid. The transient response of the PI controllers used to control the modulation index and delta can be adjusted by changing the proportional and integral coefficients of the controllers. Experimental results show that the performance of the proposed controller strategy is sufficiently close to the simulation results. The PI controllers show proper performance during severe changes in emulated wind speed.

7.2.2 After compensation: Target PF=0.90

In this case, experiment conditions are identical to those in Section 7.2.1, except the target PF is set to 0.90 instead of 0.80. Hence, the function of the inverter is to maintain the PF of the grid at 0.90, regardless of wind speed (input active power from the wind turbine emulator). Figure 7.10 provides system parameters after compensation while wind speed varies severely.

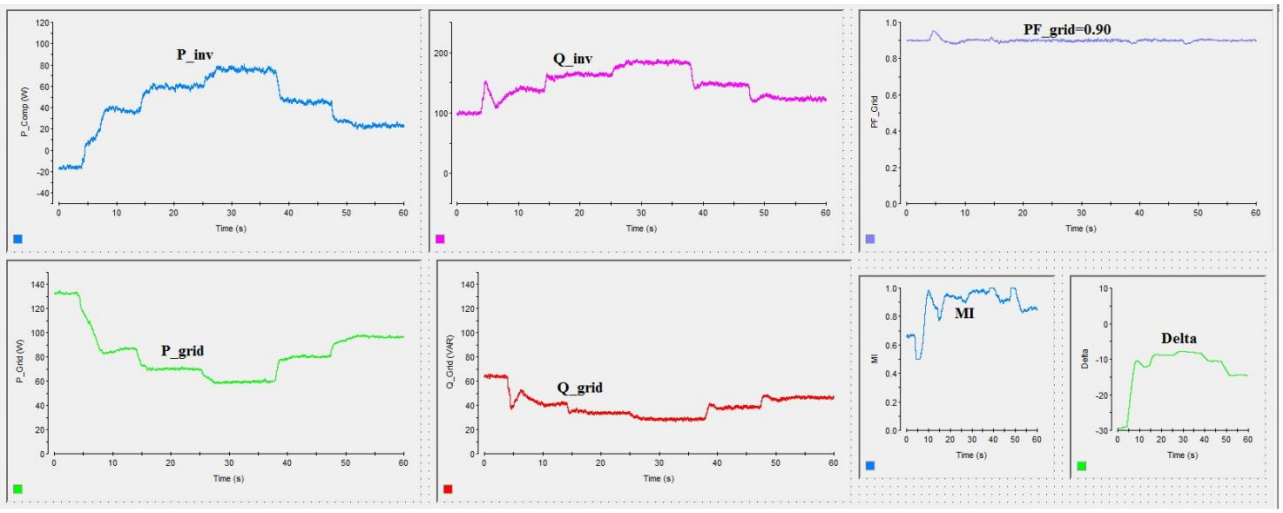


Figure 7.10 System parameters after compensation when wind is blowing (Target PF=0.90)

Figure 7.10 shows that the compensator kept the PF constant at 0.90 regardless of wind speed variation. As mentioned, the amount of active power transferred between the inverter and the grid changes with the same amount of input active power to the inverter. The amount of reactive power compensation is calculated based on the target PF and the amount of input active power. When input active power to the inverter increases, the controller system increases the power angle (delta) in order to reduce the DC link voltage. Therefore, more active power is transferred to the grid. When active power from the wind turbine is reduced, the controller decreases the power angle in order to reduce DC link voltage to maintain constancy at its reference value. Moreover, the controller system determines the value of modulation index based on the amount of input active power to the inverter and the target PF. Hence, the modulation index increased when more reactive power is needed to compensate the PF of the grid. When less reactive power is needed, the controller decreases the modulation index in order to inject less amount of reactive power to the grid. In this way, the PF of the grid remains constant at its target value over the entire time regardless of wind speed changes. Several oscillations on the target PF occur during rapid changes in input active power. The PI coefficients can be tuned in order to reach the desired response time as well as provide stability.

7.2.3 After compensation: Target PF=0.95

In this case, the target PF is 0.95 and other system parameters are kept constant. Figure 7.11 shows the system parameters for after compensation with target PF equal to 0.95.

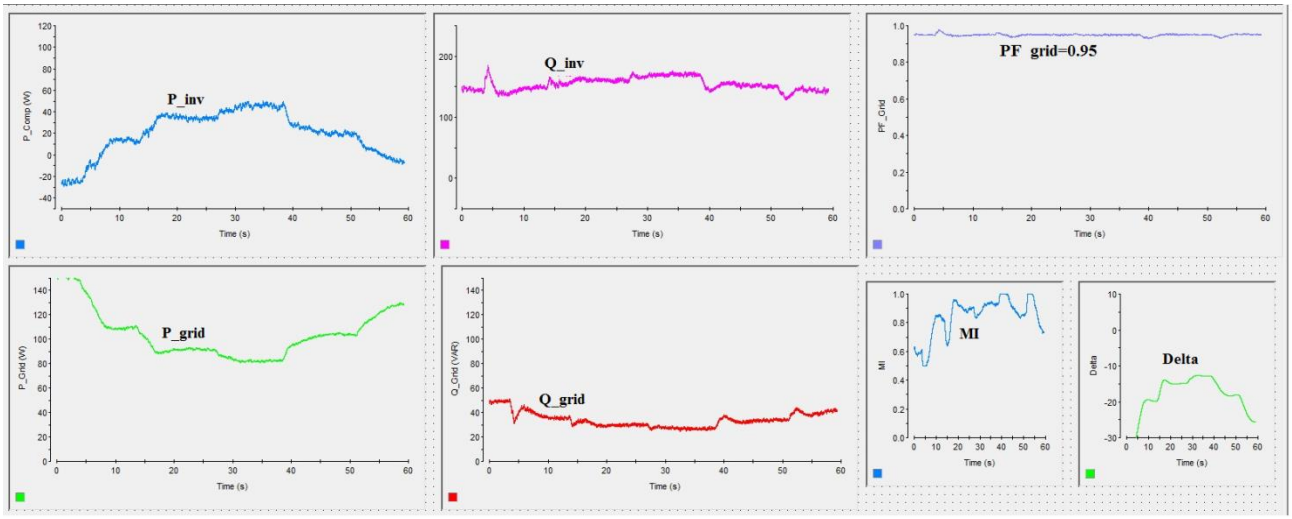


Figure 7.11 System parameters after compensation when wind is blowing (Target PF=0.95)

Figures 7.9-7.11 show that as the target PF of the grid increases, the amount of compensation for the same wind speed (input active power) also increases. The additional reactive power has to be injected by the inverter to the grid to increase the PF of the grid. In other words, higher grid PF means providing less reactive power by the grid. Therefore, more reactive power should be injected by the inverter in order to meet the required reactive power of the load. For the same amount of active power from the wind emulator, the value of modulation index also increased.

In general, the load draws less active power from the grid when more active power comes from the wind turbine. Therefore, active power from the grid to the load decreases. In order to maintain the grid PF, reactive power from the grid should also be reduced, thus increasing the amount of reactive power compensation from the inverter and increasing the modulation index. When the input active power to the inverter is reduced, more active power from the grid is pulled by the load. Therefore, to keep the grid PF constant at its target value, more reactive power is drawn from the grid, thus reducing the reactive power compensation since the load requires certain amounts of active and reactive power. Hence, the modulation index decreases. When target PF becomes higher (such as 0.95), the modulation index becomes closer to its maximum limit (which is unity). Hence, the device capability to compensate reactive power compensation is decreased. This can be solved by utilizing multiple inverters in order to reduce the individual reactive power compensation of each device.

7.3 11-Level inverter

7.3.1 After compensation: Target PF=0.80

In the 11-level experiments, effort was made to make the conditions similar to the 5-level experiments. In this case, the inverter is connected to the grid using a second-order LC filter with values 2.5 uH and 12 uF. First, the target PF is set to 0.80. In this situation, the inverter must compensate the PF of the local grid from 0.65 to 0.80 by injecting enough reactive power to the grid regardless of wind speed variation. Figure 7.12 demonstrates unfiltered output voltage of the 11-level inverter. Figure 7.13 shows the filtered output voltage and current of the inverter.

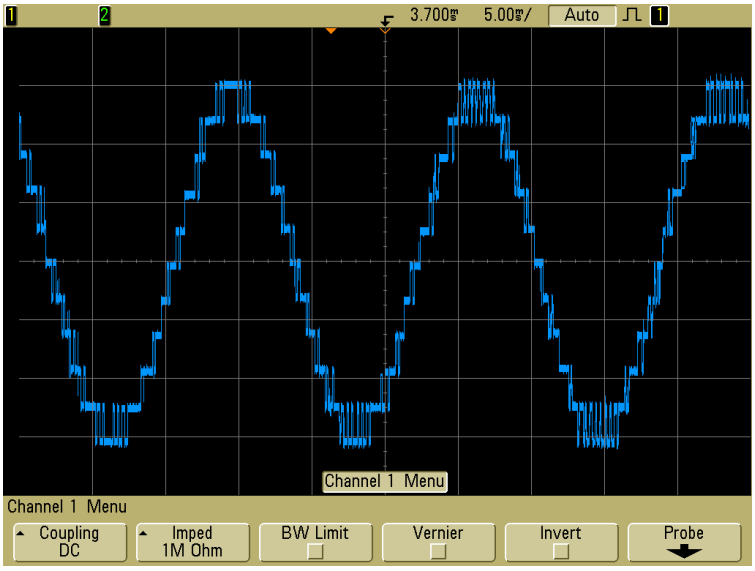


Figure 7.12 Unfiltered output voltage of the 11-level inverter

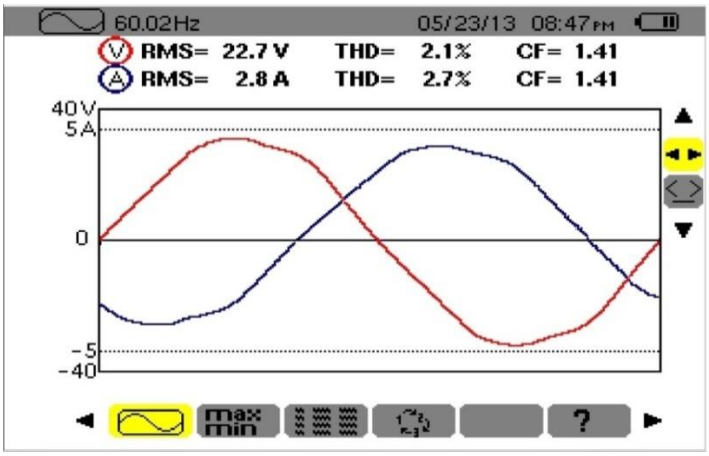


Figure 7.13 Filtered output voltage and current of the 11-level inverter

The output voltage and current THD of the 11-level inverter are 2.1% and 2.7%, respectively, demonstrating the THD improvement between the 5-level and 11-level experiments, since the experimental THD of the 5-level was 4.3% with a larger output filter. This shows that the outputs of the 11-level inverter are completely compatible with IEEE 519 standard. Figure 7.14 illustrates the filtered output voltage and current THD of the 11-level experimental model.

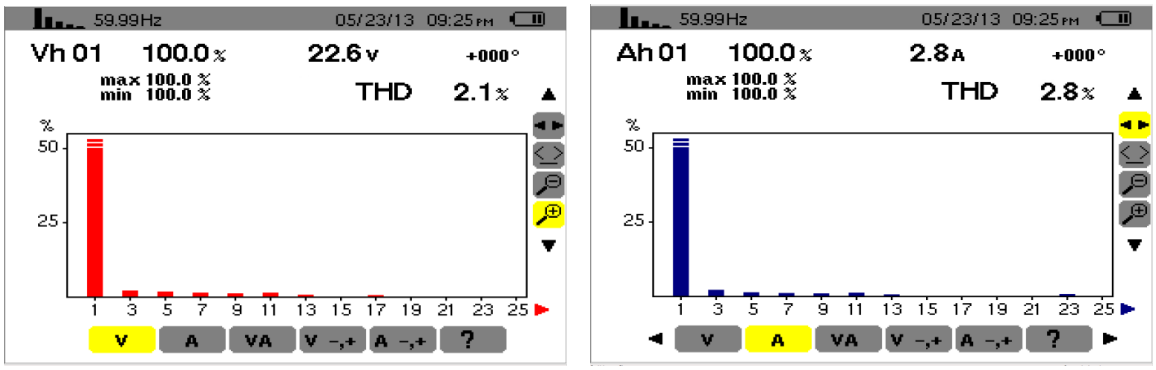


Figure 7.14 Filtered output voltage and current THD of the 11-level inverter

In this case, the inverter is connected to the grid through a transformer with the ratio of 120:24, and the switching frequency of the inverter is 2 kHz. Efficiency of the inverter is approximately 93% in the mentioned conditions

Figure 7.15 shows a complete overview of system parameters for after compensation conditions in which the target PF is equal to 0.80. In this case, no input active power is present from the wind turbine emulator to the inverter.

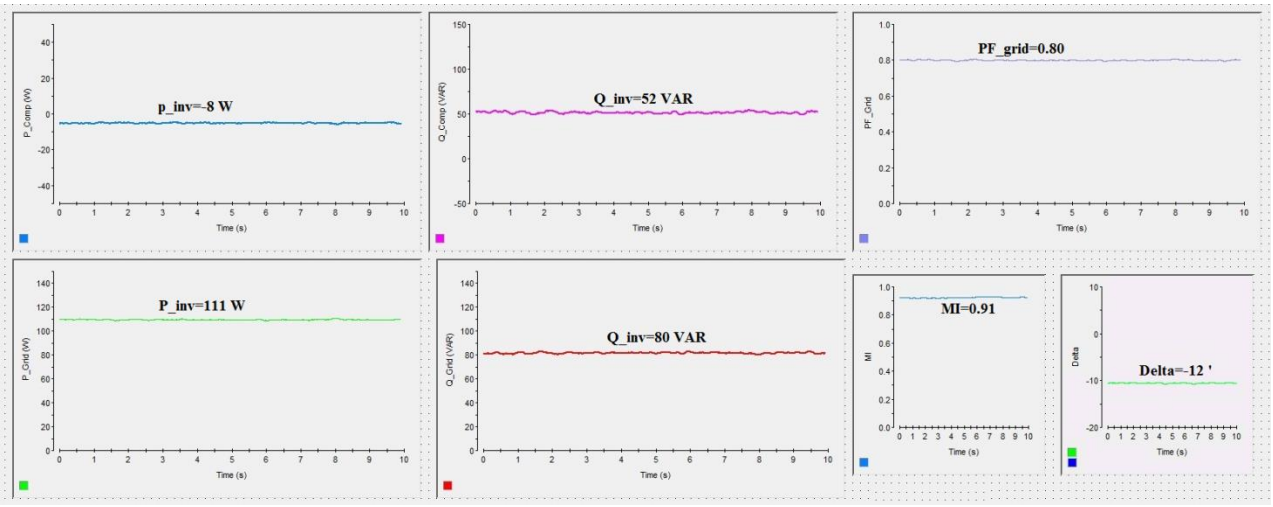


Figure 7.15 System parameters after compensation when wind speed is zero (Target PF=0.80)

As with the 5-level model, no active power is expected to transfer between the inverter and the grid; however, 8 W are drawn from the grid by the inverter to compensate internal power losses of the inverter. As shown, the compensated PF of the local grid is constant at 0.80, so the inverter is acting as a D-STATCOM to improve the PF, proving that the 11-level inverter is capable of compensating the PF of the grid from 0.65 to 0.80 when no active power occurs from the wind turbine emulator. Figure 7.16, captured by the power analyzer, validates results shown in Figure 7.15. As with the 5-level measurements, an error of approximately 2% exists between measurements of the ControlDesk program and the power analyzer.

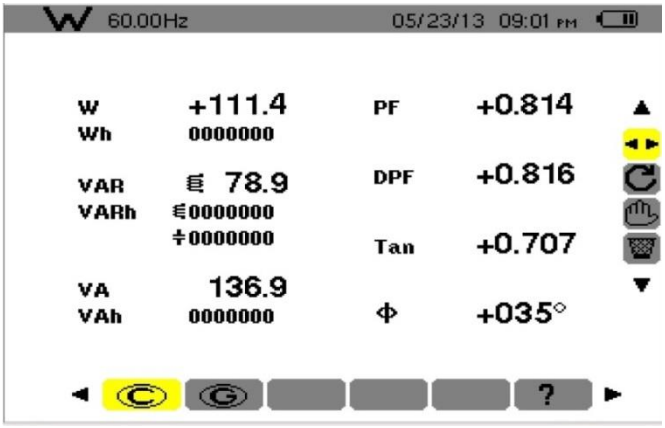


Figure 7.16 P, Q, and PF of the grid after compensation (Target PF=0.80)

Figure 7.17 shows system parameters after compensation when there is active power from the wind emulator. In this case, the inverter acts as an inverter with PF correction capability. The PF of the local grid is fixed at 0.80 with small oscillations. Figures 7.15 and 7.17 show the proper performance of the inverter in grid-connected mode operation in which the PF of the grid remains constant at its target value of 0.80. Principles of the operation of the 5- and 11-level models are identical. Differences are present between the output voltage and current of the inverter for different conditions. As demonstrated, the 11-level model has better output waveforms compatible with IEEE standards. The reactive power injected by the inverter is calculated based on the target PF and the wind speed. In addition, the inverter transfers the entire amount of active power gained from the wind emulator, excluding power losses. Figure 7.17 demonstrates that the modulation index (m) increases when the inverter is supposed to inject more reactive power to the grid, while the absolute value of delta increases when the input active power of the inverter increases (meaning that wind blows faster). As expected, the performance of the experimental 11-level model is similar to the simulations.

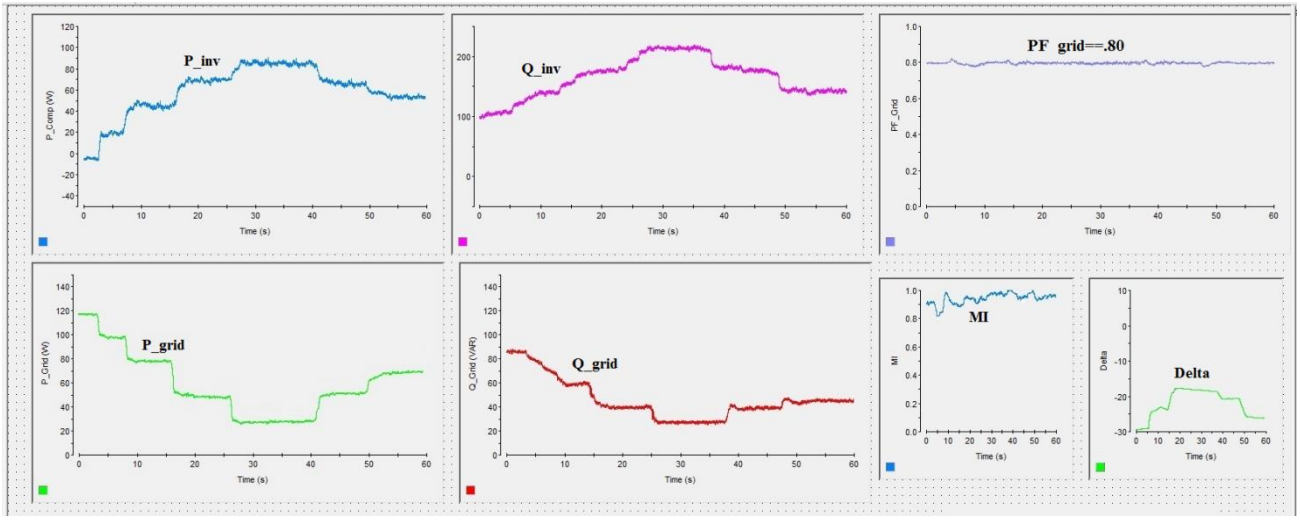


Figure 7.17 System parameters after compensation when wind is blowing (Target PF=0.80)

7.3.2 After compensation: Target PF=0.90

In this case, the target PF is set to 0.90. Hence, the inverter has to inject more reactive power to the grid than for the previous condition (target PF=0.80) in order to fix the PF. Figure 7.18 demonstrates system parameters after compensation with changing wind speeds.

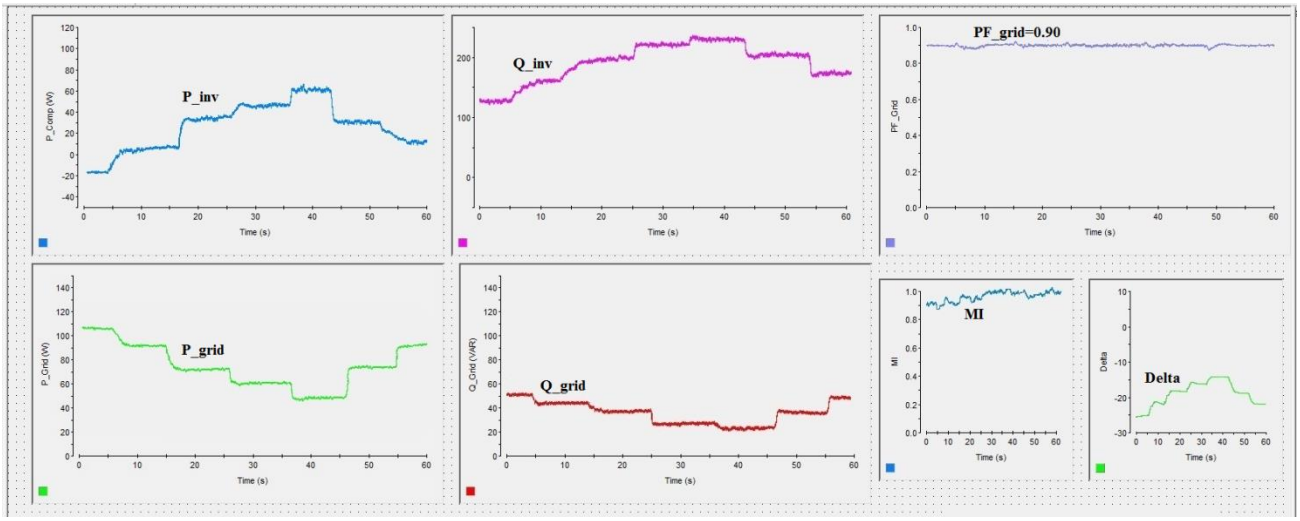


Figure 7.18 System parameters after compensation when wind is blowing (Target PF=0.90)

As shown, the compensator keeps the PF constant at 0.90, regardless of wind speed variation. The operation of the PI controllers of the controller system is identical to the 5-level model. When input active power increases, the controller system increases the power angle (delta).

When the input active power is reduced, the controller decreases the power angle. In addition, when more reactive power is needed, the controller increases the modulation index, and when less reactive power is needed, the modulation index is reduced. In this way, the PF of the grid remains constant at its target value regardless of wind speed changes. Oscillations of the target PF occur during rapid changes in input active power.

7.3.3 After compensation: Target PF=0.95

Figure 7.19 shows system parameters when the target PF is 0.95. As with the 5-level model, Figures 7.17-7.19 show that when the target PF becomes higher, the modulation index becomes closer to its maximum limit. Hence, the operational capability of the compensator is reduced. Consequently, multiples of these inverters should be used to reach the desired reactive power compensation for the entire system.

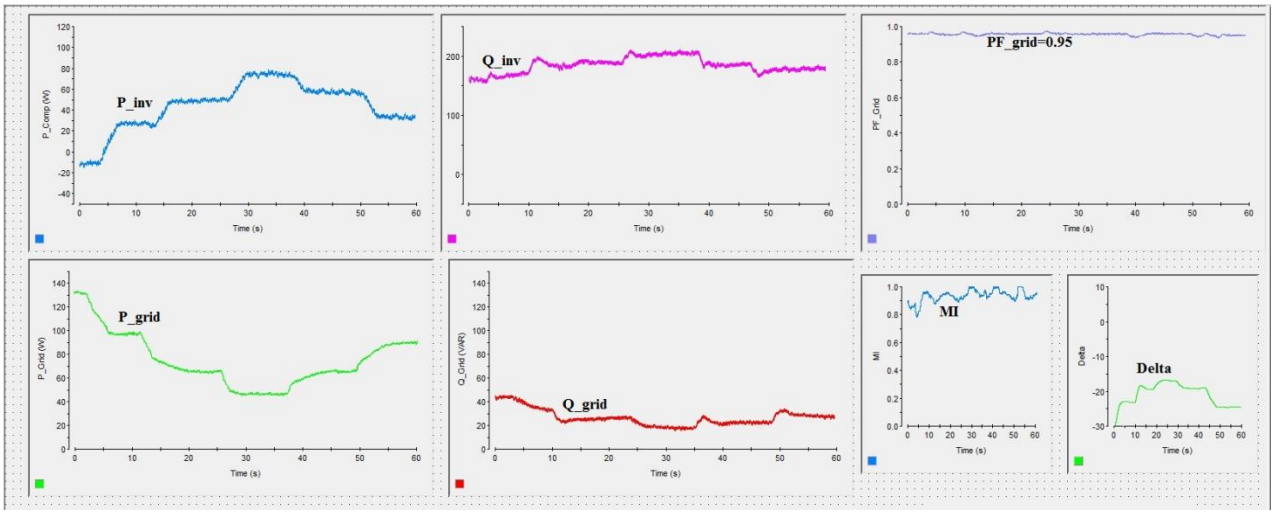


Figure 7.19 System parameters after compensation when wind is blowing (Target PF=0.95)

The PQ diagrams of the 11-level model are similar to the 5-level model because the operating principles are the same. The only difference is that active and reactive power amounts may differ in some cases due to different system parameters such as the filter.

7.4 Summary

As previously mentioned, identical experiments were done on 5- and 11-level scaled models. Experimental results on the 5-level model before compensation show that grid PF and voltage and current THDs are 0.65, 1.5% and 1.8%, respectively.

After compensation, when target PF is equal to 0.80, output voltage and current THDs become 2.1% and 4.3%. In this case, the output filter is composed of a 10 mH inductor and 25 uF capacitor. As described, the 5-level inverter is connected to the grid through a distribution transformer with turns-ratio 120:24. The efficiency of 5-level inverter is approximately 93% and it is operating at switching frequency 3 kHz. When no active power comes from wind emulator, the power loss of the inverter is 10 W, and modulation index and delta are 0.82 and 7 degrees, respectively.

11-level experimental results, in the same situations, show that the output voltage and current THDs are 2.1% and 2.8%, respectively. This shows a 1.5% improvement in current THD while utilizing a smaller output filter with values 2.5 mH and 12 uF. The 11-level experiment uses the identical transformer as the 5-level model. In this case, the switching frequency and efficiency of the inverter are 2 kHz and 94%, respectively. Moreover, when no active power comes from the wind emulator, the power loss of the inverter is 8 W, and modulation index and delta are 0.91 and 12 degrees, respectively. Table 7.1 presents a comparison between 5- and 11-level prototype models.

Table 7.1 Comparison between 5- and 11-level experimental results

Parameter	5-level Model	11-level Model
Output Filter	**10 mH, 25 uF**	**2.5 mH, 12 mF**
Switching Frequency	**3 kHz**	**2 kHz**
Efficiency	**93%**	**94%**
Distribution Transformer	**120:24**	**120:24**
Current THD	**4.3%**	**2.8%**
Voltage THD	**2.1%**	**2.1%**
Modulation Index (for identical situations)	**0.82**	**0.91**
Delta (degree) (for identical situations)	**7**	**12**
Compatibility with IEEE 519 Standard	**Yes**	**Yes**

Table 7.1 summarizes the results for 5- and 11-level scaled models in identical situations. As shown, both models are compatible with IEEE 519 standard. However, the 11-level model has better performance than the 5-level model. The 11-level model requires greater number of components, but using a smaller output filter decreases the total cost of the 11-level system. Although the 11-level model utilizes more components (Table 5.7), utilizing a smaller switching frequency results in approximately identical efficiency.

Simulation results were presented in Chapter 6; Table 7.2 compares output filter values and resulting THDs between 5- and 11-level simulations and experiments. This table indicates that the experimental results match the simulation results with an error of 5%.

Table 7.2 Comparison between simulation and experimental filter values and resulting THDs

Parameter	5-level simulation (250 W/VAR)	5-level experiment	11-level simulation (250 W/VAR)	11-level experiment
L_{filter}	10 mH	10 mH	2.5 mH	2.5 mH
C_{filter}	25 uF	25 uF	12 uF	12 uF
THD of filtered voltage	2.02%	2.1%	2.05%	2.1%
THD of current	4.19%	4.3%	2.63%	2.8%

As mentioned, the difference between experimental results and simulation results is approximately 5%. Although efforts were made to make simulations (250W/VAR model) similar to the experiments, parameters may exist that have not been considered in simulations. The difference between simulation and experimental results may be a result of parasitic parameters (parasitic resistance, capacitance, inductance) of the distribution transformer, output inductor and capacitor, or power lines. In addition, the time delay associated with the dSPACE to generate switching signals may be another reason for the difference between the simulation and experimental results. Moreover, error in measurements is another possible reason for this difference. The agreement here demonstrates the feasibility of using a full-size D-STATCOM inverter that meets IEEE standards. A detailed cost comparison between 5- and 11-level models will be presented in Chapter 8.

Chapter 8 - Conclusion and Future Work

8.1 Conclusion

The concept of a new multi-level inverter with FACTS capability was presented in this dissertation. The proposed inverter represents a new way in which small renewable sources can provide control and support in distribution systems. The MMC inverter with D-STATCOM capability supplies utilities with capacitive VAR compensation. The unique contribution of this research is to combine the two concepts of D-STATCOM and inverter using the most advanced multi-level topology to create a single-phase wind inverter with FACTS capability. The proposed power electronics device acts as a renewable energy inverter with D-STATCOM option with a hopefully lower total cost.

The primary focus of this research was to demonstrate the application of custom power electronics in renewable energy systems. Increasing the number of small to medium wind turbines can lead to several issues for local utilities, including harmonics or power factor (PF) complications. Currently, the PF of distribution power lines is controlled by utilizing small distribution static synchronous compensators (D-STATCOMs) or capacitor banks. Using traditional STATCOMs for small- or medium-sized single-phase wind applications is not economical, because the system cost increases significantly, thus creating opportunity to use smarter wind energy inverters (WEIs) with FACTS capabilities for cost-effectiveness and compatibility with IEEE standards.

The proposed inverter in this dissertation is equipped with a D-STATCOM option to regulate reactive power of local distribution lines. Functions of the proposed inverter include converting incoming power from the DC link to a suitable AC power for the main grid and fixing the local grid PF at a target PF by injecting reactive power. In the proposed control strategy, concepts of wind energy inverter (WEI) and D-STATCOM are combined to create a new inverter which possesses D-STATCOM capability at no additional cost. The control strategy also allows the inverter to act as an "inverter with D-STATCOM option" when sufficient wind is present to produce active power and to act as a "D-STATCOM" when no wind is present. The active power is controlled by adjusting the power angle (δ), or the angle between inverter and grid voltages. Reactive power is also regulated by the modulation index (m).

In the design of the proposed inverter with D-STATCOM capability, several issues were considered: 1) operating with minimum switching frequency, 2) minimizing total power losses, 3) increasing efficiency, 3) maintaining compatibility with IEEE standards, 4) cost-effectiveness of utilization for small applications.

The primary objective of the proposed inverter is to replace the regular wind application inverter with an inverter that possesses the D-STATCOM option to provide utilities additional power factor control. The proposed inverter basic design criteria includes: 1) connecting wind turbine to a single-phase feeder line, 2) ability to support turbines rated from 10–20 kW, 3) ability to compensate up to 20 kVARs of capacitive compensation regardless of wind speed and active power conversion, 4) ability to fix the PF of the feeder line at a target value set by the user (utility) if the required compensation is within the range of inverter ratings. These design criteria were considered for inverter utilization for small businesses and farms. These customers typically use up to 20 kW wind turbines because this is a proper level of generation and is financially feasible. The amount of reactive power compensation (20 kVARS) was also selected based on the corresponding wind turbine rating since it represents realistic reactive power compensation for a small- to mid-size wind turbine.

In this dissertation, 5-level and 11-level inverters were designed. Simulations for 5- and 11-level models were performed in MATLAB/Simulink environment for two systems, including 20 kW/kVAR and 250 W/VAR. A scaled version (250 W/VAR) of the inverters was built and tested in the laboratory to validate simulation results. The proposed inverter power rating is described in “W/VAR” because it is a combination of STATCOM and inverter in a single unit.

In simulations, modulation techniques were identical (PDPWM) for both models. The number of components used for an 11-level single-phase inverter is more than twice that of a 5-level inverter. However, component voltage and current ratings used for the 11-level model are smaller, thus significantly reducing the total cost of the system. This causes the 5-level inverter to be more reliable than the 11-level inverter (it has fewer parts to fail). On the other hand, the modular structure of MMC topology enables the use of several spare SMs so that the controller system might temporarily replace the impaired SM. Simulation results show that the unfiltered output voltage and the output current of the 11-level inverter contain fewer harmonics than the 5-level inverter. The simulated output current of the 5-level model (20 kW/kVAR) is not completely compatible with IEEE Standard 519 requirements because all individual harmonics

are not less than 3% of the fundamental component and the THD is not less than 5%; however, the smaller system (250 W/VAR) is compatible with IEEE standards. In the 11-level simulation, the output voltage and current (for both systems) are compatible with standards because each harmonic is less than 3% of the fundamental and the current THD is lower than 5%. This result has been achieved using a filter smaller than the 5-level model filter. Use of a smaller output filter for the 11-level model reduces the total cost of the system.

In simulations, the 5-level and 11-level systems showed similar performance in terms of controlling the PF of the grid. Active and reactive power transfer between the compensator and the grid are similar in both simulations. The 11-level model is more stable under rapid changes, such as load variations or wind speed changes, but the DC link voltage in the 11-level model experiences more oscillation than the 5-level model. A primary design objective of this inverter is minimal total cost since the inverter is intended to be used for small farms or businesses. Total cost of the 11-level system is greater than the 5-level model because the number of components increases for higher voltage levels. However, the 5-level model is unable to satisfy all IEEE standard requirements, unless it uses larger filters. Thus, a compromise exists between output quality and total system cost. Because the proposed inverter is a combination of two separate power electronic devices: an inverter and a D-STATCOM, some additional cost over current retail is acceptable.

As mentioned in Chapter 7, the comparison between simulation and experimental results shows that the experiments confirm the simulations (see Table 7.2). Outputs of 5- and 11-level experimental models are compatible with IEEE Standard 519. However, the 11-level model has better performance than the 5-level. Efficiency of the 11-level inverter with a larger number of components is approximately identical to the 5-level, which is a result of lower switching frequency. In general, performance of the 11-level inverter is better than the 5-level model; however, total cost of the 11-level inverter may be greater than the similar-rated 5-level model. Therefore, in a real system, a compromise should be made between the use of a 5-level inverter and the use of an 11-level inverter with higher performance and higher cost.

Table 8.1 details cost comparison between 5- and 11-level prototype models. Component prices are based on Digi-Key Corporation, a primary supplier and distributer of electronic components in the United States.

Table 8.1 Cost comparison between 5- and 11-level prototype models

Component	5-level model	11-level model	Cost for 5-level	Cost for 11-level
SMs capacitor	8 (50 V, 1000 uF) Each: $ 0.94	20 (25 V, 1000 uF) Each: $ 0.23	~ $ 8	~ $ 5
DC link capacitor	2 (50 V, 1000 uF) Each: $ 0.94	2 (50 V, 1000 uF) Each: $ 0.94	~ $ 2	~ $ 2
Arm inductance	2 (5 mH, 1 A) Each: $ 30	2 (5 mH, 1 A) Each: $ 30	~ $ 60	~ $ 60
Output filter	LC filter (10 mH, 25 uF) ~$35	LC filter (2.5 mH, 12 uF) ~$15	~$35	~$15
Power Switch	16 (IRF 510) Each: $ 0.91	40 (IRF 510) Each: $ 0.91	~ $ 16	~ 40
Gate drive Module	16 including: HCPL 3120, resistors, Schottkey diodes, Zener diodes Each: ~ $ 5	40 including: HCPL 3120, resistors, Schottkey diodes, Zener diodes Each: ~ $ 5	~ $ 80	~ $ 200
PC Board	$ 66 (2 Boards)	$ 99 (3 Boards)	~ $ 66	~ $ 99
Microcontroller (DSP)	TMS320F28XX ~$25	TMS320F28XX ~$25	~$25	~$25
Isolation Module	8 including opto-coupler, resistors, diodes, capacitors Each: $ 3	20 including opto-coupler, resistors, diodes, capacitors Each: $ 3	~ $ 24	~ $ 60
Labor cost (Professional electronic assembler)	3 hours Average: $15/hour	7 hours Average: $15/hour	~$45	~$95
Miscellaneous including connectors, sensors	including 14A-2.5R12, 13/10TALEMA, and connectors Each: $ 20	including 14A-2.5R12, 13/10TALEMA, and connectors Each: $ 50	~ $ 20	~ $ 50
Total			~ $ 380	~ $ 650

Table 8.1 details approximate cost for each prototype inverter. The calculated costs are for a 250W/VAR sample inverter. In order to expand the scaled inverters to higher-rated models, higher-rated components should be used. As shown, cost of the 11-level inverter is approximately twice that of the 5-level prototype model; however, its output has better quality. Therefore, depending on the application, the proper inverter must be selected.

Currently, inverters ranging from 200W to 300W cost approximately $200 to $400, depending on specifications and various manufacturers. Hence, the total cost of the proposed inverter, specifically a 5-level model, is in the market price range, considering that the proposed

inverter has more functionality than regular inverters (FACTS capability). This shows that the proposed inverter has the capability of being commercialized.

Although calculation of the total cost of higher-rated models of the proposed inverter is not straightforward, several higher-rated models of the proposed inverter are compared with current market prices in Table 8.2.

Table 8.2 Cost comparison between proposed inverter and regular inverters found in market

Power Rating	5-level model	11-level model	Market Price
250 W	~ $ 380	~ $ 650	$ 200-400
1 kW	~ $875	~ $ 1490	$ 600- $ 800
3 kW	~ $1750	~ $ 2980	$ 1400- $ 1600
10 kW	~ $ 2850	~ $ 4850	$ 3750- $ 4500
20 kW	~ $ 3850	~ $ 6550	> $ 5200

Table 8.2 shows that the cost of the proposed 5-level inverter is within or lower than the market range; however, the 11-level model is typically more expensive than regular inverters. Cost of the 11-level is more than market price, but it has more options than regular wind inverters because it is a combination of inverter and D-STATCOM and can improve the grid PF. Furthermore, Table 8.1 shows retail prices of the prototype model. Expenses of commercialized models would be much lower than retail prices (approximately 20% of retail prices). Therefore, the remaining part of the inverter price could be assumed as profit for the manufacturer.

Two important factors impact output quality of the inverter: output filter and switching frequency. Inverter output signals can be improved by using higher filter values. However, this increases total system cost which does not correlate with the cost-effectiveness objective of this research. Figure 8.1 compares output filter values (only the inductor) versus the output THD for the 5- and 11-level models (250 W/VAR). In this case, only output inductor changes and all other parameters are considered to be constant. Table 8.3 demonstrates the relationship between the output filter, output current THD, and system cost for the 5- and 11-level systems. The estimated costs are based on the 5- and 11-level retail prices shown in Table 8.1.

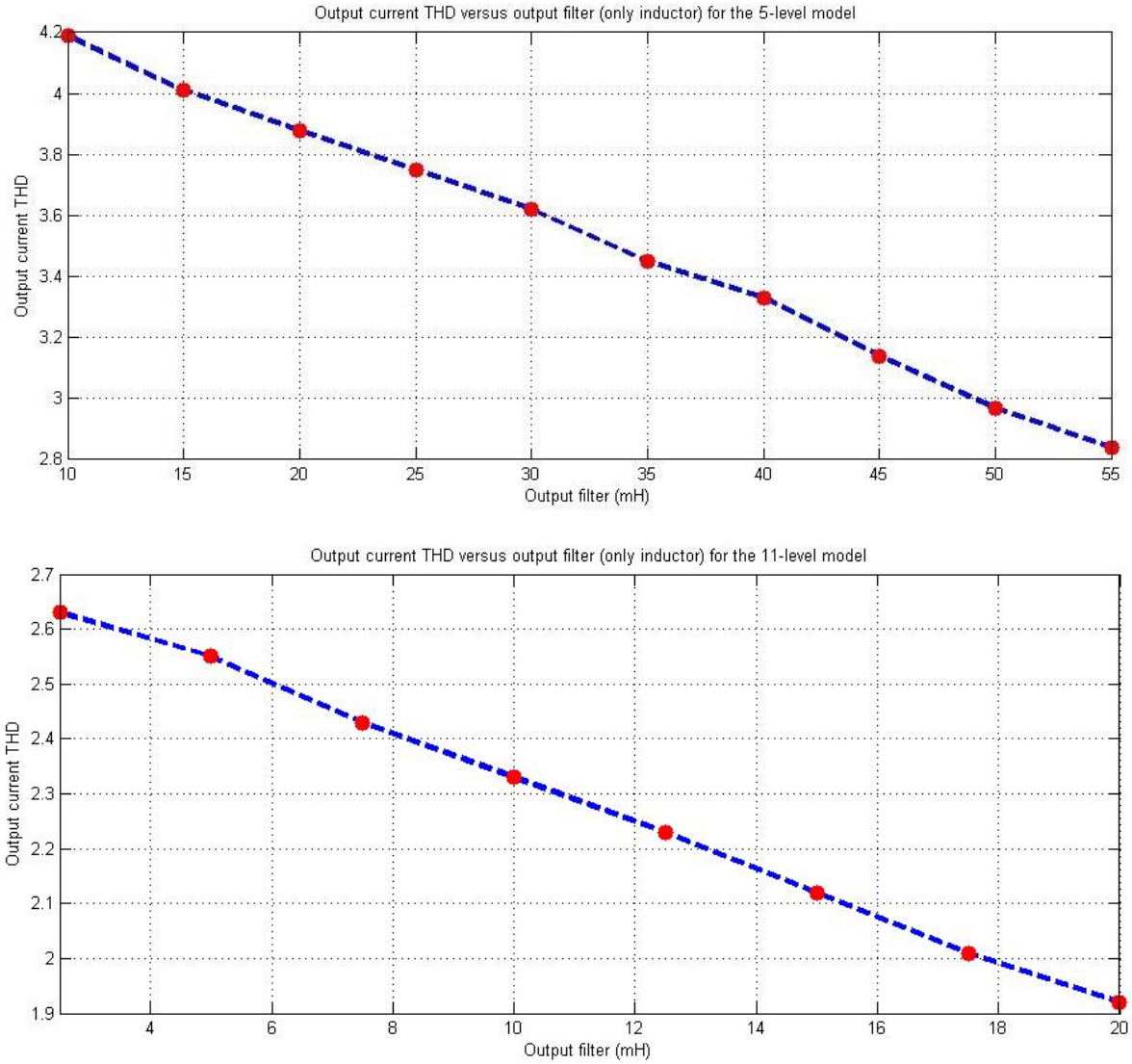


Figure 8.1 Relationship between filter (inductor) and output current THD for the 5- and 11-level inverters (250W/VAR)

Table 8.3 Relationship between filter (inductor), output current THD, and system cost for the 5- and 11-level inverters (250W/VAR)

5-Level Model			11-Level Model		
Output filter (only inductor)	Output current THD	System Cost	Output filter (only inductor)	Output current THD	System Cost
10 mH	4.19%	$ 380	2.5 mH	2.66%	$ 650
15 mH	4.01%	$ 400	5 mH	2.55%	$ 685
20 mH	3.88%	$ 425	7.5 mH	2.43%	$ 730
25 mH	3.79%	$ 455	10 mH	2.33%	$ 780
30 mH	3.62%	$ 490	12.5 mH	2.23%	$ 840
35 mH	3.45%	$ 540	15 mH	2.12%	$ 925
40 mH	3.33%	$ 585	17.5 mH	2.01%	$ 1000
45 mH	3.14%	$ 635	20 mH	1.92%	$ 1085
50 mH	2.97%	$ 690	22.5 mH	1.83%	$ 1180
55 mH	2.84%	$ 750	25 mH	1.75%	$ 1280

Although increasing the output filter improves output waveform quality, device marketability may be impacted because the retail price of the models (specifically 5-level) is on the margin compared with the market values. Therefore, with increased filter component values, the inverter may not be able to compete with other similar inverters on the market, so a compromise should be made between output filter values and system cost.

Output quality can also be improved with the use of higher switching frequencies. However, higher switching frequenciy results in efficiency reduction, which is out of the pre-defined objectives of this research. In other words, by increasing the switching frequency, output waveforms are improved, while inverter efficiency is reduced. The relationship between output current THD of the 5-level inverter (250 W/VAR) and switching frequency is shown in Figure 8.2. In this figure, all parameters are considered to be constant and only switching frequency changes.

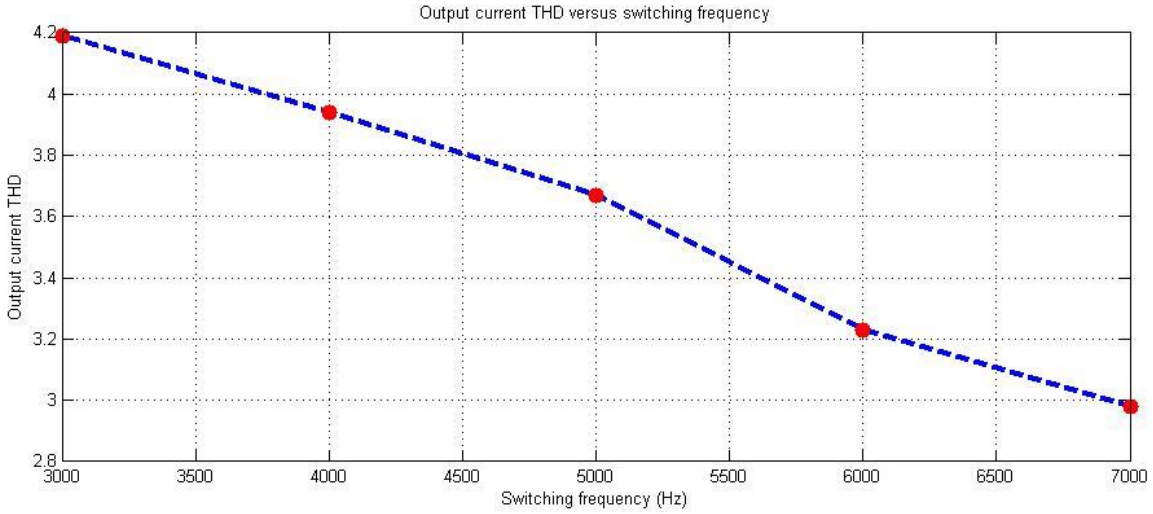


Figure 8.2 Relationship between output current THD and switching frequency for the 5-level inverter (250W/VAR)

8.2 Future Work

The goal of the prototype 5- and 11-level inverters presented in this dissertation was to show the proof of concept. However, one future project would be to implement higher-rated inverters by using higher-rated components. On the other hand, the focus of this research was to propose a new power inverter with additional functions. Therefore, the controller system was implemented by utilizing one or several dSPACEs. In real-world inverters, however, a microcontroller-based system is designed and programmed to measure and calculate feedback signals in order to generate the proper switching algorithm. Another future work of this research would be to implement the proposed inverter using a microcontroller such as digital signal processor (DSP). In addition, other multi-level topologies could be chosen to design the proposed inverter in order to reach better efficiencies and THDs, considering total cost of the system. Moreover, more advanced control strategies, such as simultaneously controlling active and reactive power with modulation index (m) and power angle (δ), could be considered in order to control the inverter power transfer.

Appendix A- MATLAB code for PWM controller block (1) for the 11-level inverter

```
function Region  = fcn(Sig1,Sig2,Sig3,Sig4,Sig5,Sig6,Sig7,Sig8,Sig9,Sig10)

Region=0;

if (Sig1==1 & Sig2==1 & Sig3==1 & Sig4==1 & Sig5==1 & Sig6==1 & Sig7==1 &
Sig8==1 & Sig9==1 & Sig10==1)
    Region=11;

elseif (Sig1==0 & Sig2==1 & Sig3==1 & Sig4==1 & Sig5==1 & Sig6==1 & Sig7==1 &
Sig8==1 & Sig9==1 & Sig10==1)
    Region=10;

elseif (Sig1==0 & Sig2==0 & Sig3==1 & Sig4==1 & Sig5==1 & Sig6==1 & Sig7==1 &
Sig8==1 & Sig9==1 & Sig10==1)
    Region=9;

elseif (Sig1==0 & Sig2==0 & Sig3==0 & Sig4==1 & Sig5==1 & Sig6==1 & Sig7==1 &
Sig8==1 & Sig9==1 & Sig10==1)
    Region=8;

elseif (Sig1==0 & Sig2==0 & Sig3==0 & Sig4==0 & Sig5==1 & Sig6==1 & Sig7==1 &
Sig8==1 & Sig9==1 & Sig10==1)
    Region=7;

elseif (Sig1==0 & Sig2==0 & Sig3==0 & Sig4==0 & Sig5==0 & Sig6==1 & Sig7==1 &
Sig8==1 & Sig9==1 & Sig10==1)
    Region=6;

elseif (Sig1==0 & Sig2==0 & Sig3==0 & Sig4==0 & Sig5==0 & Sig6==0 & Sig7==1 &
Sig8==1 & Sig9==1 & Sig10==1)
    Region=5;

elseif (Sig1==0 & Sig2==0 & Sig3==0 & Sig4==0 & Sig5==0 & Sig6==0 & Sig7==0 &
Sig8==1 & Sig9==1 & Sig10==1)
    Region=4;

elseif (Sig1==0 & Sig2==0 & Sig3==0 & Sig4==0 & Sig5==0 & Sig6==0 & Sig7==0 &
Sig8==0 & Sig9==1 & Sig10==1)
    Region=3;

elseif (Sig1==0 & Sig2==0 & Sig3==0 & Sig4==0 & Sig5==0 & Sig6==0 & Sig7==0 &
Sig8==0 & Sig9==0 & Sig10==1)
    Region=2;

elseif (Sig1==0 & Sig2==0 & Sig3==0 & Sig4==0 & Sig5==0 & Sig6==0 & Sig7==0 &
Sig8==0 & Sig9==0 & Sig10==0)
    Region=1;
end
```

Appendix B- MATLAB code for PWM controller block (2) for the 11-level inverter

```
function Switches  =
fcn(Region,I_DC_Pos,C1,C2,C3,C4,C5,C6,C7,C8,C9,C10,C11,C12,C13,C14,C15,C16,C1
7,C18,C19,C20)

Sa1=0;  Sa2=0;  Sa3=0;  Sa4=0;  Sa5=0;  Sa6=0;  Sa7=0;  Sa8=0;  Sa9=0;
Sa10=0;  Sa11=0;  Sa12=0;  Sa13=0;  Sa14=0;  Sa15=0;  Sa16=0;  Sa17=0;
Sa18=0;  Sa19=0;  Sa20=0;
Sa21=0; Sa22=0; Sa23=0; Sa24=0; Sa25=0; Sa26=0; Sa27=0; Sa28=0; Sa29=0;
Sa30=0;  Sa31=0;  Sa32=0;  Sa33=0;  Sa34=0;  Sa35=0;  Sa36=0;  Sa37=0;
Sa38=0;  Sa39=0;  Sa40=0;

UpperCaps=[1 C1; 2 C2; 3 C3; 4 C4; 5 C5; 6 C6; 7 C7; 8 C8; 9 C9; 10 C10];
LowerCaps=[11 C11; 12 C12; 13 C13; 14 C14; 15 C15; 16 C16; 17 C17; 18 C18; 19
C19; 20 C20];

UpperSort=sortrows(UpperCaps,2);
LowerSort=sortrows(LowerCaps,2);

UpperMin=UpperSort(1,1);
UpperMin2=UpperSort(2,1);
UpperMin3=UpperSort(3,1);
UpperMin4=UpperSort(4,1);
UpperMin5=UpperSort(5,1);
UpperMax=UpperSort(10,1);
UpperMax2=UpperSort(9,1);
UpperMax3=UpperSort(8,1);
UpperMax4=UpperSort(7,1);
UpperMax5=UpperSort(6,1);

LowerMin=LowerSort(1,1);
LowerMin2=LowerSort(2,1);
LowerMin3=LowerSort(3,1);
LowerMin4=LowerSort(4,1);
LowerMin5=LowerSort(5,1);
LowerMax=LowerSort(10,1);
LowerMax2=LowerSort(9,1);
LowerMax3=LowerSort(8,1);
LowerMax4=LowerSort(7,1);
LowerMax5=LowerSort(6,1);


% ..............Region=1..............%
if(Region==1)
    Sa1=0;  Sa2=1;  Sa3=0;  Sa4=1;  Sa5=0;  Sa6=1;  Sa7=0;  Sa8=1;  Sa9=0;
Sa10=1;  Sa11=0;  Sa12=1;  Sa13=0;  Sa14=1;  Sa15=0;  Sa16=1;  Sa17=0;
Sa18=1;  Sa19=0;  Sa20=1;
```

```
    Sa21=1; Sa22=0; Sa23=1; Sa24=0; Sa25=1; Sa26=0; Sa27=1; Sa28=0; Sa29=1;
Sa30=0;  Sa31=1;  Sa32=0;  Sa33=1;  Sa34=0;  Sa35=1;  Sa36=0;  Sa37=1;
Sa38=0;  Sa39=1;  Sa40=0;
end

% ..............Region=11..............%
if(Region==11)
    Sa1=1;  Sa2=0;  Sa3=1;  Sa4=0;  Sa5=1;  Sa6=0;  Sa7=1;  Sa8=0;  Sa9=1;
Sa10=0;  Sa11=1;  Sa12=0;  Sa13=1;  Sa14=0;  Sa15=1;  Sa16=0;  Sa17=1;
Sa18=0;  Sa19=1;  Sa20=0;
    Sa21=0; Sa22=1; Sa23=0; Sa24=1; Sa25=0; Sa26=1; Sa27=0; Sa28=1; Sa29=0;
Sa30=1;  Sa31=0;  Sa32=1;  Sa33=0;  Sa34=1;  Sa35=0;  Sa36=1;  Sa37=0;
Sa38=1;  Sa39=0;  Sa40=1;
end

% % ..............Region=2..............%
if (Region==2 & I_DC_Pos>=0)

    Sa1=0;  Sa2=1;  Sa3=0;  Sa4=1;  Sa5=0;  Sa6=1;  Sa7=0;  Sa8=1;  Sa9=0;
Sa10=1;  Sa11=0;  Sa12=1;  Sa13=0;  Sa14=1;  Sa15=0;  Sa16=1;  Sa17=0;
Sa18=1;  Sa19=0;  Sa20=1;
    Sa21=1;  Sa22=0;  Sa23=1;  Sa24=0;  Sa25=1;  Sa26=0;  Sa27=1;  Sa28=0;
Sa29=1;  Sa30=0;  Sa31=1;  Sa32=0;  Sa33=1;  Sa34=0;  Sa35=1;  Sa36=0;
Sa37=1;  Sa38=0;  Sa39=1;  Sa40=0;

    if(UpperMin==1)
        Sa1=1;
        Sa2=0;
    end
    if(UpperMin==2)
        Sa3=1;
        Sa4=0;
    end
    if(UpperMin==3)
        Sa5=1;
        Sa6=0;
    end
    if(UpperMin==4)
        Sa7=1;
        Sa8=0;
    end
    if(UpperMin==5)
        Sa9=1;
        Sa10=0;
    end
    if(UpperMin==6)
        Sa11=1;
        Sa12=0;
    end
    if(UpperMin==7)
        Sa13=1;
        Sa14=0;
    end
    if(UpperMin==8)
        Sa15=1;
        Sa16=0;
```

```
    end
    if(UpperMin==9)
        Sa17=1;
        Sa18=0;
    end
    if(UpperMin==10)
        Sa19=1;
        Sa20=0;
    end



    if(LowerMax==11)
        Sa21=0;
        Sa22=1;
    end
    if(LowerMax==12)
        Sa23=0;
        Sa24=1;
    end
    if(LowerMax==13)
        Sa25=0;
        Sa26=1;
    end
    if(LowerMax==14)
        Sa27=0;
        Sa28=1;
    end
    if(LowerMax==15)
        Sa29=0;
        Sa30=1;
    end
    if(LowerMax==16)
        Sa31=0;
        Sa32=1;
    end
    if(LowerMax==17)
        Sa33=0;
        Sa34=1;
    end
    if(LowerMax==18)
        Sa35=0;
        Sa36=1;
    end
    if(LowerMax==19)
        Sa37=0;
        Sa38=1;
    end
    if(LowerMax==20)
        Sa39=0;
        Sa40=1;
    end

end
```

```
if (Region==2 & I_DC_Pos<0)

    Sa1=0;  Sa2=1;  Sa3=0;  Sa4=1;  Sa5=0;  Sa6=1;  Sa7=0;  Sa8=1;  Sa9=0;
Sa10=1;  Sa11=0;  Sa12=1;  Sa13=0;  Sa14=1;  Sa15=0;  Sa16=1;  Sa17=0;
Sa18=1;  Sa19=0;  Sa20=1;
    Sa21=1;  Sa22=0;  Sa23=1;  Sa24=0;  Sa25=1;  Sa26=0;  Sa27=1;  Sa28=0;
Sa29=1;  Sa30=0;  Sa31=1;  Sa32=0;  Sa33=1;  Sa34=0;  Sa35=1;  Sa36=0;
Sa37=1;  Sa38=0;  Sa39=1;  Sa40=0;

    if(UpperMax==1)
        Sa1=1;
        Sa2=0;
    end
    if(UpperMax==2)
        Sa3=1;
        Sa4=0;
    end
    if(UpperMax==3)
        Sa5=1;
        Sa6=0;
    end
    if(UpperMax==4)
        Sa7=1;
        Sa8=0;
    end
    if(UpperMax==5)
        Sa9=1;
        Sa10=0;
    end
    if(UpperMax==6)
        Sa11=1;
        Sa12=0;
    end
    if(UpperMax==7)
        Sa13=1;
        Sa14=0;
    end
    if(UpperMax==8)
        Sa15=1;
        Sa16=0;
    end
    if(UpperMax==9)
        Sa17=1;
        Sa18=0;
    end
    if(UpperMax==10)
        Sa19=1;
        Sa20=0;
    end



    if(LowerMin==11)
        Sa21=0;
        Sa22=1;
```

```
    end
    if(LowerMin==12)
        Sa23=0;
        Sa24=1;
    end
    if(LowerMin==13)
        Sa25=0;
        Sa26=1;
    end
    if(LowerMin==14)
        Sa27=0;
        Sa28=1;
    end
    if(LowerMin==15)
        Sa29=0;
        Sa30=1;
    end
    if(LowerMin==16)
        Sa31=0;
        Sa32=1;
    end
    if(LowerMin==17)
        Sa33=0;
        Sa34=1;
    end
    if(LowerMin==18)
        Sa35=0;
        Sa36=1;
    end
    if(LowerMin==19)
        Sa37=0;
        Sa38=1;
    end
    if(LowerMin==20)
        Sa39=0;
        Sa40=1;
    end

end

% % ..............Region=5..............%
if (Region==5 & I_DC_Pos>=0)

    Sa1=0;  Sa2=1;  Sa3=0;  Sa4=1;  Sa5=0;  Sa6=1;  Sa7=0;  Sa8=1;  Sa9=0;
Sa10=1;  Sa11=0;  Sa12=1;  Sa13=0;  Sa14=1;  Sa15=0;  Sa16=1;  Sa17=0;
Sa18=1;  Sa19=0;  Sa20=1;
    Sa21=1;  Sa22=0;  Sa23=1;  Sa24=0;  Sa25=1;  Sa26=0;  Sa27=1;  Sa28=0;
Sa29=1;  Sa30=0;  Sa31=1;  Sa32=0;  Sa33=1;  Sa34=0;  Sa35=1;  Sa36=0;
Sa37=1;  Sa38=0;  Sa39=1;  Sa40=0;

    if(UpperMin==1 | UpperMin2==1 | UpperMin3==1 | UpperMin4==1)
        Sa1=1;
        Sa2=0;
    end
    if(UpperMin==2 | UpperMin2==2 | UpperMin3==2 | UpperMin4==2)
        Sa3=1;
```

```
    Sa4=0;
end
if(UpperMin==3 | UpperMin2==3 | UpperMin3==3 | UpperMin4==3)
    Sa5=1;
    Sa6=0;
end
if(UpperMin==4 | UpperMin2==4 | UpperMin3==4 | UpperMin4==4)
    Sa7=1;
    Sa8=0;
end
if(UpperMin==5 | UpperMin2==5 | UpperMin3==5 | UpperMin4==5)
    Sa9=1;
    Sa10=0;
end
if(UpperMin==6 | UpperMin2==6 | UpperMin3==6 | UpperMin4==6)
    Sa11=1;
    Sa12=0;
end
if(UpperMin==7 | UpperMin2==7 | UpperMin3==7 | UpperMin4==7)
    Sa13=1;
    Sa14=0;
end
if(UpperMin==8 | UpperMin2==8 | UpperMin3==8 | UpperMin4==8)
    Sa15=1;
    Sa16=0;
end
if(UpperMin==9 | UpperMin2==9 | UpperMin3==9 | UpperMin4==9)
    Sa17=1;
    Sa18=0;
end
if(UpperMin==10 | UpperMin2==10 | UpperMin3==10 | UpperMin4==10)
    Sa19=1;
    Sa20=0;
end



if(LowerMax==11 | LowerMax2==11 | LowerMax3==11 | LowerMax4==11)
    Sa21=0;
    Sa22=1;
end
if(LowerMax==12 | LowerMax2==12 | LowerMax3==12 | LowerMax4==12)
    Sa23=0;
    Sa24=1;
end
if(LowerMax==13 | LowerMax2==13 | LowerMax3==13 | LowerMax4==13)
    Sa25=0;
    Sa26=1;
end
if(LowerMax==14 | LowerMax2==14 | LowerMax3==14 | LowerMax4==14)
    Sa27=0;
    Sa28=1;
end
if(LowerMax==15 | LowerMax2==15 | LowerMax3==15 | LowerMax4==15)
    Sa29=0;
    Sa30=1;
```

```
    end
    if(LowerMax==16 | LowerMax2==16 | LowerMax3==16 | LowerMax4==16)
        Sa31=0;
        Sa32=1;
    end
    if(LowerMax==17 | LowerMax2==17 | LowerMax3==17 | LowerMax4==17)
        Sa33=0;
        Sa34=1;
    end
    if(LowerMax==18 | LowerMax2==18 | LowerMax3==18 | LowerMax4==18)
        Sa35=0;
        Sa36=1;
    end
    if(LowerMax==19 | LowerMax2==19 | LowerMax3==19 | LowerMax4==19)
        Sa37=0;
        Sa38=1;
    end
    if(LowerMax==20 | LowerMax2==20 | LowerMax3==20 | LowerMax4==20)
        Sa39=0;
        Sa40=1;
    end

end



if (Region==5 & I_DC_Pos<0)

    Sa1=0;  Sa2=1;  Sa3=0;  Sa4=1;  Sa5=0;  Sa6=1;  Sa7=0;  Sa8=1;  Sa9=0;
Sa10=1;  Sa11=0;  Sa12=1;  Sa13=0;  Sa14=1;  Sa15=0;  Sa16=1;  Sa17=0;
Sa18=1;  Sa19=0;  Sa20=1;
    Sa21=1;  Sa22=0;  Sa23=1;  Sa24=0;  Sa25=1;  Sa26=0;  Sa27=1;  Sa28=0;
Sa29=1;  Sa30=0;  Sa31=1;  Sa32=0;  Sa33=1;  Sa34=0;  Sa35=1;  Sa36=0;
Sa37=1;  Sa38=0;  Sa39=1;  Sa40=0;

    if(UpperMax==1 | UpperMax2==1 | UpperMax3==1 | UpperMax4==1)
        Sa1=1;
        Sa2=0;
    end
    if(UpperMax==2 | UpperMax2==2 | UpperMax3==2 | UpperMax4==2)
        Sa3=1;
        Sa4=0;
    end
    if(UpperMax==3 | UpperMax2==3 | UpperMax3==3 | UpperMax4==3)
        Sa5=1;
        Sa6=0;
    end
    if(UpperMax==4 | UpperMax2==4 | UpperMax3==4 | UpperMax4==4)
        Sa7=1;
        Sa8=0;
    end
    if(UpperMax==5 | UpperMax2==5 | UpperMax3==5 | UpperMax4==5)
        Sa9=1;
        Sa10=0;
    end
    if(UpperMax==6 | UpperMax2==6 | UpperMax3==6 | UpperMax4==6)
```

```
    Sa11=1;
    Sa12=0;
end
if(UpperMax==7 | UpperMax2==7 | UpperMax3==7 | UpperMax4==7)
    Sa13=1;
    Sa14=0;
end
if(UpperMax==8 | UpperMax2==8 | UpperMax3==8 | UpperMax4==8)
    Sa15=1;
    Sa16=0;
end
if(UpperMax==9 | UpperMax2==9 | UpperMax3==9 | UpperMax4==9)
    Sa17=1;
    Sa18=0;
end
if(UpperMax==10 | UpperMax2==10 | UpperMax3==10 | UpperMax4==10)
    Sa19=1;
    Sa20=0;
end



if(LowerMin==11 | LowerMin2==11 | LowerMin3==11 | LowerMin4==11)
    Sa21=0;
    Sa22=1;
end
if(LowerMin==12 | LowerMin2==12 | LowerMin3==12 | LowerMin4==12)
    Sa23=0;
    Sa24=1;
end
if(LowerMin==13 | LowerMin2==13 | LowerMin3==13 | LowerMin4==13)
    Sa25=0;
    Sa26=1;
end
if(LowerMin==14 | LowerMin2==14 | LowerMin3==14 | LowerMin4==14)
    Sa27=0;
    Sa28=1;
end
if(LowerMin==15 | LowerMin2==15 | LowerMin3==15 | LowerMin4==15)
    Sa29=0;
    Sa30=1;
end
if(LowerMin==16 | LowerMin2==16 | LowerMin3==16 | LowerMin4==16)
    Sa31=0;
    Sa32=1;
end
if(LowerMin==17 | LowerMin2==17 | LowerMin3==17 | LowerMin4==17)
    Sa33=0;
    Sa34=1;
end
if(LowerMin==18 | LowerMin2==18 | LowerMin3==18 | LowerMin4==18)
    Sa35=0;
    Sa36=1;
end
if(LowerMin==19 | LowerMin2==19 | LowerMin3==19 | LowerMin4==19)
    Sa37=0;
```

```
        Sa38=1;
    end
    if(LowerMin==20 | LowerMin2==20 | LowerMin3==20 | LowerMin4==20)
        Sa39=0;
        Sa40=1;
    end

end

% % ..............Region=3..............%
if (Region==3 & I_DC_Pos>=0)

    Sa1=0;  Sa2=1;  Sa3=0;  Sa4=1;  Sa5=0;  Sa6=1;  Sa7=0;  Sa8=1;  Sa9=0;
Sa10=1;  Sa11=0;  Sa12=1;  Sa13=0;  Sa14=1;  Sa15=0;  Sa16=1;  Sa17=0;
Sa18=1;  Sa19=0;  Sa20=1;
    Sa21=1;  Sa22=0;  Sa23=1;  Sa24=0;  Sa25=1;  Sa26=0;  Sa27=1;  Sa28=0;
Sa29=1;  Sa30=0;  Sa31=1;  Sa32=0;  Sa33=1;  Sa34=0;  Sa35=1;  Sa36=0;
Sa37=1;  Sa38=0;  Sa39=1;  Sa40=0;

    if(UpperMin==1 | UpperMin2==1)
        Sa1=1;
        Sa2=0;
    end
    if(UpperMin==2 | UpperMin2==2)
        Sa3=1;
        Sa4=0;
    end
    if(UpperMin==3 | UpperMin2==3)
        Sa5=1;
        Sa6=0;
    end
    if(UpperMin==4 | UpperMin2==4)
        Sa7=1;
        Sa8=0;
    end
    if(UpperMin==5 | UpperMin2==5)
        Sa9=1;
        Sa10=0;
    end
    if(UpperMin==6 | UpperMin2==6)
        Sa11=1;
        Sa12=0;
    end
    if(UpperMin==7 | UpperMin2==7)
        Sa13=1;
        Sa14=0;
    end
    if(UpperMin==8 | UpperMin2==8)
        Sa15=1;
        Sa16=0;
    end
    if(UpperMin==9 | UpperMin2==9)
        Sa17=1;
        Sa18=0;
    end
    if(UpperMin==10 | UpperMin2==10)
```

```
        Sa19=1;
        Sa20=0;
    end



    if(LowerMax==11 | LowerMax2==11)
        Sa21=0;
        Sa22=1;
    end
    if(LowerMax==12 | LowerMax2==12)
        Sa23=0;
        Sa24=1;
    end
    if(LowerMax==13 | LowerMax2==13)
        Sa25=0;
        Sa26=1;
    end
    if(LowerMax==14 | LowerMax2==14)
        Sa27=0;
        Sa28=1;
    end
    if(LowerMax==15 | LowerMax2==15)
        Sa29=0;
        Sa30=1;
    end
    if(LowerMax==16 | LowerMax2==16)
        Sa31=0;
        Sa32=1;
    end
    if(LowerMax==17 | LowerMax2==17)
        Sa33=0;
        Sa34=1;
    end
    if(LowerMax==18 | LowerMax2==18)
        Sa35=0;
        Sa36=1;
    end
    if(LowerMax==19 | LowerMax2==19)
        Sa37=0;
        Sa38=1;
    end
    if(LowerMax==20 | LowerMax2==20)
        Sa39=0;
        Sa40=1;
    end

end



if (Region==3 & I_DC_Pos<0)
```

```
    Sa1=0;  Sa2=1;  Sa3=0;  Sa4=1;  Sa5=0;  Sa6=1;  Sa7=0;  Sa8=1;  Sa9=0;
Sa10=1;  Sa11=0;  Sa12=1;  Sa13=0;  Sa14=1;  Sa15=0;  Sa16=1;  Sa17=0;
Sa18=1;  Sa19=0;  Sa20=1;
    Sa21=1;  Sa22=0;  Sa23=1;  Sa24=0;  Sa25=1;  Sa26=0;  Sa27=1;  Sa28=0;
Sa29=1;  Sa30=0;  Sa31=1;  Sa32=0;  Sa33=1;  Sa34=0;  Sa35=1;  Sa36=0;
Sa37=1;  Sa38=0;  Sa39=1;  Sa40=0;

    if(UpperMax==1 | UpperMax2==1)
        Sa1=1;
        Sa2=0;
    end
    if(UpperMax==2 | UpperMax2==2)
        Sa3=1;
        Sa4=0;
    end
    if(UpperMax==3 | UpperMax2==3)
        Sa5=1;
        Sa6=0;
    end
    if(UpperMax==4 | UpperMax2==4)
        Sa7=1;
        Sa8=0;
    end
    if(UpperMax==5 | UpperMax2==5)
        Sa9=1;
        Sa10=0;
    end
    if(UpperMax==6 | UpperMax2==6)
        Sa11=1;
        Sa12=0;
    end
    if(UpperMax==7 | UpperMax2==7)
        Sa13=1;
        Sa14=0;
    end
    if(UpperMax==8 | UpperMax2==8)
        Sa15=1;
        Sa16=0;
    end
    if(UpperMax==9 | UpperMax2==9)
        Sa17=1;
        Sa18=0;
    end
    if(UpperMax==10 | UpperMax2==10)
        Sa19=1;
        Sa20=0;
    end



    if(LowerMin==11 | LowerMin2==11)
        Sa21=0;
        Sa22=1;
    end
    if(LowerMin==12 | LowerMin2==12)
        Sa23=0;
```

```
        Sa24=1;
    end
    if(LowerMin==13 | LowerMin2==13)
        Sa25=0;
        Sa26=1;
    end
    if(LowerMin==14 | LowerMin2==14)
        Sa27=0;
        Sa28=1;
    end
    if(LowerMin==15 | LowerMin2==15)
        Sa29=0;
        Sa30=1;
    end
    if(LowerMin==16 | LowerMin2==16)
        Sa31=0;
        Sa32=1;
    end
    if(LowerMin==17 | LowerMin2==17)
        Sa33=0;
        Sa34=1;
    end
    if(LowerMin==18 | LowerMin2==18)
        Sa35=0;
        Sa36=1;
    end
    if(LowerMin==19 | LowerMin2==19)
        Sa37=0;
        Sa38=1;
    end
    if(LowerMin==20 | LowerMin2==20)
        Sa39=0;
        Sa40=1;
    end

end

% % ..............Region=4..............%
if (Region==4 & I_DC_Pos>=0)

    Sa1=0;  Sa2=1;  Sa3=0;  Sa4=1;  Sa5=0;  Sa6=1;  Sa7=0;  Sa8=1;  Sa9=0;
Sa10=1;  Sa11=0;  Sa12=1;  Sa13=0;  Sa14=1;  Sa15=0;  Sa16=1;  Sa17=0;
Sa18=1;  Sa19=0;  Sa20=1;
    Sa21=1;  Sa22=0;  Sa23=1;  Sa24=0;  Sa25=1;  Sa26=0;  Sa27=1;  Sa28=0;
Sa29=1;  Sa30=0;  Sa31=1;  Sa32=0;  Sa33=1;  Sa34=0;  Sa35=1;  Sa36=0;
Sa37=1;  Sa38=0;  Sa39=1;  Sa40=0;

    if(UpperMin==1 | UpperMin2==1 | UpperMin3==1)
        Sa1=1;
        Sa2=0;
    end
    if(UpperMin==2 | UpperMin2==2 | UpperMin3==2)
        Sa3=1;
        Sa4=0;
    end
    if(UpperMin==3 | UpperMin2==3 | UpperMin3==3)
```

```
    Sa5=1;
    Sa6=0;
end
if(UpperMin==4 | UpperMin2==4 | UpperMin3==4)
    Sa7=1;
    Sa8=0;
end
if(UpperMin==5 | UpperMin2==5 | UpperMin3==5)
    Sa9=1;
    Sa10=0;
end
if(UpperMin==6 | UpperMin2==6 | UpperMin3==6)
    Sa11=1;
    Sa12=0;
end
if(UpperMin==7 | UpperMin2==7 | UpperMin3==7)
    Sa13=1;
    Sa14=0;
end
if(UpperMin==8 | UpperMin2==8 | UpperMin3==8)
    Sa15=1;
    Sa16=0;
end
if(UpperMin==9 | UpperMin2==9 | UpperMin3==9)
    Sa17=1;
    Sa18=0;
end
if(UpperMin==10 | UpperMin2==10 | UpperMin3==10)
    Sa19=1;
    Sa20=0;
end



if(LowerMax==11 | LowerMax2==11 | LowerMax3==11)
    Sa21=0;
    Sa22=1;
end
if(LowerMax==12 | LowerMax2==12 | LowerMax3==12)
    Sa23=0;
    Sa24=1;
end
if(LowerMax==13 | LowerMax2==13 | LowerMax3==13)
    Sa25=0;
    Sa26=1;
end
if(LowerMax==14 | LowerMax2==14 | LowerMax3==14)
    Sa27=0;
    Sa28=1;
end
if(LowerMax==15 | LowerMax2==15 | LowerMax3==15)
    Sa29=0;
    Sa30=1;
end
if(LowerMax==16 | LowerMax2==16 | LowerMax3==16)
    Sa31=0;
```

```
        Sa32=1;
    end
    if(LowerMax==17 | LowerMax2==17 | LowerMax3==17)
        Sa33=0;
        Sa34=1;
    end
    if(LowerMax==18 | LowerMax2==18 | LowerMax3==18)
        Sa35=0;
        Sa36=1;
    end
    if(LowerMax==19 | LowerMax2==19 | LowerMax3==19)
        Sa37=0;
        Sa38=1;
    end
    if(LowerMax==20 | LowerMax2==20 | LowerMax3==20)
        Sa39=0;
        Sa40=1;
    end

end



if (Region==4 & I_DC_Pos<0)

    Sa1=0;  Sa2=1;  Sa3=0;  Sa4=1;  Sa5=0;  Sa6=1;  Sa7=0;  Sa8=1;  Sa9=0;
Sa10=1;  Sa11=0;  Sa12=1;  Sa13=0;  Sa14=1;  Sa15=0;  Sa16=1;  Sa17=0;
Sa18=1;  Sa19=0;  Sa20=1;
    Sa21=1;  Sa22=0;  Sa23=1;  Sa24=0;  Sa25=1;  Sa26=0;  Sa27=1;  Sa28=0;
Sa29=1;  Sa30=0;  Sa31=1;  Sa32=0;  Sa33=1;  Sa34=0;  Sa35=1;  Sa36=0;
Sa37=1;  Sa38=0;  Sa39=1;  Sa40=0;

    if(UpperMax==1 | UpperMax2==1 | UpperMax3==1)
        Sa1=1;
        Sa2=0;
    end
    if(UpperMax==2 | UpperMax2==2 | UpperMax3==2)
        Sa3=1;
        Sa4=0;
    end
    if(UpperMax==3 | UpperMax2==3 | UpperMax3==3)
        Sa5=1;
        Sa6=0;
    end
    if(UpperMax==4 | UpperMax2==4 | UpperMax3==4)
        Sa7=1;
        Sa8=0;
    end
    if(UpperMax==5 | UpperMax2==5 | UpperMax3==5)
        Sa9=1;
        Sa10=0;
    end
    if(UpperMax==6 | UpperMax2==6 | UpperMax3==6)
        Sa11=1;
        Sa12=0;
    end
```

```
if(UpperMax==7 | UpperMax2==7 | UpperMax3==7)
    Sa13=1;
    Sa14=0;
end
if(UpperMax==8 | UpperMax2==8 | UpperMax3==8)
    Sa15=1;
    Sa16=0;
end
if(UpperMax==9 | UpperMax2==9 | UpperMax3==9)
    Sa17=1;
    Sa18=0;
end
if(UpperMax==10 | UpperMax2==10 | UpperMax3==10)
    Sa19=1;
    Sa20=0;
end



if(LowerMin==11 | LowerMin2==11 | LowerMin3==11)
    Sa21=0;
    Sa22=1;
end
if(LowerMin==12 | LowerMin2==12 | LowerMin3==12)
    Sa23=0;
    Sa24=1;
end
if(LowerMin==13 | LowerMin2==13 | LowerMin3==13)
    Sa25=0;
    Sa26=1;
end
if(LowerMin==14 | LowerMin2==14 | LowerMin3==14)
    Sa27=0;
    Sa28=1;
end
if(LowerMin==15 | LowerMin2==15 | LowerMin3==15)
    Sa29=0;
    Sa30=1;
end
if(LowerMin==16 | LowerMin2==16 | LowerMin3==16)
    Sa31=0;
    Sa32=1;
end
if(LowerMin==17 | LowerMin2==17 | LowerMin3==17)
    Sa33=0;
    Sa34=1;
end
if(LowerMin==18 | LowerMin2==18 | LowerMin3==18)
    Sa35=0;
    Sa36=1;
end
if(LowerMin==19 | LowerMin2==19 | LowerMin3==19)
    Sa37=0;
    Sa38=1;
end
if(LowerMin==20 | LowerMin2==20 | LowerMin3==20)
```

```
        Sa39=0;
        Sa40=1;
    end

end



% % ..............Region=6..............%

if (Region==6 & I_DC_Pos>=0)

    Sa1=0;  Sa2=1;  Sa3=0;  Sa4=1;  Sa5=0;  Sa6=1;  Sa7=0;  Sa8=1;  Sa9=0;
Sa10=1;  Sa11=0;  Sa12=1;  Sa13=0;  Sa14=1;  Sa15=0;  Sa16=1;  Sa17=0;
Sa18=1;  Sa19=0;  Sa20=1;
    Sa21=1;  Sa22=0;  Sa23=1;  Sa24=0;  Sa25=1;  Sa26=0;  Sa27=1;  Sa28=0;
Sa29=1;  Sa30=0;  Sa31=1;  Sa32=0;  Sa33=1;  Sa34=0;  Sa35=1;  Sa36=0;
Sa37=1;  Sa38=0;  Sa39=1;  Sa40=0;

    if(UpperMin==1 | UpperMin2==1 | UpperMin3==1 | UpperMin4==1 |
UpperMin5==1)
        Sa1=1;
        Sa2=0;
    end
    if(UpperMin==2 | UpperMin2==2 | UpperMin3==2 | UpperMin4==2 |
UpperMin5==2)
        Sa3=1;
        Sa4=0;
    end
    if(UpperMin==3 | UpperMin2==3 | UpperMin3==3 | UpperMin4==3 |
UpperMin5==3)
        Sa5=1;
        Sa6=0;
    end
    if(UpperMin==4 | UpperMin2==4 | UpperMin3==4 | UpperMin4==4 |
UpperMin5==4)
        Sa7=1;
        Sa8=0;
    end
    if(UpperMin==5 | UpperMin2==5 | UpperMin3==5 | UpperMin4==5 |
UpperMin5==5)
        Sa9=1;
        Sa10=0;
    end
    if(UpperMin==6 | UpperMin2==6 | UpperMin3==6 | UpperMin4==6 |
UpperMin5==6)
        Sa11=1;
        Sa12=0;
    end
    if(UpperMin==7 | UpperMin2==7 | UpperMin3==7 | UpperMin4==7 |
UpperMin5==7)
        Sa13=1;
        Sa14=0;
    end
```

```
    if(UpperMin==8 | UpperMin2==8 | UpperMin3==8 | UpperMin4==8 |
UpperMin5==8)
        Sa15=1;
        Sa16=0;
    end
    if(UpperMin==9 | UpperMin2==9 | UpperMin3==9 | UpperMin4==9 |
UpperMin5==9)
        Sa17=1;
        Sa18=0;
    end
    if(UpperMin==10 | UpperMin2==10 | UpperMin3==10 | UpperMin4==10 |
UpperMin5==10)
        Sa19=1;
        Sa20=0;
    end



    if(LowerMax==11 | LowerMax2==11 | LowerMax3==11 | LowerMax4==11 |
LowerMax5==11)
        Sa21=0;
        Sa22=1;
    end
    if(LowerMax==12 | LowerMax2==12 | LowerMax3==12 | LowerMax4==12 |
LowerMax5==12)
        Sa23=0;
        Sa24=1;
    end
    if(LowerMax==13 | LowerMax2==13 | LowerMax3==13 | LowerMax4==13 |
LowerMax5==13)
        Sa25=0;
        Sa26=1;
    end
    if(LowerMax==14 | LowerMax2==14 | LowerMax3==14 | LowerMax4==14 |
LowerMax5==14)
        Sa27=0;
        Sa28=1;
    end
    if(LowerMax==15 | LowerMax2==15 | LowerMax3==15 | LowerMax4==15 |
LowerMax5==15)
        Sa29=0;
        Sa30=1;
    end
    if(LowerMax==16 | LowerMax2==16 | LowerMax3==16 | LowerMax4==16 |
LowerMax5==16)
        Sa31=0;
        Sa32=1;
    end
    if(LowerMax==17 | LowerMax2==17 | LowerMax3==17 | LowerMax4==17 |
LowerMax5==17)
        Sa33=0;
        Sa34=1;
    end
    if(LowerMax==18 | LowerMax2==18 | LowerMax3==18 | LowerMax4==18 |
LowerMax5==18)
        Sa35=0;
```

```
        Sa36=1;
    end
    if(LowerMax==19 | LowerMax2==19 | LowerMax3==19 | LowerMax4==19 |
LowerMax5==19)
        Sa37=0;
        Sa38=1;
    end
    if(LowerMax==20 | LowerMax2==20 | LowerMax3==20 | LowerMax4==20 |
LowerMax5==20)
        Sa39=0;
        Sa40=1;
    end

end



if (Region==6 & I_DC_Pos<0)

    Sa1=0;  Sa2=1;  Sa3=0;  Sa4=1;  Sa5=0;  Sa6=1;  Sa7=0;  Sa8=1;  Sa9=0;
Sa10=1;  Sa11=0;  Sa12=1;  Sa13=0;  Sa14=1;  Sa15=0;  Sa16=1;  Sa17=0;
Sa18=1;  Sa19=0;  Sa20=1;
    Sa21=1;  Sa22=0;  Sa23=1;  Sa24=0;  Sa25=1;  Sa26=0;  Sa27=1;  Sa28=0;
Sa29=1;  Sa30=0;  Sa31=1;  Sa32=0;  Sa33=1;  Sa34=0;  Sa35=1;  Sa36=0;
Sa37=1;  Sa38=0;  Sa39=1;  Sa40=0;

    if(UpperMax==1 | UpperMax2==1 | UpperMax3==1 | UpperMax4==1 |
UpperMax5==1)
        Sa1=1;
        Sa2=0;
    end
    if(UpperMax==2 | UpperMax2==2 | UpperMax3==2 | UpperMax4==2 |
UpperMax5==2)
        Sa3=1;
        Sa4=0;
    end
    if(UpperMax==3 | UpperMax2==3 | UpperMax3==3 | UpperMax4==3 |
UpperMax5==3)
        Sa5=1;
        Sa6=0;
    end
    if(UpperMax==4 | UpperMax2==4 | UpperMax3==4 | UpperMax4==4 |
UpperMax5==4)
        Sa7=1;
        Sa8=0;
    end
    if(UpperMax==5 | UpperMax2==5 | UpperMax3==5 | UpperMax4==5 |
UpperMax5==5)
        Sa9=1;
        Sa10=0;
    end
    if(UpperMax==6 | UpperMax2==6 | UpperMax3==6 | UpperMax4==6 |
UpperMax5==6)
        Sa11=1;
        Sa12=0;
    end
```

```
    if(UpperMax==7 | UpperMax2==7 | UpperMax3==7 | UpperMax4==7 |
UpperMax5==7)
        Sa13=1;
        Sa14=0;
    end
    if(UpperMax==8 | UpperMax2==8 | UpperMax3==8 | UpperMax4==8 |
UpperMax5==8)
        Sa15=1;
        Sa16=0;
    end
    if(UpperMax==9 | UpperMax2==9 | UpperMax3==9 | UpperMax4==9 |
UpperMax5==9)
        Sa17=1;
        Sa18=0;
    end
    if(UpperMax==10 | UpperMax2==10 | UpperMax3==10 | UpperMax4==10 |
UpperMax5==10)
        Sa19=1;
        Sa20=0;
    end


    if(LowerMin==11 | LowerMin2==11 | LowerMin3==11 | LowerMin4==11 |
LowerMin5==11)
        Sa21=0;
        Sa22=1;
    end
    if(LowerMin==12 | LowerMin2==12 | LowerMin3==12 | LowerMin4==12 |
LowerMin5==12)
        Sa23=0;
        Sa24=1;
    end
    if(LowerMin==13 | LowerMin2==13 | LowerMin3==13 | LowerMin4==13 |
LowerMin5==13)
        Sa25=0;
        Sa26=1;
    end
    if(LowerMin==14 | LowerMin2==14 | LowerMin3==14 | LowerMin4==14 |
LowerMin5==14)
        Sa27=0;
        Sa28=1;
    end
    if(LowerMin==15 | LowerMin2==15 | LowerMin3==15 | LowerMin4==15 |
LowerMin5==15)
        Sa29=0;
        Sa30=1;
    end
    if(LowerMin==16 | LowerMin2==16 | LowerMin3==16 | LowerMin4==16 |
LowerMin5==16)
        Sa31=0;
        Sa32=1;
    end
    if(LowerMin==17 | LowerMin2==17 | LowerMin3==17 | LowerMin4==17 |
LowerMin5==17)
        Sa33=0;
        Sa34=1;
```

```
    end
    if(LowerMin==18 | LowerMin2==18 | LowerMin3==18 | LowerMin4==18 |
LowerMin5==18)
        Sa35=0;
        Sa36=1;
    end
    if(LowerMin==19 | LowerMin2==19 | LowerMin3==19 | LowerMin4==19 |
LowerMin5==19)
        Sa37=0;
        Sa38=1;
    end
    if(LowerMin==20 | LowerMin2==20 | LowerMin3==20 | LowerMin4==20 |
LowerMin5==20)
        Sa39=0;
        Sa40=1;
    end

end
% % ..............Region=7..............%

if (Region==7 & I_DC_Pos>=0)

    Sa1=1;  Sa2=0;  Sa3=1;  Sa4=0;  Sa5=1;  Sa6=0;  Sa7=1;  Sa8=0;  Sa9=1;
Sa10=0;  Sa11=1;  Sa12=0;  Sa13=1;  Sa14=0;  Sa15=1;  Sa16=0;  Sa17=1;
Sa18=0;  Sa19=1;  Sa20=0;
    Sa21=0;  Sa22=1;  Sa23=0;  Sa24=1;  Sa25=0;  Sa26=1;  Sa27=0;  Sa28=1;
Sa29=0;  Sa30=1;  Sa31=0;  Sa32=1;  Sa33=0;  Sa34=1;  Sa35=0;  Sa36=1;
Sa37=0;  Sa38=1;  Sa39=0;  Sa40=1;

    if(UpperMax==1 | UpperMax2==1 | UpperMax3==1 | UpperMax4==1)
        Sa1=0;
        Sa2=1;
    end
    if(UpperMax==2 | UpperMax2==2 | UpperMax3==2 | UpperMax4==2)
        Sa3=0;
        Sa4=1;
    end
    if(UpperMax==3 | UpperMax2==3 | UpperMax3==3 | UpperMax4==3)
        Sa5=0;
        Sa6=1;
    end
    if(UpperMax==4 | UpperMax2==4 | UpperMax3==4 | UpperMax4==4)
        Sa7=0;
        Sa8=1;
    end
    if(UpperMax==5 | UpperMax2==5 | UpperMax3==5 | UpperMax4==5)
        Sa9=0;
        Sa10=1;
    end
    if(UpperMax==6 | UpperMax2==6 | UpperMax3==6 | UpperMax4==6)
        Sa11=0;
        Sa12=1;
    end
    if(UpperMax==7 | UpperMax2==7 | UpperMin3==7 | UpperMax4==7)
        Sa13=0;
        Sa14=1;
```

```
end
if(UpperMax==8 | UpperMax2==8 | UpperMax3==8 | UpperMax4==8)
    Sa15=0;
    Sa16=1;
end
if(UpperMax==9 | UpperMax2==9 | UpperMax3==9 | UpperMax4==9)
    Sa17=0;
    Sa18=1;
end
if(UpperMax==10 | UpperMax2==10 | UpperMax3==10 | UpperMax4==10)
    Sa19=0;
    Sa20=1;
end


if(LowerMin==11 | LowerMin2==11 | LowerMin3==11 | LowerMin4==11)
    Sa21=1;
    Sa22=0;
end
if(LowerMin==12 | LowerMin2==12 | LowerMin3==12 | LowerMin4==12)
    Sa23=1;
    Sa24=0;
end
if(LowerMin==13 | LowerMin2==13 | LowerMin3==13 | LowerMin4==13)
    Sa25=1;
    Sa26=0;
end
if(LowerMin==14 | LowerMin2==14 | LowerMin3==14 | LowerMin4==14)
    Sa27=1;
    Sa28=0;
end
if(LowerMin==15 | LowerMin2==15 | LowerMin3==15 | LowerMin4==15)
    Sa29=1;
    Sa30=0;
end
if(LowerMin==16 | LowerMin2==16 | LowerMin3==16 | LowerMin4==16)
    Sa31=1;
    Sa32=0;
end
if(LowerMin==17 | LowerMin2==17 | LowerMin3==17 | LowerMin4==17)
    Sa33=1;
    Sa34=0;
end
if(LowerMin==18 | LowerMin2==18 | LowerMin3==18 | LowerMin4==18)
    Sa35=1;
    Sa36=0;
end
if(LowerMin==19 | LowerMin2==19 | LowerMin3==19 | LowerMin4==19)
    Sa37=1;
    Sa38=0;
end
if(LowerMin==20 | LowerMin2==20 | LowerMin3==20 | LowerMin4==20)
    Sa39=1;
    Sa40=0;
end
```

```
end



if (Region==7 & I_DC_Pos<0)

    Sa1=1;  Sa2=0;  Sa3=1;  Sa4=0;  Sa5=1;  Sa6=0;  Sa7=1;  Sa8=0;  Sa9=1;
Sa10=0;  Sa11=1;  Sa12=0;  Sa13=1;  Sa14=0;  Sa15=1;  Sa16=0;  Sa17=1;
Sa18=0;  Sa19=1;  Sa20=0;
    Sa21=0;  Sa22=1;  Sa23=0;  Sa24=1;  Sa25=0;  Sa26=1;  Sa27=0;  Sa28=1;
Sa29=0;  Sa30=1;  Sa31=0;  Sa32=1;  Sa33=0;  Sa34=1;  Sa35=0;  Sa36=1;
Sa37=0;  Sa38=1;  Sa39=0;  Sa40=1;

    if(UpperMin==1 | UpperMin2==1 | UpperMin3==1 | UpperMin4==1)
        Sa1=0;
        Sa2=1;
    end
    if(UpperMin==2 | UpperMin2==2 | UpperMin3==2 | UpperMin4==2)
        Sa3=0;
        Sa4=1;
    end
    if(UpperMin==3 | UpperMin2==3 | UpperMin3==3 | UpperMin4==3)
        Sa5=0;
        Sa6=1;
    end
    if(UpperMin==4 | UpperMin2==4 | UpperMin3==4 | UpperMin4==4)
        Sa7=0;
        Sa8=1;
    end
    if(UpperMin==5 | UpperMin2==5 | UpperMin3==5 | UpperMin4==5)
        Sa9=0;
        Sa10=1;
    end
    if(UpperMin==6 | UpperMin2==6 | UpperMin3==6 | UpperMin4==6)
        Sa11=0;
        Sa12=1;
    end
    if(UpperMin==7 | UpperMin2==7 | UpperMin3==7 | UpperMin4==7)
        Sa13=0;
        Sa14=1;
    end
    if(UpperMin==8 | UpperMin2==8 | UpperMin3==8 | UpperMin4==8)
        Sa15=0;
        Sa16=1;
    end
    if(UpperMin==9 | UpperMin2==9 | UpperMin3==9 | UpperMin4==9)
        Sa17=0;
        Sa18=1;
    end
    if(UpperMin==10 | UpperMin2==10 | UpperMin3==10 | UpperMin4==10)
        Sa19=0;
        Sa20=1;
    end
```

```
    if(LowerMax==11 | LowerMax2==11 | LowerMax3==11 | LowerMax4==11)
        Sa21=1;
        Sa22=0;
    end
    if(LowerMax==12 | LowerMax2==12 | LowerMax3==12 | LowerMax4==12)
        Sa23=1;
        Sa24=0;
    end
    if(LowerMax==13 | LowerMax2==13 | LowerMax3==13 | LowerMax4==13)
        Sa25=1;
        Sa26=0;
    end
    if(LowerMax==14 | LowerMax2==14 | LowerMax3==14 | LowerMax4==14)
        Sa27=1;
        Sa28=0;
    end
    if(LowerMax==15 | LowerMax2==15 | LowerMax3==15 | LowerMax4==15)
        Sa29=1;
        Sa30=0;
    end
    if(LowerMax==16 | LowerMax2==16 | LowerMax3==16 | LowerMax4==16)
        Sa31=1;
        Sa32=0;
    end
    if(LowerMax==17 | LowerMax2==17 | LowerMax3==17 | LowerMax4==17)
        Sa33=1;
        Sa34=0;
    end
    if(LowerMax==18 | LowerMax2==18 | LowerMax3==18 | LowerMax4==18)
        Sa35=1;
        Sa36=0;
    end
    if(LowerMax==19 | LowerMax2==19 | LowerMax3==19 | LowerMax4==19)
        Sa37=1;
        Sa38=0;
    end
    if(LowerMax==20 | LowerMax2==20 | LowerMax3==20 | LowerMax4==20)
        Sa39=1;
        Sa40=0;
    end
end

% % ..............Region=8..............%
if (Region==8 & I_DC_Pos>=0)

    Sa1=1;  Sa2=0;  Sa3=1;  Sa4=0;  Sa5=1;  Sa6=0;  Sa7=1;  Sa8=0;  Sa9=1;
Sa10=0;  Sa11=1;  Sa12=0;  Sa13=1;  Sa14=0;  Sa15=1;  Sa16=0;  Sa17=1;
Sa18=0;  Sa19=1;  Sa20=0;
    Sa21=0;  Sa22=1;  Sa23=0;  Sa24=1;  Sa25=0;  Sa26=1;  Sa27=0;  Sa28=1;
Sa29=0;  Sa30=1;  Sa31=0;  Sa32=1;  Sa33=0;  Sa34=1;  Sa35=0;  Sa36=1;
Sa37=0;  Sa38=1;  Sa39=0;  Sa40=1;

    if(UpperMax==1 | UpperMax2==1 | UpperMax3==1)
        Sa1=0;
        Sa2=1;
```

```
end
if(UpperMax==2 | UpperMax2==2 | UpperMax3==2)
    Sa3=0;
    Sa4=1;
end
if(UpperMax==3 | UpperMax2==3 | UpperMax3==3)
    Sa5=0;
    Sa6=1;
end
if(UpperMax==4 | UpperMax2==4 | UpperMax3==4)
    Sa7=0;
    Sa8=1;
end
if(UpperMax==5 | UpperMax2==5 | UpperMax3==5)
    Sa9=0;
    Sa10=1;
end
if(UpperMax==6 | UpperMax2==6 | UpperMax3==6)
    Sa11=0;
    Sa12=1;
end
if(UpperMax==7 | UpperMax2==7 | UpperMin3==7)
    Sa13=0;
    Sa14=1;
end
if(UpperMax==8 | UpperMax2==8 | UpperMax3==8)
    Sa15=0;
    Sa16=1;
end
if(UpperMax==9 | UpperMax2==9 | UpperMax3==9)
    Sa17=0;
    Sa18=1;
end
if(UpperMax==10 | UpperMax2==10 | UpperMax3==10)
    Sa19=0;
    Sa20=1;
end



if(LowerMin==11 | LowerMin2==11 | LowerMin3==11)
    Sa21=1;
    Sa22=0;
end
if(LowerMin==12 | LowerMin2==12 | LowerMin3==12)
    Sa23=1;
    Sa24=0;
end
if(LowerMin==13 | LowerMin2==13 | LowerMin3==13)
    Sa25=1;
    Sa26=0;
end
if(LowerMin==14 | LowerMin2==14 | LowerMin3==14)
    Sa27=1;
    Sa28=0;
end
```

```
    if(LowerMin==15 | LowerMin2==15 | LowerMin3==15)
        Sa29=1;
        Sa30=0;
    end
    if(LowerMin==16 | LowerMin2==16 | LowerMin3==16)
        Sa31=1;
        Sa32=0;
    end
    if(LowerMin==17 | LowerMin2==17 | LowerMin3==17)
        Sa33=1;
        Sa34=0;
    end
    if(LowerMin==18 | LowerMin2==18 | LowerMin3==18)
        Sa35=1;
        Sa36=0;
    end
    if(LowerMin==19 | LowerMin2==19 | LowerMin3==19)
        Sa37=1;
        Sa38=0;
    end
    if(LowerMin==20 | LowerMin2==20 | LowerMin3==20)
        Sa39=1;
        Sa40=0;
    end

end


if (Region==8 & I_DC_Pos<0)

    Sa1=1;  Sa2=0;  Sa3=1;  Sa4=0;  Sa5=1;  Sa6=0;  Sa7=1;  Sa8=0;  Sa9=1;
Sa10=0;  Sa11=1;  Sa12=0;  Sa13=1;  Sa14=0;  Sa15=1;  Sa16=0;  Sa17=1;
Sa18=0;  Sa19=1;  Sa20=0;
    Sa21=0;  Sa22=1;  Sa23=0;  Sa24=1;  Sa25=0;  Sa26=1;  Sa27=0;  Sa28=1;
Sa29=0;  Sa30=1;  Sa31=0;  Sa32=1;  Sa33=0;  Sa34=1;  Sa35=0;  Sa36=1;
Sa37=0;  Sa38=1;  Sa39=0;  Sa40=1;

    if(UpperMin==1 | UpperMin2==1 | UpperMin3==1)
        Sa1=0;
        Sa2=1;
    end
    if(UpperMin==2 | UpperMin2==2 | UpperMin3==2)
        Sa3=0;
        Sa4=1;
    end
    if(UpperMin==3 | UpperMin2==3 | UpperMin3==3)
        Sa5=0;
        Sa6=1;
    end
    if(UpperMin==4 | UpperMin2==4 | UpperMin3==4)
        Sa7=0;
        Sa8=1;
    end
    if(UpperMin==5 | UpperMin2==5 | UpperMin3==5)
        Sa9=0;
        Sa10=1;
```

```
end
if(UpperMin==6 | UpperMin2==6 | UpperMin3==6)
    Sa11=0;
    Sa12=1;
end
if(UpperMin==7 | UpperMin2==7 | UpperMin3==7)
    Sa13=0;
    Sa14=1;
end
if(UpperMin==8 | UpperMin2==8 | UpperMin3==8)
    Sa15=0;
    Sa16=1;
end
if(UpperMin==9 | UpperMin2==9 | UpperMin3==9)
    Sa17=0;
    Sa18=1;
end
if(UpperMin==10 | UpperMin2==10 | UpperMin3==10)
    Sa19=0;
    Sa20=1;
end


if(LowerMax==11 | LowerMax2==11 | LowerMax3==11)
    Sa21=1;
    Sa22=0;
end
if(LowerMax==12 | LowerMax2==12 | LowerMax3==12)
    Sa23=1;
    Sa24=0;
end
if(LowerMax==13 | LowerMax2==13 | LowerMax3==13)
    Sa25=1;
    Sa26=0;
end
if(LowerMax==14 | LowerMax2==14 | LowerMax3==14)
    Sa27=1;
    Sa28=0;
end
if(LowerMax==15 | LowerMax2==15 | LowerMax3==15)
    Sa29=1;
    Sa30=0;
end
if(LowerMax==16 | LowerMax2==16 | LowerMax3==16)
    Sa31=1;
    Sa32=0;
end
if(LowerMax==17 | LowerMax2==17 | LowerMax3==17)
    Sa33=1;
    Sa34=0;
end
if(LowerMax==18 | LowerMax2==18 | LowerMax3==18)
    Sa35=1;
    Sa36=0;
end
if(LowerMax==19 | LowerMax2==19 | LowerMax3==19)
```

```
        Sa37=1;
        Sa38=0;
    end
    if(LowerMax==20 | LowerMax2==20 | LowerMax3==20)
        Sa39=1;
        Sa40=0;
    end
end


% % ..............Region=9..............%
if (Region==9 & I_DC_Pos>=0)

    Sa1=1;  Sa2=0;  Sa3=1;  Sa4=0;  Sa5=1;  Sa6=0;  Sa7=1;  Sa8=0;  Sa9=1;
Sa10=0;  Sa11=1;  Sa12=0;  Sa13=1;  Sa14=0;  Sa15=1;  Sa16=0;  Sa17=1;
Sa18=0;  Sa19=1;  Sa20=0;
    Sa21=0;  Sa22=1;  Sa23=0;  Sa24=1;  Sa25=0;  Sa26=1;  Sa27=0;  Sa28=1;
Sa29=0;  Sa30=1;  Sa31=0;  Sa32=1;  Sa33=0;  Sa34=1;  Sa35=0;  Sa36=1;
Sa37=0;  Sa38=1;  Sa39=0;  Sa40=1;

    if(UpperMax==1 | UpperMax2==1)
        Sa1=0;
        Sa2=1;
    end
    if(UpperMax==2 | UpperMax2==2)
        Sa3=0;
        Sa4=1;
    end
    if(UpperMax==3 | UpperMax2==3)
        Sa5=0;
        Sa6=1;
    end
    if(UpperMax==4 | UpperMax2==4)
        Sa7=0;
        Sa8=1;
    end
    if(UpperMax==5 | UpperMax2==5)
        Sa9=0;
        Sa10=1;
    end
    if(UpperMax==6 | UpperMax2==6)
        Sa11=0;
        Sa12=1;
    end
    if(UpperMax==7 | UpperMax2==7)
        Sa13=0;
        Sa14=1;
    end
    if(UpperMax==8 | UpperMax2==8)
        Sa15=0;
        Sa16=1;
    end
    if(UpperMax==9 | UpperMax2==9)
        Sa17=0;
        Sa18=1;
    end
```

```
    if(UpperMax==10 | UpperMax2==10)
        Sa19=0;
        Sa20=1;
    end

    if(LowerMin==11 | LowerMin2==11)
        Sa21=1;
        Sa22=0;
    end
    if(LowerMin==12 | LowerMin2==12)
        Sa23=1;
        Sa24=0;
    end
    if(LowerMin==13 | LowerMin2==13)
        Sa25=1;
        Sa26=0;
    end
    if(LowerMin==14 | LowerMin2==14)
        Sa27=1;
        Sa28=0;
    end
    if(LowerMin==15 | LowerMin2==15)
        Sa29=1;
        Sa30=0;
    end
    if(LowerMin==16 | LowerMin2==16)
        Sa31=1;
        Sa32=0;
    end
    if(LowerMin==17 | LowerMin2==17)
        Sa33=1;
        Sa34=0;
    end
    if(LowerMin==18 | LowerMin2==18)
        Sa35=1;
        Sa36=0;
    end
    if(LowerMin==19 | LowerMin2==19)
        Sa37=1;
        Sa38=0;
    end
    if(LowerMin==20 | LowerMin2==20)
        Sa39=1;
        Sa40=0;
    end

end


if (Region==9 & I_DC_Pos<0)

    Sa1=1;  Sa2=0;  Sa3=1;  Sa4=0;  Sa5=1;  Sa6=0;  Sa7=1;  Sa8=0;  Sa9=1;
Sa10=0;  Sa11=1;  Sa12=0;  Sa13=1;  Sa14=0;  Sa15=1;  Sa16=0;  Sa17=1;
Sa18=0;  Sa19=1;  Sa20=0;
```

```
    Sa21=0;  Sa22=1;  Sa23=0;  Sa24=1;  Sa25=0;  Sa26=1;  Sa27=0;  Sa28=1;
Sa29=0;  Sa30=1;  Sa31=0;  Sa32=1;  Sa33=0;  Sa34=1;  Sa35=0;  Sa36=1;
Sa37=0;  Sa38=1;  Sa39=0;  Sa40=1;

    if(UpperMin==1 | UpperMin2==1)
        Sa1=0;
        Sa2=1;
    end
    if(UpperMin==2 | UpperMin2==2)
        Sa3=0;
        Sa4=1;
    end
    if(UpperMin==3 | UpperMin2==3)
        Sa5=0;
        Sa6=1;
    end
    if(UpperMin==4 | UpperMin2==4)
        Sa7=0;
        Sa8=1;
    end
    if(UpperMin==5 | UpperMin2==5)
        Sa9=0;
        Sa10=1;
    end
    if(UpperMin==6 | UpperMin2==6)
        Sa11=0;
        Sa12=1;
    end
    if(UpperMin==7 | UpperMin2==7)
        Sa13=0;
        Sa14=1;
    end
    if(UpperMin==8 | UpperMin2==8)
        Sa15=0;
        Sa16=1;
    end
    if(UpperMin==9 | UpperMin2==9)
        Sa17=0;
        Sa18=1;
    end
    if(UpperMin==10 | UpperMin2==10)
        Sa19=0;
        Sa20=1;
    end


    if(LowerMax==11 | LowerMax2==11)
        Sa21=1;
        Sa22=0;
    end
    if(LowerMax==12 | LowerMax2==12)
        Sa23=1;
        Sa24=0;
    end
    if(LowerMax==13 | LowerMax2==13)
        Sa25=1;
```

```
        Sa26=0;
    end
    if(LowerMax==14 | LowerMax2==14)
        Sa27=1;
        Sa28=0;
    end
    if(LowerMax==15 | LowerMax2==15)
        Sa29=1;
        Sa30=0;
    end
    if(LowerMax==16 | LowerMax2==16)
        Sa31=1;
        Sa32=0;
    end
    if(LowerMax==17 | LowerMax2==17)
        Sa33=1;
        Sa34=0;
    end
    if(LowerMax==18 | LowerMax2==18)
        Sa35=1;
        Sa36=0;
    end
    if(LowerMax==19 | LowerMax2==19)
        Sa37=1;
        Sa38=0;
    end
    if(LowerMax==20 | LowerMax2==20)
        Sa39=1;
        Sa40=0;
    end
end

% % ..............Region=10..............%
if (Region==10 & I_DC_Pos>=0)

    Sa1=1;  Sa2=0;  Sa3=1;  Sa4=0;  Sa5=1;  Sa6=0;  Sa7=1;  Sa8=0;  Sa9=1;
Sa10=0;  Sa11=1;  Sa12=0;  Sa13=1;  Sa14=0;  Sa15=1;  Sa16=0;  Sa17=1;
Sa18=0;  Sa19=1;  Sa20=0;
    Sa21=0;  Sa22=1;  Sa23=0;  Sa24=1;  Sa25=0;  Sa26=1;  Sa27=0;  Sa28=1;
Sa29=0;  Sa30=1;  Sa31=0;  Sa32=1;  Sa33=0;  Sa34=1;  Sa35=0;  Sa36=1;
Sa37=0;  Sa38=1;  Sa39=0;  Sa40=1;

    if(UpperMax==1)
        Sa1=0;
        Sa2=1;
    end
    if(UpperMax==2)
        Sa3=0;
        Sa4=1;
    end
    if(UpperMax==3)
        Sa5=0;
        Sa6=1;
    end
    if(UpperMax==4)
        Sa7=0;
```

```
    Sa8=1;
end
if(UpperMax==5)
    Sa9=0;
    Sa10=1;
end
if(UpperMax==6)
    Sa11=0;
    Sa12=1;
end
if(UpperMax==7)
    Sa13=0;
    Sa14=1;
end
if(UpperMax==8)
    Sa15=0;
    Sa16=1;
end
if(UpperMax==9)
    Sa17=0;
    Sa18=1;
end
if(UpperMax==10)
    Sa19=0;
    Sa20=1;
end

if(LowerMin==11)
    Sa21=1;
    Sa22=0;
end
if(LowerMin==12)
    Sa23=1;
    Sa24=0;
end
if(LowerMin==13)
    Sa25=1;
    Sa26=0;
end
if(LowerMin==14)
    Sa27=1;
    Sa28=0;
end
if(LowerMin==15)
    Sa29=1;
    Sa30=0;
end
if(LowerMin==16)
    Sa31=1;
    Sa32=0;
end
if(LowerMin==17)
    Sa33=1;
    Sa34=0;
end
if(LowerMin==18)
    Sa35=1;
```

```
        Sa36=0;
    end
    if(LowerMin==19)
        Sa37=1;
        Sa38=0;
    end
    if(LowerMin==20)
        Sa39=1;
        Sa40=0;
    end

end

if (Region==10 & I_DC_Pos<0)

    Sa1=1;  Sa2=0;  Sa3=1;  Sa4=0;  Sa5=1;  Sa6=0;  Sa7=1;  Sa8=0;  Sa9=1;
Sa10=0;  Sa11=1;  Sa12=0;  Sa13=1;  Sa14=0;  Sa15=1;  Sa16=0;  Sa17=1;
Sa18=0;  Sa19=1;  Sa20=0;
    Sa21=0;  Sa22=1;  Sa23=0;  Sa24=1;  Sa25=0;  Sa26=1;  Sa27=0;  Sa28=1;
Sa29=0;  Sa30=1;  Sa31=0;  Sa32=1;  Sa33=0;  Sa34=1;  Sa35=0;  Sa36=1;
Sa37=0;  Sa38=1;  Sa39=0;  Sa40=1;

    if(UpperMin==1)
        Sa1=0;
        Sa2=1;
    end
    if(UpperMin==2)
        Sa3=0;
        Sa4=1;
    end
    if(UpperMin==3)
        Sa5=0;
        Sa6=1;
    end
    if(UpperMin==4)
        Sa7=0;
        Sa8=1;
    end
    if(UpperMin==5)
        Sa9=0;
        Sa10=1;
    end
    if(UpperMin==6)
        Sa11=0;
        Sa12=1;
    end
    if(UpperMin==7)
        Sa13=0;
        Sa14=1;
    end
    if(UpperMin==8)
        Sa15=0;
        Sa16=1;
    end
    if(UpperMin==9)
        Sa17=0;
```

```
        Sa18=1;
    end
    if(UpperMin==10)
        Sa19=0;
        Sa20=1;
    end

    if(LowerMax==11)
        Sa21=1;
        Sa22=0;
    end
    if(LowerMax==12)
        Sa23=1;
        Sa24=0;
    end
    if(LowerMax==13)
        Sa25=1;
        Sa26=0;
    end
    if(LowerMax==14)
        Sa27=1;
        Sa28=0;
    end
    if(LowerMax==15)
        Sa29=1;
        Sa30=0;
    end
    if(LowerMax==16)
        Sa31=1;
        Sa32=0;
    end
    if(LowerMax==17)
        Sa33=1;
        Sa34=0;
    end
    if(LowerMax==18)
        Sa35=1;
        Sa36=0;
    end
    if(LowerMax==19)
        Sa37=1;
        Sa38=0;
    end
    if(LowerMax==20)
        Sa39=1;
        Sa40=0;
    end
end

Switches=[Sa1  Sa2  Sa3  Sa4  Sa5  Sa6  Sa7  Sa8  Sa9   Sa10  Sa11  Sa12
Sa13  Sa14  Sa15  Sa16  Sa17  Sa18  Sa19  Sa20 Sa21 Sa22 Sa23 Sa24 Sa25 Sa26
Sa27 Sa28 Sa29  Sa30  Sa31  Sa32  Sa33  Sa34  Sa35  Sa36  Sa37  Sa38  Sa39
Sa40];
```

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