Karlsruhe Institute of Technology

Elektrotechnisches Institut (ETI)
Prof. Dr.-Ing. Michael Braun
Prof. Dr.-Ing. Martin Doppelbauer
Prof. Dr.-Ing. Marc Hiller
Kaiserstr.12. 76131 Karlsruhe

Elektrotechnisches Institut

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Authors:	Christian Axtmann, Johannes Kolb, Michael Braun
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A Novel DC/3AC-Converter Topology with Reduced Component Effort

Christian Axtmann
Institute of Electrical Engineering
Karlsruhe Institute of Technology
Karlsruhe, Germany
Email: christian.axtmann@kit.edu

Johannes Kolb
SHARE at KIT
Schaeffler Technologies AG & Co. KG
Karlsruhe, Germany
Email: johannes.kolb@schaeffler.com

Michael Braun
Institute of Electrical Engineering
Karlsruhe Institute of Technology
Karlsruhe, Germany
Email: michael.braun@kit.edu

***Abstract*—A novel topology is proposed that interfaces between one or multiple DC sources and a three-phase machine. The DC-side converter consists of two half-bridges that form a specialized converter. The half-bridges operate at a reduced voltage which reduces inductor effort and switching losses. The resulting four DC-link levels power two three-phase bridges that can drive open-winding machines. The circuit is analyzed and compared to the common three-phase-bridge with DC converter by means of component stress and thus component effort. Finally, closed loop control is examined, synthesized and confirmed by simulation results.**

I. Introduction

In today's world of electric transportation, many measures are taken to improve the cruising range and costs of hybrid or full electric vehicles (HEV, EV). In the design process of electric vehicles, the volume and costs of individual submodules is one of the most crucial criteria to optimize as they define the total costs and efficiency.

[1] and [2] state cost distributions in power electronic converters, furthermore [1] also states a volume distribution. Regarding volume, most space is taken up by air (approx. 50%) followed by cooling and passive components (approx. 20% each). About one third of material costs fall upon semiconductors, followed by passives (approx. 26%) and sensors (approx. 25%).

By system integration, the 'air'-fraction in volume can be reduced. Examples for recent developments in this field are double sided cooled modules (DSC modules) that shrink the power modules size [3] and thus increase power density. Because of the improved heat transfer, cooling effort can also be reduced. Among others, this offers the possibility to integrate power electronics into a wheel hub drive [4].

The second most important leverage to shrink the converter's volume are the passive components, such as DC-link capacitances and DC-converter inductances. [5] shows that a higher pulse frequency can lead to smaller filters and thus passive components, which is already reachable for high power converters when using novel semiconductor materials such as silicon carbide (SiC). Besides pulse frequency, [5] reduces the total converter volume (up to a certain point) by interleaving multiple DC converters. In [6] and [7] magnetic coupling of inductors of interleaved phases can reduce inductor volume even further. In this contribution, the approach is also to tackle the DC-converter inductances. Recent research [8] has brought up another way to decrease the inductor volume by decreasing the pulsed voltage across the inductor. Since this is independent from the aforementioned remedies of increased pulse frequency and interleaved DC converters, they are still applicable additionally in the proposed topology and could lead to an even further reduction in component size.

In the following publication, the basic idea of splitting the DC-link and attaching DC-converters and three-phase bridges to the partial voltages and aim of the proposed topology is explained. A circuit analysis reveals the working principle. Thereupon, a control scheme for all degrees of freedom is derived. Subsequently, the topology is compared to a three-phase bridge with boost converter, regarding component expense. Simulation results demonstrate correct operation of the derived control scheme. A conclusion and an outlook finish the contribution.

II. The novel Converter Topology

The novel topology is presented in fig. 1. The circuit consists of two half-bridges that form a DC converter with reduced voltage ($\mathrm{T_{T1}}$, $\mathrm{T_{T2}}$, $\mathrm{T_{B1}}$, $\mathrm{T_{B2}}$) and two three-phase bridges ($\mathrm{T_{11}}$-$\mathrm{T_{26}}$). Because of the reduced working-voltage of the DC converter, semiconductors with smaller blocking voltage and down-scaled inductors can be used in the DC converter stage to achieve the same current ripple as a common three-phase bridge with boost converter.

Hence, the converter-topology is aimed to reduce the converter volume. Also, if multiple sources are used, the overall growth of the converter is less than that of a comparable three-phase bridge with boost converter, because only smaller DC converter 'submodules' need to be replicated.

The proposed circuit is based on patent application [9]. The basic concept of half-bridges that utilize a fraction of the total DC-link voltage was issued in [8] for a battery-fed multilevel H-bridge cell. An idea of feeding a four-level T-type converter with this kind of DC converter is published in [10] for an uninterruptible power supply. By attaching two three-phase-bridges to the two inner resp. outer potentials, an open-winding machine can be fed. With an adequate control of the three-phase-bridges, it is possible to run the machine over the span of source voltage of modern battery systems. The advantage

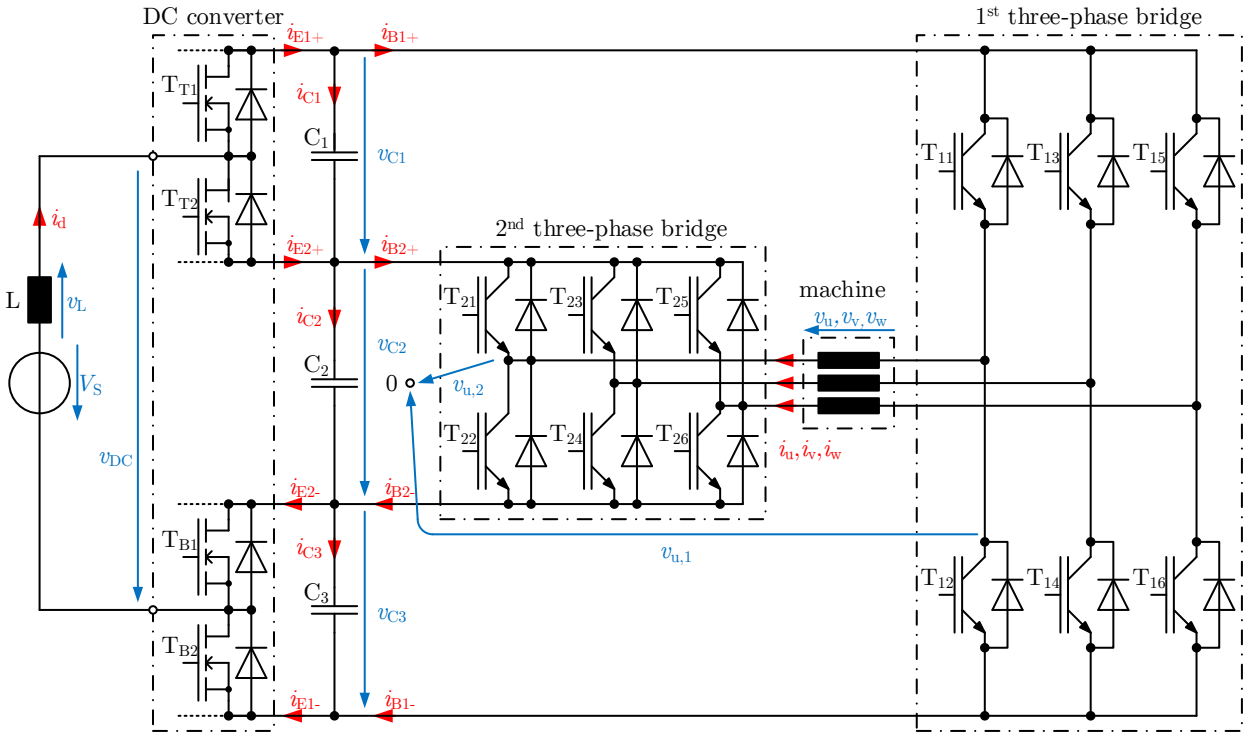

Fig. 1. Schematic of the proposed topology. All mentioned voltages and currents are marked.

of the proposed topology is the reduction in size of the DC converter. Both semiconductor and inductor volume can be decreased, which is shown in the next section.

III. Circuit Analysis

The following circuit analysis is done for ideal components, thus neglecting the parasitic resistance of both inductors and capacitors as well as the drop voltage and switching behavior of semiconductors. The source voltage V_S needs to be in the range of

$$v_{C2} \leq V_S \leq v_{C1} + v_{C2} + v_{C3} \tag{1}$$

otherwise the DC converter's freewheeling diodes conduct. The DC converter features 4 switching states, as shown in fig. 2. Assuming stationary operation, the DC converter's output-voltage is

$$v_{DC} = V_S \tag{2}$$

so that the inductor-voltage is

$$v_L = 0 \tag{3}$$

Furthermore, if the symmetry $u_{C1} = u_{C3}$ is assumed, v_{DC} is adjusted by switching between the two switching states a) and d) from fig. 2, so that the source current i_d either flows through T_{T1} and T_{B2} or T_{T2} and T_{B1}.

So, the half-bridges output currents $i_{E,x}$ result in

$$i_{E1+} = i_{E1-} = i_{E1} = \frac{V_S - v_{C2}}{v_{C1} + v_{C3}} \cdot i_d \tag{4}$$

$$i_{E2+} = i_{E2-} = i_{E2} = \left(1 - \frac{V_S - v_{C2}}{v_{C1} + v_{C3}}\right) \cdot i_d \tag{5}$$

To get constant DC-link voltages, the DC-link capacitor currents i_{Cn} must be zero, which means that the current consumption $i_{B,x}$ of the attached three-phase-bridges must compensate the sourced currents of the DC-converter in the particular DC-link rails:

$$i_{Bx} = i_{Ex}|_{x=1,2} \tag{6}$$

If a power P_A has to be transferred from the DC source to the machine's terminals, then both three-phase bridges can contribute a fraction of the total output power, so that

$$P_A = P_{B1} + P_{B2} \tag{7}$$

Furthermore, if losses are neglected, the source current can be expressed as

$$i_d = \frac{P_A}{V_S} \tag{8}$$

As the DC voltage of the three-phase bridges is known, the DC input currents of each bridge can be expressed as

$$i_{B1} = \frac{P_{B1}}{v_{C1} + v_{C2} + v_{C3}} = \frac{b \cdot P_A}{v_{C1} + v_{C2} + v_{C3}} \tag{9}$$

$$i_{B2} = \frac{P_{B2}}{v_{C2}} = \frac{(1-b) \cdot P_A}{v_{C2}} \tag{10}$$

The parameter b defines the distribution of the total output-power to the three-phase bridges. Solving (6) with (4), (5), (8), (9) and (10) for b brings

$$b = \frac{(V_S - v_{C2})(v_{C1} + v_{C2} + v_{C3})}{V_S (v_{C1} + v_{C3})} \tag{11}$$

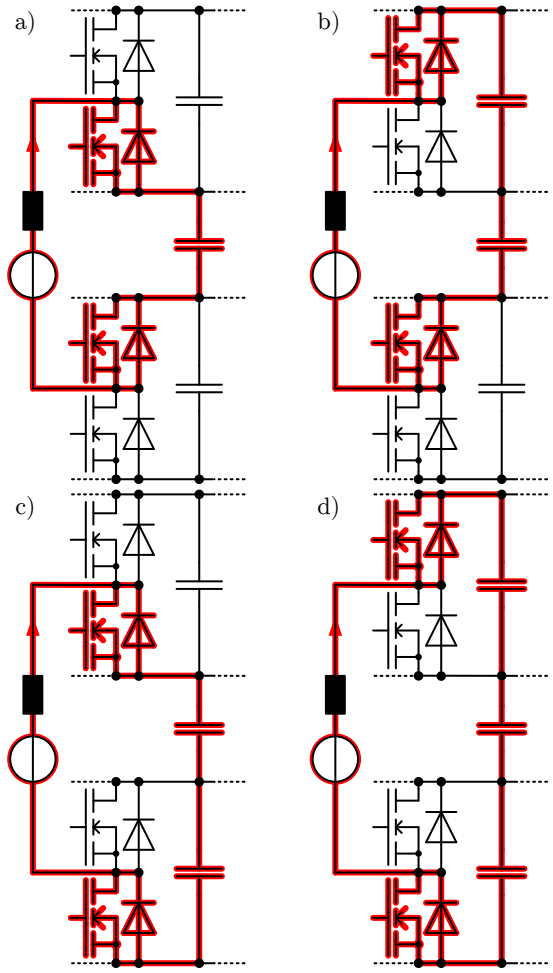

Fig. 2. Possible switching states of the primary DC converter. In stationary and symmetric operation, only states a) and d) are used. The states b) and c) can be used to control the symmetry of $u_{C1} - u_{C3}$ (see section IV-C).

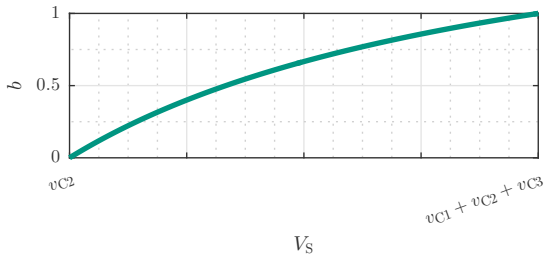

Fig. 3. Distribution b of the total output-power to the two three-phase bridges as a function of V_S and a fixed ratio of $\frac{v_{C1}}{v_{C2}} = 0.5$ and symmetry ($v_{C1} = v_{C3}$). It can be seen that the power distribution is defined for the whole supply voltage range.

Fig. 3 depicts the dependence of b on V_S. This arises the question, how the power distribution is achieved. Examining the power balance of bridge 1 shows

$$P_{B1} = \frac{3}{2}\,\hat{I}\,\hat{V}_{B1}\cos(\varphi) \stackrel{!}{=} b \cdot P_A = b \cdot \frac{3}{2}\,\hat{I}\,\hat{V}_M\cos(\varphi) \quad (12)$$

$$\hat{V}_{B1} = b \cdot \hat{U}_M \quad (13)$$

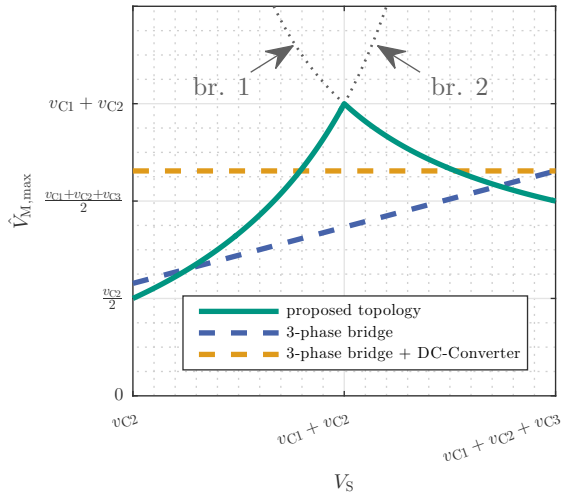

Fig. 4. Maximum achievable phase voltage amplitude of the proposed topology for varying source voltage. As a comparison, the maximum achievable machine voltage of a common three-phase bridge with wye-connected machine is shown (blue) and with additional DC converter (yellow, see fig. 11).

Similar calculation for bridge 2 leads to

$$\hat{V}_{B2} = (1 - b) \cdot \hat{V}_M \quad (14)$$

In eq. (12) P_B is the power that one bridge transfers. $\hat{I}$ and $\hat{V}_{Bn}$ are the three-phase bridge's AC-side voltages, $\hat{V}_M$ is the machine's phase voltage amplitude. It can be seen that the power distribution can be achieved by distribution of the wanted machine voltage to the associated three-phase bridges.

Since the particular amplitudes of the three-phase bridges are a function of the source voltage, the maximum achievable machine voltage amplitudes must be investigated. This is done separately for each bridge. The maximum AC amplitude that a three-phase bridge can create (without zero-sequence) is half the DC-link voltage (defined phase-to-neutral). So, solving (13) with (11) results in

$$b \cdot \hat{V}_{M,max} = \hat{V}_{B1,max}\left(= \frac{v_{C1} + v_{C2} + v_{C3}}{2}\right) \quad (15)$$

$$\hat{V}_{M,max}\Big|_{B1,max} = \frac{(v_{C1} + v_{C3})\,V_S}{2\,(V_S - v_{C2})} \quad (16)$$

In similar manner, the operating limit of bridge 2 is achieved at

$$\hat{V}_{M,max}\Big|_{B2,max} = \frac{(v_{C1} + v_{C3})\,V_S}{2\,(v_{C1} + v_{C2} + v_{C3} - V_S)} \quad (17)$$

If none of the three-phase bridges may leave their linear operating rage, the maximum achievable phase voltage amplitude $\hat{V}_{M,max}$ is

$$\hat{V}_{M,max} = \min\left(\hat{V}_{M,max}\Big|_{B1,max}, \hat{V}_{M,max}\Big|_{B2,max}\right) \quad (18)$$

Fig. 4 shows the maximum achievable phase voltage amplitude $\hat{V}_{M,max}$ as a function of the source voltage V_S. As a reference, the maximum phase voltage amplitude of a three-phase bridge with and without DC converter is shown. By

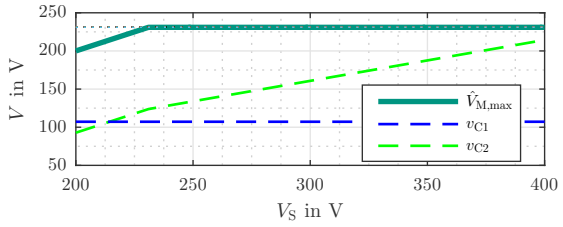

Fig. 5. Example of the maximum achievable phase voltage amplitude for a source voltage in the range of 200 V to 400 V and a machine with 230 V phase voltage amplitude.

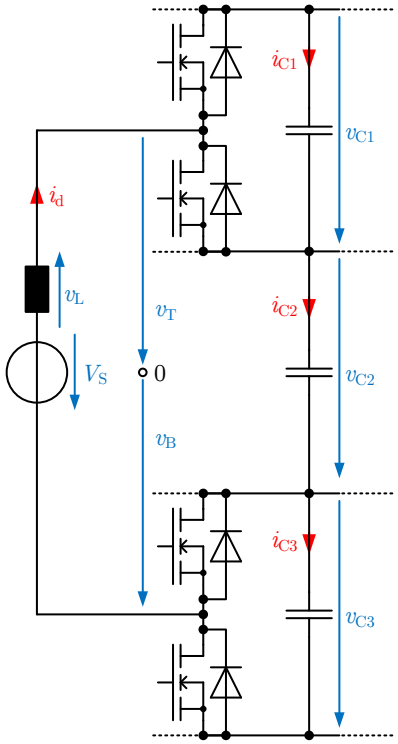

Fig. 6. Subcircuit of the DC converter. The converter output-voltage can be divided in $v_T + v_B$.

adapting the DC-link voltages as a function of the source voltage, the operating range can be flattened and expanded. An exemplary implementation is shown in fig. 5.

IV. Control Analysis and Synthesis

As it can be seen in fig. 1, there are 3 DC-link capacitors and one inductor per voltage source besides the machine. As every of these energy storages contribute one degree of freedom, there are overall 4 degrees of freedom: i_{Ln}, v_{C1}, v_{C2}, v_{C3}. These degrees of freedom must be controlled for proper operation of the proposed topology, which is described in the following paragraphs.

A. Control of the inductor current i_{Ln}

For the analysis of the inductor current control loop, the ohmic resistance of the inductor is neglected.

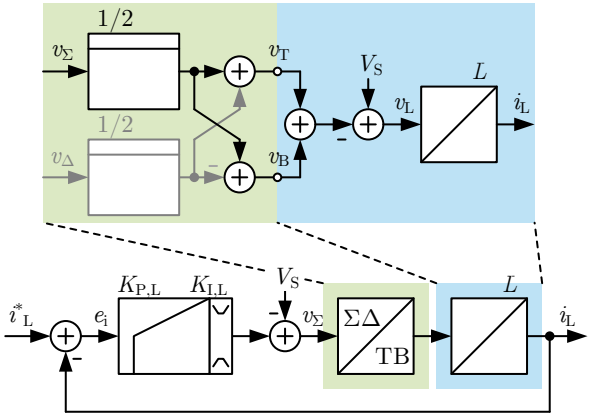

Fig. 7. Control path of the inductor current. The sum voltage $v_\Sigma = v_T + v_B$ can adjust the inductor voltage. The difference voltage v_Δ has no effect for current control. The source voltage V_S is a (measurable) disturbance value that can be precontrolled.

The analysis is valid for all sources n, so that the index is omitted for the sake of clarity. Starting from the known relation between voltage and current of an inductor

$$v_L(t) = L \cdot \frac{\mathrm{d}i_L(t)}{\mathrm{d}t} \tag{19}$$

and fig. 1, it can be seen that the inductor voltage is the difference between the source voltage and the DC converter output voltage

$$v_L(t) = V_S - v_{DC}(t) \tag{20}$$

The DC converter voltage v_{DC} can be split in two voltages v_T and v_B that are referenced to a virtual potential "0" laying in the middle of v_{C2}, as shown in fig. 6. So every half of the DC converter can create a separate mean voltage within a pulse period in the range of

$$v_T \in [\frac{V_{C2}}{2}; \frac{V_{C2}}{2} + V_{C1}] \tag{21}$$

resp.

$$v_B \in [\frac{V_{C2}}{2}; \frac{V_{C2}}{2} + V_{C3}]. \tag{22}$$

v_T and v_B can be expressed in terms of sum and difference by

$$v_\Sigma = v_T + v_B \qquad v_\Delta = v_T - v_B \tag{23}$$

resp.

$$v_T = \frac{1}{2}(v_\Sigma + v_\Delta) \qquad v_B = \frac{1}{2}(v_\Sigma - v_\Delta) \tag{24}$$

The sum v_Σ matches the DC converter's output voltage v_{DC}, whereas the difference v_Δ does not influence v_{DC}. Therefore v_Σ can be used for current control of the source inductances and v_Δ remains for the control of another degree of freedom. This is used in section IV-C. The resulting control path is shown in fig. 7. Common control design strategies (e.g. amplitude optimum) can be applied for the current controller, as the control path is linear within its operating limits.

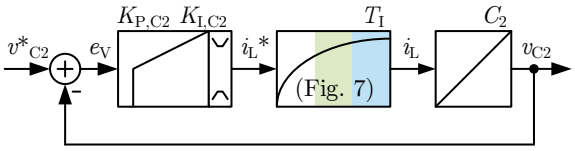

Fig. 8. Cascaded control scheme of the inner capacitor voltage v_{C2}. The subsidiary control of the inductor current can be approximated as a PT1 element. Its time constant T_I is then the reciprocal of the current-control loop crossover frequency.

B. Control of the inner capacitor voltage v_{C2}

The inductor current always flows through the inner capacitor C_2, independent from the particular switching state of the DC converter. This is illustrated in fig. 2. On the contrary, the current flowing through the outer capacitors C_1 and C_3 is a function of the switching state (see also fig. 2).

This qualifies the primary DC converter to control the inner capacitor voltage v_{C2}. It would also be possible to control the sum voltage $v_{C1} + v_{C2} + v_{C3}$. But as the current through the outer capacitors is a function of the DC converter's duty cycle (see fig. 2), the non-linearity of the circuit because of its right-half-plane zero needs to be considered. The structure of the derived closed loop voltage control is shown in fig. 8. Again, the control path is linear within its operating range, so that common design strategies can be applied as voltage controller (e.g. symmetrical optimum).

C. Control of the outer capacitor voltage symmetry $v_{C1} - v_{C3}$

The outer capacitor voltages are controlled in terms of symmetry and absolute value. This is advantageous, as the DC converter still features a way of intervention by adjusting the difference voltage v_Δ which can be used for symmetry control. The absolute capacitor voltages are finally controlled by adequate current consumption of the three-phase bridges.

Aim of the symmetry control is to keep the difference $v_{C1} - v_{C3} = 0$. Assuming identical capacitances ($C_3 = C_1$), this difference can be expressed as

$$v_{C1} - v_{C3} = \frac{1}{C_1} \int i_{C1}\,\mathrm{d}t - \frac{1}{C_3} \int i_{C3}\,\mathrm{d}t \tag{25}$$

$$v_{C1} - v_{C3} = \frac{1}{C_1} \int i_{C1} - i_{C3}\,\mathrm{d}t \tag{26}$$

Replacing the capacitor currents by the duty cycles and inductor current yields the non-linear equation

$$v_{C1} - v_{C3} = \frac{1}{C_1} \int i_L \left(\underbrace{\frac{v_T - \frac{v_{C2}}{2}}{v_{C1}}}_{a_{T_{T1}}} - \underbrace{\frac{v_B - \frac{v_{C2}}{2}}{v_{C3}}}_{a_{T_{B2}}} \right) \mathrm{d}t \tag{27}$$

In a first step, this can be linearized around its operating point at $v_{C1} \approx v_{C3}$ (symmetry)

$$v_{C1} - v_{C3} = \frac{1}{C_1} \int \frac{i_L}{v_{C1}} (v_T - v_B)\,\mathrm{d}t \tag{28}$$

$$v_{C1} - v_{C3} = \frac{1}{C_1} \int \frac{i_L}{v_{C1}} v_\Delta\,\mathrm{d}t \tag{29}$$

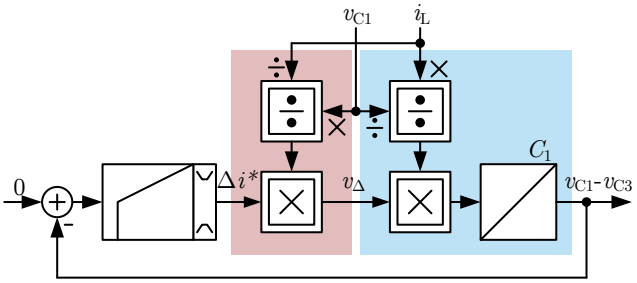

Fig. 9. Control scheme for symmetry control of $v_{C1} - v_{C3}$. The control path itself is still non-linear (blue) and is linearized with its inverse function (red).

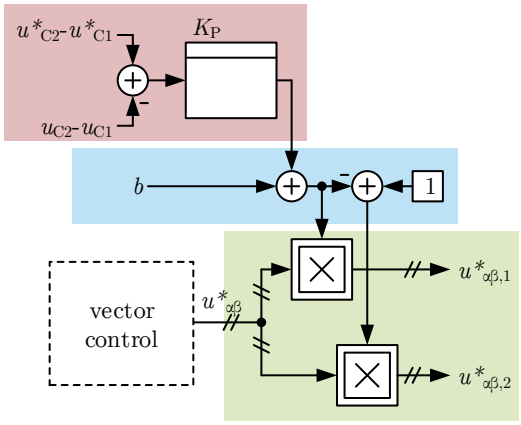

Fig. 10. Control scheme for voltage (and thus power) distribution in α/β (green). The power distribution b is shown in blue. Because of this feed-forward-control, a P-controller is sufficient for keeping the capacitor voltages at its set-points (red).

The resulting control path is shown in fig. 9. The resulting transfer function is still non-linear but can be linearized with its inverse function as v_{C1} and i_L are measured values.

D. Control of the absolute outer capacitor voltages v_{C1} and v_{C3} and machine control

As final degree of freedom, the absolute values of the outer capacitor voltages need to be controlled. This can be achieved by varying the current consumption of the attached three-phase bridges. Because of the advantageous feed-forward control of the power distribution among the bridges with factor b, the prevailing ratios of the capacitor voltages are only minimally disturbed. Hence, a simple P-controller is sufficient to keep the wanted symmetry of capacitors C_1 resp. C_3 and C_2.

The control scheme is shown in fig. 10. The voltage space-vector $u^*_{\alpha\beta}$ of an common overlaid vector control is weighted with b resp. $1 - b$ which results in the voltage space-vectors for both the three-phase bridges. Since b was derived to fulfill eq. (6), no deviation in the DC-link voltages should appear. Remaining deviations or set-point steps can be taken over by a P-controller.

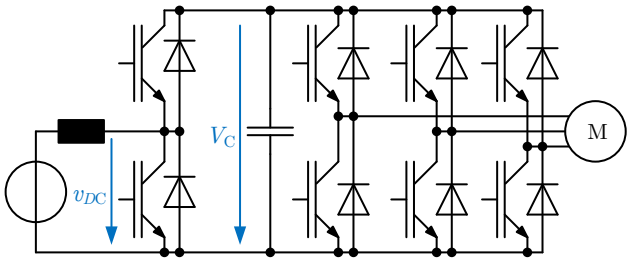

Fig. 11. Common three-phase bridge with attached boost-converter as reference topology.

V. Comparison of the Component Expense to a Three-Phase Bridge with Boost Converter

Since it is one of the most common power converters, a three-phase bridge with attached DC converter (fig. 11) serves as a reference for comparison (below indexed 'ref'). This reference is chosen because of the identical functionality, such as the possibility to attach multiple sources and a constant maximum phase voltage amplitude. The three-phase bridge has the ability to generate a zero-sequence voltage, so that a higher modulation depth can be achieved. The proposed topology is feeding an open-winding machine, so a zero-sequence in voltage leads to an (unwanted) zero-sequence in current. Thus, the machine's absolute phase voltage must be considered.

Moreover, equal sources and machines for both topologies are assumed. First, the DC-link voltage constraints are compared, followed by the estimation of the inductor and semiconductor volumes. The section is concluded by the calculation of the capacitor volume.

If the source voltage ranges from $V_{\mathrm{S,min}}$ to $V_{\mathrm{S,max}}$, the maximum DC-link voltage of the three-phase bridge can reach $V_{\mathrm{S,max}}$. As a result, the boost converter's output-voltage (fig. 11) is a function of the DC-link voltage:

$$v_{\mathrm{DC,ref}} \sim V_{\mathrm{C}} = V_{\mathrm{S,max}} \tag{30}$$

Because of eq. (1), the DC-link voltages for the proposed topology are chosen to $v_{\mathrm{C2}} = V_{\mathrm{S,min}}$ and $v_{\mathrm{C1}} + v_{\mathrm{C2}} + v_{\mathrm{C3}} = V_{\mathrm{S,max}}$. This results in the proportionality

$$v_{\mathrm{DC,novel}} \sim V_{\mathrm{S,max}} - V_{\mathrm{S,min}} \tag{31}$$

Following [11], the volume $\mathrm{Vol_L}$ of an inductor is a function of its stored energy and thus proportional to its value of inductance

$$\mathrm{Vol_L} \sim L^{0.77} \tag{32}$$

It should be noted that [5] and [6] state a linear dependence between stored energy and volume of an inductor. So the use of the exponent 0.77 from [11] depicts an worse case. Generally spoken, the inductance is a function of the available voltage and tolerable current ripple.

$$L \sim \frac{v_{\mathrm{L}}}{\Delta i_{\mathrm{L}}} \tag{33}$$

Aiming for equal current ripple for both topologies, the inductor's value reduces by

$$\frac{\mathrm{Vol_{L,novel}}}{\mathrm{Vol_{L,ref}}} = \left(\frac{V_{\mathrm{S,max}} - V_{\mathrm{S,min}}}{V_{\mathrm{S,max}}}\right)^{0.77} = \left(1 - \frac{V_{\mathrm{S,min}}}{V_{\mathrm{S,max}}}\right)^{0.77} \tag{34}$$

The DC converter's transistors also shrink in size, as their breakdown voltage V_{br} is reduced from $V_{\mathrm{S,max}}$ to $\frac{V_{\mathrm{S,max}} - V_{\mathrm{S,min}}}{2}$. [11] states a dependency for IGBT volume $\mathrm{Vol_{Tr}}$ vs. breakdown voltage V_{br} as

$$\mathrm{Vol_{Tr}} \sim V_{\mathrm{br}}^{1.8} \tag{35}$$

Keeping in mind that the number of switches is doubled, the reduction in DC converter semiconductor-volume is

$$\frac{\mathrm{Vol_{Tr,DC,novel}}}{\mathrm{Vol_{Tr,DC,ref}}} \sim 2 \cdot \left(\frac{V_{\mathrm{S,max}} - V_{\mathrm{S,min}}}{2\,V_{\mathrm{S,max}}}\right)^{1.8} = 2 \cdot \left(\frac{1}{2} - \frac{1}{2} \cdot \frac{V_{\mathrm{S,min}}}{V_{\mathrm{S,max}}}\right)^{1.8} \tag{36}$$

Depending on the particular implementation, it might benefical to use MOSFETs here. If so, [11] states that semiconductor volume is additionally increased by factor 2.5.

In the same way, the change in semiconductor volume of the AC side can be estimated. The number of semiconductors has doubled, but the second three-phase bridge has a lower operating voltage:

$$\frac{\mathrm{Vol_{Tr,AC,novel}}}{\mathrm{Vol_{Tr,AC,ref}}} \sim 1 + \left(\frac{V_{\mathrm{S,min}}}{V_{\mathrm{S,max}}}\right)^{1.8} \tag{37}$$

At last, the capacitor expense needs to be considered. Following [11], the volume of an electrolytic capacitor $\mathrm{Vol_C}$ is a function of the working voltage V_{C} and RMS current $I_{\mathrm{C,rms}}$:

$$\mathrm{Vol_C} \sim (V_{\mathrm{C}})^{1.5} \cdot (I_{\mathrm{C,rms}})^{1} \tag{38}$$

[13] derives the DC-link capacitor's RMS current stress of a three-phase bridge. In the reference topology, the two RMS currents of both the boost converter and the three-phase bridge additively superimpose [13, app. A], so that $I_{\mathrm{C,rms,ref}} = I_{\mathrm{boost,rms}} + I_{\mathrm{bridge,rms}}$ (worst-case scenario). In the proposed topology, the outer capacitors are also stressed by $I_{\mathrm{C,rms,ref}}$, so that the reduction in volume is

$$\frac{\mathrm{Vol_{C1+3}}}{\mathrm{Vol_{C,ref}}} \sim 2 \cdot \left(\frac{V_{\mathrm{S,max}} - V_{\mathrm{S,min}}}{2\,V_{\mathrm{S,max}}}\right)^{1.5} = 2 \cdot \left(\frac{1}{2} - \frac{1}{2} \cdot \frac{V_{\mathrm{S,min}}}{V_{\mathrm{S,max}}}\right)^{1.5} \tag{39}$$

The inner capacitor is stressed by $2 \cdot I_{\mathrm{bridge,rms}}$ but only by a neglectable amount of RMS current from the DC converter (because of buck-converter behaviour, see fig. 2), so that the change in volume can be approximated by

$$\frac{\mathrm{Vol_{C2}}}{\mathrm{Vol_{C,ref}}} \sim \left(\frac{V_{\mathrm{S,min}}}{V_{\mathrm{S,max}}}\right)^{1.5} \cdot \left(\frac{2\,I_{\mathrm{bridge,rms}}}{I_{\mathrm{boost,rms}} + I_{\mathrm{bridge,rms}}}\right)^{1} < \left(\frac{V_{\mathrm{S,min}}}{V_{\mathrm{S,max}}}\right)^{1.5} \cdot 2 \tag{40}$$

Finally, the total capacitor volume change is

$$\frac{\mathrm{Vol}_{\mathrm{C,novel}}}{\mathrm{Vol}_{\mathrm{C,ref}}} = \frac{\mathrm{Vol}_{\mathrm{C1+3}}}{\mathrm{Vol}_{\mathrm{C,ref}}} + \frac{\mathrm{Vol}_{\mathrm{C2}}}{\mathrm{Vol}_{\mathrm{C,ref}}} \tag{41}$$

For a source voltage range of $\frac{V_{\mathrm{S,max}}}{V_{\mathrm{S,min}}} = \frac{2}{1}$, the achievable changes in component volume are shown in table I.

TABLE I
CHANGE IN COMPONENT VOLUME FOR A SOURCE VOLTAGE RANGE OF $\frac{V_{\mathrm{S,max}}}{V_{\mathrm{S,min}}} = \frac{2}{1}$

Component	Reference Topology	Proposed Topology
Inductor	100 %	59 %
Capacitors	100 %	95.7 %
DC converter semicond.	100 %	16 %
AC converter semicond.	100 %	129 %

The results in table I show the change in component effort. First, the inductor volume is significantly reduced. This is caused by the smaller pulsed voltage across the inductor, which is one of the main characteristics of the proposed topology. Known optimizations from state-of-the-art DC-converters, like multiple interleaved phases and higher pulse frequency can still be applied, as these are independent from the particular topology. So these optimizations can reduce the total inductor-volume even further.

The total DC-link capacitor volume stays nearly unchanged. With optimized pulse patterns on the DC- and AC-side, capacitor current shaping could be achieved to reduce the capacitor RMS-current and thus the total capacitor volume.

At first sight, the aforementioned reduction in passive component effort seems to happen at the expense of semiconductor effort.

But, as both DC and AC converter have to transfer about the same amount of power, the semiconductor volume should be considered in sum per topology. Hence, the reference topology virtually has a component expense of 200%, compared to 145% of the proposed topology. This means that the total semiconductor effort is reduced to about 72.5%.

VI. Simulation Results

A simulation was conducted to validate the proposed circuit analysis and control scheme. The source voltage is assumed to stay constant, an open-winding induction motor is simulated as machine. The rotational speed is also assumed constant. Dimensioning of the passive components, set-point values and machine parameters of its T-equivalent circuit are listed in table II. Both inductor-current and capacitor-voltage controllers are designed as symmetric optimized controllers. The machine currents are controlled by a direct field oriented control (direct FOC) as it is e.g. described in [12, ch. 13]. Because of the open-winding configuration of the machine, a zero current controller must be added. Otherwise, an uncontrolled zero sequence in current can occur.

The result of a load step in machine torque is shown in fig. 12. The step in output-power is not fed back to the DC-converter controller. So for the DC-link voltage controller, the step depicts a disturbance value. By feed-forwarding the output-power, the DC-link voltage transient could be further improved.

TABLE II
PARAMETERS USED FOR SIMULATION

Parameter	Value	Explanation
f_{S}	8 kHz	Semiconductor Switching Frequency
L	800 µH	DC converter inductance
C_1, C_3	450 µF	outer DC-link capacitors
C_2	300 µF	inner DC-link capacitor
V_{S1}	300 V	source voltage
$V^*_{\mathrm{C1}} = V^*_{\mathrm{C3}}$	110 V	DC-link setpoint voltage
V^*_{C2}	160 V	DC-link setpoint voltage
L_{m}	70 mH	magnetizing inductance
$L_{\mathrm{S}\sigma}$	2 mH	stator leakage inductance
R_{S}	0.4 Ω	stator resistance
$L'_{\mathrm{R}\sigma}$	2 mH	rotor leakage inductance
R'_{R}	0.8 Ω	rotor resistance

VII. Conclusion and Outlook

In this publication, a novel converter topology is introduced. It is designated to drive a three-phase machine from one or multiple sources. The component effort of the needed DC converters and its inductors to couple various DC sources can be reduced by decreasing its switching voltage. A circuit analysis was done to prove the working principle of the topology as well as its present limitations. A basic estimation of component expense was done in comparison to the common three-phase bridge. Finally, a closed loop control was synthesized and simulation results were given. Future work will include more in-depth control analysis, determination of component stress and losses as well as experimental results.

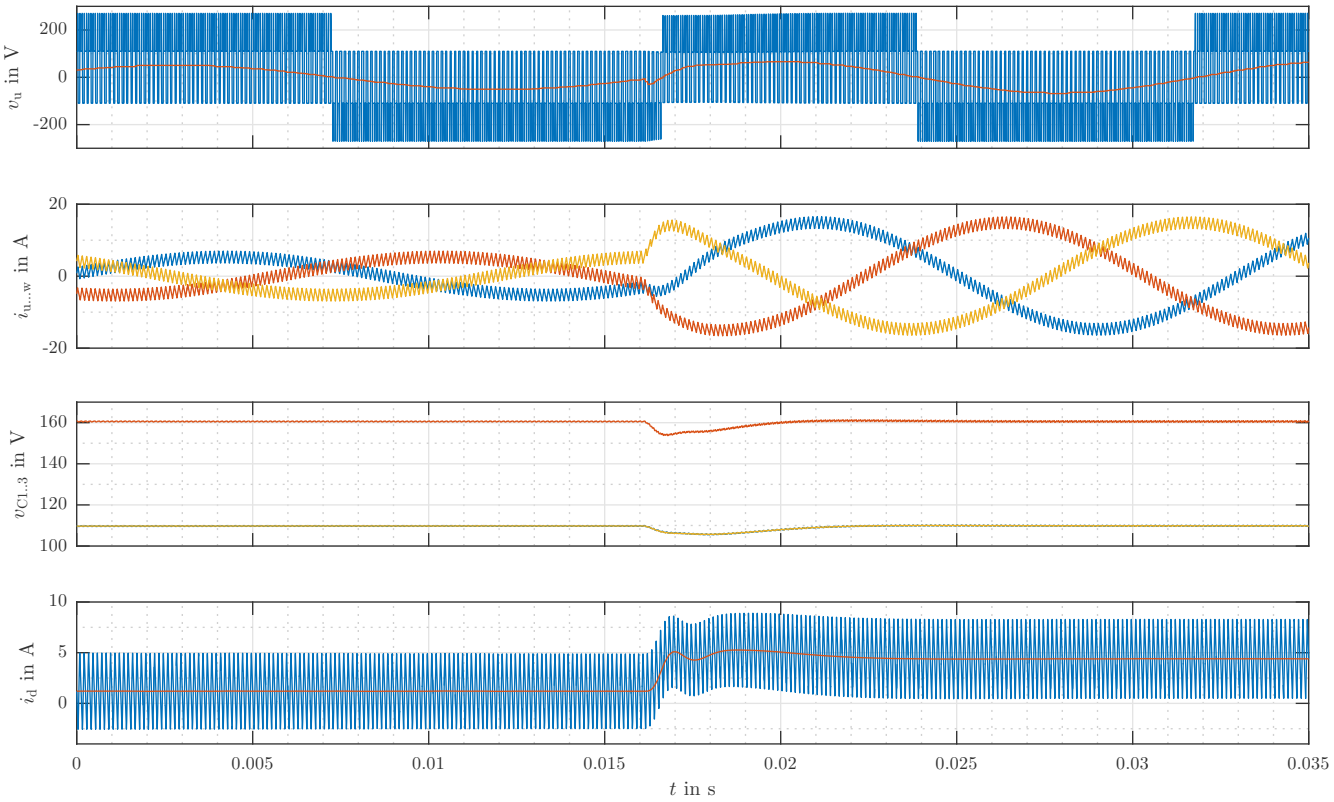

Fig. 12. Simulation results for a load step from $1\,\mathrm{Nm}$ to $3\,\mathrm{Nm}$ at $t = 16\,\mathrm{ms}$, resulting in a q-current step from $4.9\,\mathrm{A}$ to $14.7\,\mathrm{A}$. The first plot shows the machine's phase-voltages, the second plot the phase-currents. The third plot shows the DC-link voltages and indicates the function of the synthesized control scheme. The fourth plot shows the inductor current of the DC converter.

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