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Institute:	Karlsruhe Institute of Technology (KIT) Elektrotechnisches Institut (ETI) Electrical Drives and Power Electronics
Type:	Conference Proceedings
Published at:	20th European Conference on Power Electronics and Applications (EPE 2018), Riga, Lettland, 17.09.2018 – 21.09.2018 Publisher: IEEE, Piscataway (NJ) Year: 2017 ISBN: 978-90-75815-28-3 Pages: 1-9
Hyperlinks:	Scopus: 85057068277

Optimized Control of a Novel DC/3AC Converter Topology with Reduced Component Effort

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Keywords

≪Adjustable speed drive≫, ≪Control methods for electrical systems≫,
≪Converter control≫, ≪Power converters for EV≫

Abstract

A previously proposed traction converter topology can reduce component effort and converter volume by decreasing the pulsed voltage across the DC-converter inductance. However, the maximum voltage across the machine phases then becomes a function of the DC source voltage. In this paper, an optimization is presented to ensure a constant maximum phase voltage over a wide source voltage spread.

Introduction

To improve the overall performance of an electric vehicle (EV), many measures are taken today. Main criticisms address the limited cruising range and the relatively high costs of an EV. These result in the key design goals of the electric drivetrain: volume, costs and efficiency. [1] and [2] mention compositions of volume and costs of a typical converter, which is visualized in Fig. 1.

It can clearly be seen that about half of the converters volume is taken up by air. A known solution to reduce this fraction is integration. Most recent developments regarding packaging of semiconductors are double sided cooled modules [3]. These improves heat transfer which eases cooling at the expense of a more complex mechanical design. The second important leverage are passive components with about 20% in volume and 30% in costs. Generally, these expenses can be tackled by e.g. higher switching frequencies, especially for DC-DC converters. Novel semiconductor materials such as silicon carbide

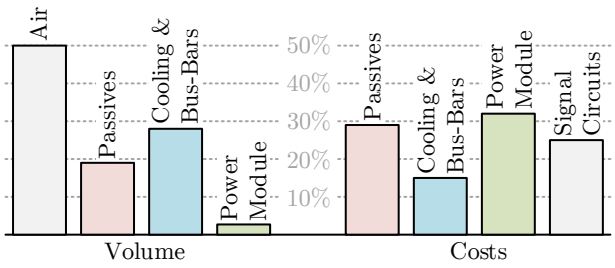

Fig. 1: Typical composition of volume and costs inside a converter. Data merged from [1] and [2].

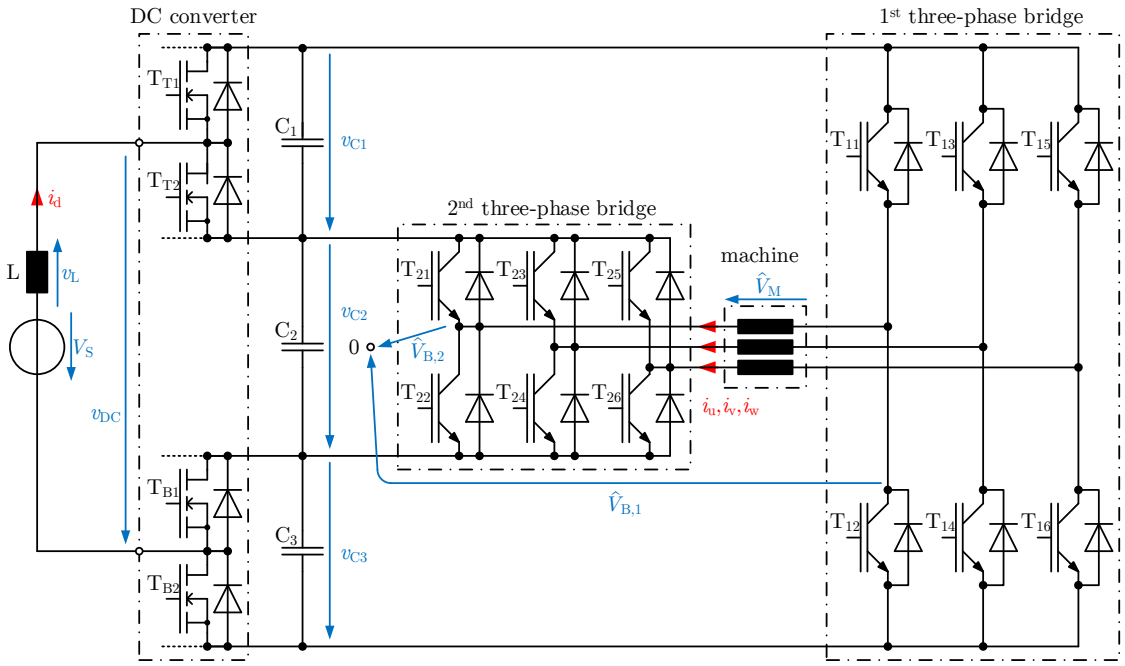

Fig. 2: Schematic of the proposed topology. All mentioned voltages and currents are labelled.

(SiC) have shown to be a possible part of the solution. As SiC semiconductors create less switching-losses and thus enable higher switching frequencies, smaller passive components can be used to improve power density [4]. Further approaches can be applied such as e.g. interleaved phases [5] or magnetic coupling [6] to especially reduce the inductor effort. The idea of the novel topology is also to reduce the DC-converter inductance. The topology takes advantage of the (dis-)charge characteristic of voltage sources like batteries and fuel cells. Conventional boost converters can operate down to nearly zero source voltage. However, the voltage of a battery does not drop below a certain voltage when totally discharged. The novel topology utilizes this fact in that way that it only switches between the minimum and maximum possible source voltage, hence reducing the voltage time area of the inductor. [7] shows that besides the inductance, the semiconductor effort can also be reduced, regarding to present comparative methods [8]. The aforementioned remedies of increased pulse frequency or interleaved phases are still applicable to the novel topology, so the proposed idea presents a totally independent way of reduction in component expense. In the following publication, the novel converter topology and the underlying idea are briefly introduced. The addressed problem of the maximum phase voltage as a function of the source voltage is explained and an optimization is proposed to achieve a constant maximum phase voltage over a wide range of the source voltage. An exemplary application of the derived algorithm for a typical drive system is shown and experimentally validated by a laboratory-scale demonstrator.

The Novel Converter Topology

The schematic of the proposed converter topology is shown in Fig. 2. The DC converter part consists of two half bridges (T_{T1}, T_{T2} resp. T_{B1}, T_{B2}) that are attached to the outer voltages of a tripartite DC link. Two three-phase bridges (T_{11} - T_{26}) are connected to the inner resp. outer potentials and are thus fed by the interior DC link voltage, resp. by the sum voltage. Because of the lower working voltage of the DC converter half bridges, semiconductors with smaller blocking voltages can be used. Because of the voltage offset v_{C2}, the inductance L can be chosen significantly smaller to achieve the same current ripple as in a conventional boost converter. If multiple sources are used, only smaller submodules have to be replicated, which leads to even further volume improvement in comparison. The basic idea of an offset voltage for DC-converters (i.e. a non-zero minimum output voltage) is introduced in [9] for a battery powered multilevel cell and is adapted to a maximum power point tracking circuit in [10] and [11]. In [7] and [12], the proposed traction converter is derived.

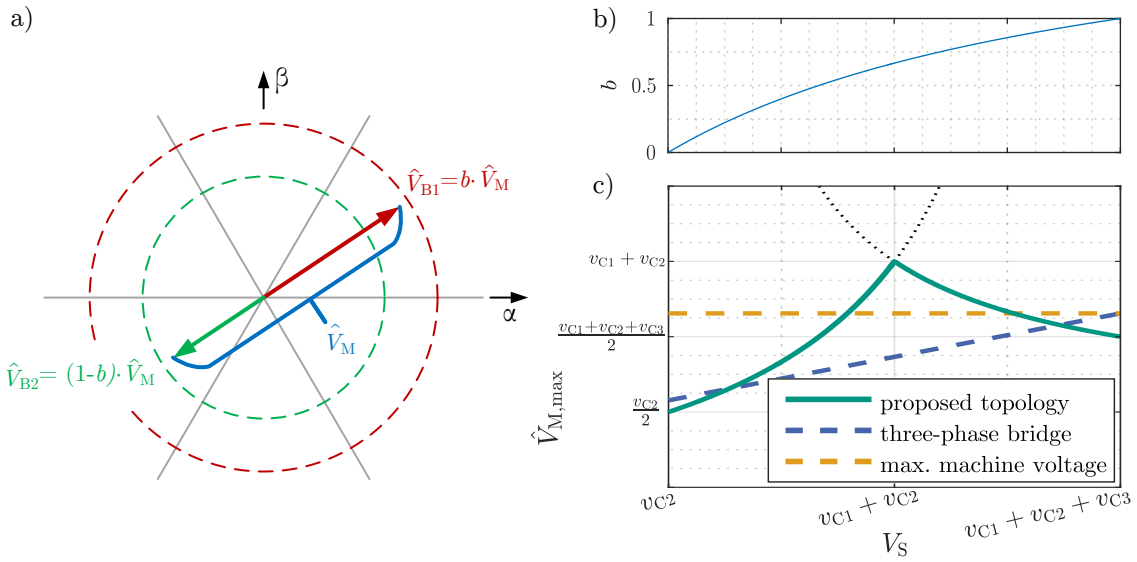

Fig. 3: a) Exemplary voltage distribution to the two three-phase bridges to obtain a certain phase voltage space vector. b) Distribution b of the total output-power to the two three-phase bridges as a function of V_S and a fixed ratio of $\frac{v_{C1}}{v_{C2}} = 0.5$ and $v_{C1} = v_{C3}$. c) Normalized maximum phase voltage amplitude of the proposed topology as a function of the source voltage (green), compared to that of a common three-phase bridge (blue) and with additional boost converter (yellow) [7].

Control of the Novel Converter Topology

The circuit and control analysis in [7] shows the operating principle of the proposed topology. The main aspects will be briefly summarized in this chapter, further details can be found in [7]. The boundary condition for the source voltage V_S is

$$v_{C2} \leq V_S \leq v_{C1} + v_{C2} + v_{C3} \tag{1}$$

with the DC-link capacitor voltages v_{C1}, v_{C2}, v_{C3} as shown in Fig. 2. Otherwise the freewheeling diodes of the DC converter will conduct and cause a short-circuit. The output-voltages of the three-phase bridges create the voltages across the motor phases. Each three phase bridge contributes a fraction b resp. $(1-b)$ of the machines total phase voltages as a function of the source voltage V_S inside its boundary conditions. The following set-points result for the voltage amplitude of each bridge $\hat{V}_{B1}$ resp. $\hat{V}_{B2}$ for a given desired phase voltage amplitude $\hat{V}_M$:

$$\hat{V}_{B1} = b \cdot \hat{U}_M \tag{2}$$

$$\hat{V}_{B2} = (1-b) \cdot \hat{V}_M \tag{3}$$

$$b = \frac{(V_S - v_{C2})(v_{C1} + v_{C2} + v_{C3})}{V_S (v_{C1} + v_{C3})} \tag{4}$$

The approach of voltage distribution is depicted in Fig. 3 a). For any source voltage inside its boundary conditions, a valid voltage distribution $b \in [0;1]$ can be found, which can be seen in Fig. 3b). The three-phase bridges work with sine-modulation without zero-sequence, so the operating limits $\hat{V}_{M,max}\big|_{B1,max}$ and $\hat{V}_{M,max}\big|_{B2,max}$ of the bridges define the maximum achievable phase voltage $\hat{V}_{M,max}$ which is again a function of the source voltage

$$\hat{V}_{M,max} = \min\left(\hat{V}_{M,max}\big|_{B1,max}, \hat{V}_{M,max}\big|_{B2,max}\right) \tag{5}$$

with

$$\hat{V}_{\mathrm{M,max}}\big|_{\mathrm{B1,max}} = \frac{(v_{\mathrm{C1}} + v_{\mathrm{C3}})\, V_{\mathrm{S}}}{2\,(V_{\mathrm{S}} - v_{\mathrm{C2}})} \tag{6}$$

$$\hat{V}_{\mathrm{M,max}}\big|_{\mathrm{B2,max}} = \frac{(v_{\mathrm{C1}} + v_{\mathrm{C3}})\, V_{\mathrm{S}}}{2\,(v_{\mathrm{C1}} + v_{\mathrm{C2}} + v_{\mathrm{C3}} - V_{\mathrm{S}})} \tag{7}$$

The maximum achievable phase voltage amplitude $\hat{V}_{\mathrm{M,max}}$ as a function of the source voltage V_{S} is shown in Fig. 3 c). It is compared to the maximum achievable phase voltages of a three-phase bridge with and without a boost converter and symmetrical PWM (i.e. with zero-sequence). A spread in source voltage of 2:1 is assumed, so that v_{C2} equals the minimum source voltage and $v_{\mathrm{C1}} + v_{\mathrm{C2}} + v_{\mathrm{C3}}$ equals its maximum. It can be seen that, on the one hand, the novel converter topology already outperforms the reference topologies in certain voltage ranges. On the other hand, areas remain where the reference topologies excel the proposed topology near the minimum and maximum of the source voltage. This problem will be addressed and solved in the following paragraph.

Optimization of the inner DC-link voltage

The aim of the optimization is to achieve a constant maximum phase voltage amplitude over the whole source voltage range. So the task is to manipulate the DC-link voltages as a function of the source voltage to get a flat and constant maximum phase voltage amplitude as it is achieved by a normal three-phase bridge with boost converter.

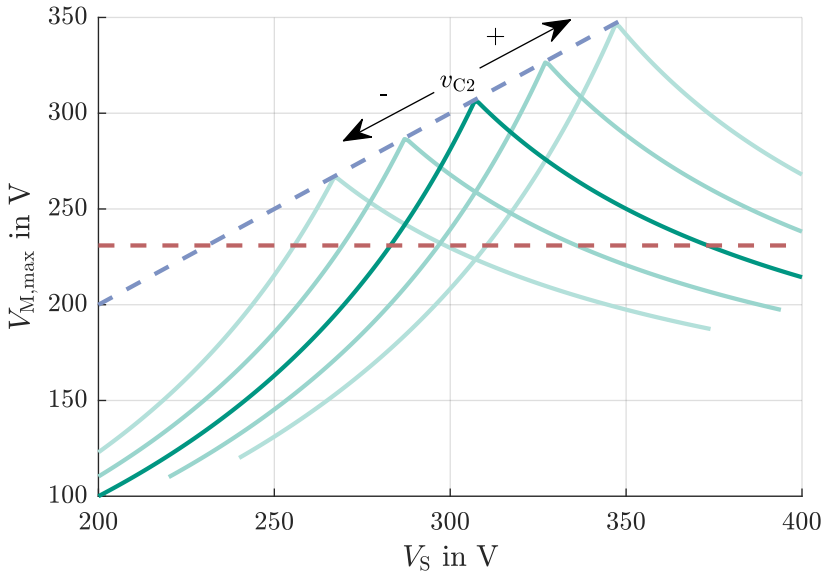

Fig. 4: An exemplary set of curves, showing the maximum phase voltage $\hat{V}_{\mathrm{M,max}}$ as a function of the source voltage V_{S} for various capacitor voltages v_{C2} (green). Also shown is the wanted machine voltage (red) and the locus of the intersection of Equations (6) and (7) (blue).

As the locus of the intersection of Equations (6) and (7) divides the desired machine voltage in two parts (Fig. 4 blue/red), the proposed optimization method will consider three cases. These are

- $V_{\mathrm{S}} = V_{\mathrm{S,max}} > \hat{V}^{*}_{\mathrm{M,max}}$ (right hand of the intersection blue/red)
- $V_{\mathrm{S}} = \hat{V}^{*}_{\mathrm{M,max}}$ (the intersection)
- $V_{\mathrm{S}} < \hat{V}^{*}_{\mathrm{M,max}}$ (left hand of the intersection)

Here, $\hat{V}^{*}_{\mathrm{M,max}}$ is the maximum phase voltage amplitude. First, the maximum source voltage $V_{\mathrm{S}} = V_{\mathrm{S,max}} > \hat{V}^{*}_{\mathrm{M,max}}$ will be considered. Since this is the highest source voltage, it is sensible to choose a DC-link voltage distribution from the right half of Fig. 3 c), where bridge 1 determines the maximum phase voltage

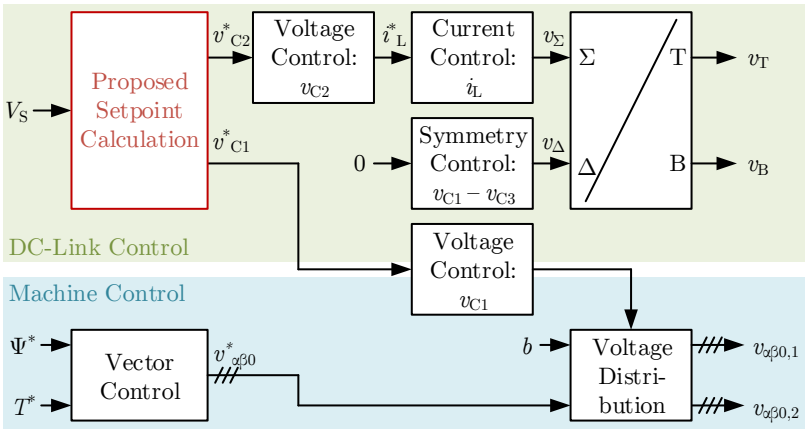

Fig. 5: Control scheme with the proposed voltage set-point calculation added. The contents of the individual boxes are described in [7].

amplitude. This will result in the smallest possible capacitor voltages. Symmetry of the outer capacitors C1 and C3 will be assumed, so that $v^*_{C1} = v^*_{C3}$. The applicable machine voltage levels are $+v_{C1}+v_{C2}$, $+v_{C1}$, $-v_{C3}$ and $-v_{C2}-v_{C3}$. The ratio $\frac{v_{C2}}{v_{C1}}$ remains as a degree of freedom. In this publication, it will be constrained by an equal step height in machine voltage, which means $v^*_{C2} = 2v^*_{C1}$. Other ratios might be sensible too, but would need separate examination. Solving (6) with the given constraints results in

$$v^*_{C2}(V_S = V_{S,max}) = \frac{2V_{S,max} \cdot \hat{V}^*_{M,max}}{V_{S,max} + 2\hat{V}^*_{M,max}} \tag{8}$$

$$v^*_{C1} = v^*_{C3} = \frac{1}{2} v^*_{C2}(V_S = V_{S,max}) = \frac{V_{S,max} \cdot \hat{V}^*_{M,max}}{V_{S,max} + 2\hat{V}^*_{M,max}} \tag{9}$$

as set point voltages for the DC-link capacitors. For a falling source voltage, the maximum achievable phase voltage amplitude will unnecessarily rise (according to Fig. 3 c). So the DC-link voltages can be reduced as the source voltage reduces. The inner capacitor voltage v^*_{C2} is reduced, the voltages of C1 and C3 remain at the determined set points. This lowers the particular working voltage of both three-phase bridges, which is advantageous regarding losses as the DC-converter already has a quite small operating voltage. The next point to calculate is $V_S = \hat{V}^*_{M,max}$. Here, the maximum point of the curve from Fig. 3 c) is used, which results in the smallest possible capacitor voltages. The maximum achievable phase voltage amplitude is then

$$\hat{V}_{M,max} = v_{C1} + v_{C2} = V_S \tag{10}$$

With the value for v^*_{C1} given from above, the set point value for the inner capacitor voltage determines to

$$v^*_{C2}(V_S = \hat{V}^*_{M,max}) = \hat{V}^*_{M,max} - v^*_{C1} = \hat{V}^*_{M,max} \cdot \left(1 - \frac{V_{S,max}}{V_{S,max} + 2\hat{V}^*_{M,max}}\right) \tag{11}$$

Between the considered points, v_{C2} can be interpolated linearly, e.g. by

$$v^*_{C2}(V_S) = \frac{\Delta v^*_{C2}}{\Delta V_S} \text{ for } V_S \in [\hat{V}^*_{M,max}; V_{S,max}] \tag{12}$$

with

$$\Delta v^*_{C2} = v^*_{C2}(V_S = V_{S,max}) - v^*_{C2}(V_S = \hat{V}^*_{M,max}) \tag{13}$$

$$\Delta V_S = V_{S,max} - \hat{V}^*_{M,max} \tag{14}$$

For $V_S < \hat{V}^*_{M,max}$, the wanted maximum phase voltage cannot be reached anymore. In that case, the inner capacitor voltage is determined by

$$v^*_{C2}(V_S < \hat{V}^*_{M,max}) = V_S - v^*_{C1} \text{ for } V_S \in [\hat{V}^*_{S,min}; \hat{V}^*_{M,max}] \tag{15}$$

The proposed set-point calculations are added to the existing control scheme from [7]. This is shown in Fig. 5.

Results of the Optimization

Fig. 6 shows exemplary results of the optimization for a state of the art traction system. The battery is assumed to have a voltage from 200 V to 400 V, resulting in a ratio of 2:1. This is a quite broad range, considering that many lithium batteries feature a voltage range of 2.6 V to 4.1 V, which results in a ratio of only 1.6:1. The wanted maximum machine phase voltage is assumed $\hat{V}^*_{M,max} = \frac{400\,V}{\sqrt{3}} \approx 231\,V$, which could be created by a three-phase bridge with attached boost converter across the whole source voltage and thus is a good reference. It can be seen, that for a wide source voltage range, the maximum phase voltage has a flat appearance and the inner capacitor voltage can be reduced significantly.

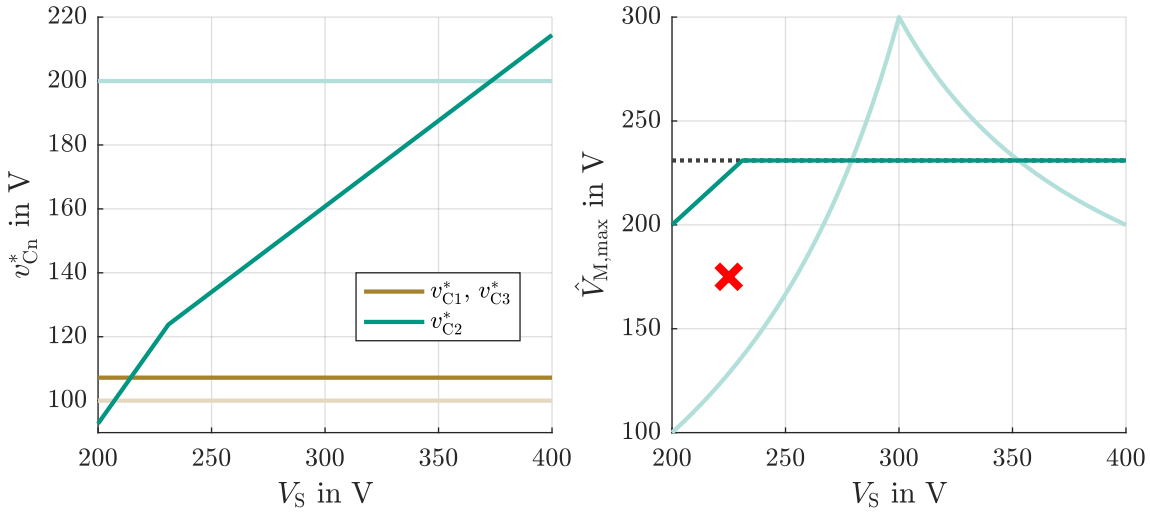

Fig. 6: Left: Optimized capacitor voltages v^*_{C1} (brown) and v^*_{C2} (green). The corresponding fixed DC-link voltages from [7] are shown as a reference in light colors. Right: Resulting maximum phase voltage amplitude $\hat{V}_{M,max}$ (green). Again, the maximum phase voltage amplitude from [7] is shown as a reference in light green. The operating point marked in red can only be reached with the proposed optimization. This point is used in the 'Experimental Validation' section.

Experimental Validation

An experimental validation is performed with a demonstrator converter in laboratory size. The converter is housed inside a converter cabinet that is equipped with different power electronic building blocks, as seen in Fig. 7. One building block is the DC-converter, equipped with IRFP4868 N-channel-MOSFETs by Infineon (Fig. 7 a). The board can drive up to two sources and features supervision of all voltages, currents and temperatures. Another building block is the three-phase bridge, equipped with a FS75R12KT4 IGBT-module by Infineon (Fig. 7 b). The three-phase bridge also supervises all currents and voltages.

As motor an 4 kW induction machine DFV112M2 by SEW is used (Fig. 7 c). A TMS320C6748 digital signal processor from Texas Instruments (TI) runs the control algorithm, that is a field oriented control, the DC-converter control [7] and the calculation of the proposed optimized DC-link voltages. Several THS1204 AD-converters by TI sample all relevant currents and voltages with 1.5MSps. A Cyclone IV field programmable gate array (FPGA) from Altera is used as modulator. The background of the digital

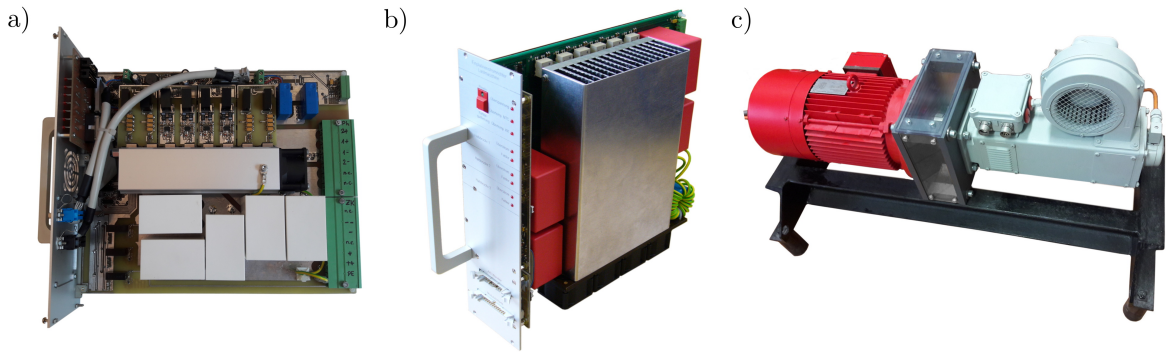

Fig. 7: a) Power electronic building block: DC-converter, b) Power electronic building block: Three-phase bridge, c) Machine set: Induction machine and DC-machine.

Table I: Machine set-point values

Parameter	Description	Set-point
n	Rotational speed	$1500\,\mathrm{min}^{-1}$
i_d	d-axis current	4.38 A
i_q	q-axis current	2 A
V_S	source-voltage	225 V

Table II: Set-point voltages for the DC-link

Parameter	Description	Set-point
$v_{\mathrm{C1}} = v_{\mathrm{C3}}$	Outer capacitor voltages	107.4 V
v_{C2}	Inner capacitor voltage	119.3 V

signal processing system is described in [13]. To show the correctness of the proposed optimization, a set-point has to be set that requires a phase voltage that is only reachable with optimized capacitor voltages. This set-point is listed in Table I.

The wanted d- and q-axis currents in combination with the set rotational speed require a phase-voltage amplitude of 175 V. Together with the given source voltage, the operating point would not be reachable with the former choice of DC-link voltages ($v_{\mathrm{C1,3}} = 100\,\mathrm{V}$ and $v_{\mathrm{C2}} = 200\,\mathrm{V}$). This wanted operating point is marked with a red cross in Fig. 6. With the proposed optimization, the set-point voltage change according to Table II. Thus, the needed phase voltage is achievable.

The measurement results are shown in Fig. 8. It can be seen from Fig. 8 a) that the phase-voltage amplitude can be generated without limitation. The red lines show the maximum phase for fixed, non-optimized capacitor voltages. It is evident, that wanted operating point of $v_\mathrm{u} = 175\,\mathrm{V}$ can be reached. At this point, the maximum phase voltage amplitude is 225 V. Fig. 8 b) shows that the field oriented control works sufficiently. Fig. 8 c) shows the DC-link voltages. The set-points are chosen according to the proposed algorithm.

In the current implementation of the converter topology, the control of the outer capacitor voltages currently depict a problem. To temporarily overcome this problem, an additional DC-converter is used, according to Fig. 9. It transfers a small amount of energy from the inner to the outer capacitors to compensate parasitic effects and to control the outer capacitor voltages. As mentioned in [7], the voltages can also be controlled by variation of the voltage distribution factor b, if active power is transferred. However, the use of this converter does not affect the aforementioned optimization algorithm. This problem and solution will be addressed separately in future publications.

Conclusion and Outlook

A novel traction converter topology was previously published and showed significant reduction component effort. However, restrictions had to be accepted regarding the maximum machine phase voltage. In this paper, an optimization of the DC-link voltages is proposed to overcome these disadvantages. As an additional benefit, the optimization results in even smaller DC-link voltages which should affect the total converter efficiency and hardware effort. A prototype for experimental validation is built and an experimental validation shows the correctness of the derived optimization.

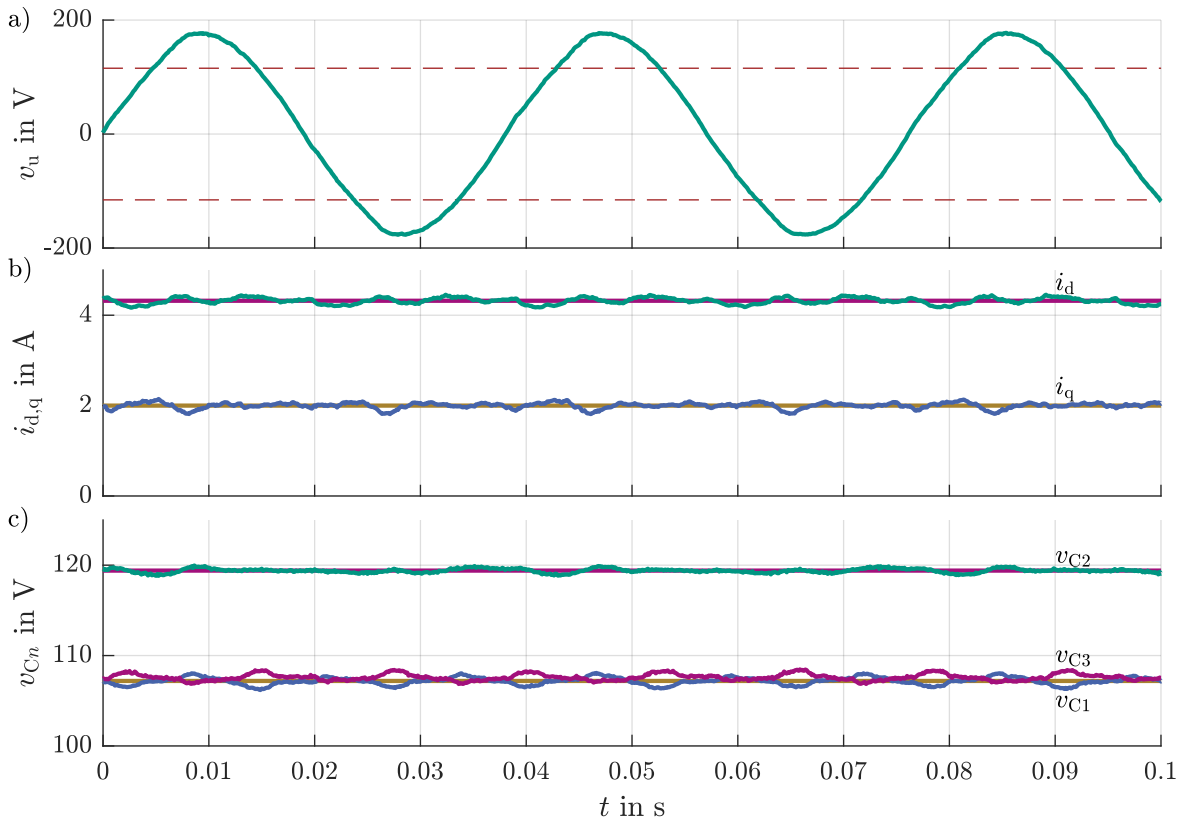

Fig. 8: Measurement results with optimized capacitor voltages. a) The phase voltage v_u across the first winding. The dashed red lines show the theoretical voltage limit if fixed capacitor voltages were used. b) Set-points and measured d- and q-axis current of the machine of the field oriented control. c) Setpoint and measured DC-link capacitor voltages. The set-points are gained by the proposed optimization.

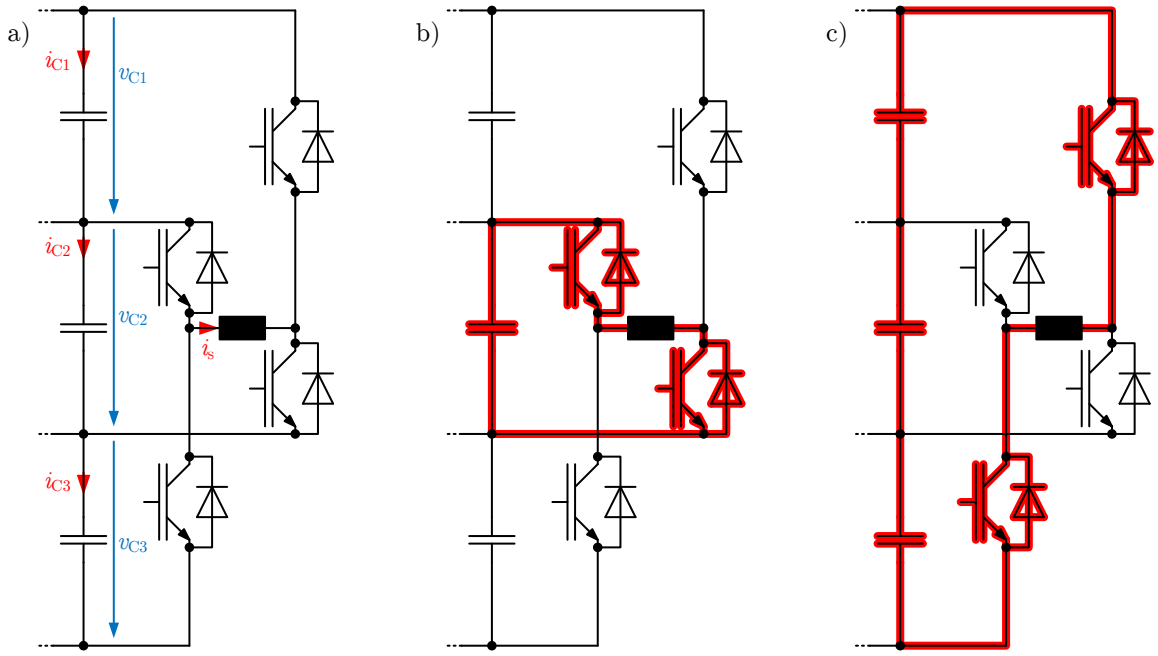

Fig. 9: a) chematic of the provisional DC-converter used to control the outer capacitor voltages. b) and c) the two switching states needed to control the outer capacitor voltages.

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