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A Modular Converter- and Signal-Processing-Platform for Academic Research in the Field of Power Electronics

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Abstract— **For academic research it is mandatory that the theoretical evaluation and modelling of new control methods, modulation schemes, electrical machines, power electronic topologies, etc. is validated with accurate measurements. To guarantee a high quality and high performance research it is necessary to have a modular, scalable, user-friendly, adaptable and affordable system. This allows to put the focus on the research topics themselves rather than spending a high effort on the pure implementation of the theoretical research results. The system described in this paper consists of a software environment/toolchain and a hardware platform. The hardware platform can be subdivided into a power electronics platform and a System on Chip based signal processing system. Besides the hardware platform also a user-friendly software environment/toolchain for model-based research is developed and illustrated in this paper. This new system enables rapid-prototyping of new algorithms, hardware and topologies.**

Keywords— *Education Tool, Power Electronic Platform, Signal Processing System, rapid control prototyping.*

I. INTRODUCTION

The Institute of Electrical Engineering (ETI) at KIT has three main research topics: "Electrical Drives and Power Electronics", "Hybrid Electric Vehicles" and "Power Electronic Systems". Three professors, 26 scientific assistants and about 50 students deal with issues concerning these research topics. In order to ensure a high quality and fast academic research for such a large number of scientists it is necessary to have a modular and cost-efficient signal processing and power electronics platform. There are several powerful commercial platforms available, but they are expensive and only allow very limited access to the complete system-level, which is a prerequisite in academic research. The described self-developed platform is used for academic research in PhD projects, student laboratories and bachelor- or master theses. So far, the platform has consisted of a modular DSP signal processing system [1] and a single PCB Silicon Insulated Gate Bipolar Transistors (Si-IGBTs) converter with an output rating up to 30 kW. For future academic research, a new modular platform is necessary. This paper describes the next generation of the signal processing system based on a System on Chip (ETI-SoC system), and the new modular single PCB converter (ETI-combi-EPSR), which can be used with either Silicon Carbide Metal–Oxide–Semiconductor Field-Effect Transistors (SiC-MOSFETs) or Si-IGBTs. Furthermore, the necessary software environment/toolchain for a simple usage of the new hardware platform is described.

II. DEVELOPMENT PROCESS

The development process of new software e.g. control algorithms and modulation schemes or new hardware components like electrical machines or power electronics topologies can be roughly divided in three steps. First, the complete system is analyzed and developed in **simulation**. Model-based development in simulation is essential to enable short research times. Therefore, accurate machine models parametrized by finite element analysis (FEA) or test-bench measurements, exact physical models of the power electronics or precise battery models are available. After the simulation phase, a feasible **hardware** has to be chosen and assembled to confirm the simulation results. Due to the modularity of the ETI platform, a fast test-bench setup is possible. Finally, the hardware has to be commissioned and appropriate tests and measurements can used for the **validation**.
Subsequently, a typical development process of a new electrical machine test-bench is described. This test-bench is used to investigate novel machine control methods.

Simulation:
1. Analysis of an electrical machine with FEA
2. Generation of an electrical machine parameter set
3. Parametrization of a Mathworks Matlab/Simscape electrical machine model
4. Design/Implementation of the converter for the electrical machine in Mathworks Matlab/Simscape
5. Design of the modulator for the converter in Mathworks Matlab/Stateflow
6. Design/Implementation of the machine control in Mathworks Matlab/Simulink
7. Simulation and parametric study of the entire test-bench

8. C-code generation of the developed machine algorithm for the signal processing system
9. HDL-code generation of the modulator for the signal processing system

Hardware:
1. Assembling of the modular power electronics and signal processing components
2. Dimensioning of the necessary passive components, interfaces and peripherals for the test-bench
3. Startup of the test-bench

Validation:
1. Implementation of the developed software on the signal processing system
2. Automated measurements/tests with the Monitor Control Tool based on National Instruments LabView

The time effort for this development process was significant reduced by the usage of the signal processing and the power electronics platform.

III. Signal processing platform

System on Chip devices are well-proven in cell phones or software defined radio devices but they are used more and more in automation and control technology [1]. The structural benefit of the System on Chip (SoC) device allows hardware/software co-design and makes them essential for modern automation and control devices.
The proposed system is based on the Xilinx programmable SoC family "Zynq-7000". For the ETI signal-processing platform Avnet's "PicoZed 7030" System on Module (SoM) with the "Zynq Z-7030" and necessary peripheral hardware was chosen (TABLE 1). On the SoM additional hardware components like memory devices or Ethernet driver are already implemented.

TABLE I
AVNET'S PICOZED 7030 SOM [2]

	PicoZed 7030
Processor Core	DUAL CORE ARM CORTEX A9
On-Chip Memory	256 KB
Peripherals	CAN, UART, I2C, ...
Clock Rate	667 MHz
Computer Performance	1334 MFLOPS
Memory	1 GB DDR
Ethernet	10/100/1000 Mbit
Programmable Logic	KINTEX-7
Logic Cells	125 000
PL IOs	250

To achieve downward compatibility with the existing "ETI-DSP system" described in [3] a carrier card for the SoM device is necessary. The existing "ETI-DSP system" is a modular real time measurement and control system in single (100 x 160 mm²) or double euroboard format

(233 x 160 mm²). The components are assembled in a subrack with a backplane for power supply and internal communication. The developed carrier card for the "PicoZed 7030" SoM device can be used in the existing system with modular extension boards or as a single system. In Fig. 1 the new ETI-SoC system is illustrated. It was designed for multiple purposes. Therefore a plurality of interfaces was implemented such as Ethernet, Memory card slot, galvanic insulated CAN transceiver, JTAG and USB. A proprietary asynchronous parallel communication bus was connected via backplane connector for internal communication.
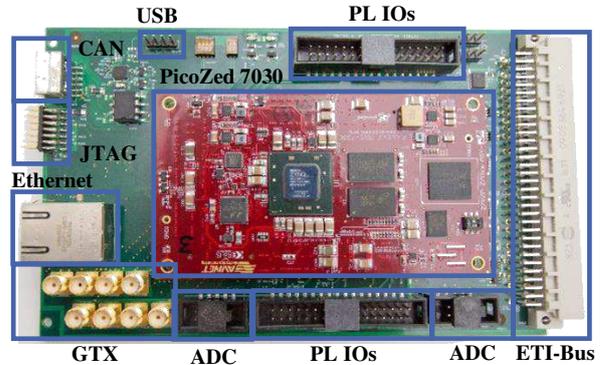

Fig. 1. Topview of the ETI-SoC carrier card design

The SoC system provides another extension ability by the four highspeed Xilinx GTX transceivers, which were attached to SMA connectors. The communication with these transceivers was successfully tested with a data rate of 6.25 Gbit per second. In Fig. 2 the eye pattern is shown. In the middle of the bit cycle the eye is still open with a Bit Error Rate (BER) of 10^{-6}, hence a communication is possible. With this high-speed communication interface an IO-expansion or sharing of computing performance of the SoC device is possible.
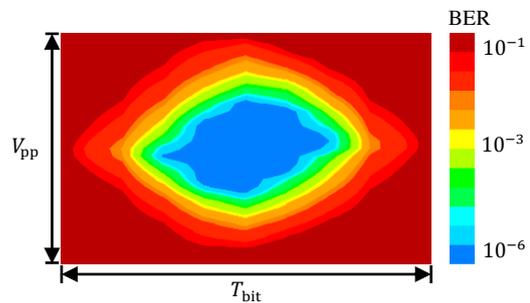

Fig. 2. Eye pattern for a data rate of 6.25 Gbit

On the bottom side of the ETI-SoC system a LVDS connector was attached to facilitate an extension of the carrier card with a second application dependent board.
For control applications it is mandatory to digitize analog measured values. Therefore, six Analog Digital Converters (ADCs) with an analog gain stage were implemented in order to handle ± 10 V input signals. The assembled Linear Technology ADC "LTC2323-14" has a sample rate of five Mega samples per second (Msps) with
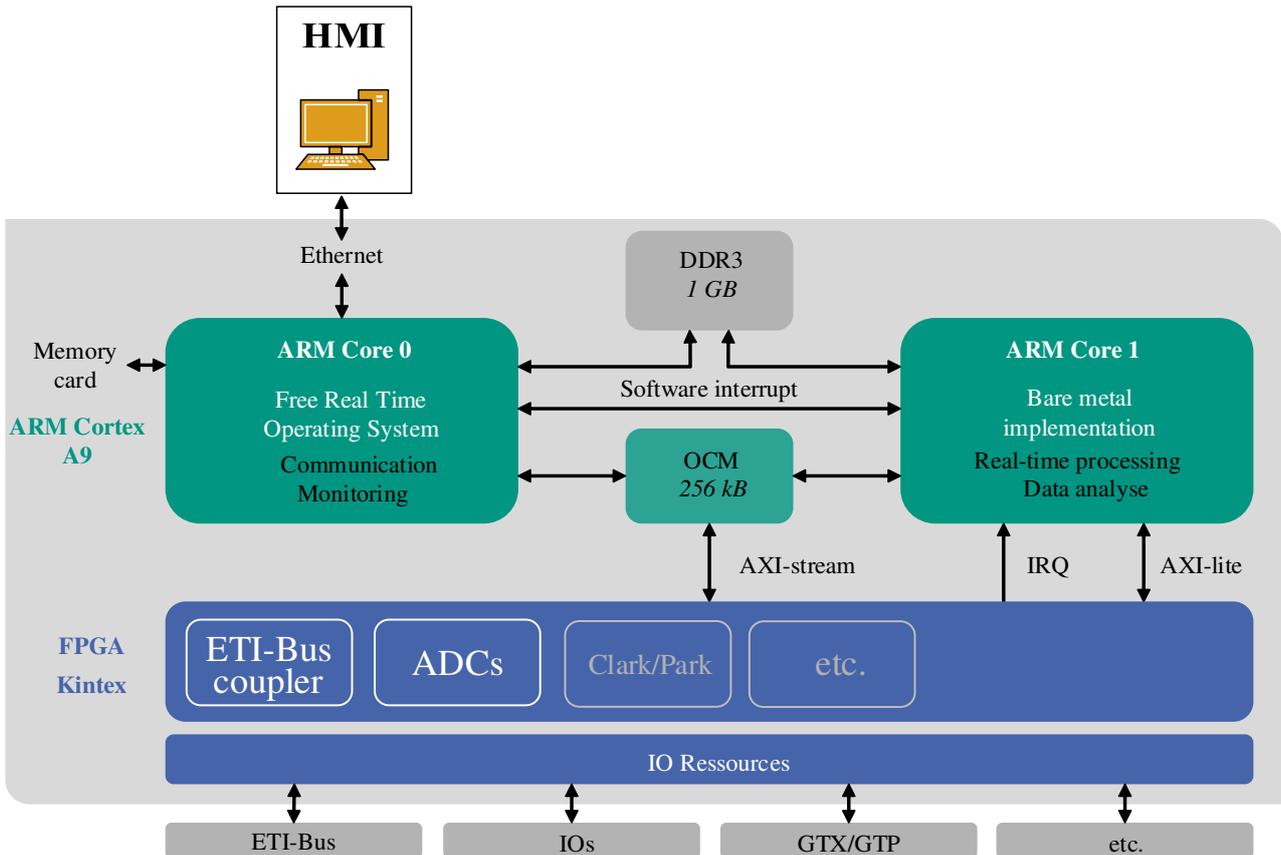
Fig. 3. Block diagram of the ETI-SoC software structure

a resolution of 15 bit. The measured latency of the entire measurement chain was only 400 ns.

To generate the signals for the converter and peripherals also the FPGA programmable logic IOs (PL IOs) of the SoC were attached to two 34 pin connectors.

The eight layer carrier card was designed with ALTIUM Designer during a student's master thesis. Due to the necessary differential routing of the LVDS and the GTX transceivers an accurate design is essential. Therefore, the signal integrity of the whole carrier card design was evaluated with ANSYS SiWave-PI.

IV. SIGNAL PROCESSING SOFTWARE DESIGN

To allow students a fast software development of novel control methods and modulation schemes besides the hardware platform also a software environment and toolchain must be given. The students develop the new algorithms in Matlab/Simulink and use the provided software environment. This allows that only the developed software interfaces in Matlab/Simulink must be addressed to use the particular functions of the SoC without the knowledge of the subordinate code. The developed software environment is described in this section.

To understand the developed software environment the internal system design of the SoC must be known. The used Zynq SoC consists of a dual core ARM Cortex A9

processor, a Kintex-7 FPGA and peripheral units which suit well for real time measurement and control systems.

The whole block diagram of the Xilinx Zynq-7000 AP SoC is described in [4]. For the proposed implementation the ARM cores are separately used as an asymmetric multiprocessing system. The whole customized system structure is shown in Fig. 3.

On the first ARM core, ARM core 0, FreeRTOS a slim real-time operating system for embedded devices was implemented. ARM core 0 is responsible for the data exchange of the measured and calculated values with the HMI (host/control computer). For this purpose the FreeRTOS+TCP stack is used. The implemented algorithms, which are developed by the students, are only executed on the second ARM core ARM core 1 due to time-critical latency requirements. The algorithms are realized as raw program code without any operation system, called bare metal implementation. Thereby the program code can be written in C or directly generated with the Matlab/Simulink C-code generation out of the model-based simulation.

Due to this structure, with ARM core 0 as a communication system and ARM core 1 as processing system, the algorithms for the ARM core 1 can be flexibly reconfigured online. The fast execution of these algorithms on ARM core 1 within a defined time up to

10 µs make e.g. the control of power electronics with real time requirements possible.

The software environment also contains the communication between the FPGA and the ARM cores. Hence, measured values from the ADCs, the IO values and control sequences can transmit and receive from the FPGA and the ARM cores. The FPGA also manage the external ETI-Bus and is used as a flexible programmable logic part. For the data transfer between the FPGA and the ARM core 1 the Xilinx AXI4 stream protocol, part of the Advanced Microcontroller Bus Architecture (AMBA), is used. The developed protocol for the AXI4 stream with direct memory access was adapted so that the communication is similar to the existing bus-system described in [3] with a parallel data bus and corresponding address bits. The buffering of the data is utilized in the On-Chip memory (OCM) with a RX- and TX-buffer. The inter processor communication is possible due to synchronized ARM cores via software generated interrupts. The data and control sequences are also transferred between the Ethernet socket/HMI and the ARM core. Due to the easy exchange between the FPGA and the ARM Cores the SoC allow hard/software codesign of the developed functional designs. The executed code on the ARM core 1 is capable to be operated in real time.

On the control computer the developed Monitor Control Tool [3], based on LabView, visualize the received data. For the use of this communication the user only has to import a devised communication block in the designed Matlab/Simulink code model.

V. POWER ELECTRONICS PLATFORM

To evaluate new control methods or modulation schemes besides the signal processing also a power electronics platform is necessary. In Fig. 4 the new ETI-combi-EPSR is depicted. It consists of a local control unit (CU) and the power electronics unit.
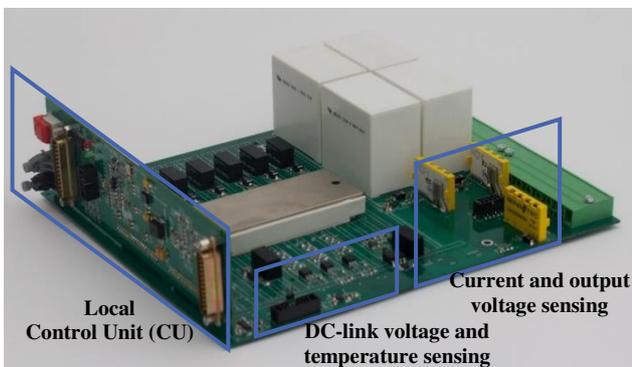

Fig. 4. ETI-combi-EPSR with a Local Control Unit and a power electronics unit

A. Power Electronics Unit

The power electronics unit was designed in such a way that it can either be equipped with Infineon Si-IGBT module FS75R12KT4 or with Wolfspeed SiC-MOSFET module CCS050M12CM2. The output ratings are 30 kW for the Si-IGBT and 40 kW for the SiC-MOSFET, depending on the switching frequency.

The converter was equipped with measuring systems for the output currents, the heatsink temperature, the DC-link voltage and the output voltages. The combination of switching frequencies in the range up to 100 kHz and new control methods like Direct Adaptive Current Control [5] leads to high demands on the current measurement. Therefore, CMS3000 family current sensors from SENSITEC with a bandwidth of 2 MHz were applied. Since the converter will be used in student laboratories, all measurements are potential free to minimize the risk of accidents.

The converter was analyzed with ANSYS SiWave-DC to check the current density on the PCB [6]. In Fig. 5 the current density on the PCB is illustrated. The PCB was designed in in accordance with the IPC-2221 [7].
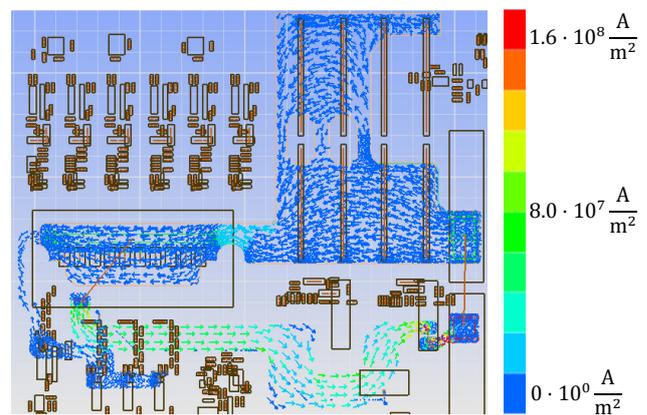

Fig. 5. Simulation with ANSYS SiWave-DC of the current density of one output phase of the three phase converter

B. Local Control Unit

The local control unit consists of a MAX10 FPGA from Altera, an ADS8528SPM Analog-Digital converter from Texas Instruments, digital/analog interfaces and a 50 Mbit/s optical interface. By the use of the CU several tasks of the ETI-SoC system can be carried out. Hence, the resources of the ETI-SoC system are fully available for the superposed control algorithm. Depending on the carried out tasks the CU can be equipped with a MAX10 FPGA from 8000 up to 25000 logic elements. Therefore, it is possible to adapt the CU depending on the application. For the minimal requirements such as monitoring tasks, error management, temperature control and modulation 8000 logic elements are sufficient. If an autarkic system is required, for example an Active Front End (AFE) or a DC/DC converter a MAX10 with 25000 logic elements is necessary. In this case, the ETI-SoC has only to provide the reference values and enable signals and thus no process time of the ETI-SoC is needed. To allow the communication the optical interface is used so the ETI-

SoC system and the CU can be spatially separated. Due to the modular design the CU can also be used for other power electronics system, e.g. the control of one phase of a 3-Level T-Type Neutral Point Clamped Inverter.

VI. EDUCATIONAL USE

At the ETI several lectures cover issues of electric machine design, electrical drive control, power electronics and circuit design. Besides the theoretical knowledge transfer it is also important to teach how to put the theoretical knowledge into practice e.g. in laboratory. Hence, laboratory experiments are necessary which can be built with the described modular platform. Besides that, new control methods or machines developed in PhD programs must be validated. Therefore test benches must be designed with the help of students e.g. as student workers or in different bachelor and master theses by means of the described modular platform.

To allow that universal use of the platform it must be continuously developed. During this development process, several students' projects are supervised in which the students learn to use the knowledge gained from the lectures. Thus, the PCBs for the ETI-combi-EPSR and the ETI-SoC system were developed and validated in one master thesis [8]. The signal processing software design was designed in several master theses [9], [10], [11], [12] and afterward further developed with student workers. Hence, the platform is always used with state of the art devices and can be easily applied for different projects. Three sample projects are subsequently described.

A. Power Hardware in the Loop system

At the ETI a Power Hardware-in-the-Loop (PHiL) system was developed by a PhD student. The system consists of the square-wave powered Modular Multilevel Converter (SPMMC) with a push-pull-converter [13]. The SPMMC can utilize a high-precision 3AC voltage source from DC up to nearly medium frequency [13]. This voltage source is used to emulate permanent magnet synchronous machines with nonlinear magnetics. In Fig. 6 the PHIL and a machine inverter (DUT) are illustrated.

The aim of the PHIL is to show the same behavior as the emulated machine on its terminals. Thus, a DUT can't differentiate whether the PHIL is connected to its terminals or the real machine. For this purpose the SPMMC has to utilize an output voltage v_{ay0} (number of phase: $y \in \{1, 2, 3\}$) that the current i_x is the same as in the real machine. Therefore, the reaction time of the output voltage v_{ay0} must be small in comparison to the switching frequency of the DUT. This is reached with a new hybrid control approach [14], which allows a modulation frequency of the output voltage v_{ay0} of 100 kHz.

For the emulation of the machine a model must be calculated. To utilize a correct output voltage v_{ay0} the voltage of the DUT must be measured with a high sample rate and subsequent the machine model must be calculated.

This is done with a rate of 2.5 MHz. The FPGA clock of the ETI-SoC system for the model calculation is 75 MHz. Thus, the system has only 30 cycles for the whole calculation. During that calculation, eight memory accesses to look-up tables are necessary to utilize the correct voltage. Since the calculation itself needs 23 cycles, only 7 cycles are available for the memory accesses. This access time is only possible since the ETI-SoC system has an intern block RAM of 9.3 Mbit with an access time of one cycle [15]. Hence, the new ETI-SoC system made it possible to build up a high-precision PHIL emulation for permanent magnet synchronous machines with nonlinear magnetics.
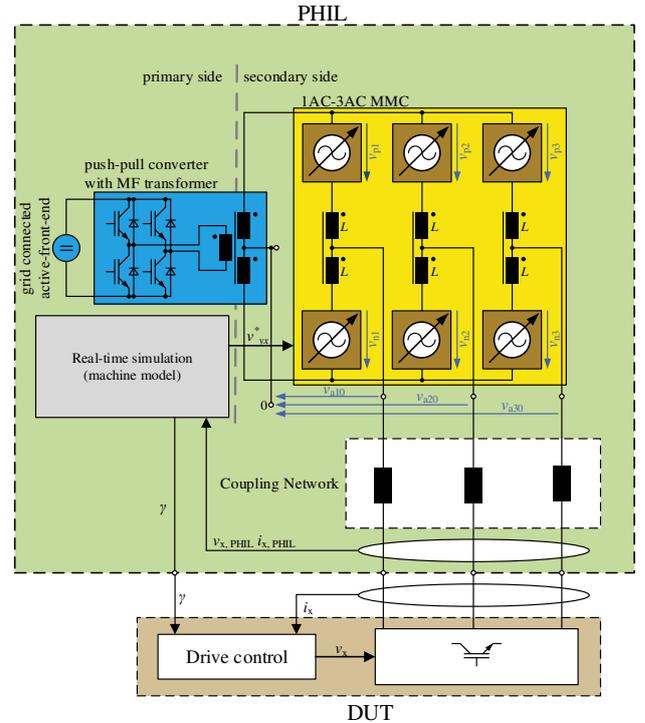

Fig. 6. Power Hardware-in-the-Loop (PHiL) system

B. Motor test-bench

The validation of new electrical machine designs during PhD programs [16] makes extensive measurement of the developed prototypes necessary. Therefore, different motor test-benches with customized signal processing and power electronics hardware are necessary. The buildup of these motor test-benches is often done in student's bachelor and master theses and supervised by the PhD candidates.

For future investigations with high switching frequency inverters for drives and dynamic control of electrical machines a new motor test-bench with Si- and SiC inverter based on the ETI-combi-EPSR was developed in a student bachelor thesis [17].

After the bachelor studies the students have the theoretical knowledge of electrical engineering. Especially within the specialization in power electronics and drives students can enroll lectures about electrical machines and drives, PCB

and electrical circuit design and converter control. These lectures are *"Electrical Machines and Power Electronics"*, *"Industrial circuitry"* and *"Converter control technique"*. By building a motor test-bench students can put their learned knowledge into practice.

The described test-bench was developed with the new modular platform. The student started with the design of the cabinet and the power electronic circuit. For this motor test-bench, shown in Fig. 7, the device under test motor and the load motor are coupled directly against each other. For the power supply an active-front (AFE) and a power choke is necessary. For the AFE an ETI-combi-EPSR with SiC-MOSFETs has been used concerning chapter V. The power choke was calculated by the student based on the *"converter control technique"* lecture.
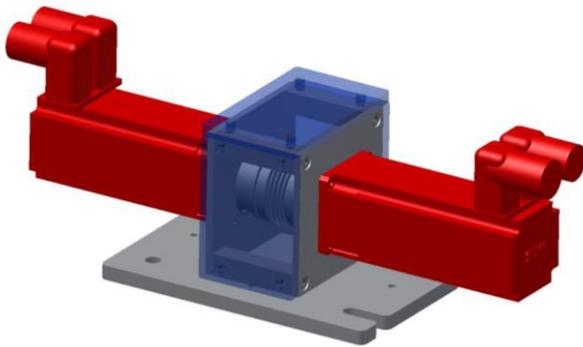

Fig. 7. Motor test-bench setup

The AFE controller was designed based on the "Control of Electrical Drives" lecture. The motor inverters were built up with two ETI-combi-EPSR one with Si-IGBTs and one with SiC-MOSFETs. Hence, a fast buildup of the test bench within one Bachelor thesis was possible. The ETI-SoC system signal processing hardware was used for the motor control and monitoring of the motor test-bench. The modular signal processing system had to be adapted for this purpose. Modular extensions for the rotor angle and temperature measuring boards were assembled. Different customized interface circuit boards were designed with Altium Designer and manufactured. Successive commissioning of the designed boards and the assembled cabinet and programming of the signal processing system with Matlab/Simulink and National Instruments Labview concluded the thesis.

Hence, the student could connect the knowledge of power electronics, drives, information technology, electrical circuit design and control theory from the bachelor studies during the thesis [18].

In Fig. 8 the complete motor test-bench is shown. The control and monitoring computer and the ETI-SoC system can be seen in the upper part. The power electronic consisting of three ETI-combi-EPSR and the power choke is shown in the lower part.
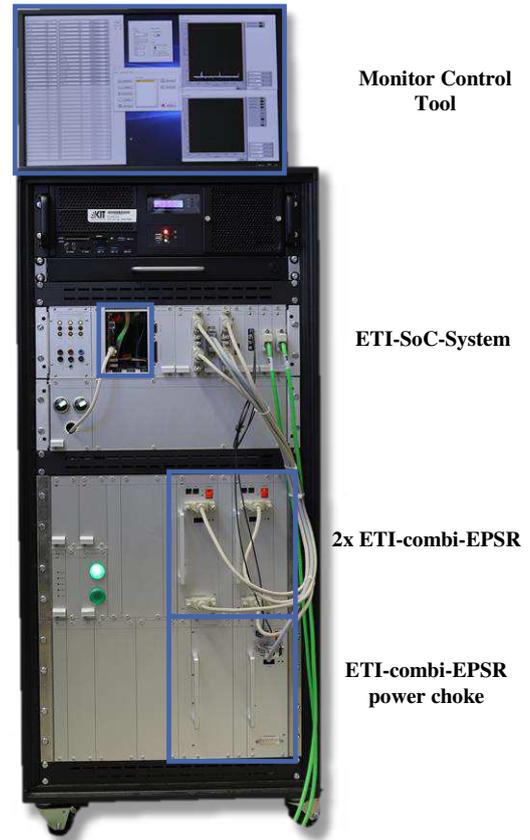

Fig. 8. Motor test-bench cabinet

C. Formula Student

Another application of the modular signal processing hardware is in the formula student team "ka-raceing" (Fig. 9). In the season 2016/17 the signal processing system controlled the drive train of the KIT electric car. For the all-wheel-drive racing car each wheel is powered by a motor over a self-designed axis. One signal processing system thereby executes two predictive motor control algorithms and the required monitoring [19] for one axis with two motors in less than 40 µs.

Fig. 9. Formula Student: *KIT16e* (www.ka-raceing.de)

VII. Conclusion

In this paper a modular platform of a signal processing system and a modular converter system for multiple research projects was introduced. With software based development of different algorithms, code generation for C-code and HDL-code fast rapid-prototyping in academic research is possible. Furthermore the modular, flexible converter platform allows fast validation on an experimental set-up for high quality research. Also three sample projects are described which were built with the new modular platform.

VIII. Acknowledgement

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