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An approach to reducing complexity of neuromorphic fault dictionary construction for analogue integrated circuits

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Abstract

© 2018 IEEE. This paper is mainly focused on the reducing a complexity of fault dictionary constructing for analog integrated circuits based on neural network. The benefits of fault dictionary based on neural network (NN) such as associative operating mode and small influence of the number of considered faults on the NN architecture are presented. The problems of constructing the neuromorphic fault dictionary in the aspect of big data are discussed. The approach to selection the essential characteristics of controlled parameters during testing and fault diagnostics as well as to reduction of the training set dimension is proposed. The principal component analysis (PCA) and criterion based on the explained residual variance are applied for reduction the number of coefficients used for the neural network training. The decomposition of design flow corresponding to the proposed approach is presented. The experimental results demonstrates efficiency as the time and computational cost reduction for the construction of neuromorphic fault dictionary, which provides high fault coverage up to 100 %.

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Keywords

Analog circuits, Design-for-testability, Neuromorphic fault dictionary, Principal component analysis, Testing and diagnostics

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