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Automated simulation of faults in analog circuits based on parallel paradigm

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Abstract

© 2017 IEEE. Fault simulation is very important task for testing and fault diagnostics based on the concept of simulation before test. Catastrophic and parametric faults as well as component tolerances can make strong or weak influence on a correct circuit behavior. Therefore it is necessary to estimate such influence during design stage in order to provide high quality testing and diagnosis for the circuit under test. The number of potential faults in analog circuits is tremendous and the fault simulation requires essential computational resources as well as takes much time. The approach to the fault simulation in analog circuits based on parallel paradigm providing automation of the design-for-testability concept and essential reduction of the fault simulation time is proposed. The decomposition of the fault simulation task according to parallel paradigm is presented. The architecture of parallel simulation system is considered, and FSM for operation of the main host and executive nodes are described. Two scenarios of possible interoperability between the main host and executive nodes based on cascade scheme and deferred scheme are proposed. Experimental results for both scenarios are presented.

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Keywords

analog circuits, design automation, design-for-testability, fault simulation, Monte Carlo method, parallel paradigm

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