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FPGA implementation of LTE turbo decoder using MAX-log MAP algorithm

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Abstract

© 2017 IEEE. Implementation of an efficient turbo decoder with low complexity, short delay and insignificant performance degradation is currently a quite challenging task. The paper presents an implementation of a 3GPP TS 36.212 LTE turbo decoder. The design of the turbo decoder has been optimized to achieve efficient FPGA resource utilization. This design can be useful for applications, which is critical to resource utilizations, but do not need high throughput.

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Keywords

BCJR, FPGA implementation, LTE turbo decoder, MAP, MAX-log MAP, Turbo decoder

References

[1] M. Rovini and A. Martinez, "Efficient stopping rule for turbo decoders, " Electronics Letters, vol. 42, no. 4, pp. 235-236, 16 Feb. 2006.

[2] 3GPP, TS 36. 212 V12. 2. 0 Technical Specification, pp. 12-15, 2014.

[3] L. Bahl, J. Cocke, F. Jelinek, and J. Raviv "Optimal Decoding of Linear Codes for minimizing symbol error rate, " IEEE Transactions on Information Theory, vol. IT-20 (2), pp. 284-287, March 1974.

[4] C. Berrou, A. Glavieux, and P. Thitimajshima, "Near Shannon limit error correcting coding and decoding: turbo-codes, " Proc. IEEE Int. Conf. Communications, pp. 1064-1070, May 1993.

[5] S. G. Mosin, "The Features of Integrated Technologies Development in Area of ASIC Design, " Proc. of 9th Conf. The Experience of Designing and Application of CAD System in Microelectronics (CADSM'07), pp. 292-295, 2007.

[6] S. J. Lee, N. R. Shanbhag, and A. C. Singer, "Area-Efficient High-Throughput MAP Decoder Architectures, " IEEE Trans. Very Large Scale Integration (VLSI) Systems, vol. 13, no. 8, pp. 921-933, 2005.

[7] L. Li and R. Maunder, "Analysis of low power implementational issues of turbo-like Codes in Body Area Networks, " University of Southampton, pp. 13-31, November 2009.

[8] L. Li, R. Maunder, B. Al-Hashimi, and L. Hanzo, "A low-complexity turbo decoder architecture for energy-efficient wireless sensor networks, " IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 21, pp. 14-22, January 2013.

[9] J.-S. Lin, M.-D. Shieh, Ch.-Y. Liu and D.-W. Yang, "Efficient highlyparallel turbo decoder for 3GPP LTE-Advanced", VLSI Design Automation and Test (VLSI-DAT) 2015 International Symposium, pp. 1-4, 2015.

[10] S. M. Karim, I. Chakrabarti, "An Improved Low-Power High-Throughput Log-MAP Turbo Decoder, " IEEE Trans. on Consumer Electronics, vol. 56, no. 2, pp. 450-457, 2010.

[11] S. Sanjay, "A Simplified and Efficient Implementation of FPGA-Based Turbo Decoder, " Conference Proceedings of the 2003 IEEE International, pp. 207-211, 2003.

[12] Y. Tong, T.-H. Yeap, J.-Y. Chouinard, "VHDL Implementation of a Turbo Decoder With Log-MAP-Based Iterative Decoding, " IEEE Trans. on Instrum. and Measurement, vol. 53, no. 4, pp. 1268-1278, 2004.